



**256K x 36, 512K x 18
2.5V Synchronous ZBT™ SRAMs
Smart ZBT™ Feature
2.5V I/O, Burst Counter
Pipelined Outputs**

**Preliminary
IDT71T656
IDT71T658**

Features

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high performance system speed - 200 MHz (3.2 ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Smart ZBT™ Feature - Eases system timing requirements and reduces the likelihood of bus contention
- ◆ With Smart ZBT™ the output turn-on (tCLZ) is adaptable to the user's system and is a function of the cycle time.
- ◆ Backward compatible with IDT's existing ZBT offerings.
- ◆ User selectable Smart ZBT™ or Original ZBT™ mode pin (\overline{MS})
- ◆ Internally synchronized output buffer enable eliminates the need to control \overline{OE}
- ◆ Single R/\overline{W} (READ/WRITE) control pin
- ◆ Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- ◆ 4-word burst capability (interleaved or linear)
- ◆ Individual byte write ($\overline{BW1}$ - $\overline{BW4}$) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 2.5V power supply ($\pm 5\%$)
- ◆ 2.5V I/O Supply (V_{DDO})
- ◆ Packaged in a JEDEC standard 100-lead plastic thin quad flatpack (TQFP) and 119-lead ball grid array (BGA).

Description

The IDT71T656/58 are 2.5V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71T656/58 offer the user an optional Smart functionality which simplifies system timing requirements when turning the bus around between writes and reads. Traditionally, SRAMs are designed with fast turn-on times (tCLZ) in order to meet the requirements of high speed applications. This fast turn-on may lead to bus contention at slower speeds, i.e. 133 MHz and slower, since these designs oftentimes use less aggressive ASICs/controllers with loose turn-off parameters (tCHZ). Thus at slower speeds, more margin on the RAM's tCLZ may be needed to compensate for the slow turn-off of the ASIC/controller. The IDT71T656/58 have the ability to provide this extra margin by allowing tCLZ to adapt to the user's system.

With the Smart ZBT™ feature, the output turn-on time (tCLZ) adapts to the user's system and is solely a function of cycle time (tCYC). Thus with Smart ZBT™, tCLZ is independent of process, voltage, and temperature variations. With this deterministic output turn-on feature, the guess work of when the SRAM begins to drive the bus is removed, therefore

Pin Description Summary

A0-A18	Address Inputs	Input	Synchronous
$\overline{CE1}$, CE2, $\overline{CE2}$	Chip Enables	Input	Synchronous
\overline{OE}	Output Enable	Input	Asynchronous
R/\overline{W}	Read/Write Signal	Input	Synchronous
\overline{CEN}	Clock Enable	Input	Synchronous
$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/ \overline{LD}	Advance burst address / Load new address	Input	Synchronous
\overline{LBO}	Linear / Interleaved Burst Order	Input	Static
I/O0-I/O31, I/OP1-I/OP4	Data Input / Output	I/O	Synchronous
VDD, VDDO	Core Power, I/O Power	Supply	Static
VSS	Ground	Supply	Static
\overline{MS}	Smart ZBT™ Mode Enable	Input	Static

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Description (cont.)

easing system timing requirements. The Smart feature allows the turn-on time of the ZBT™ SRAM output drivers (tCLZ) to adapt to match the requirements of the system.

The IDT71T656/58 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable (\overline{CEN}) pin allows operation of the IDT71T656/58 to be suspended as long as necessary. All synchronous inputs are ignored when (\overline{CEN}) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE1}$, $CE2$, $\overline{CE2}$) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/\overline{LD} is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes)

will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71T656/58 have an on-chip burst counter. In the burst mode, the IDT71T656/58 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the \overline{LBO} input pin. The \overline{LBO} pin selects between linear and interleaved burst sequence. The ADV/\overline{LD} signal is used to load a new external address ($ADV/\overline{LD} = \text{LOW}$) or increment the internal burst counter ($ADV/\overline{LD} = \text{HIGH}$).

The IDT71T656/58 SRAMs utilize IDT's latest high-performance 2.5V CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-lead thin plastic quad flatpack (TQFP) as well as a 119-lead ball grid array (BGA).

Pin Definitions⁽¹⁾

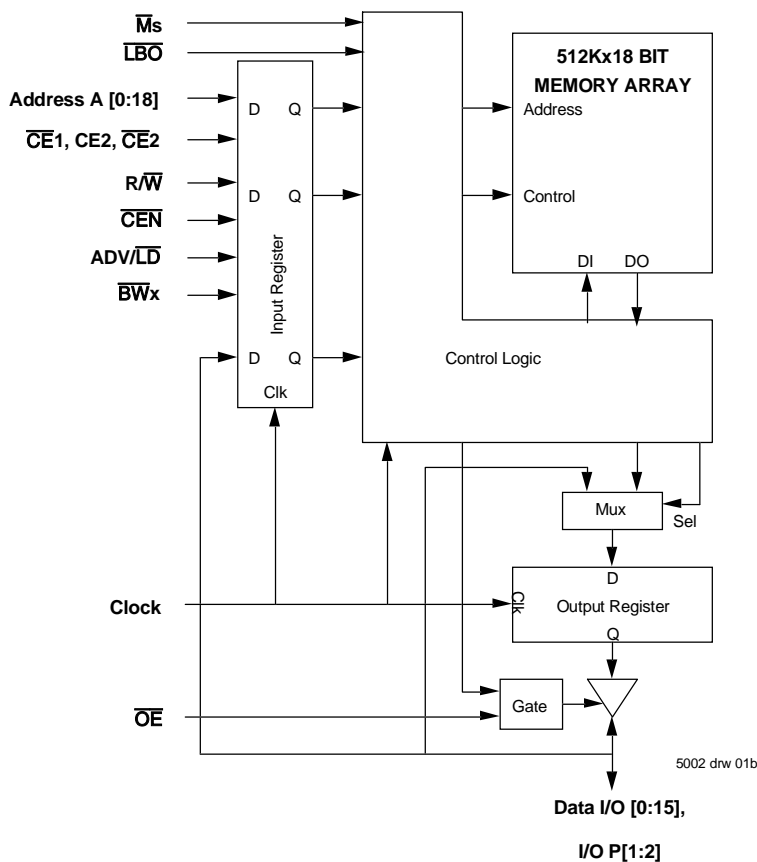
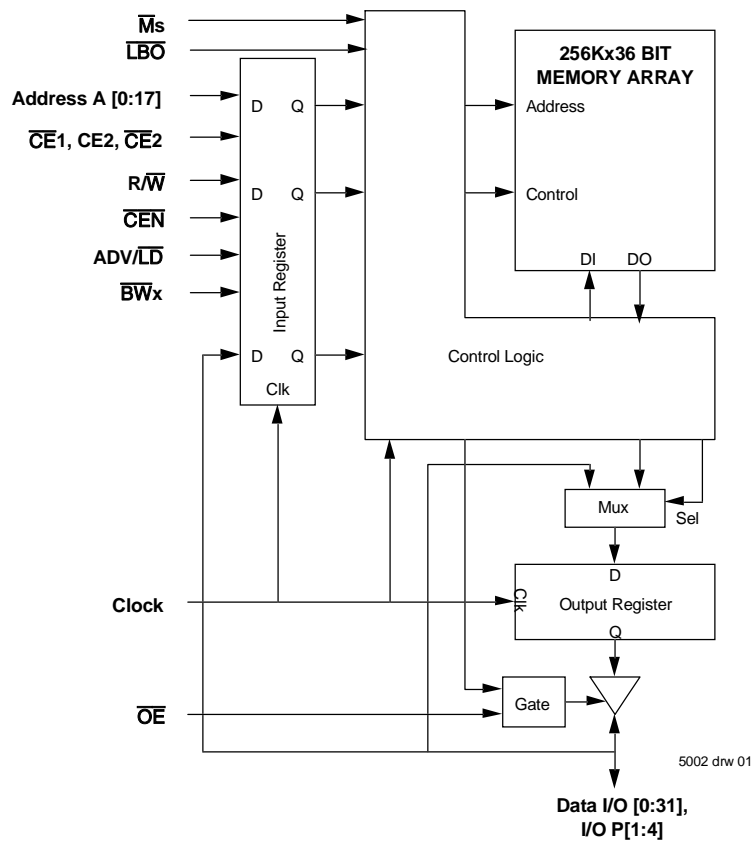
Symbol	Pin Function	I/O	Active	Description
A0-A18	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/\overline{LD} low, \overline{CEN} low, and true chip enables.
ADV/\overline{LD}	Advance / Load	I	N/A	ADV/\overline{LD} is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/\overline{LD} is low with the chip deselected, any burst in progress is terminated. When ADV/\overline{LD} is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/\overline{LD} is sampled high.
R/\overline{W}	Read / Write	I	N/A	R/\overline{W} signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
\overline{CEN}	Clock Enable	I	LOW	Synchronous Clock Enable Input. When \overline{CEN} is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of \overline{CEN} sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, \overline{CEN} must be sampled low at rising edge of clock.
$\overline{BW1}-\overline{BW4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/\overline{W} and ADV/\overline{LD} are sampled low) the appropriate byte write signal ($\overline{BW1}-\overline{BW4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/\overline{W} is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW1}-\overline{BW4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE1}$, $\overline{CE2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE1}$ and $\overline{CE2}$ are used with $CE2$ to enable the IDT71T656/58 ($\overline{CE1}$ or $\overline{CE2}$ sampled high or $CE2$ sampled low) and ADV/\overline{LD} low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
$CE2$	Chip Enable	I	HIGH	Synchronous active high chip enable. $CE2$ is used with $\overline{CE1}$ and $\overline{CE2}$ to enable the chip. $CE2$ has inverted polarity but otherwise identical to $\overline{CE1}$ and $\overline{CE2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71T656/58. Except for \overline{OE} , all timing references for the device are made with respect to the rising edge of CLK.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
\overline{LBO}	Linear Burst Order	I	LOW	Burst order selection input. When \overline{LBO} is high the Interleaved burst sequence is selected. When \overline{LBO} is low the Linear burst sequence is selected. \overline{LBO} is a static input and it must not change during device operation.
\overline{OE}	Output Enable	I	LOW	Asynchronous output enable. \overline{OE} must be low to read data from the 71T656/58. When \overline{OE} is high the I/O pins are in a high-impedance state. \overline{OE} does not need to be actively controlled for read and write cycles. In normal operation, \overline{OE} can be tied low.
\overline{MS}	Smart ZBT™ Enable	I	LOW	Smart ZBT™ mode enable input. When \overline{MS} is low the Smart ZBT™ mode is selected. When \overline{MS} is high the original ZBT™ mode is selected. \overline{MS} is a static input and it must not change during device operation.
VDD	Power Supply	N/A	N/A	2.5V core power supply.
VDDO	Power Supply	N/A	N/A	2.5V I/O Supply.
VSS	Ground	N/A	N/A	Ground.

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NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	2.375	2.5	2.625	V
V _{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage - Inputs	1.7	—	V _{DD} + 0.3	V
V _{IH}	Input High Voltage - I/O	1.7	—	V _{DDQ} + 0.3	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

5002 tbl 03

NOTE:

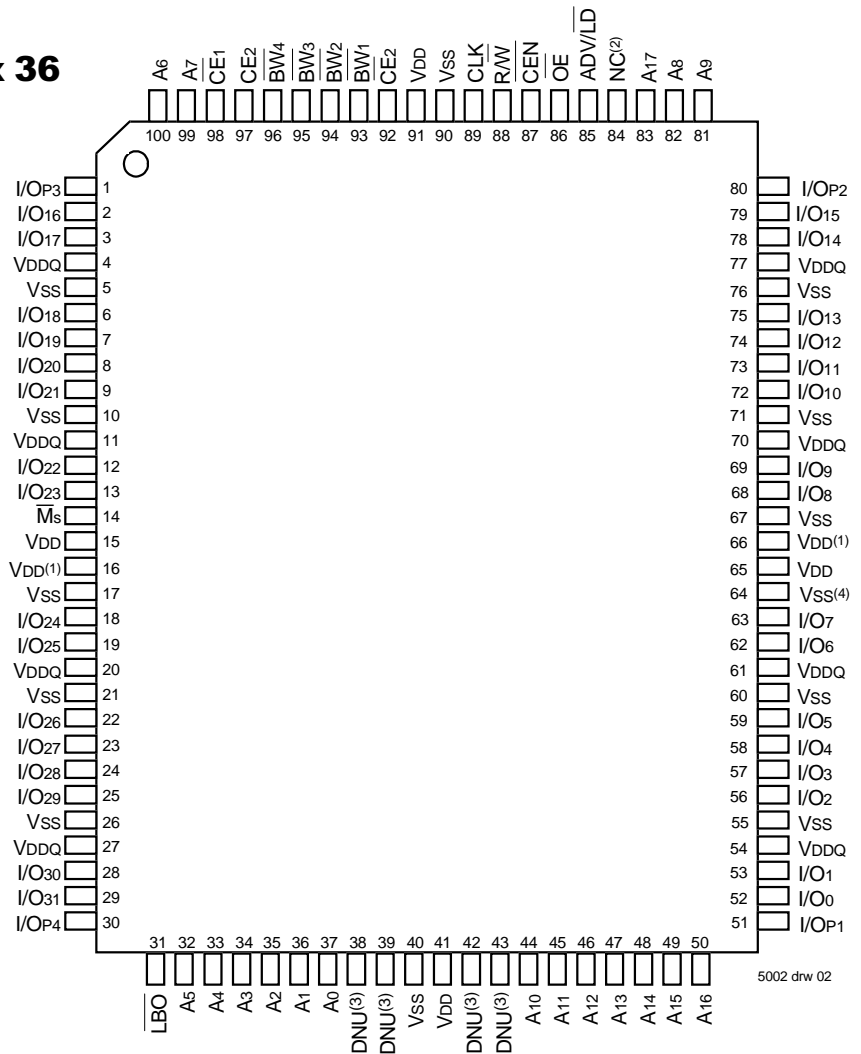
- V_{IL} (min.) = -0.8V for pulse width less than tcyc/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V _{SS}	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	0V	2.5V±5%	2.5V±5%

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Pin Configuration - 256K x 36



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Mode	\overline{Ms}
Smart ZBT™	V _{SS}
Original ZBT™	V _{DD}

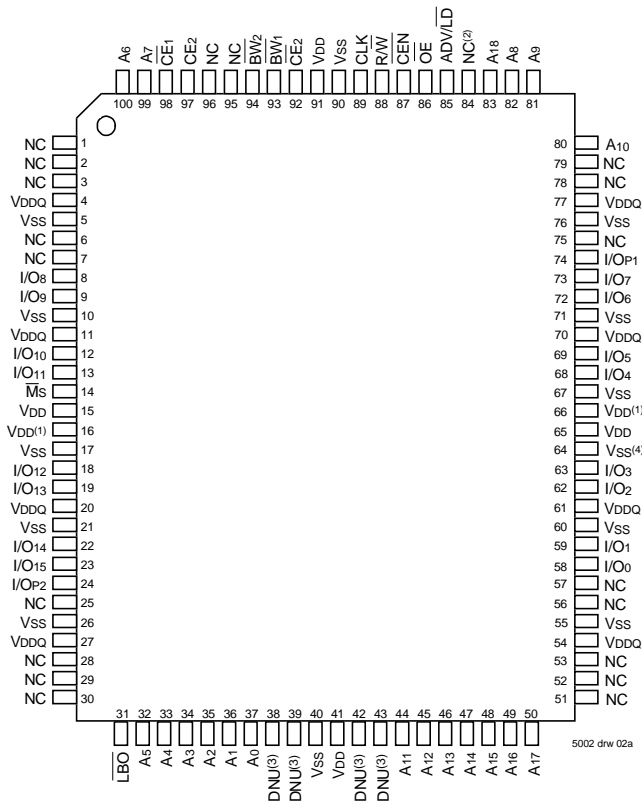
5002 tbl 05a

Top View TQFP

NOTES:

- Pins 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
- Pin 84 is reserved for a future 16M.
- DNU = Do not use
- Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$.

Pin Configuration - 512K x 18



Top View TQFP

NOTES:

1. Pins 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pin 84 is reserved for a future 16M.
3. DNU = Do not use
4. Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$.

Mode	$\bar{M}s$
Smart ZBT™	V _{SS}
Original ZBT™	V _{DD}

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Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +3.6	V
V _{TERM} ^(3,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD}	V
V _{TERM} ^(4,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD} +0.5	V
V _{TERM} ^(5,6)	Terminal Voltage with Respect to GND	-0.5 to V _{VDDQ} +0.5	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	2.0	W
I _{OUT}	DC Output Current	50	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{VDDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.

Capacitance

(T_A = +25°C, f = 1.0MHz, TQFP Package)

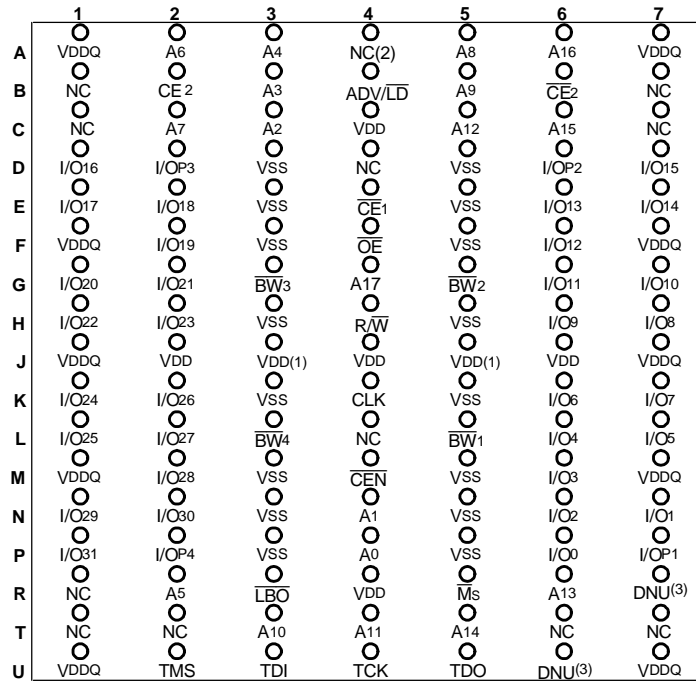
Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	5	pF
C _{IO}	I/O Capacitance	V _{OUT} = 3dV	7	pF

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NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration - 256K X 36 BGA(1,2,3)



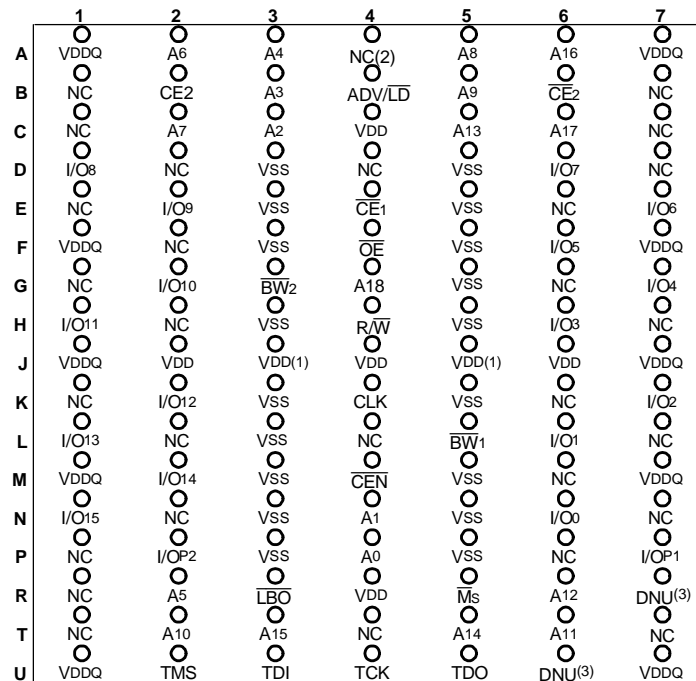
5002 drw 13A

Top View

Mode	Ms
Smart ZBT™	Vss
Original ZBT™	VDD

5002 tb1 05a

Pin Configuration - 512K X 18 BGA(1,2,3)



5002drw 13B

Top View

NOTES:

- J3 and J5 do not have to be directly connected to VDD as long as the input voltage is \geq VIH.
- A4 is reserved for future 16M.
- DNU = Do not use

Synchronous Truth Table⁽¹⁾

\overline{CEN}	R/W	Chip ⁽⁵⁾ Enable	ADV/LD	\overline{BW}_x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D ⁽⁷⁾
L	H	Select	L	X	External	X	LOAD READ	Q ⁽⁷⁾
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) ⁽²⁾	D ⁽⁷⁾
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) ⁽²⁾	Q ⁽⁷⁾
L	X	Deselect	L	X	X	X	DESELECT or STOP ⁽³⁾	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND ⁽⁴⁾	Previous Value

5002 tbl 08

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- When ADV/LD signal is sampled high, the internal burst counter is incremented. The $\overline{R/W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
- Deselect cycle is initiated when either \overline{CE}_1 , or \overline{CE}_2 is sampled high or CE₂ is sampled low) and ADV/LD is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
- When \overline{CEN} is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- To select the chip requires $\overline{CE}_1 = L$, $\overline{CE}_2 = L$, CE₂ = H on these chip enables. Chip is deselected if any one of the chip enables is false.
- Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
- Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes⁽¹⁾

OPERATION	R/W	\overline{BW}_1	\overline{BW}_2	$\overline{BW}_3^{(3)}$	$\overline{BW}_4^{(3)}$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/OP ₁) ⁽²⁾	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/OP ₂) ⁽²⁾	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/OP ₃) ^(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/OP ₄) ^(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5002 tbl 09

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- Multiple bytes may be selected during the same cycle.
- N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO}=VDD$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

5002 tbl 10

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table ($\overline{LBO}=VSS$)

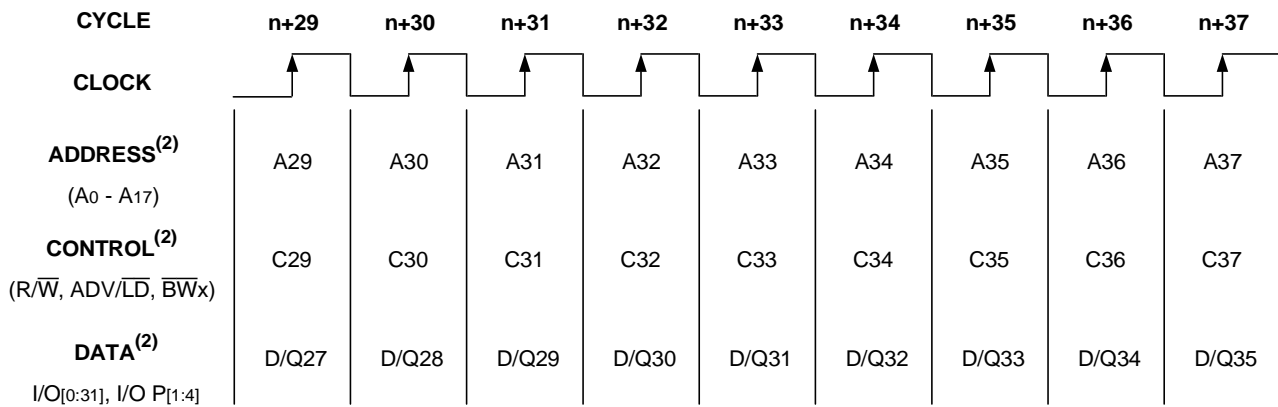
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

5002 tbl 11

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram⁽¹⁾



5002 drw 03

NOTES:

1. This assumes \overline{CEN} , $\overline{CE1}$, $CE2$, $\overline{CE2}$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles⁽²⁾

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(1)}$	\overline{CEN}	\overline{BWx}	\overline{OE}	I/O	Comments
n	A0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A1	H	L	L	L	X	L	Q0	Load read
n+3	X	X	L	H	L	X	L	Q0+1	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q1	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q2	Deselect or STOP
n+8	A3	L	L	L	L	L	L	Q2+1	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A4	L	L	L	L	L	X	D3	Load write
n+11	X	X	L	H	L	X	X	D3+1	Deselect or STOP
n+12	X	X	H	X	L	X	X	D4	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load write
n+14	A6	H	L	L	L	X	X	Z	Load read
n+15	A7	L	L	L	L	L	X	D5	Load write
n+16	X	X	H	X	L	L	L	Q6	Burst write
n+17	A8	H	L	L	L	X	X	D7	Load read
n+18	X	X	H	X	L	X	X	D7+1	Burst read
n+19	A9	L	L	L	L	L	L	Q8	Load write

5002 tbl 12

NOTES:

- $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.
- H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation⁽¹⁾

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	\overline{CEN}	\overline{BWx}	\overline{OE}	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q0	Contents of Address A0 Read Out

5002 tbl 13

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.

Burst Read Operation⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}\bar{x}$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q ₀₊₁	Address A ₀₊₁ Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q ₀₊₂	Address A ₀₊₂ Read Out, Inc. Count
n+5	A ₁	H	L	L	L	X	L	Q ₀₊₃	Address A ₀₊₃ Read Out, Load A ₁
n+6	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q ₁	Address A ₁ Read Out, Inc. Count
n+8	A ₂	H	L	L	L	X	L	Q ₁₊₁	Address A ₁₊₁ Read Out, Load A ₂

5002 tbl 14

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E} = L$ is defined as $\bar{C}\bar{E}_1 = L$, $\bar{C}\bar{E}_2 = L$ and $C\bar{E}_2 = H$. $\bar{C}\bar{E} = H$ is defined as $\bar{C}\bar{E}_1 = H$, $\bar{C}\bar{E}_2 = H$ or $C\bar{E}_2 = L$.

Write Operation⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}\bar{x}$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D ₀	Write to Address A ₀

5002 tbl 15

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E} = L$ is defined as $\bar{C}\bar{E}_1 = L$, $\bar{C}\bar{E}_2 = L$ and $C\bar{E}_2 = H$. $\bar{C}\bar{E} = H$ is defined as $\bar{C}\bar{E}_1 = H$, $\bar{C}\bar{E}_2 = H$ or $C\bar{E}_2 = L$.

Burst Write Operation⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}\bar{x}$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+3	X	X	H	X	L	L	X	D ₀₊₁	Address A ₀₊₁ Write, Inc. Count
n+4	X	X	H	X	L	L	X	D ₀₊₂	Address A ₀₊₂ Write, Inc. Count
n+5	A ₁	L	L	L	L	L	X	D ₀₊₃	Address A ₀₊₃ Write, Load A ₁
n+6	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+7	X	X	H	X	L	L	X	D ₁	Address A ₁ Write, Inc. Count
n+8	A ₂	L	L	L	L	L	X	D ₁₊₁	Address A ₁₊₁ Write, Load A ₂

5002 tbl 16

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{C}\bar{E} = L$ is defined as $\bar{C}\bar{E}_1 = L$, $\bar{C}\bar{E}_2 = L$ and $C\bar{E}_2 = H$. $\bar{C}\bar{E} = H$ is defined as $\bar{C}\bar{E}_1 = H$, $\bar{C}\bar{E}_2 = H$ or $C\bar{E}_2 = L$.

Read Operation with Clock Enable Used⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ \bar{LD}	$\bar{CE}^{(2)}$	\bar{CEN}	\bar{BW}_x	\bar{OE}	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A ₁	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+4	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+5	A ₂	H	L	L	L	X	L	Q ₀	Address A ₀ Read out (bus trans.)
n+6	A ₃	H	L	L	L	X	L	Q ₁	Address A ₁ Read out (bus trans.)
n+7	A ₄	H	L	L	L	X	L	Q ₂	Address A ₂ Read out (bus trans.)

5002 tbl 17

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Write Operation with Clock Enable Used⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ \bar{LD}	$\bar{CE}^{(2)}$	\bar{CEN}	\bar{BW}_x	\bar{OE}	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A ₁	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A ₂	L	L	L	L	L	X	D ₀	Write Data D ₀
n+6	A ₃	L	L	L	L	L	X	D ₁	Write Data D ₁
n+7	A ₄	L	L	L	L	L	X	D ₂	Write Data D ₂

5002 tbl 18

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{CE} = L$ is defined as $\bar{CE}_1 = L$, $\bar{CE}_2 = L$ and $CE_2 = H$. $\bar{CE} = H$ is defined as $\bar{CE}_1 = H$, $\bar{CE}_2 = H$ or $CE_2 = L$.

Read Operation with Chip Enable Used⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ $\bar{L}D$	$\bar{C}E^{(2)}$	$\bar{C}EN$	$\bar{B}Wx$	$\bar{O}E$	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A ₀	H	L	L	L	X	X	Z	Address and Control meet setup.
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read out. Load A ₁ .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q ₁	Address A ₁ Read out. Deselected.
n+7	A ₂	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q ₂	Address A ₂ Read out. Deselected.

5002 tbl 19

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{C}E = L$ is defined as $\bar{C}E_1 = L$, $\bar{C}E_2 = L$ and $CE_2 = H$. $\bar{C}E = H$ is defined as $\bar{C}E_1 = H$, $\bar{C}E_2 = H$ or $CE_2 = L$.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used⁽¹⁾

Cycle	Address	R/ \bar{W}	ADV/ $\bar{L}D$	$\bar{C}E^{(2)}$	$\bar{C}EN$	$\bar{B}Wx$	$\bar{O}E$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A ₀	L	L	L	L	L	X	Z	Address and Control meet setup.
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A ₁	L	L	L	L	L	X	D ₀	Address D ₀ Write in. Load A ₁ .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D ₁	Address D ₁ Write in. Deselected.
n+7	A ₂	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D ₂	Address D ₂ Write in. Deselected.

5002 tbl 20

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{C}E = L$ is defined as $\bar{C}E_1 = L$, $\bar{C}E_2 = L$ and $CE_2 = H$. $\bar{C}E = H$ is defined as $\bar{C}E_1 = H$, $\bar{C}E_2 = H$ or $CE_2 = L$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 2.5V \pm 5\%$)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{LI} $	Input Leakage Current	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	5	μA
$ I_{LI} $	\overline{LBO} Input Leakage Current ⁽¹⁾	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	30	μA
$ I_{LO} $	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{DDQ}$, Device Deselected	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +6mA, V_{DD} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -6mA, V_{DD} = \text{Min.}$	2.0	—	V

5002 tbl 21

NOTE:

1. The \overline{LBO} pin will be internally pulled to V_{DD} if it is not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ ($V_{DD} = 2.5V \pm 5\%$)

Symbol	Parameter	Test Conditions	200MHz	166MHz	133MHz	100MHz	Unit
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, $ADV/\overline{LD} = X, V_{DD} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$	400	350	300	250	mA
$ISB1$	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$	40	40	40	40	mA
$ISB2$	Clock Running Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$	130	120	110	100	mA
$ISB3$	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}, V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$	40	40	40	40	mA

5002 tbl 22

NOTES:

- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$; $f=0$ means no input lines are changing.
- For I/Os $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$.

AC Test Load

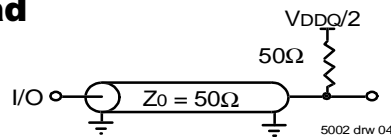


Figure 1. AC Test Load

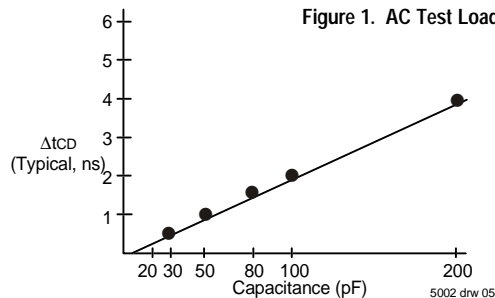


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	($V_{DDQ}/2$)
Output Timing Reference Levels	($V_{DDQ}/2$)
AC Test Load	See Figure 1

5002 tbl 23

AC Electrical Characteristics

(V_{DD} = 2.5V±5%, T_A = 0 to 70°C)

(Smart ZBT™ Mode, $\bar{M}s = V_{SS}$)

Symbol	Parameter	133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	7.5	—	10	—	ns
t _F ⁽¹⁾	Clock Frequency	—	133	—	100	MHz
t _{CH} ⁽²⁾	Clock High Pulse Width	2.2	—	3.2	—	ns
t _{CL} ⁽²⁾	Clock Low Pulse Width	2.2	—	3.2	—	ns
Output Parameters						
t _{CD}	Clock High to Valid Data	—	(t _{CYC} / 3) + 2.0 ⁽⁵⁾	—	(t _{CYC} / 3) + 2.0 ⁽⁵⁾	ns
t _{CDL}	Clock High to Data Change	(t _{CYC} / 3) - 0.2 ⁽⁵⁾	—	(t _{CYC} / 3) - 0.2 ⁽⁵⁾	—	ns
t _{CLZ} ^(3,4)	Clock High to Output Active	(t _{CYC} / 3) - 0.2 ⁽⁵⁾	—	(t _{CYC} / 3) - 0.2 ⁽⁵⁾	—	ns
t _{CHZ} ^(3,4)	Clock High to Data High-Z	1.5	3	1.5	3.3	ns
t _{OE}	Output Enable Access Time	—	4.2	—	5	ns
t _{OLZ} ^(3,4)	Output Enable Low to Data Active	0	—	0	—	ns
t _{OHZ} ^(3,4)	Output Enable High to Data High-Z	—	4.2	—	5	ns
Set Up Times						
t _{SE}	Clock Enable Setup Time	1.7	—	2.0	—	ns
t _{SA}	Address Setup Time	1.7	—	2.0	—	ns
t _{SD}	Data In Setup Time	1.7	—	2.0	—	ns
t _{SW}	Read/Write (R/W) Setup Time	1.7	—	2.0	—	ns
t _{ADV}	Advance/Load (ADV/LD) Setup Time	1.7	—	2.0	—	ns
t _{SC}	Chip Enable/Select Setup Time	1.7	—	2.0	—	ns
t _{SB}	Byte Write Enable ($\bar{B}Wx$) Setup Time	1.7	—	2.0	—	ns
Hold Times						
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.5	—	0.5	—	ns
t _{HW}	Read/Write (R/W) Hold Time	0.5	—	0.5	—	ns
t _{HADV}	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
t _{HB}	Byte Write Enable ($\bar{B}Wx$) Hold Time	0.5	—	0.5	—	ns

5002 tbl 23a

NOTES:

- t_F = 1/t_{CYC}.
- Measured as HIGH above 0.6V_{DD0} and LOW below 0.4V_{DD0}.
- Transition is measured ±200mV from steady-state.
- These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
- Smart ZBT functionality only guaranteed at 66 MHz ≤ f ≤ 133 MHz.

AC Electrical Characteristics

(VDD = 2.5V +/-5%, TA = 0 to 70°C)

(Traditional ZBT™ Mode, $\bar{M}s = VDD$)

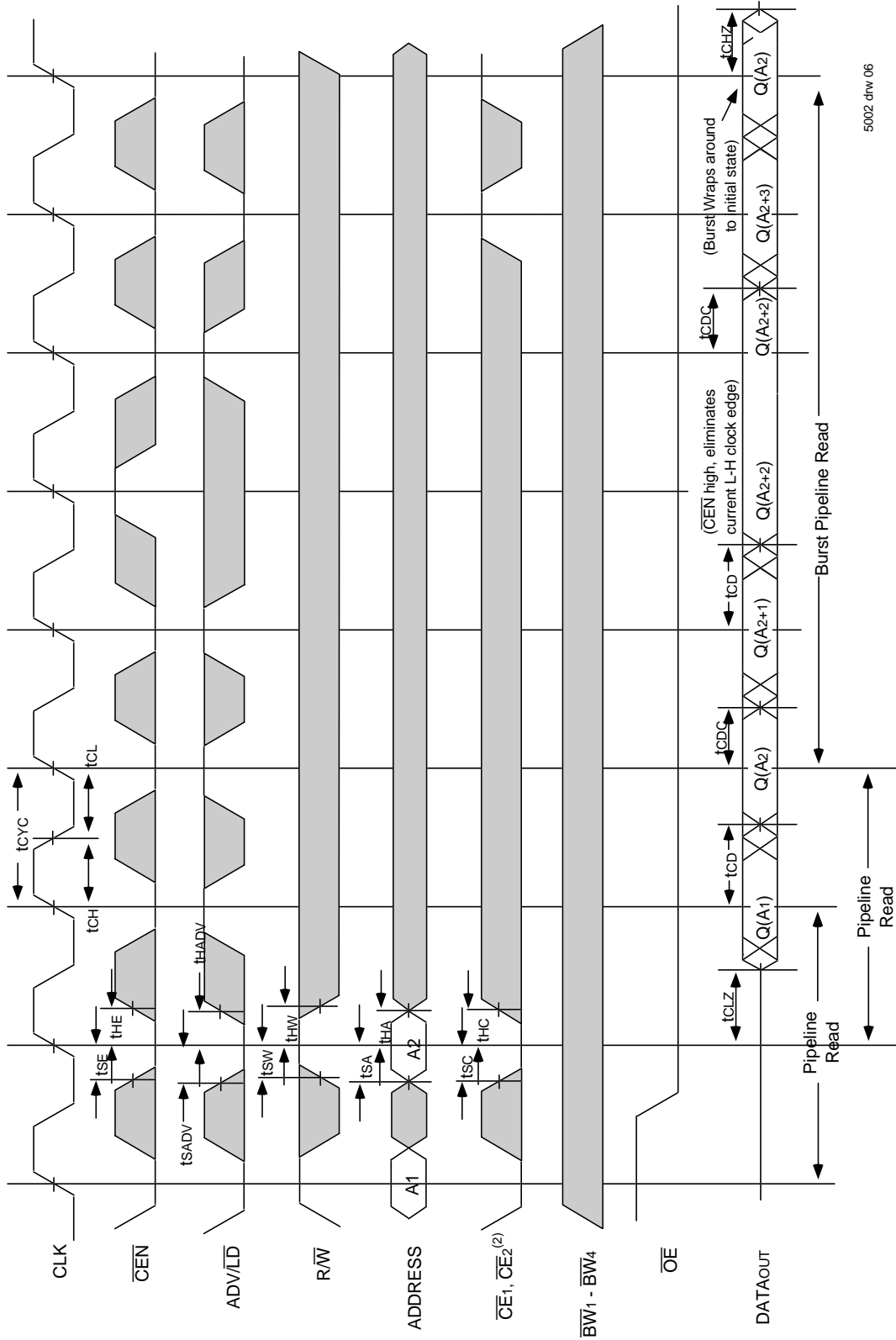
Symbol	Parameter	200MHz		166MHz		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	5	—	6	—	7.5	—	10	—	ns
t _F ⁽¹⁾	Clock Frequency	—	200	—	166	—	133	—	100	MHz
t _{CH} ⁽²⁾	Clock High Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns
t _{CL} ⁽²⁾	Clock Low Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns
Output Parameters										
t _{CD}	Clock High to Valid Data	—	3.2	—	3.5	—	4.2	—	5	ns
t _{CDc}	Clock High to Data Change	1	—	1	—	1	—	1	—	ns
t _{CLZ} ^(3,4,5)	Clock High to Output Active	1	—	1	—	1	—	1	—	ns
t _{CHZ} ^(3,4,5)	Clock High to Data High-Z	1	3	1	3	1	3	1	3.3	ns
t _{OE}	Output Enable Access Time	—	3.2	—	3.5	—	4.2	—	5	ns
t _{OLZ} ^(3,4)	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t _{OHZ} ^(3,4)	Output Enable High to Data High-Z	—	3.5	—	3.5	—	4.2	—	5	ns
Set Up Times										
t _{SE}	Clock Enable Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SA}	Address Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SD}	Data In Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SW}	Read/Write (R/W) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{ADV}	Advance/Load (ADV/LD) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SC}	Chip Enable/Select Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SB}	Byte Write Enable (BWx) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
Hold Times										
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HW}	Read/Write (R/W) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HADV}	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HB}	Byte Write Enable (BWx) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

NOTES:

- t_F = 1/t_{CYC}.
- Measured as HIGH above 0.6V_{DD0} and LOW below 0.4V_{DD0}.
- Transition is measured ±200mV from steady-state.
- These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
- To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 2.625V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 2.375V).

5002 tbl 24

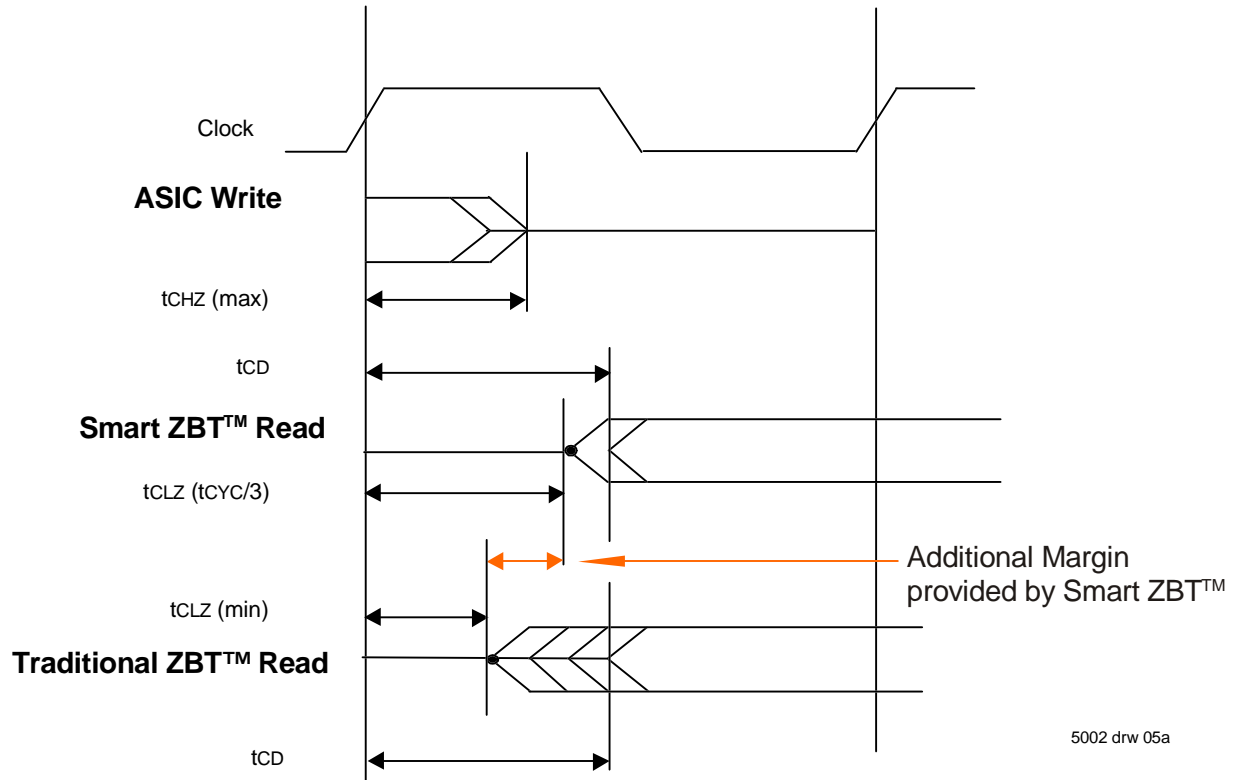
Timing Waveform of Read Cycle(1,2,3,4)



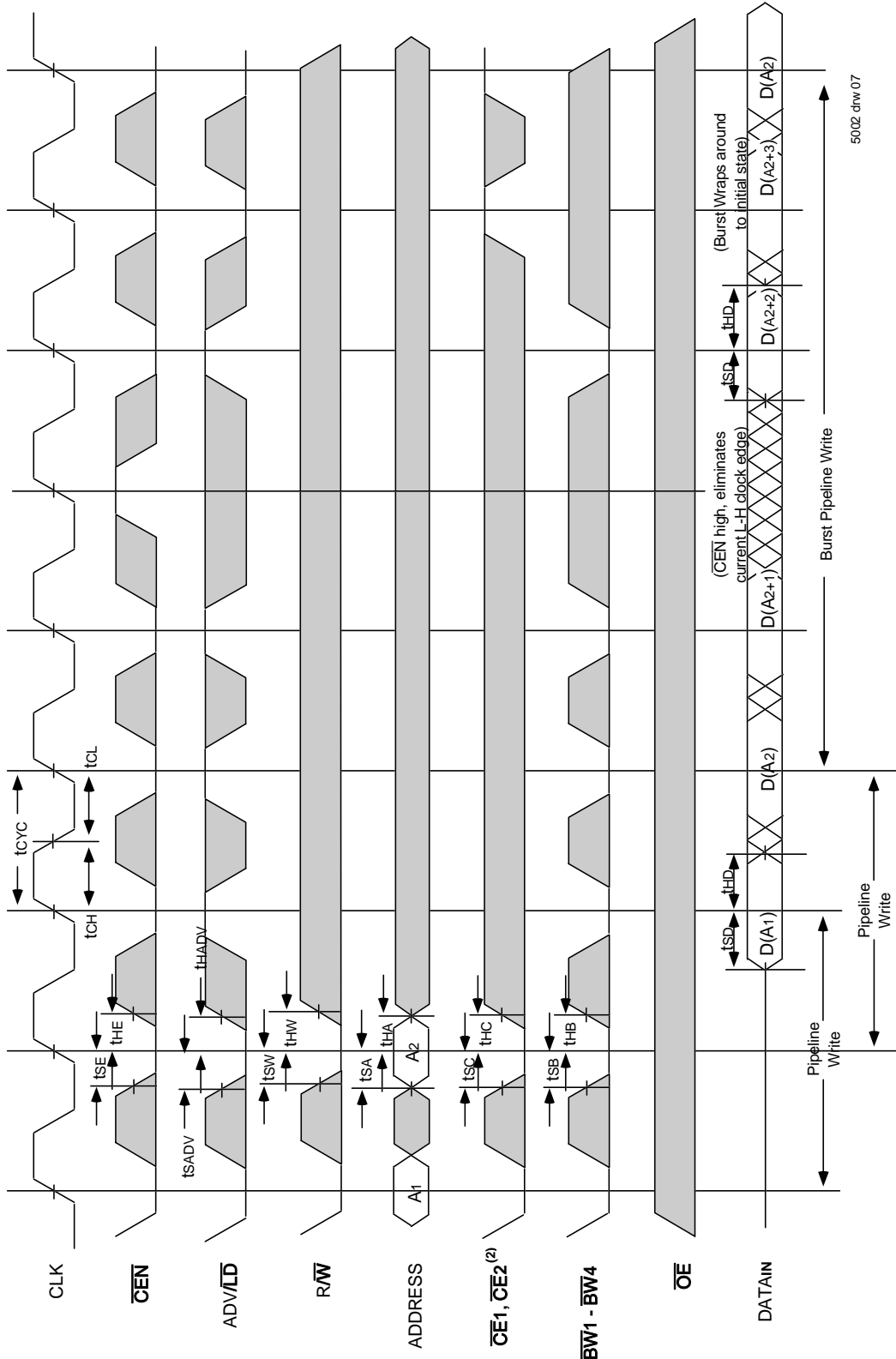
NOTES:

1. $Q(A_1)$ represents the first output from the external address A_1 . $Q(A_2)$ represents the first output from the external address A_2 ; $Q(A_2-1)$ represents the next output data in the burst sequence of the base address A_2 , etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

Smart ZBT™ Timing



Timing Waveform of Write Cycles(1,2,3,4,5)

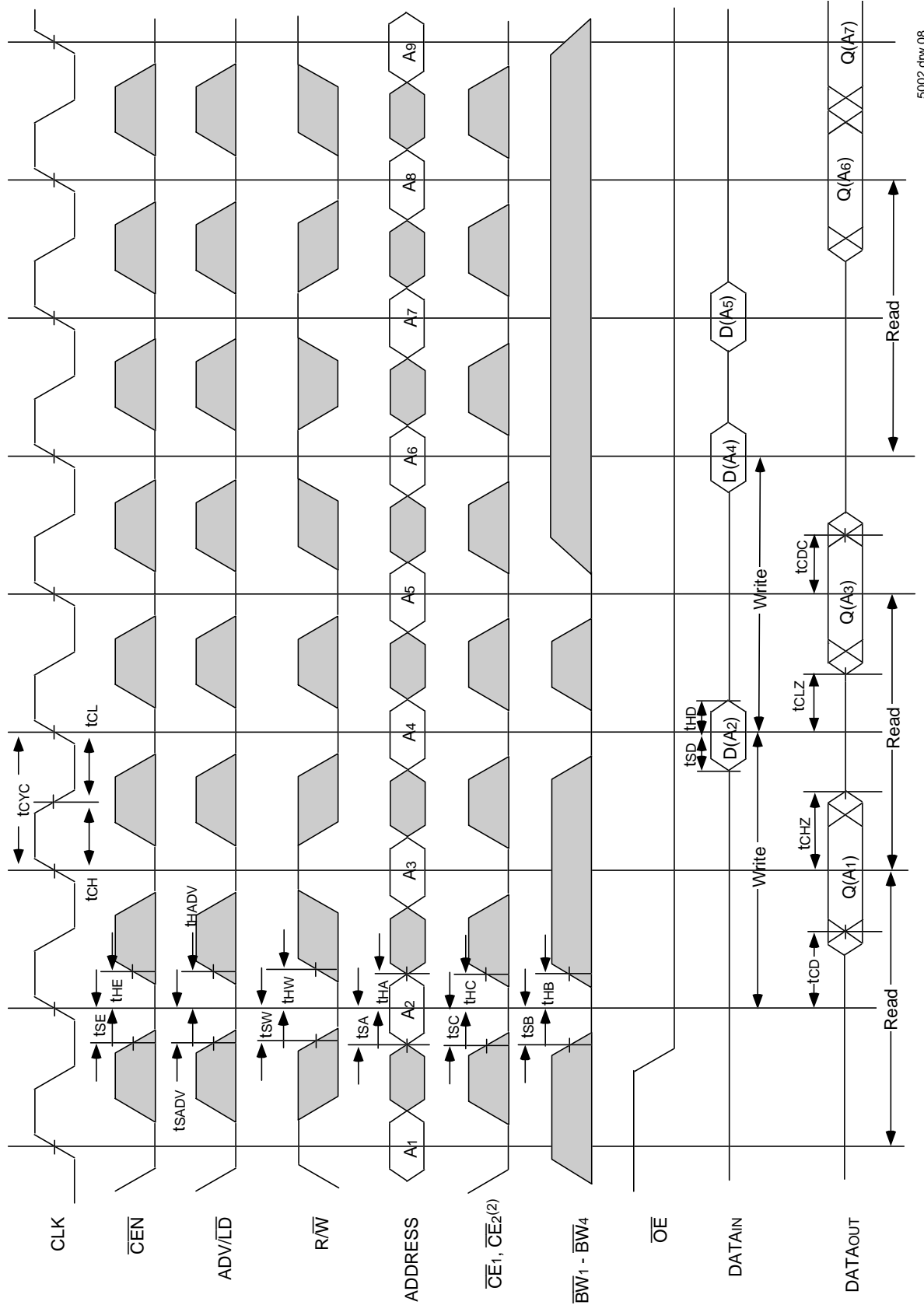


5002 drw 07

NOTES:

1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst; sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. RW is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the RW signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles(1.2.3)

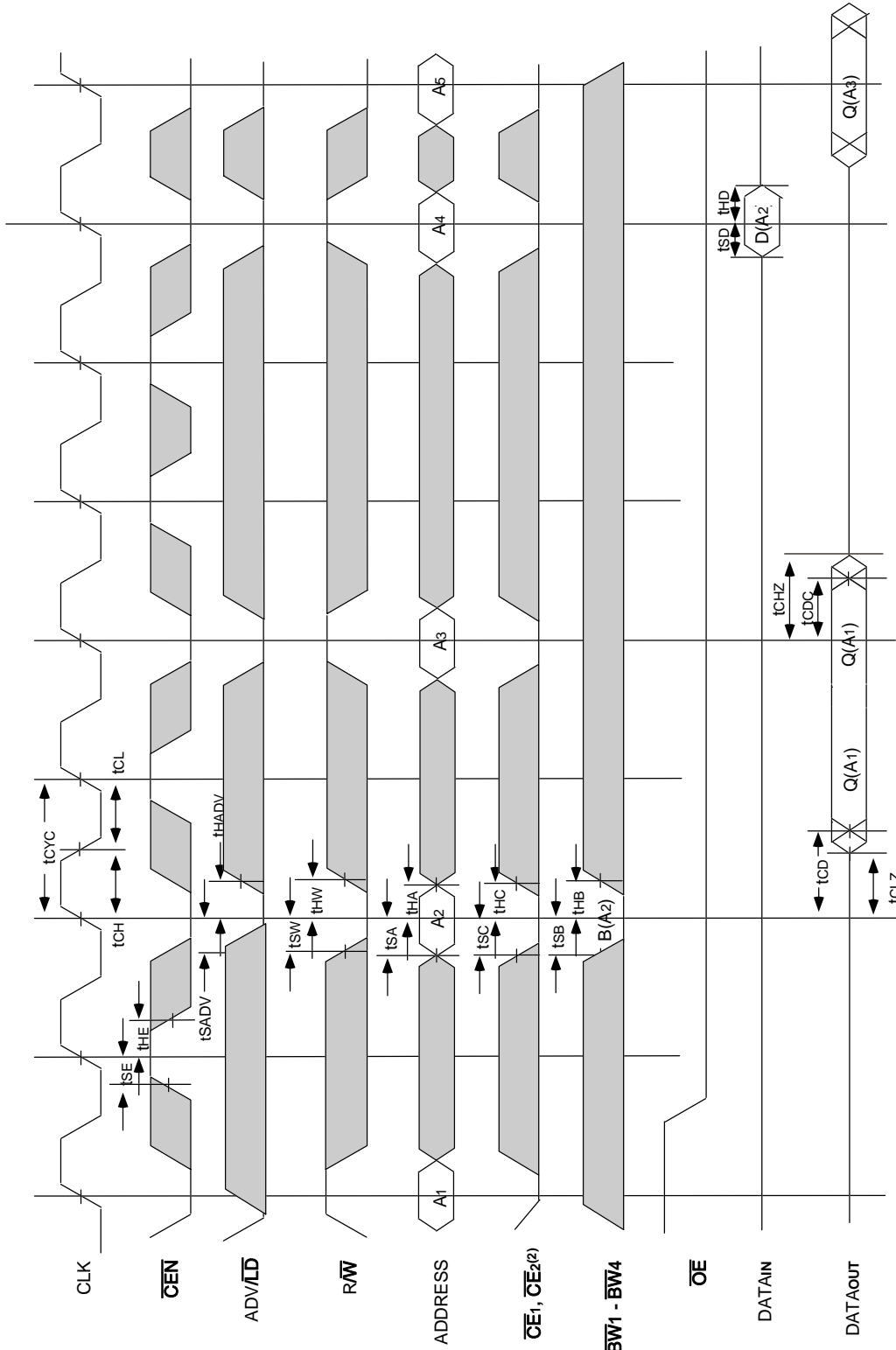


5002 drw 08

NOTES:

1. O (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE1}$ and $\overline{CE2}$ signals. For example, when $\overline{CE1}$ and $\overline{CE2}$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (\overline{BWx}) must be valid on all write and burst-write cycles. A write cycle is initiated when \overline{RW} signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CEN}}$ Operation (1,2,3,4)

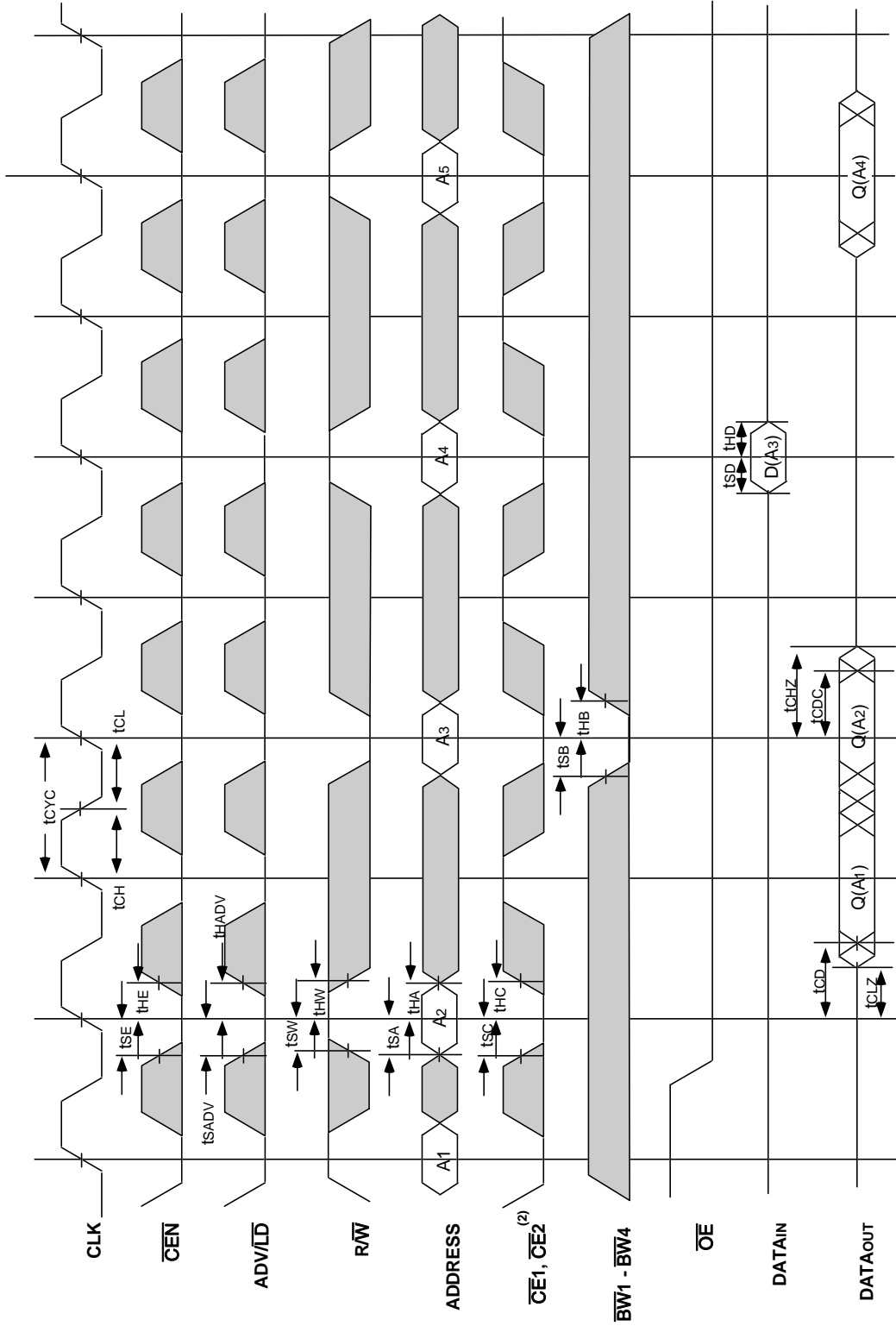


5002 drw 09

NOTES:

1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ signals. For example, when $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BWx}}$) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{R/W}}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of \overline{CS} Operation(1,2,3,4)

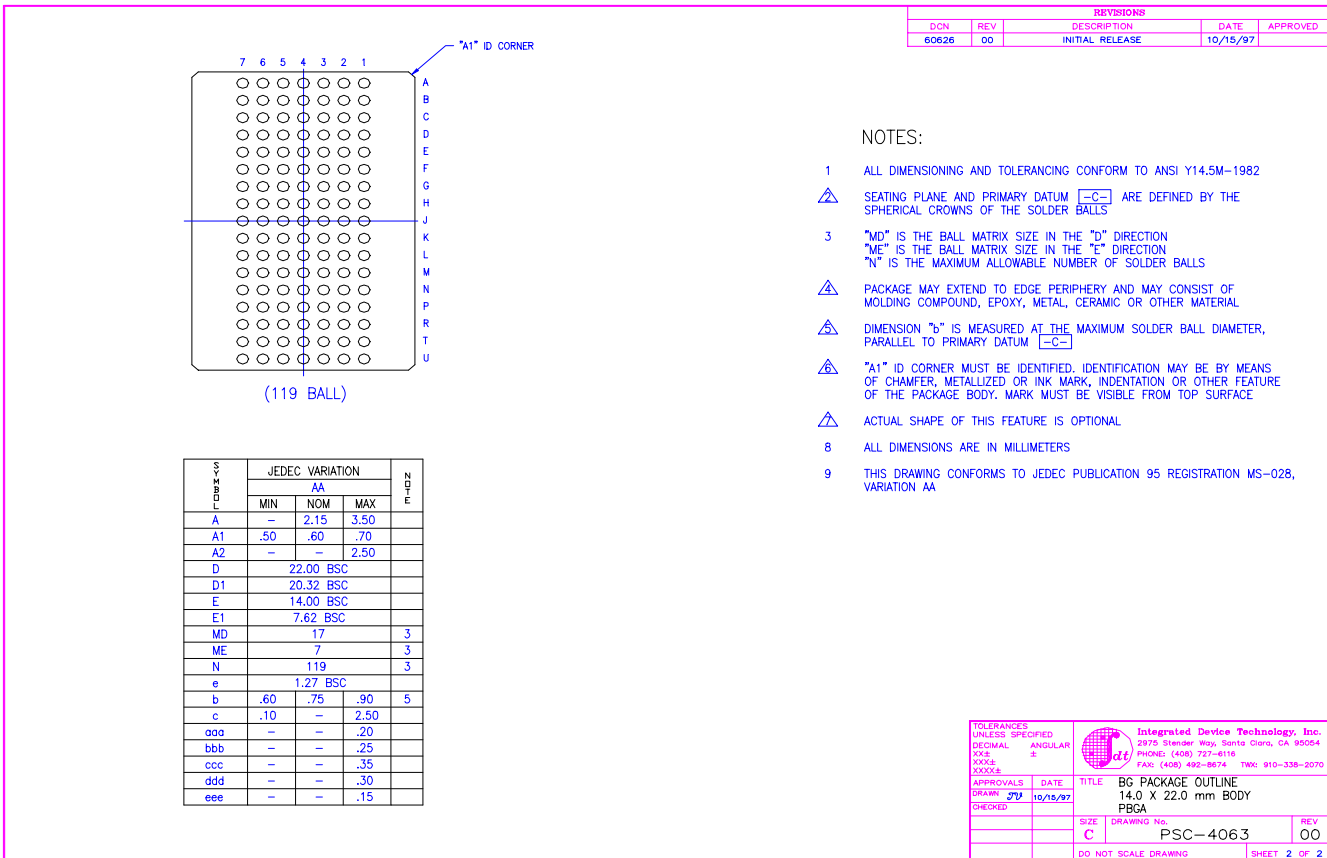
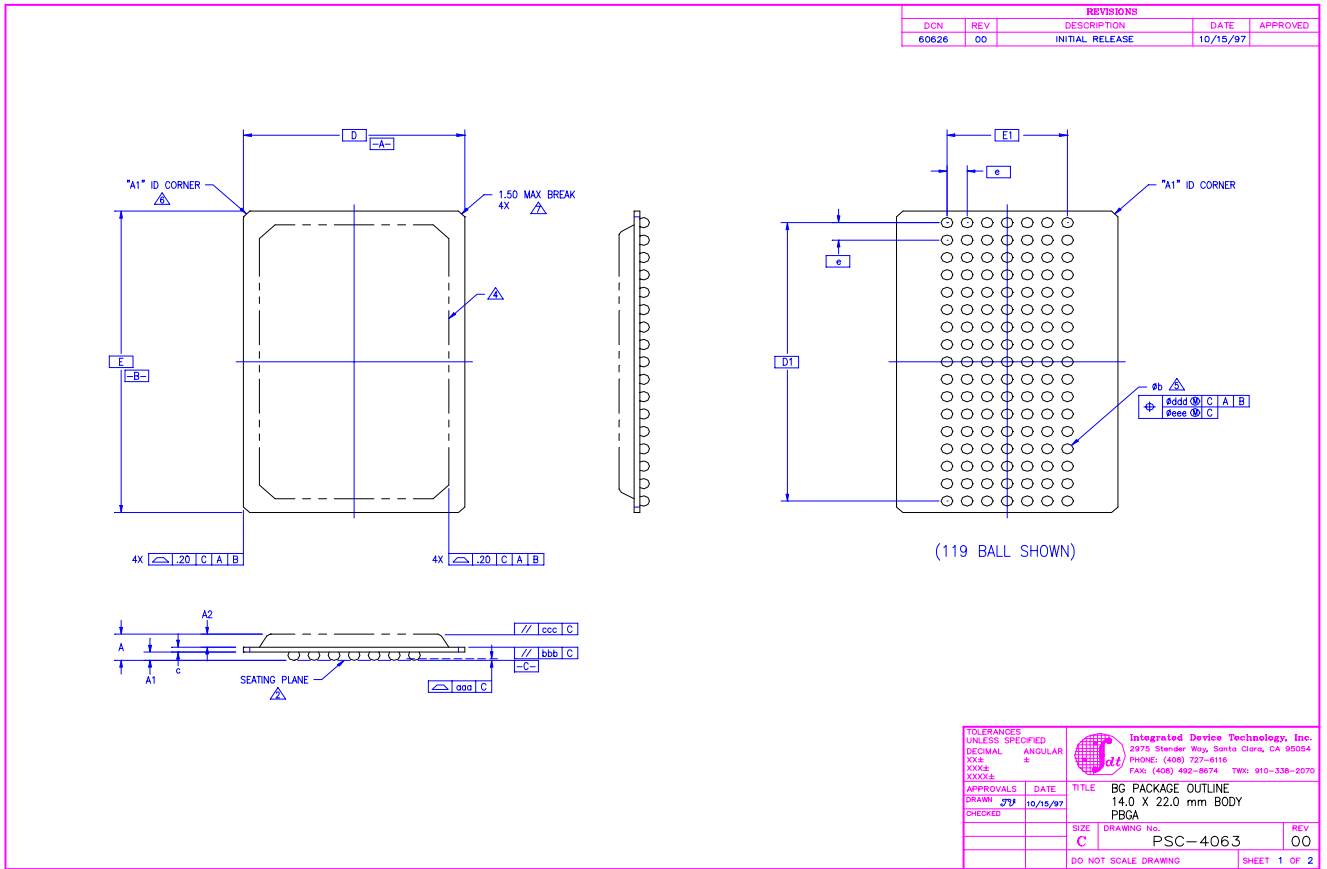


5002 drw 10

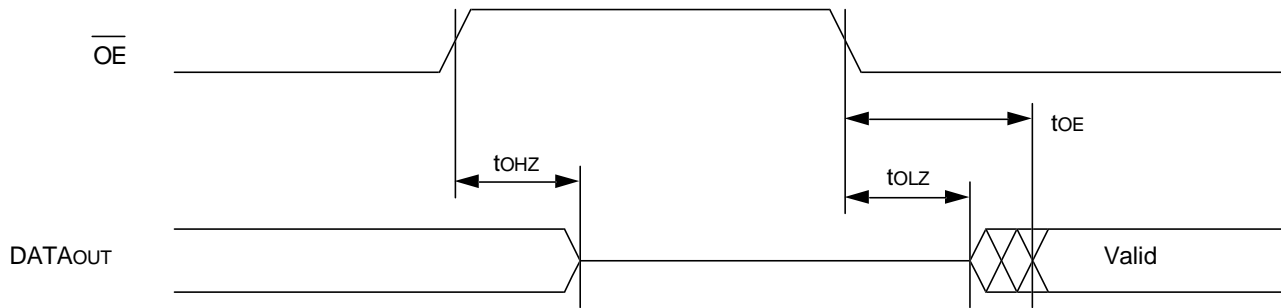
NOTES:

1. Q(A₁) represents the first output from the external address A₁. D(A₃) represents the input data to the SRAM corresponding to address A₃.
2. $\overline{CE2}$ timing transitions are identical but inverted to the $\overline{CE1}$ and $\overline{CE2}$ signals. For example, when $\overline{CE1}$ and $\overline{CE2}$ are LOW on this waveform, $\overline{CE2}$ is HIGH.
3. \overline{CEN} when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when \overline{RW} signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

119-Lead Ball Grid Array (BGA) Package Diagram Outline



Timing Waveform of \overline{OE} Operation⁽¹⁾

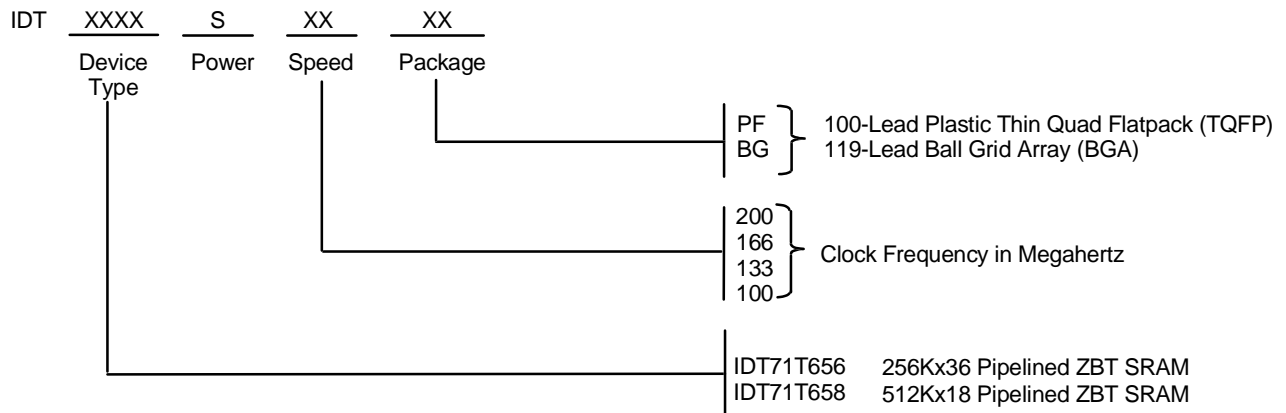


5002 drw 11

NOTE:

1. A read operation is assumed to be in progress.

Ordering Information



5002 drw 12

Datasheet Document History

7/26/99		Updated to new format; posted on website
8/23/99		Added Smart ZBT™ functionality
	Pp. 4, 5	Added Note 4 and changed pins 38, 42, and 43 to DNU
	Pg. 6	Changed B2 to CE2 and U6 to DNU
	Pg. 15	Improved t_{CD} and $t_{OE(MAX)}$ at 166MHz Revised $t_{CHZ(MIN)}$ for $f \leq 133$ MHz Revised $t_{OHZ(MAX)}$ for $f \leq 133$ MHz Improved t_{CH} , t_{CL} for $f \leq 166$ MHz Improved setup times for 100–200 MHz
	Pg. 24	Added Datasheet Document History
10/4/99	Pg. 14	Revised AC Electrical Characteristics table
	Pg. 15	Revised t_{CHZ} to match t_{CLZ} and t_{DC} at 133MHz and 100MHz



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