Dense-Pac Microsystems, Inc.

32KX8 BASED

CMOS SRAM FAMILY

DESCRIPTION:

The Dense-Pac 32K X 8 family consists of asynchronous Static Random Access Memories (SRAMs), complete with memory interface logic and on-board capacitors, available in the organizations and packages described below.

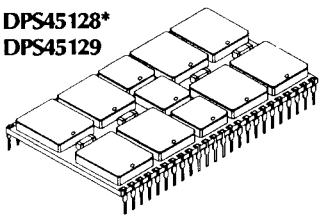
These memories are ideally suited for high-performance applications where fast access times and ease of use are required.

FEATURES:

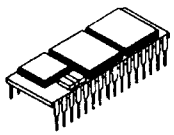
- Organizations Available:
  - DPS4648 - 64K X 8
  - DPS4968 - 96K X 8
  - DPS8M624 - 64K X 16
  - DPS8M612 - 32K X 16
  - DPS41288 - 128K X 8
  - DPS42568 - 256K X 8, 128K X 16
  - DPS45128 - 512K X 8
  - DPS45129 - 256K X 16
  - DPS96122 - 256K X 16, 512K X 8
- Fast Access Times: 85, 100, 120, 150ns (max)
- Completely Static Operation: No Clock or Refresh Needed
- Single +5V Power Supply ± 10% Tolerance
- Separate Battery Backup Supply Pins on the DPS45128
- TTL Compatible
- Low Data Retention Voltage: 2.0V Min.
- Standard Package:
  - 32-Pin DIP - DPS4648, DPS4968, DPS41288
  - 40-Pin DIP - DPS8M624, DPS8M612
  - 48-Pin DIP - DPS45128, DPS45129
  - 68-Pin DIP - DPS96122
  - 54-Pin Dual-Leaded SIP - DPS42568

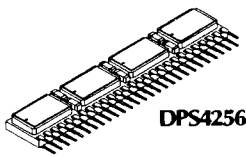
PIN NAMES	
A0-A19	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{CET}$, $\overline{CETA}$-$\overline{CETH}$	Top Chip Enables
$\overline{CEB}$, $\overline{CEBA}$-$\overline{CEBH}$	Bottom Chip Enables
$\overline{OE}$	Output Enable
$\overline{OET}$, $\overline{OEB}$	Top, Bottom Output Enables
$\overline{WE}$	Write Enable
$\overline{WET}$, $\overline{WEB}$	Top, Bottom Write Enables
$\overline{BEN}$	Buffer Enable
$\overline{UB}$, $\overline{LB}$	Upper, Lower Byte Control
BDIR	Buffer Direction
BV_{DD}	Power to Buffer
V_{DD}	Power (+5V)
V_{SS}	Ground
NC	No Connect

DPS45128*
DPS45129



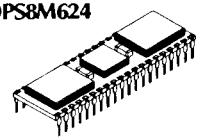
DPS4648
DPS4968
DPS41288

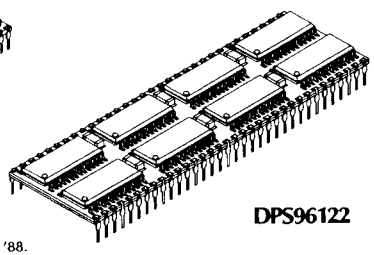




DPS42568

DPS8M612
DPS8M624

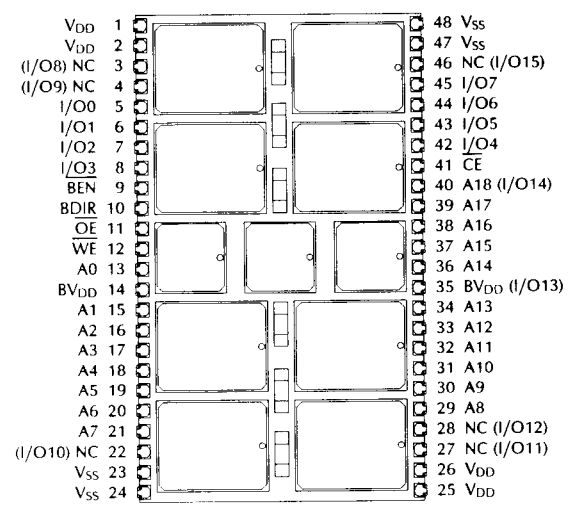




DPS96122

* Co-fired version available Q4 '88.

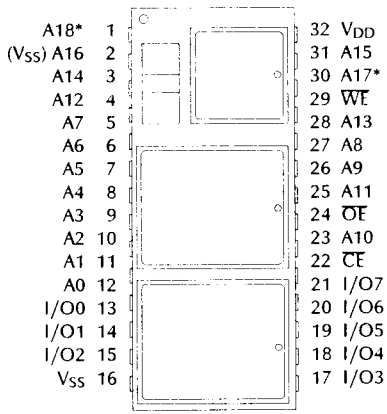
MODULE PIN-OUT DIAGRAMS



NOTE: Pin names for the DPS45129 are in parenthesis where they differ from the DPS45128.

DPS45128, DPS45129

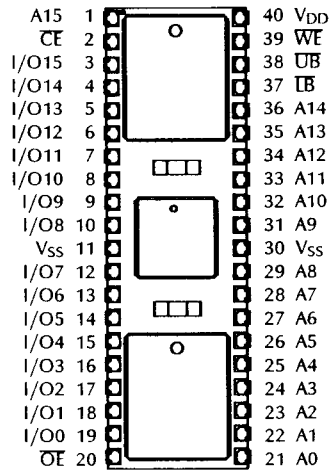
MODULE PIN-OUT DIAGRAMS (Continued)



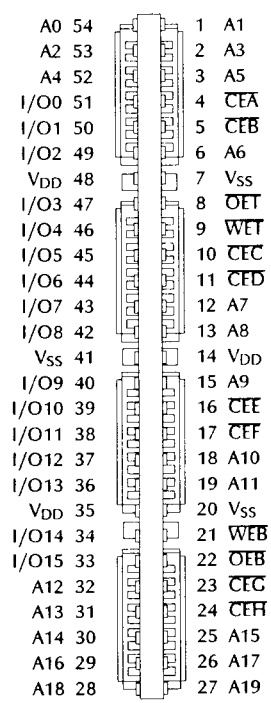
NOTE: Pin 2, for DPS4968 is in parentheses where it differs from the DPS4648 and the DPS41288.

* Design Engineers should allocate in designs pins 1 and 30 for address lines A18 & A17, respectively, for 256K X 8 and 512K X 8 versions.

DPS4968, DPS4648, DPS41288

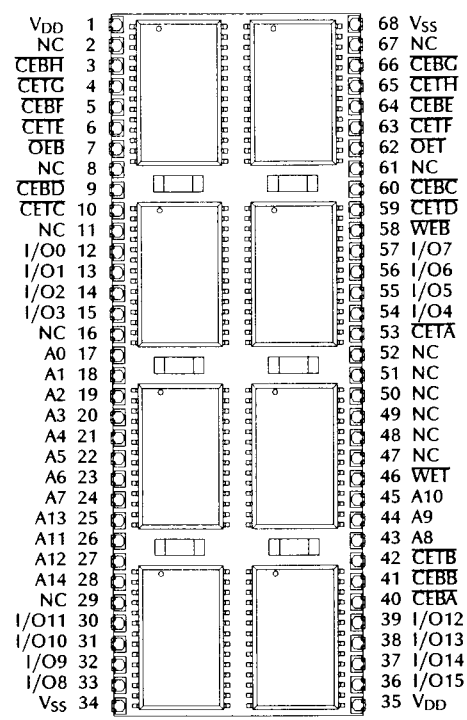


DPS8M612, DPS8M624



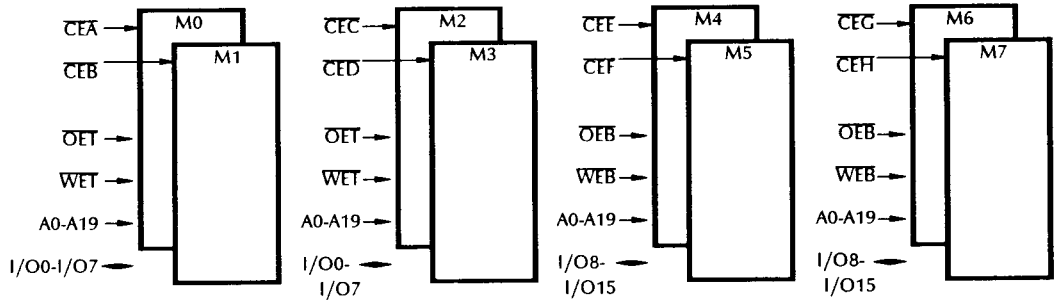
BOTTOM VIEW

DPS42568

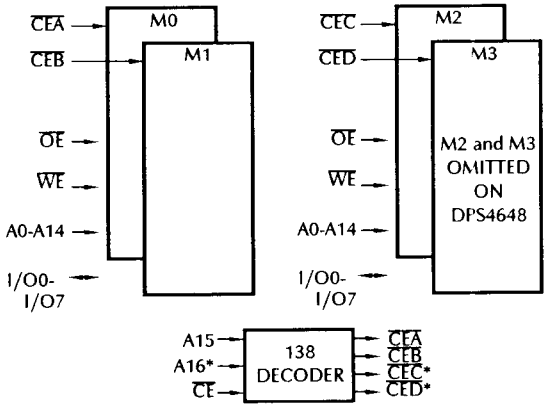


DPS96122

FUNCTIONAL BLOCK DIAGRAMS

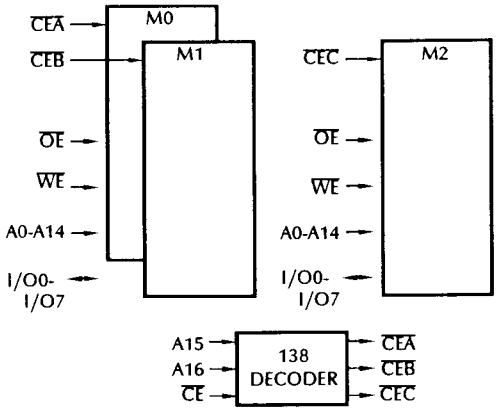


DPS42568

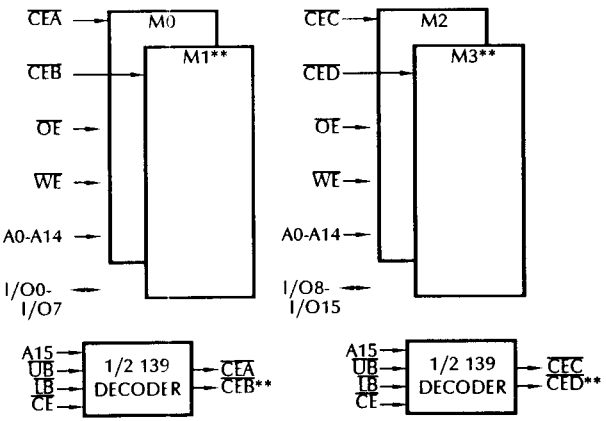


* Not applicable to the DPS4648

DPS4648, DPS41288



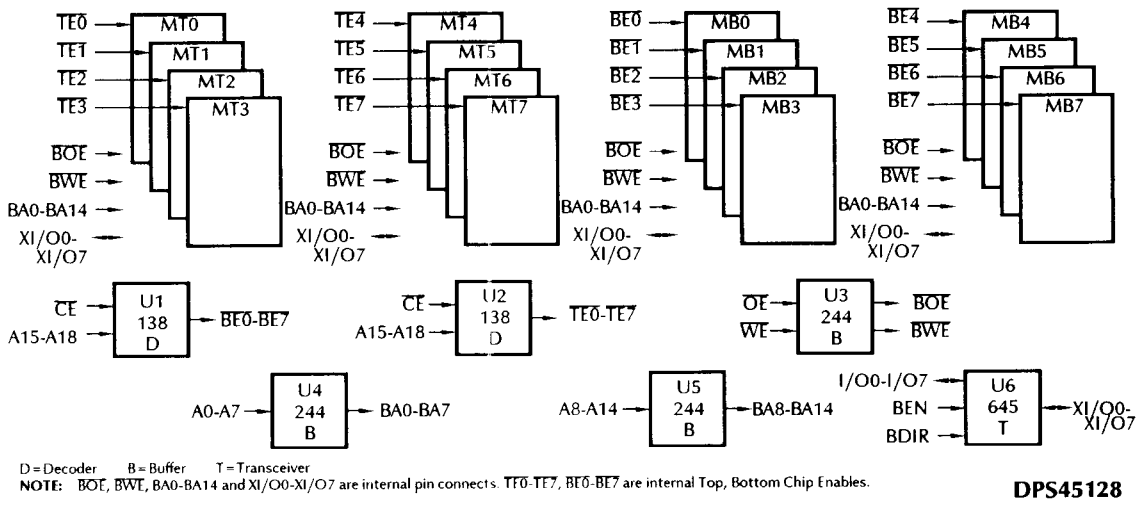
DPS4968



** Not applicable to the DPS8M612

DPS8M612, DPS8M624

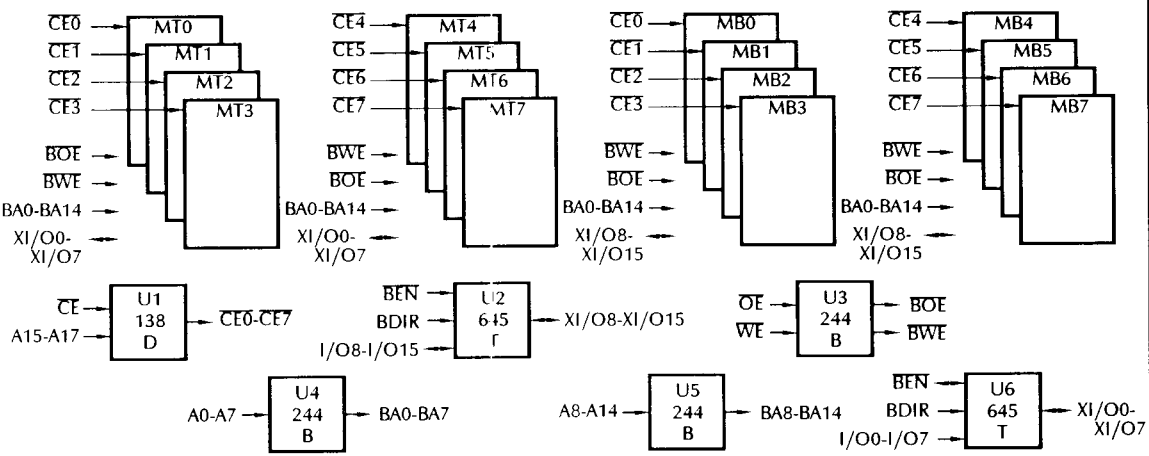
FUNCTIONAL BLOCK DIAGRAMS (Continued)



D = Decoder B = Buffer T = Transceiver

NOTE: $\overline{BOE}$, $\overline{BWE}$, BA0-BA14 and XI/O0-XI/O7 are internal pin connects. $\overline{TE0}$-$\overline{TE7}$, $\overline{BE0}$-$\overline{BE7}$ are internal Top, Bottom Chip Enables.

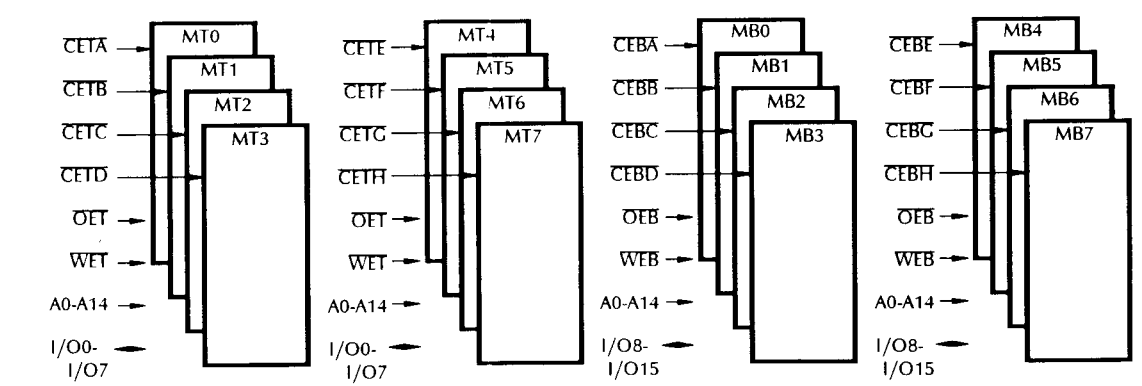
DPS45128



D = Decoder B = Buffer T = Transceiver

NOTE: $\overline{BOE}$, $\overline{BWE}$, BA0-BA14 and XI/O0-XI/O15 are internal pin connects. $\overline{CE0}$-$\overline{CE7}$ are internal Chip Enables.

DPS45129



DPS96122

DC OPERATING CHARACTERISTICS: Over Operating Ranges

Symbol	Characteristics	Test Conditions		DPS4648 Max.	DPS4968 Max.	DPS41288 Max.	DPS42568 Max.	DPS45128 Max.	DPS45129 Max.	DPS8M612 Max.	DPS8M624 Max.	DPS96122 Max.	Unit
I_{IN}	Input Leakage Current (All Inputs)	$\overline{CE}=V_{IH}$ $V_{IN}=0.V$ and 5.5V	M	±10	±10	±10	±20	±20	±20	±10	±10	-	µA
			I	±10	±10	±10	±20	±20	±20	±10	±10	±20	
			C	±10	±10	±10	±20	±20	±20	±10	±10	±20	
I_{OUT}	Output Leakage Current (On Data Output)	$\overline{CE}=V_{IH}$ $V_{OUT}=0.V$ and 5.5V	M	±10	±10	±10	±20	±20	±20	±10	±10	-	µA
			I	±10	±10	±10	±20	±20	±20	±10	±10	±20	
			C	±10	±10	±10	±20	±20	±20	±10	±10	±20	
I_{CC1}	Operating Power Supply Current (Static)	$\overline{CE}=V_{IL}$ Output Open	M	22	24	26	47	110	130	35	39	50(63)	mA
			I	22	24	26	47	110	130	35	39	50(63)	
			C	22	24	26	47	110	130	35	39	50(63)	
I_{CC2}	Operating Power Supply Current (Dynamic)	Min. Read Cycle Duty = 100%	M	67	70	75	137	285	355	125	129	95(153)	mA
			I	67	70	75	137	285	355	125	129	95(153)	
			C	67	70	75	137	285	355	125	129	95(153)	
I_{SB1}	Standby Power Supply Current	See Note 1	M	0.50	0.65	0.80	1.10	25	25	0.50	0.80	2.00	mA
			I	0.25	0.35	0.40	0.70	25	25	0.25	0.40	1.40	
			C	0.17	0.25	0.30	0.45	25	25	0.17	0.30	0.90	
I_{SB2}	Standby Power	$\overline{CE}=V_{IH}$	M	9	11	13	21	115	115	9	13	37	mA
			I	9	11	13	21	115	115	9	13	37	
			C	9	11	13	21	115	115	9	13	37	
I_{CCDR2}	Data Retention Current	$V_{DR}=2.0V$	M	300	350	400	550	1900	1900	300	400	900	µA
			I	150	165	200	260	800	500	150	200	400	
			C	50	60	70	100	300	300	50	70	120	
I_{CCDR3}	Data Retention Current	$V_{DR}=3.0V$	M	500	550	600	850	3000	3000	400	600	1350	µA
			I	200	225	250	400	1200	1200	200	250	600	
			C	75	85	100	150	450	450	75	100	200	

NOTE: Characteristics for DPS96122 256K x 16 organization are listed in parenthasis, the 512K x 8 organization characteristics are listed first.

DC OUTPUT CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	$I_{OH}=-1.0mA$	2.4	-	V
V_{OL}	LOW Voltage	$I_{OL}=2.1mA$	-	0.4	V

RECOMMENDED OPERATING RANGE[2]

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2	-	$V_{DD}+.3$	V
V_{IL}	Input LOW Voltage	-0.5[3]		0.8	V

ABSOLUTE MAXIMUM RATINGS[4]

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Temperature Under Bias	-55 to +125	°C
Supply Voltage [2]	-0.5 to + 7.0	V
Input Voltage [2]	-0.5 to V_{DD} + 0.5	V
Output Voltage [2]	-0.5 to V_{DD} + 0.5	V

TRUTH TABLE

Mode	Chip Enable	Write Enable	Output Enable	Power Level	I/O Pin
Not Selected	HIGH	Don't Care	Don't Care	Standby	HIGH-Z
D_{OUT} Disable	LOW	HIGH	HIGH	Active	HIGH-Z
Read	LOW	HIGH	LOW	Active	D_{OUT}
Write	LOW	LOW	Don't Care	Active	D_{IN}

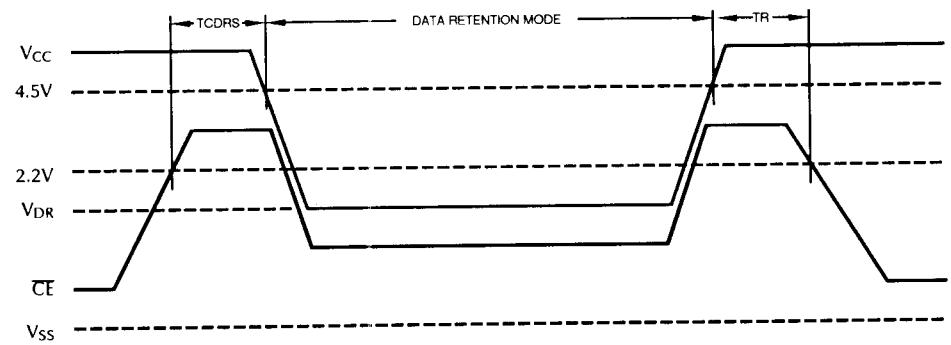
CAPACITANCE[5]: $T_A=25°C$, F = 1.0MHz

Symbol	Parameter	DPS4648 Max.	DPS4968 Max.	DPS41288 Max.	DPS42568 Max.	DPS4512X Max.	DPS8M612 Max.	DPS8M624 Max.	DPS96122 Max.	Unit	Condition
C_{ADR}	Address Input	20	25	30	60	15	20	30	160	pF	$V_{IN}=0V$
C_{CE}	Chip Enable	10	15	20	10	15	10	10	160		
C_{WE}	Write Enable	10	15	30	30	15	10	10	80		
C_{OE}	Output Enable	10	15	30	10	15	10	10	160		
$C_{I/O}$	Data In/Out	25	30	45	45	15	25	25	80		

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{CC}$-0.2V	2.0	5.0	5.5	V
t_{CDRS}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

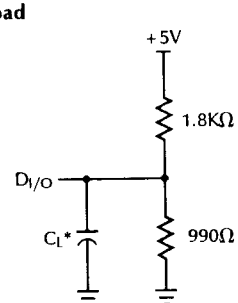
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled. $\overline{CE} \leq V_{CC}$-0.2V.



AC TEST CONDITIONS

Input Pulse Levels	0.5V to 2.5V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	0.8V and 2.2V

Figure 1. Output Load



*Including scope and jig capacitance.

OUTPUT LOAD

Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE : Over operating ranges [11]

No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable Access Time		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [6, 7]	10		10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [6, 7]	5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [6, 7]		35		40		45		55	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [6, 7]		30		35		40		50	ns
10	t_{OC}	Output Hold from Chip Enable	0		0		0		0		ns

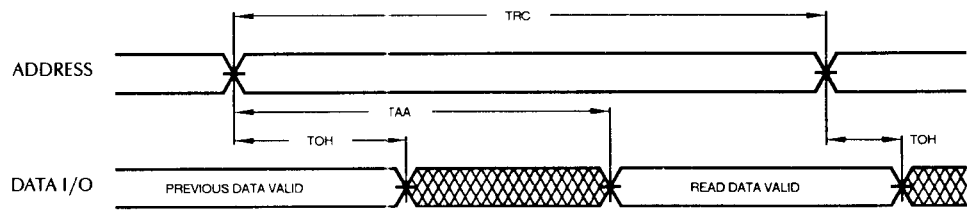
NOTE: Dense-Pac has specialized suppliers that may provide better A.C. Characteristics.

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8, 9, 11]

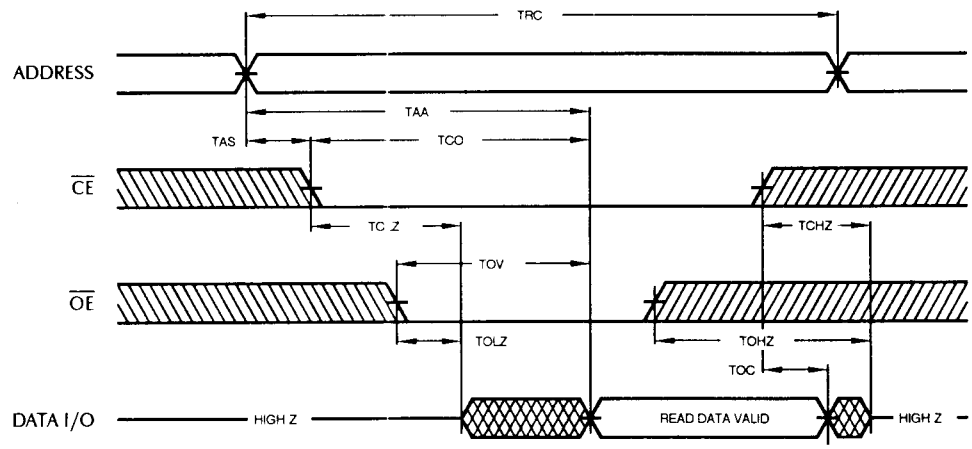
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min	Max.	Min.	Max	.Min.	Max.	Min.	Max	
11	t_{WC}	Write Cycle Time	85		100		120		150		ns
12	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
13	t_{CW}	Chip Enable to End of Write	75		90		100		120		ns
14	t_{DW}	Data Valid End of Write	35		40		50		60		ns
15	t_{DH}	Data Hold Time [10]	0		0		0		0		ns
16	t_{WP}	Write Pulse Width	65		75		90		110		ns
17	t_{AS}	Address Setup Time*	0		0		0		0		ns
18	t_{AH}	Address Hold Time [10]	5		5		5		5		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [6, 7]		35		40		45		55	ns
20	t_{WLZ}	Write Enable to Output in LOW-Z [6, 7]	5		5		5		5		ns

NOTE: Dense-Pac has specialized suppliers that may provide better A.C. Characteristics.
*Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



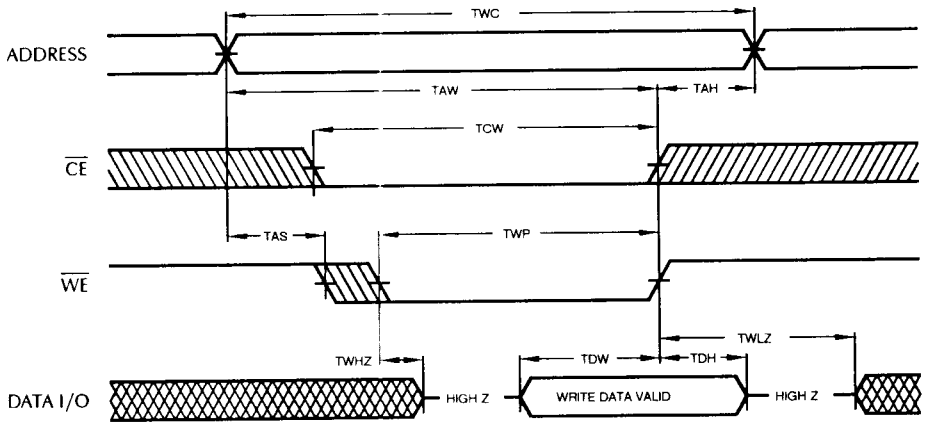
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



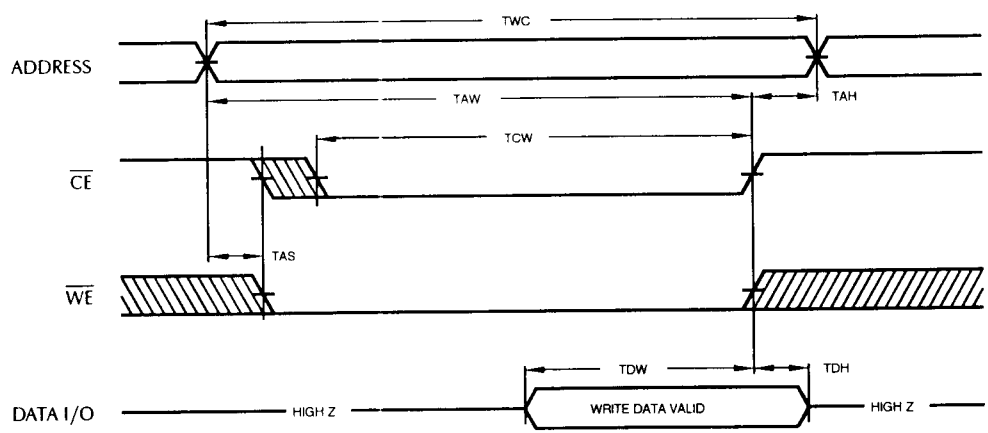
WAVEFORM KEY

Data Valid | Transition from HIGH to LOW | Transition from LOW to HIGH | Data Undefined or Don't Care

WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



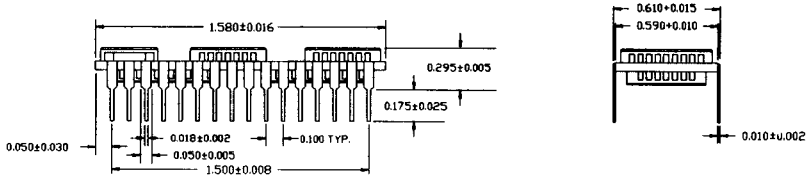
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is Don't Care.



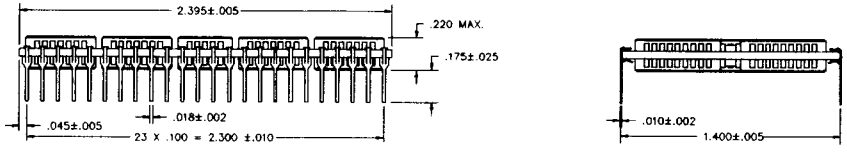
NOTES:

1. This parameter is measured whith input levels either $\geq V_{DD}$-0.2V or $\leq$ 0.2V, including $\overline{CE}$ which must be $\geq V_{DD}$-0.2V. This condition results in significant reduction in current in the input buffer circutry and consequently a lower overall current level.
2. All voltages are with respect to V_{SS}.
3. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC levels).
4. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is sampled and not 100% tested.
6. Transition is measured at the point of $\pm$ 500mV from steady state voltage.
7. This parameter is measured with Load 2 Figure 1.
8. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH the I/O pins are in the output state and the input signal of opposite phase to the outputs must not be applied.
9. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
10. t_{DH} and t_{AH} may be as long as 20ns max. on modules with decoders when performing Write Cycle 2 i.e. $\overline{CE}$ controlled write cycles. This is due to the propagation delay added by the decoder.
11. Some AC Operating Conditions and Characteristics may vary on modules with buffers and transceivers due to propagation delays added by these logic devices. For example t_{AS} is 10ns for the DPS45128 and DPS45129.

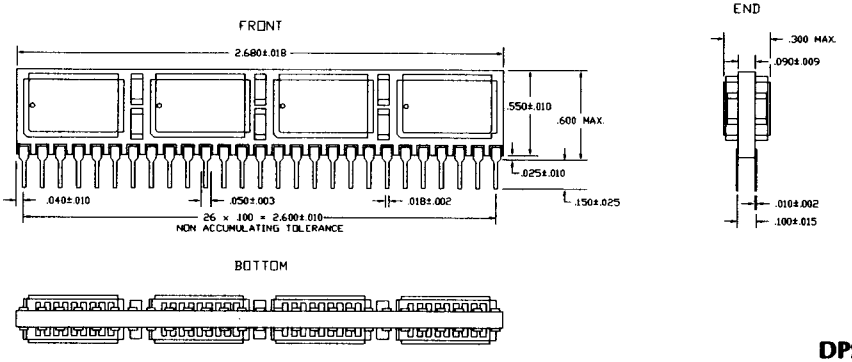
MECHANICAL DIAGRAMS



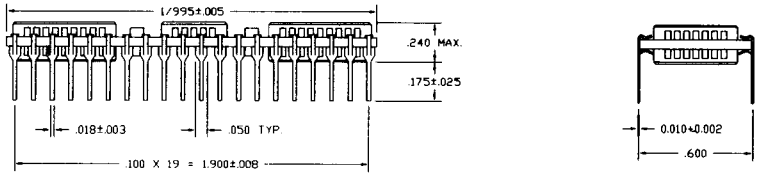
DPS4648*, DPS4968, DPS41288



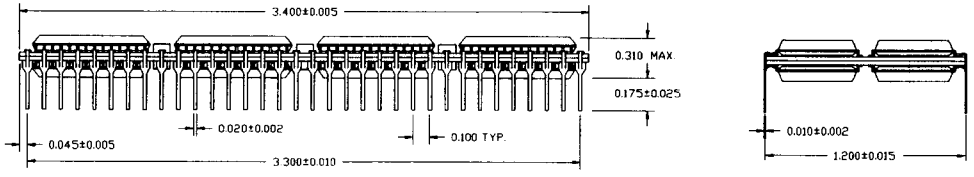
DPS45128, DPS45129



DPS42568



DPS8M612*, DPS8M624



DPS96122

* Does not have any devices on the bottom of module.

ORDERING INFORMATION

Part Number	Access Time	Temperature	Part Number	Access Time	Temperature
DPS4648-100C	100ns	0 to 70°C	DPS4648-85C	85ns	0 to 70°C
DPS4648-150C	150ns	0 to 70°C	DPS4648-120C	120ns	0 to 70°C
DPS4648-100I	100ns	-40 to 85°C	DPS4648-85I	85ns	-40 to 85°C
DPS4648-150I	150ns	-40 to 85°C	DPS4648-120I	120ns	-40 to 85°C
DPS4648-85M	85ns	-55 to 125°C	DPS4648-100M	100ns	-55 to 125°C
DPS4648-120M	120ns	-55 to 125°C	DPS4648-150M	150ns	-55 to 125°C
DPS4968-100C	100ns	0 to 70°C	DPS4968-85C	85ns	0 to 70°C
DPS4968-150C	150ns	0 to 70°C	DPS4968-120C	120ns	0 to 70°C
DPS4968-100I	100ns	-40 to 85°C	DPS4968-85I	85ns	-40 to 85°C
DPS4968-150I	150ns	-40 to 85°C	DPS4968-120I	120ns	-40 to 85°C
DPS4968-85M	85ns	-55 to 125°C	DPS4968-100M	100ns	-55 to 125°C
DPS4968-120M	120ns	-55 to 125°C	DPS4968-150M	150ns	-55 to 125°C
DPS41288-100C	100ns	0 to 70°C	DPS41288-85C	85ns	0 to 70°C
DPS41288-150C	150ns	0 to 70°C	DPS41288-120C	120ns	0 to 70°C
DPS41288-100I	100ns	-40 to 85°C	DPS41288-85I	85ns	-40 to 85°C
DPS41288-150I	150ns	-40 to 85°C	DPS41288-120I	120ns	-40 to 85°C
DPS41288-85M	85ns	-55 to 125°C	DPS41288-100M	100ns	-55 to 125°C
DPS41288-120M	120ns	-55 to 125°C	DPS41288-150M	150ns	-55 to 125°C
DPS42568-100C	100ns	0 to 70°C	DPS42568-85C	85ns	0 to 70°C
DPS42568-150C	150ns	0 to 70°C	DPS42568-120C	120ns	0 to 70°C
DPS42568-100I	100ns	-40 to 85°C	DPS42568-85I	85ns	-40 to 85°C
DPS42568-150I	150ns	-40 to 85°C	DPS42568-120I	120ns	-40 to 85°C
DPS42568-85M	85ns	-55 to 125°C	DPS42568-100M	100ns	-55 to 125°C
DPS42568-120M	120ns	-55 to 125°C	DPS42568-150M	150ns	-55 to 125°C
DPS45128-100C	100ns	0 to 70°C	DPS45128-85C	85ns	0 to 70°C
DPS45128-150C	150ns	0 to 70°C	DPS45128-120C	120ns	0 to 70°C
DPS45128-100I	100ns	-40 to 85°C	DPS45128-85I	85ns	-40 to 85°C
DPS45128-150I	150ns	-40 to 85°C	DPS45128-120I	120ns	-40 to 85°C
DPS45128-85M	85ns	-55 to 125°C	DPS45128-100M	100ns	-55 to 125°C
DPS45128-120M	120ns	-55 to 125°C	DPS45128-150M	150ns	-55 to 125°C
DPS45129-100C	100ns	0 to 70°C	DPS45129-85C	85ns	0 to 70°C
DPS45129-150C	150ns	0 to 70°C	DPS45129-120C	120ns	0 to 70°C
DPS45129-100I	100ns	-40 to 85°C	DPS45129-85I	85ns	-40 to 85°C
DPS45129-150I	150ns	-40 to 85°C	DPS45129-120I	120ns	-40 to 85°C
DPS45129-85M	85ns	-55 to 125°C	DPS45129-100M	100ns	-55 to 125°C
DPS45129-120M	120ns	-55 to 125°C	DPS45129-150M	150ns	-55 to 125°C
DPS8M612-100C	100ns	0 to 70°C	DPS8M612-85C	85ns	0 to 70°C
DPS8M612-150C	150ns	0 to 70°C	DPS8M612-120C	120ns	0 to 70°C
DPS8M612-100I	100ns	-40 to 85°C	DPS8M612-85I	85ns	-40 to 85°C
DPS8M612-150I	150ns	-40 to 85°C	DPS8M612-120I	120ns	-40 to 85°C
DPS8M612-85M	85ns	-55 to 125°C	DPS8M612-100M	100ns	-55 to 125°C
DPS8M612-120M	120ns	-55 to 125°C	DPS8M612-150M	150ns	-55 to 125°C
DPS8M624-100C	100ns	0 to 70°C	DPS8M624-85C	85ns	0 to 70°C
DPS8M624-150C	150ns	0 to 70°C	DPS8M624-120C	120ns	0 to 70°C
DPS8M624-100I	100ns	-40 to 85°C	DPS8M624-85I	85ns	-40 to 85°C
DPS8M624-150I	150ns	-40 to 85°C	DPS8M624-120I	120ns	-40 to 85°C
DPS8M624-85M	85ns	-55 to 125°C	DPS8M624-100M	100ns	-55 to 125°C
DPS8M624-120M	150ns	-55 to 125°C	DPS8M624-150M	150ns	-55 to 125°C
DPS96122-100C	100ns	0 to 70°C	DPS96122-85C	85ns	0 to 70°C
DPS96122-150C	150ns	0 to 70°C	DPS96122-120C	120ns	0 to 70°C
DPS96122-100I	100ns	-40 to 85°C	DPS96122-85I	85ns	-40 to 85°C
DPS96122-150I	150ns	-40 to 85°C	DPS96122-120I	120ns	-40 to 85°C

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