NEC®

MASTER/SLAVE T FLIP-FLOP

UPG701B
UPG701P

FEATURES

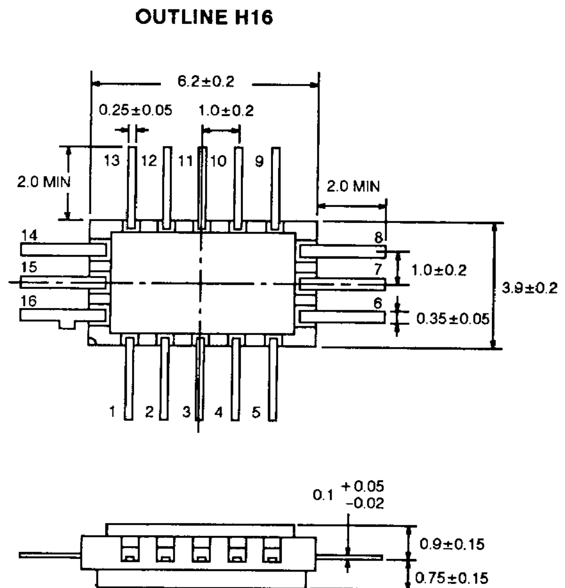
- **LOGIC LEVELS AND SUPPLY VOLTAGES ARE ECL COMPATIBLE**
- **ULTRA HIGH SPEED** (Operating Clock Frequency-5 GHz)
- **HERMETICALLY SEALED PACKAGE ASSURES HIGH RELIABILITY**

DESCRIPTION AND APPLICATIONS

The UPG701B is a high speed GaAs digital integrated circuit. It is a Master-Slave T-type Flip Flop that operates with Set/Reset functions. When the clock input is High, the output is changed. When the clock input is Low, the output state remains unchanged. Its operating clock speed is 5 GHz typically. It is ECL compatible both in I/O levels and supply voltages. The 16-pin ceramic package is low loss and hermetically sealed. Devices are highly reliable because of the stability of WSi refractory gate metallization. This device is compatible with other NEC MSI and SSI GaAs logic products, and can be tested using a MD16EVAL 16-pin evaluation kit.

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H16



ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE				UPG701B, UPG701P H16, CHIP		
SYMBOLS	**PARAMETERS**	**TEST CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{DD}	Supply Current	V_{DD} = 0 V V_{TT} = -2 V (50 Ω termination) V_{SS} = -5.2 V	mA		80	130
I_{SS}	Supply Current		mA		60	90
V_{OH}	High Level Output Voltage		V	-1.0	-0.8	-0.6
V_{OL}	Low Level Output Voltage		V	-2.0	-1.8	-1.6
V_{TH}	Threshold Voltage		V		-1.3	
I_{OH}	High Level Output Current		mA		25	
I_{OL}	Low Level Output Current		mA		4	
I_{IH}	High Level Input Current		mA		.75	
I_{IL}	Low Level Input Current		mA		.05	
$f_{\phi MAX}$	Maximum Clock Frequency		GHz	4	5	
t_{PD}	Switching Time		ps		300	400
t_R*	Output Rise Time		ps		130	200
t_F*	Output Fall Time		ps		120	200

Notes: *The time from 20% to 80% of output voltage.

1. The V_{CS} and V_{CSB} are normally open. They can also be used as a bias adjustment to optimize operating frequency or output waveform. The V_{CS} and V_{CSB} are bias terminals which are used to adjust the Flip Flop circuit current and output level respectively.
2. The metallized section on the back surface of the package is used as a heat sink and is shared with V_{SS} terminal (V_{SS} = -5.2 V normally). Note: Do not ground the metallized section to GND (0 V). This is to prevent a short circuit with V_{DD} or some other terminals.

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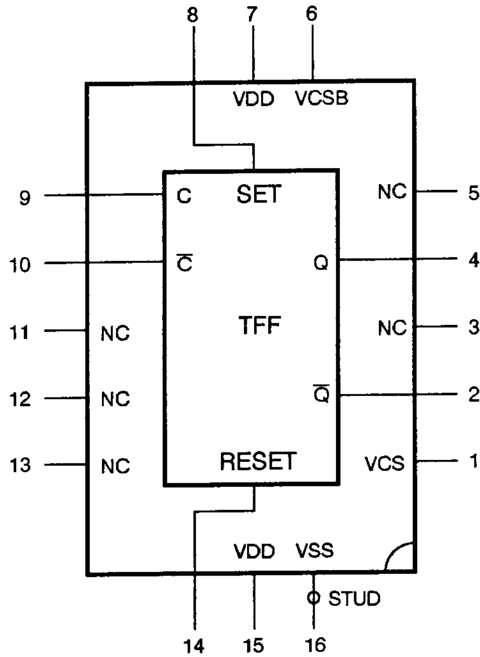
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+4
V_{SS}	Supply Voltage	V	-8
V_{TT}	Terminating Voltage	V	$-V_{DD}$-4
V_{IN}	Input Voltage	V	$V_{DD}-V_{SS}$
T_{STG}	Storage Temperature	°C	-65 to +175
$T_{C(OP)}$	Operating Case Temperature	°C	-65 to +125
P_T	Total Power Dissipation	mW	550

CONNECTION DIAGRAM



HANDLING PROCEDURE

When handling the device a ground strap should be used to prevent Electric Static Discharge (ESD) that can damage the GaAs MES FETs in the IC.

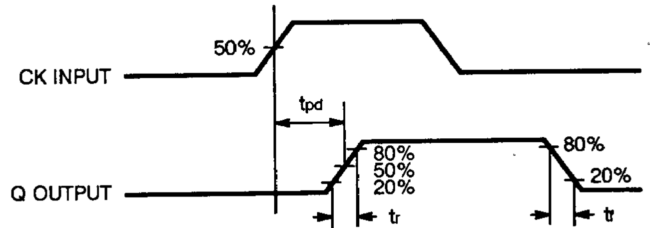
TRUTH TABLE

INPUT			OUTPUT	
CLOCK	SET	RESET	Qn + 1	Q̄n + 1
(rising edge)	LOW	LOW	Q̄n	Qn
(falling edge)	LOW	LOW	Qn	Q̄n
UNRELATED	HIGH	LOW	HIGH	LOW
UNRELATED	LOW	HIGH	LOW	HIGH
UNRELATED	HIGH	HIGH	UNCERTAIN	UNCERTAIN

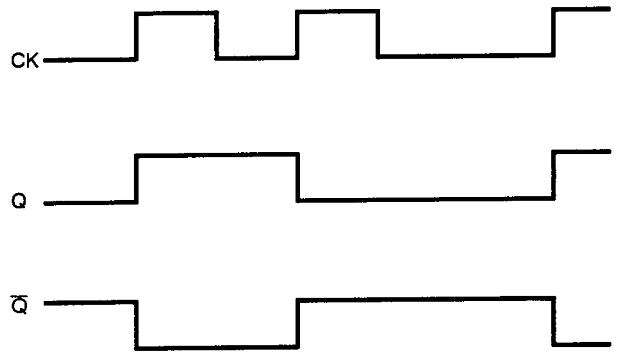
Notes:

1. The above conditions are effective when clock input is connected to C. When C̄ is connected to clock signal, UPG701 will be triggered on the falling edge of clock.
2. Set and reset functions are fully synchronous with respect to clock.

OPERATIONAL WAVEFORMS



FUNCTION DIAGRAM



$Q_N + 1 = \overline{Q}_N$

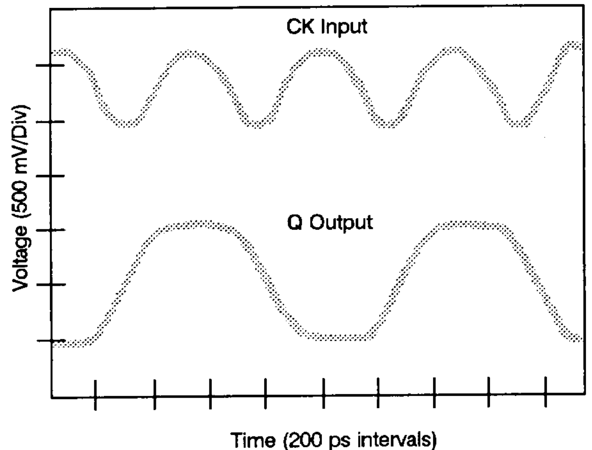
$Q_N + 1$; The output after the clock pulse

Q_N; The output before the clock pulse

When the clock input is High, the output state is changed.

When the clock input is Low, the output state remains unchanged.

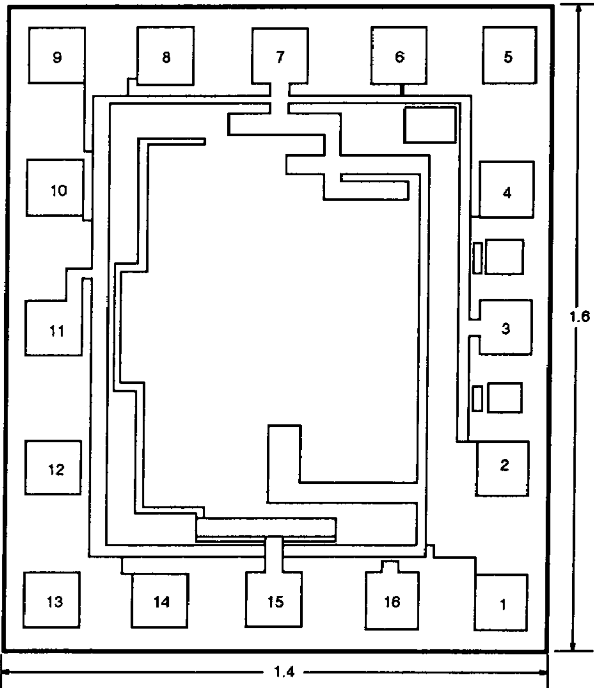
UPG701B WAVEFORM (2.0 GHz CLOCK FREQUENCY)



Time (200 ps intervals)

OUTLINE DIMENSIONS (Units in mm)

UPG701P (CHIP)



1. V_{CS}
2. $\overline{Q}$
3. NC
4. Q
5. NC
6. V_{CSB}
7. V_{DD}
8. Set
9. C_K
10. $\overline{C_K}$
11. NC
12. NC
13. NC
14. Reset
15. V_{DD}
16. V_{SS}

RECOMMENDED CHIP ASSEMBLY CONDITIONS

Die Attachment

Atmosphere:	N_2 gas	
Temperature:	320 ± 3°C	
AuSn Preform:	UPG701P	0.7 x 0.7 x 0.05t (mm), 2 piece

The use of hard solder (AuSi or AuGe) is not recommended. Don't use a solder which has a melting point higher than AuSn.

Base material: CuW, Cu, KV

Epoxy Die Attach is not recommended.

Bonding:

Machine:	TCB
Wire:	30 μm diameter Au wire
Temperature:	260 ± 10°C
Bonding Force:	44 ± 5g
Atmosphere:	N_2 gas