

# TC74VHC175F, TC74VHC175FT, TC74VHC175FK

## Quad D-Type Flip Flop with Clear

The TC74VHC175 is an advanced high speed CMOS QUAD D-TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These four flip-flops are controlled by a clock input (CK) and a clear input (CLR).

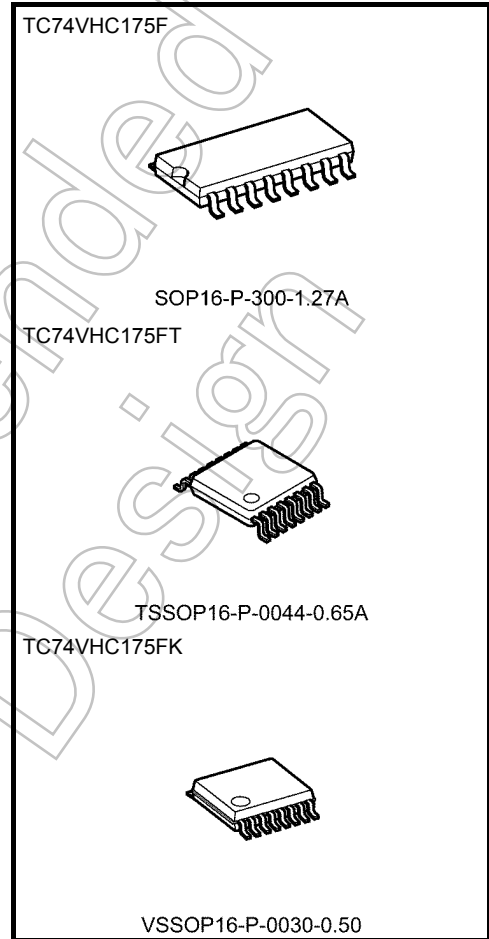
The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and  $\bar{Q}1$  thru  $\bar{Q}4$ ) on the positive-going edge of the clock pulse.

When the CLR input is held low, the Q outputs are at the low logic level and the  $\bar{Q}$  outputs are at the high logic level, regardless of other input conditions.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High speed:  $f_{max} = 210$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (opr) = 2$  to  $5.5$  V
- Low noise:  $V_{OLP} = 0.8$  V (max)
- Pin and function compatible with 74ALS175

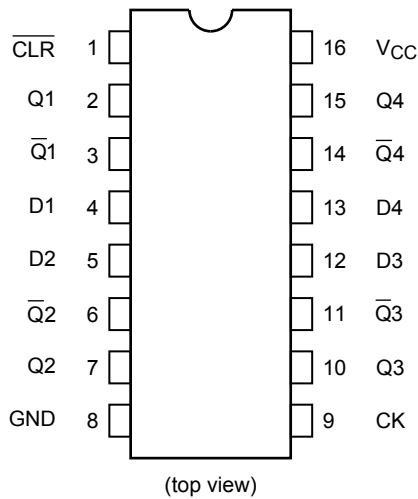


**Weight**

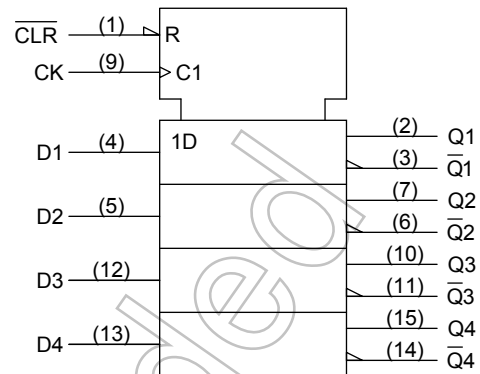
SOP16-P-300-1.27A	: 0.18 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

Start of commercial production  
1991-11

**Pin Assignment**



**IEC Logic Symbol**

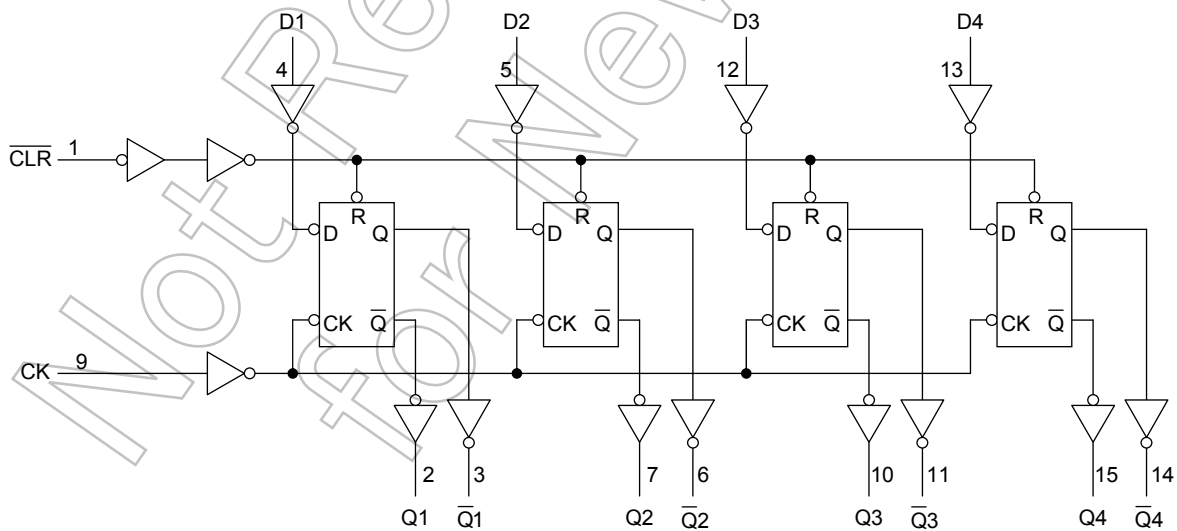


**Truth Table**

Inputs			Outputs		Function
$\overline{\text{CLR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	X	X	L	H	Clear
H	L		L	H	—
H	H		H	L	—
H	X		$Q_n$	$\overline{Q}_n$	No Change

X: Don't care

**System Diagram**



**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Operating Range (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating range must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V	
Low-level input voltage	V <sub>IL</sub>	—	2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA	

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (CK)	t <sub>w</sub> (L)	—	3.3 ± 0.3	—	5.0	5.0	ns
	t <sub>w</sub> (H)	—	5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ )	t <sub>w</sub> (L)	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t <sub>s</sub>	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	4.0	4.0	
Minimum hold time	t <sub>h</sub>	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.0	1.0	
Minimum removal time ( $\overline{\text{CLR}}$ )	t <sub>rem</sub>	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (CK-Q, $\bar{Q}$ )	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	7.5	11.5	1.0	13.5	ns
				50	—	10.0	15.0	1.0	17.0	
	5.0 ± 0.5		15	—	4.8	7.3	1.0	8.5		
			50	—	6.3	9.3	1.0	10.5		
Propagation delay time ( $\bar{\text{CLR}}-Q, \bar{Q}$ )	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	6.3	10.1	1.0	12.0	ns
				50	—	8.8	13.6	1.0	15.5	
	5.0 ± 0.5		15	—	4.3	6.4	1.0	7.5		
			50	—	5.8	8.4	1.0	9.5		
Maximum clock frequency	f <sub>max</sub>	—	3.3 ± 0.3	15	90	140	—	75	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	85	115	—	75	—	
Output to output skew	t <sub>osLH</sub>	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
	t <sub>osHL</sub>		5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	—	(Note 2)	—	44	—	—	—	pF	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

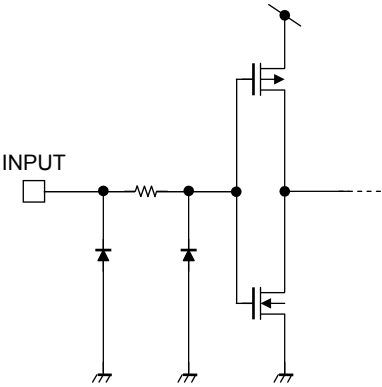
And the total C<sub>PD</sub> when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD (total)} = 30 + 14 \cdot n$$

### Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Max	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.4	-0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Input Equivalent Circuit**

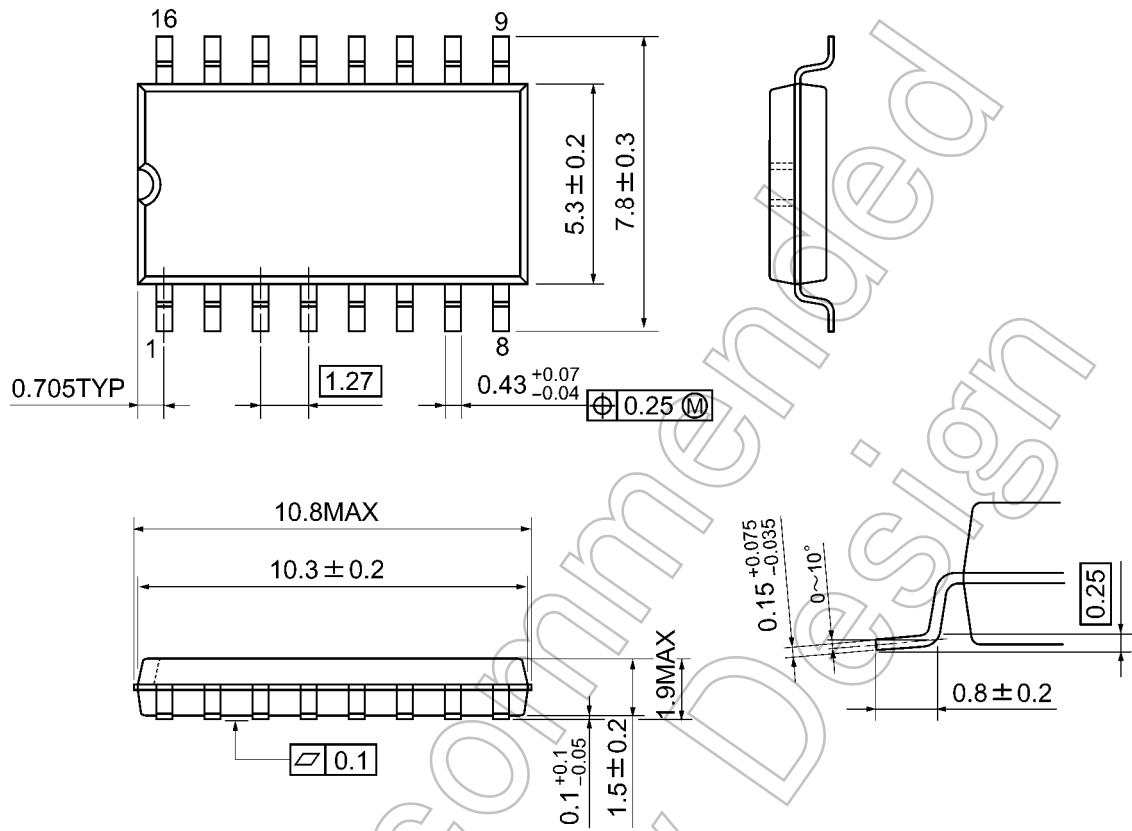


Not Recommended  
for New Design

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



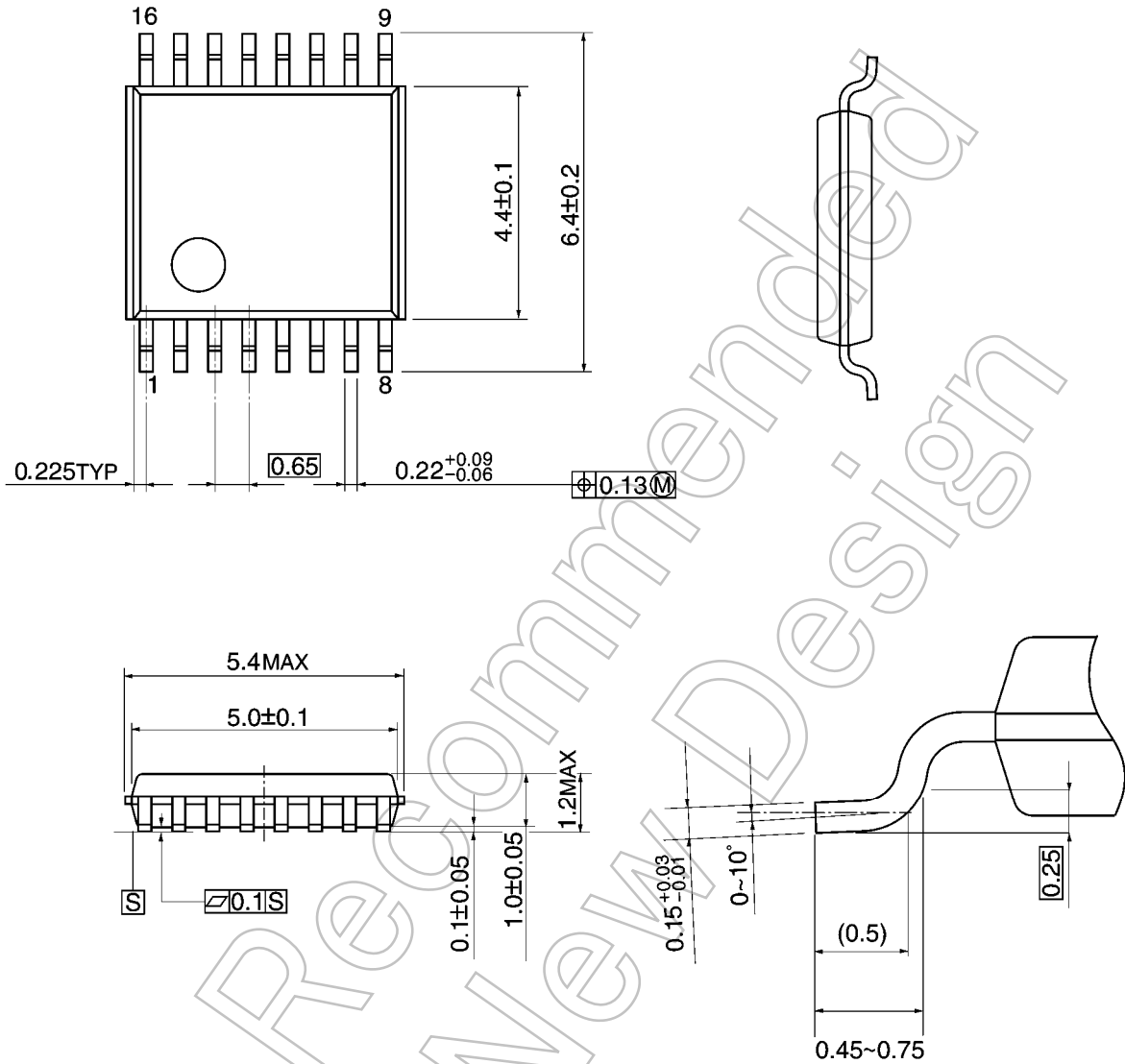
Weight: 0.18 g (typ.)

Not Recommended for New Design

**Package Dimensions**

TSSOP16-P-0044-0.65A

Unit: mm



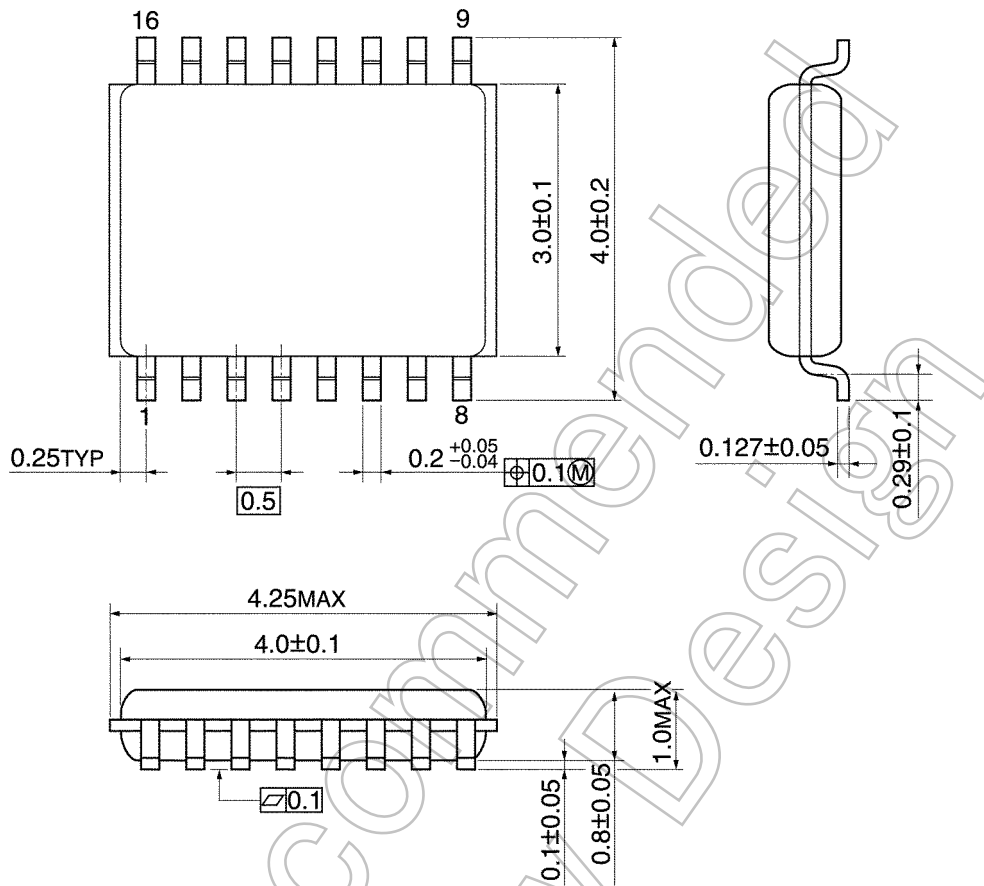
Weight: 0.06 g (typ.)

Not Recommended for New Design

## Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

Not Recommended for New Design

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