



16K x 1 ECL RAM

SY10480-8/10
 SY100480-8/10
 SY101480-8/10

T-46-23-05

FEATURES

- Address access time, tAA: 8/10ns max.
- Chip select access time, tAC: 4/5ns max.
- Choice of two edge rates: 800 or 1500ps (typ.)
- Eliminates write recovery glitch found on competitors' ECL RAMs
- Power supply current, IEE: -220mA min.
- Designed for alpha particle Immunity
- Built with advanced ASSET™ I technology
- Fully compatible with industry standard 10K/100K/101K ECL I/O levels
- Noise margins Improved with on-chip voltage and temperature compensation
- Open emitter output for easy memory expansion
- Available in hermetic DIP and Flatpack

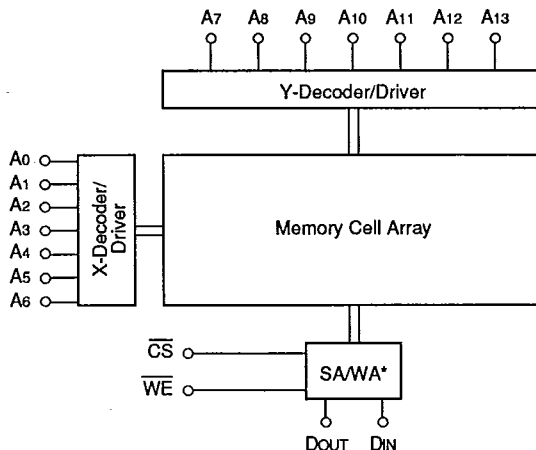
DESCRIPTION

The Synergy SY10/100/101480 are 16384-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 16384-words-by-1-bit and meet the standard 10K/100K family I/O signal levels at both -4.5V (100K) and -5.2V (101K) supply levels. All devices feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101480 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

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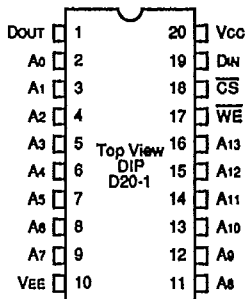
BLOCK DIAGRAM



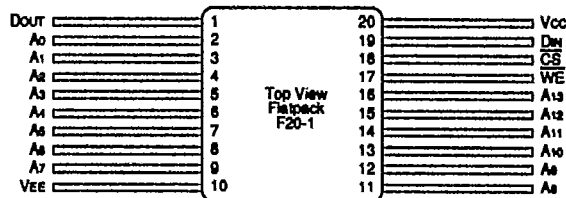
* SA = Sense Amplifier
 WA = Write Amplifier



PIN CONFIGURATIONS



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PIN NAMES

Label	Function
A0 - A13	Address Inputs
CS	Chip Select
WE	Write Enable
DIN	Data Input
DOUT	Data Output
Vcc	GND (0V)
VEE	Supply Voltage

TRUTH TABLE

Input			Output	Mode
CS	WE	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101480 are 16384-bit RAMs organized as 16384-words-by-1-bit. Memory cell selection is achieved by using the 14 address bits designated as A0 through A13. Each of the 2¹⁴ possible input address combinations corresponds to a unique word location in memory. The active low Chip Select (CS) is provided for memory expansion. The active low Write Enable (WE) controls the read and write operation. Data resident on the DIN input is written into the addressed location only when WE and CS are held low. In order to perform a read

operation, WE is held high, CS is held low and the non-inverted output data at the addressed location is transferred to DOUT to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to -2.0V or an equivalent circuit must be used to provide the specified output levels.

The output is brought to a logical low level when the RAM is being written into (WE = LOW) or when the device is deselected via the active low chip select pin (CS = HIGH).



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SY10/100/101480-8
SY10/100/101480-10

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Rating	Symbol	Value	Unit
VEE Pin Potential to Vcc Pin	VEE	+0.5 to -7.0	V
Input Voltage	V _{IN}	+0.5 to -2.0	V
DC Output Current (Output High)	I _{OUT}	-30	mA
Temperature Under Bias	T _c	-55 to +125	°C
Storage Temperature	T _{store}	-65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Supply Voltage ⁽¹⁾	10K	VEE	-5.46	-5.2	-4.94	V
	Case Temperature	T _c	0	25	75	°C
Supply Voltage ⁽¹⁾	100K	VEE	-4.8	-4.5	-4.2	V
	Case Temperature	T _c	0	25	85	°C
Supply Voltage ⁽¹⁾	101K	VEE	-5.72	-5.2	-4.68	V
	Case Temperature	T _c	0	25	85	°C

NOTE:

1. Referenced to Vcc.

RISE AND FALL TIME

Parameter	Code ⁽¹⁾	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	t _r	—	800	—	ps
	S	t _r	—	1500	—	ps
Output Fall Time	F	t _f	—	800	—	ps
	S	t _f	—	1500	—	ps

NOTE:

1. F = Fast Edge Rate
S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C _{IN}	—	4	—	pF
Output Pin Capacitance	C _{OUT}	—	5	—	pF

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SY10/100/101480-8
SY10/100/101480-10**10K DC ELECTRICAL CHARACTERISTICS**

VCC = 0V; Tc = 0°C to 75°C; VEE = -5.2V; Airflow > 2.5m/s; Output Load = 50Ω to -2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
VOH	Output High Voltage	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV	VIN = VIH Max. or VIL Min.
VOL	Output Low Voltage	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV	VIN = VIH Max. or VIL Min.
VOHC	Output High Voltage	0°C 25°C 75°C	-1020 -980 -920	— — —	mV	VIN = VIH Min. or VIL Max.
VOLC	Output Low Voltage	0°C 25°C 75°C	— — —	-1645 -1630 -1605	mV	VIN = VIH Min. or VIL Max.
VIH	Input High Voltage	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV	Guaranteed Input Voltage High for All Inputs
VIL	Input Low Voltage	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV	Guaranteed Input Voltage Low for All Inputs
IIH	Input High Current	0°C to 75°C	0.0	20	μA	VIN = VIH Max.
IIL	Input Low Current	0°C to 75°C	-2	2	μA	VIN = VIL Min.
IIL	\overline{BS} Input Low Current	0°C to 75°C	30	170	μA	VIN = VIL Min.
IIH	\overline{BS} Input High Current	0°C to 75°C	40	220	μA	VIN = VIH Max.
IIL	\overline{WE} Input Low Current	0°C to 75°C	-2	35	μA	VIN = VIL Min.
IIH	\overline{WE} Input High Current	0°C to 75°C	0.0	60	μA	VIN = VIH Max.
IEE	Power Supply Current — 8ns — 10ns	0°C to 75°C	-260 -220	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICSVCCA = 0V
VCC = 0VVEE = -4.5V (100K)
VEE = -5.2V (101K)

Tc = 0°C to 85°C

Airflow > 2.5m/s
Output Load = 50Ω to -2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
VOH	Output High Voltage	-1025	-880	mV	VIN = VIH Max. or VIL Min.
VOL	Output Low Voltage	-1810	-1620	mV	VIN = VIH Max. or VIL Min.
VOHC	Output High Voltage	-1035	—	mV	VIN = VIH Min. or VIL Max.
VOLC	Output Low Voltage	—	-1610	mV	VIN = VIH Min. or VIL Max.
VIH	Input High Voltage	-1165	-880	mV	Guaranteed Input Voltage High for All Inputs
VIL	Input Low Voltage	-1810	-1475	mV	Guaranteed Input Voltage Low for All Inputs
IIH	Input High Current	0.0	20	μA	VIN = VIH Max.
IIL	Input Low Current	-2	2	μA	VIN = VIL Min.
IIL	\overline{BS} Input Low Current	30	170	μA	VIN = VIL Min.
IIH	\overline{BS} Input High Current	40	220	μA	VIN = VIH Max.
IIL	\overline{WE} Input Low Current	-2	35	μA	VIN = VIL Min.
IIH	\overline{WE} Input High Current	0.0	60	μA	VIN = VIH Max.
IEE	Power Supply Current	-220	—	mA	All Inputs and Outputs Open



AC ELECTRICAL CHARACTERISTICS

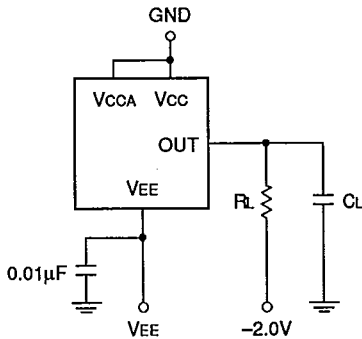
AC TEST CONDITIONS

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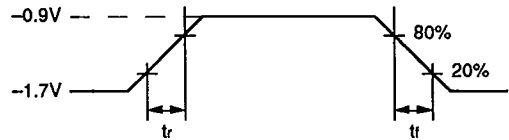
VCC = VCCA = 0V Output Load = 50Ω to -2.0V
 VEE = -5.2V ± 5% (10K) Tc = 0°C to 75°C (10K)
 VEE = -4.5V ± 0.3V (100K) Tc = 0°C to 85°C (100K/101K)
 VEE = -5.2V ± 0.52V (101K) Airflow > 2.5m/s

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Loading Condition



Input Pulse



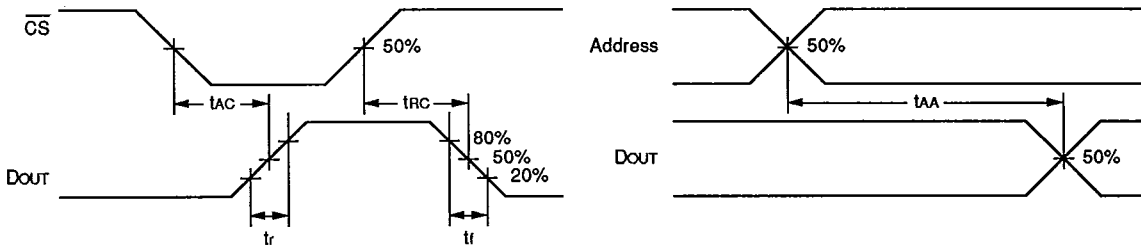
$t_r = t_f = 1.0\text{ns typ.}$
 OUTPUT LOAD: $R_L = 50\Omega$
 $C_L = 5\text{pF}^* \text{ (typ.)}$
 * (Modeled as 50Ω transmission line terminated to -2V.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol	Parameter	SY10480-8 SY100480-8 SY101480-8		SY10480-10 SY100480-10 SY101480-10		Unit
		Min.	Max.	Min.	Max.	
tAA	Address Access Time	—	8	—	10	ns
tAB	Block Select Access Time	—	4	—	5	ns
tRB	Block Select Recovery Time	—	4	—	5	ns

READ CYCLE TIMING DIAGRAM



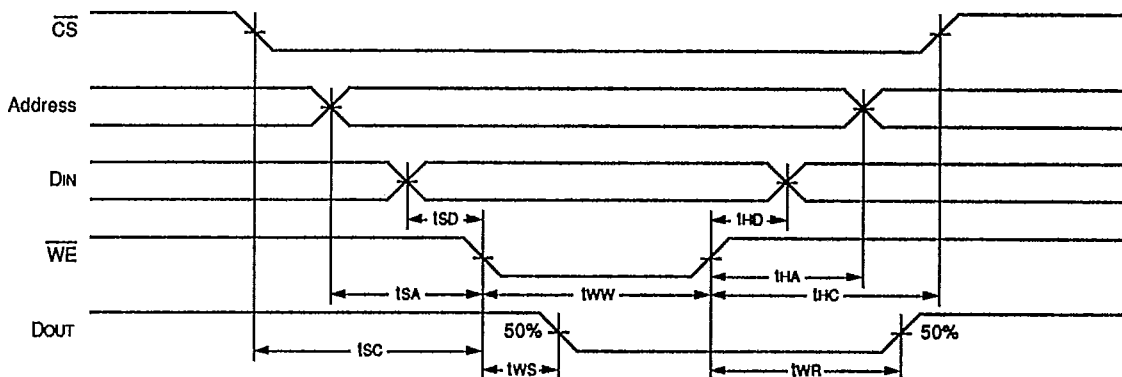


WRITE CYCLE

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Symbol	Parameter	SY10480-8 SY100480-8 SY101480-8		SY10480-10 SY100480-10 SY101480-10		Unit
		Min.	Max.	Min.	Max.	
t _{WW}	Write Pulse Width	8	---	10	---	ns
t _{WS}	Write Disable Time	---	4	---	5	ns
t _{WR}	Write Recovery Time	---	8	---	10	ns
t _{SA}	Address Set-up Time	2	---	2	---	ns
t _{SB}	Block Select Set-up Time	2	---	2	---	ns
t _{SD}	Data Set-up Time	2	---	2	---	ns
t _{HA}	Address Hold Time	1	---	1	---	ns
t _{HB}	Block Select Hold Time	1	---	1	---	ns
t _{HD}	Data Hold Time	1	---	1	---	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
8	SY10480-8DCF	Fast	D20-1	Commercial
	SY10480-8DCS	Standard	D20-1	Commercial
8	SY10480-8FCF	Fast	F20-1	Commercial
	SY10480-8FCS	Standard	F20-1	Commercial
8	SY100480-8DCF	Fast	D20-1	Commercial
	SY100480-8DCS	Standard	D20-1	Commercial
8	SY100480-8FCF	Fast	F20-1	Commercial
	SY100480-8FCS	Standard	F20-1	Commercial
8	SY101480-8DCF	Fast	D20-1	Commercial
	SY101480-8DCS	Standard	D20-1	Commercial
8	SY101480-8FCF	Fast	F20-1	Commercial
	SY101480-8FCS	Standard	F20-1	Commercial

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
10	SY10480-10DCS	Standard	D20-1	Commercial
	SY10480-10FCS	Standard	F20-1	Commercial
10	SY100480-10DCS	Standard	D20-1	Commercial
	SY100480-10FCS	Standard	F20-1	Commercial
10	SY101480-10DCS	Standard	D20-1	Commercial
	SY101480-10FCS	Standard	F20-1	Commercial