0.54" 2-Character 14-Segment Alphanumeric LED Displays With MOS I.C. Driver

LTM-8647A Series

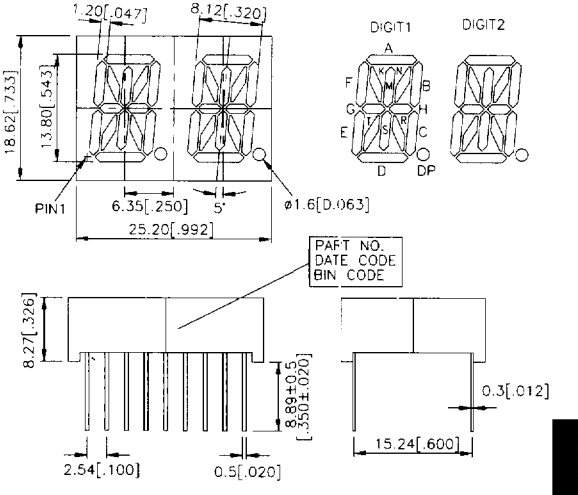
Features

- 0.54 inch (13.8mm) digit height, 14-segment character.
- Wide supply voltage operation.
- Serial data input.
- Constant Current drivers.
- Continuous brightness control.
- Solid state reliability, long operation life.
- Wide viewing angle.
- Choices of six bright colors-yellow/red/bright-red/green/orange/high efficiency red.
- TTL compatible.

Description

The LTM-8647A series are dual character 14-segment alphanumeric display modules, having a built-in M5450 MOS integrated circuits. The integrated circuit contains serial data input, 35 bit shift registers. 34 LED driver output and a brightness control. The red devices utilize LED chips which are made from GaAsP on a GaAs substrate. The bright red and green, yellow devices utilize LED chips which are made from GaP on a transparent GaP substrate. The orange and high efficiency red devices utilize LED chips which are made from GaAsP on a transparent GaP substrate. The MOS integrated circuit are produced with N-channel silicon gate technology. Red and bright red displays have black face and red segments . Green and yellow, orange displays have gray face and white segments. High efficiency red displays have red face and red segments.

Package Dimensions



Notes: All dimensions are in millimeters (inches).
Tolerance :
± 0.25mm (0.010") unless otherwise noted.

Devices

Part No. LTM-						Description
Yellow	Red	Bright Red	Green	Orange	Hi.-Eff.Red	
8647AY	8647AR	8647AP	8647AG	8647AE	8647AHR	Dual Character, with I.C. Driver

Pin Connection

Pin No.	Description	Pin No.	Description
1	Bit 32 Output	10	No Pin
2	Bit 33 Output	11	No Pin
3	Bit 34 Output	12	No Pin
4	Data Input	13	Vss* 1
5	Clock Input	14	Vss* 1
6	Data Enable	15	No Pin
7	V_{DD}	16	No Pin
8	V_{LED}	17	Bit 31 Output
9	Brt Control	18	No Pin

Note:Pin no 13 & 14 are internally connected.

Absolute Maximum Ratings at Ta=25 ℃

Parameter	Symbol	Min.	Max.	Units
Supply Voltage * 1	V_{DD}	-0.3	12	V
Input Voltage	V_I	-0.3	12	V
Off State Output Voltage	$V_{O(off)}$		12	V
LED Supply Voltage	V_{LED}	2.8	3.5	V
Power Dissipation of IC * 2	P_D(IC)		335	mW
Supply Current	I_{DD}		8.5	mA
Operating Temperature Range	T_{op}	-20	+60	℃
Storage Temperature Range	T_{stg}	-20	+60	℃
Solder Temperature 1/16 inch Below Seating Plane for 3 Seconds at 260 ℃				

Note: 1. All voltages are with respect to Vss(GND)
2. Power dissipation of IC is given by $P_D=(V_{LED}-V_F) \cdot (I_F) \cdot$ (No. of Segments)+(8.5mA) $\cdot (V_{DD})$
*V_F is LED forward voltage.

Recommended Operating Condition at Ta=25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Supply Voltage	V_{DD}	4.75		11	V	
Input Voltage Logical "0" Level Logical "1" Level Logical "1" Level	V_I	 -0.3 2.2 V_{DD} -2		 0.8 V_{DD} V_{DD}	 V V V	 ± 10 μ A Input Bias 4.75V < V_{DD} < 5.25V V_{DD} > 5.25V
Brightness Input Current	I_B	0		0.75	mA	
Brightness Input Voltage	V_B	3		4.3	V	Input Current =750 μ A
Off State Voltage	Vo(off)			11	V	
Output Sink Current Segment Off Segment On Input Clock Frequency	 F_{CLOCK}	 0	 3 6	 10 0.5	 μ A mA mA MHZ	 I_B=0 μ A I_B=100 μ A I_B=200 μ A
Output Matching	Io			± 20	%	

Electrical/Optical Characteristics at Ta=25 ℃

LTM-8647AR

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	200	550		μ cd	I_B=0.4mA
Peak Emission Wavelength	λ P		655		nm	I_B=0.4mA
Spectral Line Half-Width	Δ λ		24		nm	I_B=0.4mA
Dominant Wavelength	λ d		651		nm	I_F=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B=0.4mA

LTM-8647AP

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	320	900		μ cd	I_B=0.4mA
Peak Emission Wavelength	λ P		697		nm	I_B=0.4mA
Spectral Line Half-Width	Δ λ		90		nm	I_B=0.4mA
Dominant Wavelength	λ d		638		nm	I_F=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B=0.4mA

LTM-8647AG

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	800	2300		μ cd	IB=0.4mA
Peak Emission Wavelength	λ P		565		nm	IB=0.4mA
Spectral Line Half-Width	Δ λ		30		nm	IB=0.4mA
Dominant Wavelength	λ d		569		nm	IF=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		IB=0.4mA

LTM-8647AY

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	800	2300		μ cd	IB=0.4mA
Peak Emission Wavelength	λ P		585		nm	IB=0.4mA
Spectral Line Half-Width	Δ λ		35		nm	IB=0.4mA
Dominant Wavelength	λ d		588		nm	IF=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		IB=0.4mA

LTM-8647AE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	800	2300		μ cd	IB=0.4mA
Peak Emission Wavelength	λ P		630		nm	IB=0.4mA
Spectral Line Half-Width	Δ λ		40		nm	IB=0.4mA
Dominant Wavelength	λ d		621		nm	IF=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		IB=0.4mA

LTM-8647AHR

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Average Luminous Intensity	Iv	800	2300		μ cd	IB=0.4mA
Peak Emission Wavelength	λ P		635		nm	IB=0.4mA
Spectral Line Half-Width	Δ λ		40		nm	IB=0.4mA
Dominant Wavelength	λ d		621		nm	IF=20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		IB=0.4mA

Functional Description

Serial data transfer from the data source to the display driver is accomplished with 2 signals serial data and colck. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is completed, thus provding nonmultiplexed, direct drive to the display. Output change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the output current of LED display. A 1nF capacitor ahould be connected to brightness control, Pin 7 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 7 which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

Figure 1 shows the input data format. A start bit of logical "1" preceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data . The shift registers are static master-salve configuration. There is no clear for master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers won't clear. When power is first applied to the chip, an internal power ON, a reset signal is generated which reset all registers and all latches. The START bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the segment A of the digit 1. A logical "1" at the input will turn on the appropriate LED. Figure 2 shows the timing relationship between data, clock, and DATA ENABLE. A max. clock frequency of 0.5MHz is assumed.

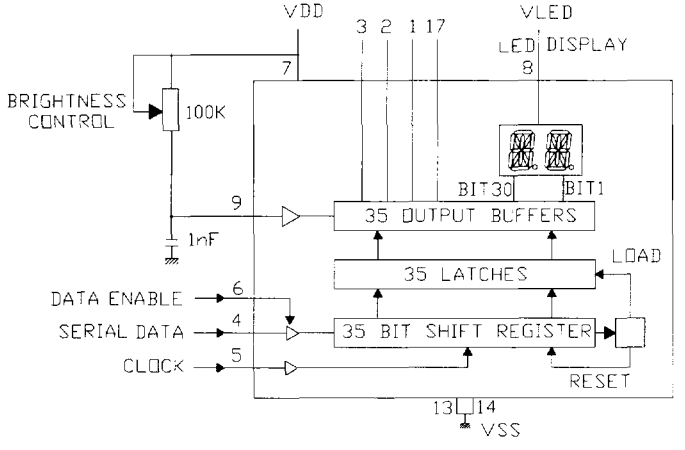


Figure 1. Internal Block Diagram

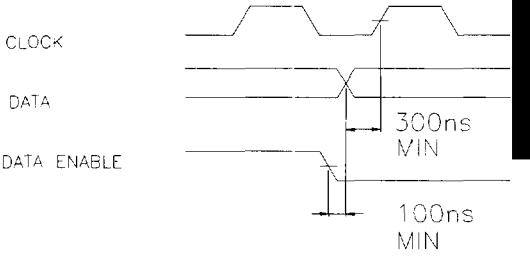


Figure 2. Input Data Format

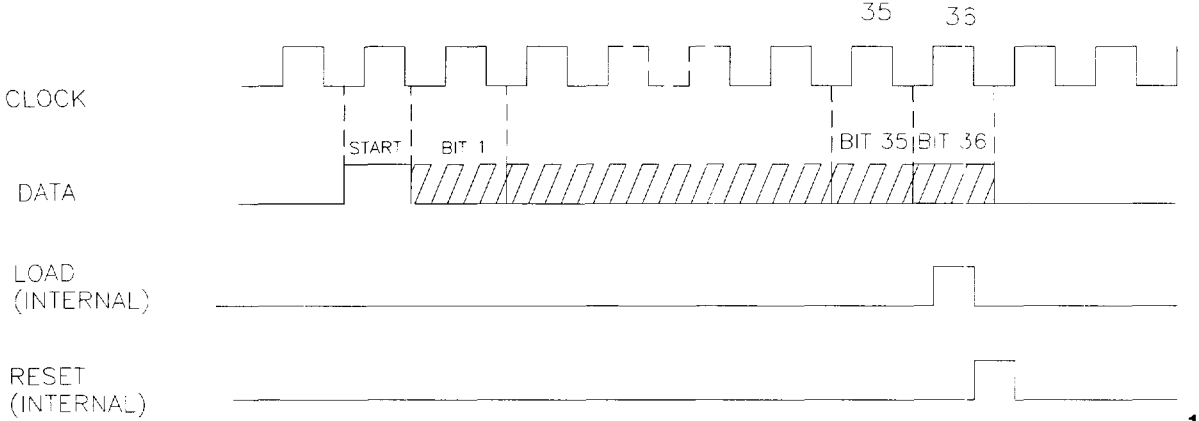


Figure 3. Timing Relationship

Table I Serial Data Input Sequence

Bit	Digit	Segment	Bit	Digit	Segment
1	2	A	18	1	D
2	2	B	.19	1	E
3	2	C	20	1	F
4	2	D	21	1	G
5	2	E	22	1	H
6	2	F	23	1	K
7	2	G	24	1	M
8	2	H	25	1	N
9	2	K	26	1	R
10	2	M	27	1	S
11	2	N	28	1	T
12	2	R	29	1	DP
13	2	S	30	2	DP
14	2	T	31		Pin 17
15	1	A	32		Pin 1
16	1	B	33		Pin 2
17	1	C	34		Pin 3