

ML2308**Preliminary****Stereo Recording/Playback LSI with Built-in Buffer Memory**

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

Both a serial interface and a parallel interface are available with the ML2308 through the use of a pin switch. Refer to pages 3 to 15 for information on the serial interface, and pages 16 to 22 for information on the parallel interface.

GENERAL DESCRIPTION

The ML2308 is a stereo recording/playback LSI that has integrated in a single chip all the functions required for recording and playing back audio data.

Analog signals fed into the microphone or line inputs are converted into digital signals by the analog to digital converter, and output to external equipment via the buffer memory. Further, digital signals from external equipment are converted into PWM signals by the 1-bit digital to analog converter, and output by the PWM driver that can directly drive the headphones. The influence of noise is lower with the ML2308 when compared with the mixed analog LSI, since most of the signals are digitally processed inside the LSI.

FEATURES

User Interfaces

- Supports Serial Peripheral Interface (SPI) or 8-bit bus interface
- Buffer memory for audio data buffer: 128 bytes (64 bytes each for left and right channels)
- Buffer memory status output pins FUL, MID, EMP

Codec section/audio input and output sections

- Audio synthesis method:
μ-law G.711 compliant 8-bit PCM, 8-bit/16-bit linear PCM, 8-bit Oki non-linear PCM, 2-bit/3-bit/4-bit/5-bit/6-bit/7-bit/8-bit ADPCM2
- Sampling frequency: 4.0 kHz to 48 kHz (selectable with commands)
- Built-in stereo Δ-Σ type 1-bit A/D converter S/(N+D): 80 dB DR, S/N: 85 dB
- Built-in stereo Δ-Σ type 1-bit D/A converter S/(N+D): 85 dB DR, S/N: 90 dB
- Built-in PWM driver for driving a speaker (150mW max., RL = 16Ω)
- Microphone amplifier × 2, Line amplifier × 2 (Stereo)
- Dynamic Range Control (DRC) automatic recording level adjustment function
- Recording input level detect function

Control commands

- Volume control: 32 steps, 0 dB to -60 dB, 2 dB incremental, OFF
- PAN control: 16 steps, 0 dB to -28 dB, 2 dB incremental, OFF

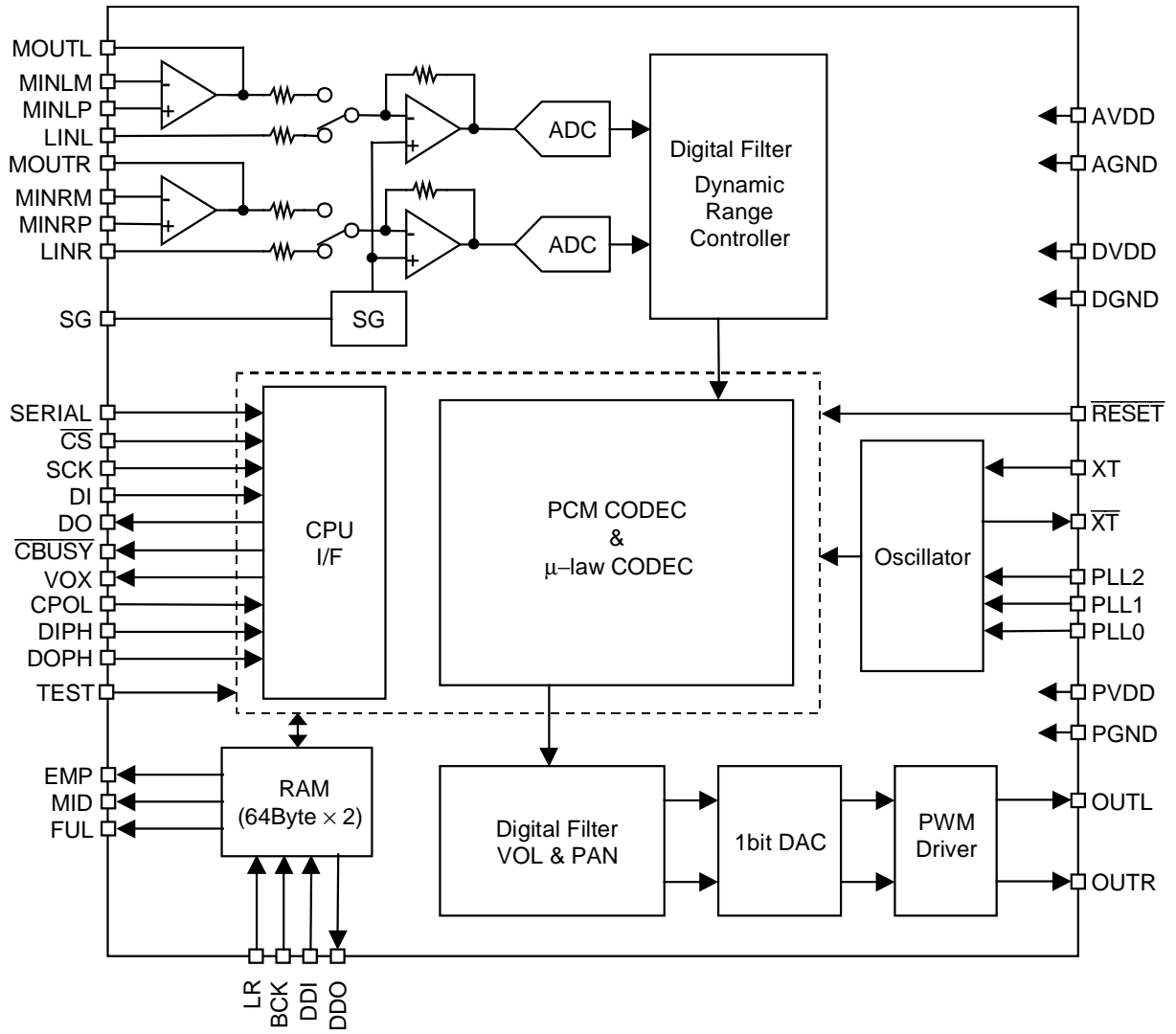
- Power supply voltage : +2.7 V to +3.6 V
- Operating temperature : -20°C to +70°C
- Source oscillation frequency : 3.0 MHz to 6.5 MHz
- Package : 48-pin plastic QFN (P-VQFN48-0707-0.50-1) (ML2308GP)

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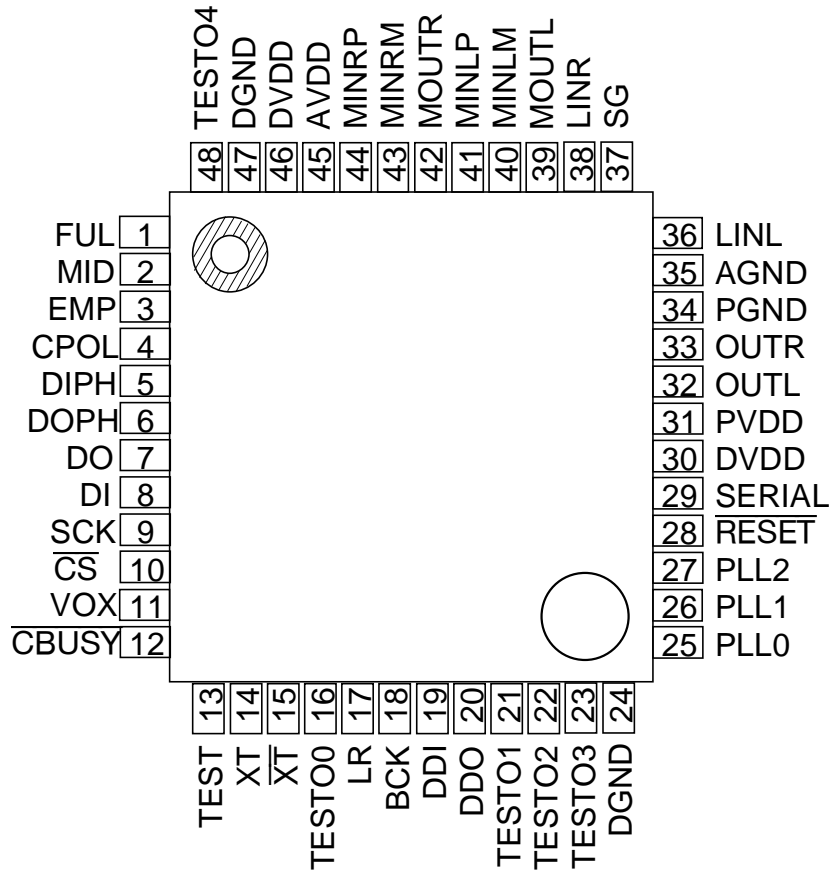
(1) SERIAL INTERFACE

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

48-pin plastic VQFN (Serial interface)



DESCRIPTION OF PINS

Command Interface Related Pins

Pin number	Pin name	I/O	Description
28	$\overline{\text{RESET}}$	I	The reset input pin. At "L" level input, the LSI is initialized. At that time, oscillation is stopped and the power is shut off. When turning the power on, input at the "L" level, and change to the "H" level once the supplied power voltage has been stabilized.
29	SERIAL	I	The parallel/serial interface select pin. Fixed to "H" level when the serial interface is selected.
10	$\overline{\text{CS}}$	I	The chip select input pin. At "L" level input, the command interface for the SCK, DI, and DO pins is enabled.
9	SCK	I	The command data input and status output serial clock input pin.
8	DI	I	The command data serial data input pin.
7	DO	O	The serial data output pin. The status signal in the LSI is output as a serial data, when a command is input subsequently following the input of the RDSTAT command.
4	CPOL	I	The pin to select the input pulse polarity of the SCK pin. When the CPOL pin is at the "L" level, the SCK will become "H" active. When the CPOL pin is at the "H" level, the SCK will become "L" active.
5	DIPH	I	The edge of the SCK pulse, at which data input at the DI pin is taken in the LSI, is selected with this pin. When the DIPH pin is at the "L" level, the data input at the DI pin is taken in the LSI at the rising edge of the SCK pulse. When the DIPH pin is at the "H" level, the data input at the DI pin is taken in the LSI at the falling edge of the SCK pulse.
6	DOPH	I	The edge of the SCK pulse, at which data is output to the DO pin, is selected with this pin. When the DOPH pin is at the "L" level, data is output to the DO pin at the falling edge of the SCK pulse. When the DOPH pin is at the "H" level, data is output to the DO pin at the rising edge of the SCK pulse.
12	$\overline{\text{CBUSY}}$	O	This pin outputs data at "L" level during command processing. Commands should be input with the $\overline{\text{CBUSY}}$ pin at the "H" level.
11	VOX	O	The audio level detect signal output pin for recording. After recording has started, this pin outputs "H" once the recording input signal amplitude reaches the prescribed level.

Audio Interface Related Pins

Pin number	Pin name	I/O	Description
17	LR	I	<p>This pin inputs the left or right side channel select signal for writing the audio data in the buffer memory or reading the audio data from the buffer memory.</p> <p>The outputs of the respective status signals in the buffer memory (EMP, MID and FUL) are switched by the input level of the LR pin input. Note that the status signal of the buffer memory is an output of a channel status signal that is opposite to that of the selected channel.</p> <p>[I²S format selected] When the LR pin is at the "L" level, access to the buffer memory of the left side will be permitted. The status signal of the buffer memory of the right side will be output. When the LR pin is at the "H" level, access to the buffer memory of the right side will be permitted. The status signal of the buffer memory of the left side will be output.</p> <p>[Front-aligned MSB first format selected] When the LR pin is at the "L" level, access to the buffer memory of the right side will be permitted. The status signal of the buffer memory of the left side will be output. When the LR pin is at the "H" level, access to the buffer memory of the left side will be permitted. The status signal of the buffer memory of the right side will be output.</p>
18	BCK	I	The serial clock input pin for buffer memory input and output.
19	DDI	I	This is the pin for the input of serial data to the buffer memory. Data is taken into the LSI at the rising edge of the BCK clock.
20	DDO	O	This is the pin for the output of serial data from the buffer memory. Data is output serially at the falling edge of the BCK clock.
1	FUL	O	<p>The status signal, indicating that the entire buffer memory is full of data, will be output. A "H" active or "L" active selection can be made with the OPT command.</p> <p>Recorded data after the buffer memory becomes full is not stored in the buffer memory and is discarded.</p> <p>Therefore, any data written after the buffer memory becomes full will not be played back.</p>
2	MID	O	<p>The status signal, indicating that at least half of the buffer memory is filled with data, will be output. A "H" active or "L" active selection can be made with the OPT command.</p> <p>Ordinarily, access to the buffer memory is controlled by the output of the MID pin.</p>
3	EMP	O	The status signal, indicating that there is no data in the entire buffer memory, will be output. A "H" active or "L" active selection can be made with the OPT command.

Analog, Clock or Power Supply Related Pins

Pin number	Pin name	I/O	Description
39	MOUTL	O	The output pin of the microphone amplifier on the left side.
40	MINLM	I	The inverted input pin of the microphone amplifier on the left side.
41	MINLP	I	The non-inverted input pin of the microphone amplifier on the left side.
42	MOUTR	O	The output pin of the microphone amplifier on the right side.
43	MINRM	I	The inverted input pin of the microphone amplifier on the right side.
44	MINRP	I	The non-inverted input pin of the microphone amplifier on the right side.
36	LINL	I	The input pin of the line amplifier on the left side.
38	LINR	I	The input pin of the line amplifier on the right side.
37	SG	O	The output pin for the reference voltage (signal ground) of the analog circuit.
33	OUTR	O	The playback output pin for the right side. An external LC filter has been configured to eliminate a high-frequency component, as the PWM pulse is output.
32	OUTL	O	The playback output pin for the left side. An external LC filter has been configured to eliminate a high-frequency component, as the PWM pulse is output.
14	XT	I	An oscillator connection pin. When using an external clock, input it from this pin.
15	\overline{XT}	O	An oscillator connection pin. When using an external clock, leave this open.
25,26,27	PLL2-0	I	The multiplication setting pins for the built-in PLL. Set them so that the PLL output does not exceed 100 MHz.
13	TEST	I	A test pin. Fix it at "L". It has a built-in pull-down resistor
16,21,22,23,48	TESTO4-0	O	Test pins. Leave them open when the circuit board is connected.
30,46	DVDD	—	The digital power supply pins. Connect a bypass capacitor of 0.1 μ F or more between these pins and the DGND pin.
24,47	DGND	—	The digital ground pins.
45	AVDD	—	The analog power supply pin. Connect a bypass capacitor of 0.1 μ F or more between this pin and the AGND pin.
35	AGND	—	The analog ground pin.
31	PVDD	—	The power supply pin for the PWM driver. Connect a bypass capacitor of 0.1 μ F or more between this pin and the PGND pin.
34	PGND	—	The ground pin for the PWM driver.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +5.0	V
Input voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Storage temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 3.6	V
Operating temperature	T_{op}	—	-20 to +70	$^\circ\text{C}$
Source clock frequency	f_{osc}	—	3.0 to 6.5	MHz

ELECTRICAL CHARACTERISTICS**DC Characteristics**

$DV_{DD} = AV_{DD} = 2.7$ to 3.6 V
 DGND = AGND = 0 V, $T_a = -20$ to $+70^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
“H” input voltage	V_{IH}	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
“L” input voltage	V_{IL}	—	-0.3	—	0.6	V
“H” output voltage	V_{OH}	$I_{OH} = -1$ mA	$V_{DD} - 0.4$	—	—	V
“L” output voltage	V_{OL}	$I_{OL} = 2$ mA	—	—	0.4	V
“H” input current (Note 1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	μA
“H” input current (Note 2)	I_{IH2}	$V_{IH} = V_{DD}$	0.3	—	20	μA
“H” input current (Note 3)	I_{IH3}	$V_{IH} = V_{DD}$	30	—	150	μA
“H” input current (Note 4)	I_{IL1}	$V_{IL} = \text{GND}$	-10	—	—	μA
“L” input current (Note 2)	I_{IL2}	$V_{IL} = \text{GND}$	-20	—	-0.3	μA
Operating current consumption	I_{DD}	$f_{osc} = 4.096$ MHz at no load	—	TBD	40	mA
Current consumption during power down	I_{DDs}	$T_a = -20$ to $+70^\circ\text{C}$	—	TBD	10	μA

- Notes:
1. Applies to input pins excluding XT and TEST pins.
 2. Applies to XT pin.
 3. Applies to TEST pin.
 4. Applies to input pins excluding XT pin.

Analog Section CharacteristicsDV_{DD} = AV_{DD} = 2.7 to 3.6 VDGND = AGND = 0 V, T_a = -20 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MIN input impedance	R _{INM}	—	100	—	—	kΩ
LINL, LINR input impedance	R _{INL}	When line input is used	22	32	42	kΩ
LIN1, LIN2 input amplitude	V _{LIN}	—	—	—	0.6 × V _{DD}	V _{pp}
MOUT, LOU _{TL} , LOU _{TR} output load resistance	R _{OUTA}	—	100	—	—	kΩ
Microphone amplifier gain setting range	G _{MIC}	—	—	—	30	dB
Line amplifier voltage gain error	G _{LINE}	—	-10	0	10	%
SG output voltage	V _{SG}	—	0.48 × V _{DD}	0.5 × V _{DD}	0.52 × V _{DD}	V
SG output resistance	R _{SG}	—	12	15	18	kΩ
OUTL, OUTR output power	P _{OUT}	At BTL output and R _L = 16Ω	—	—	150	mW

DESCRIPTION OF FUNCTIONS

Command Interface

1. SPI mode

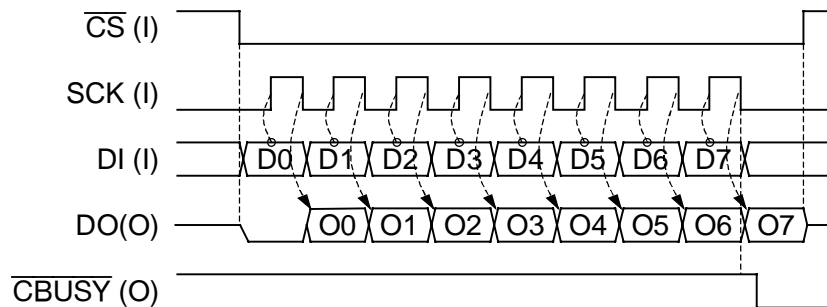
The ML2308 supports eight types of SPI modes as available command interface modes. These SPI modes can be selected with the CPOL pin, DIPH pin and DOPH pin. Fix the output level to “L” or “H” as the SPI mode setting cannot be changed once the power has been turned on.

Setting descriptions for the CPOL pin, DIPH pin and DOPH pin are shown below:

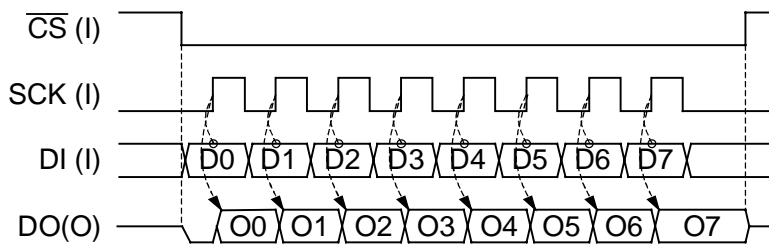
Pin	Input Level	Setting descriptions
CPOL	“L” level	“H” pulse is input as the SCK pulse.
	“H” level	“L” pulse is input as the SCK pulse.
DIPH	“L” level	The input data of the DI pin is taken in at the rising edge of the SCK pulse.
	“H” level	The input data of the DI pin is taken in at the falling edge of the SCK pulse.
DOPH	“L” level	Data is output to the DO pin at the falling edge of the SCK pulse.
	“H” level	Data is output to the DO pin at the rising edge of the SCK pulse.

Timing diagrams of respective SPI modes are shown below:

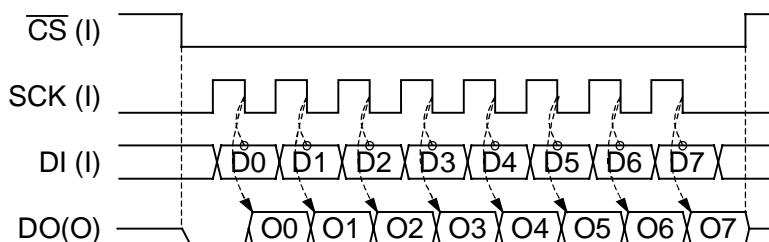
- CPOL = “L”, DIPH = “L”, DOPH = “L”



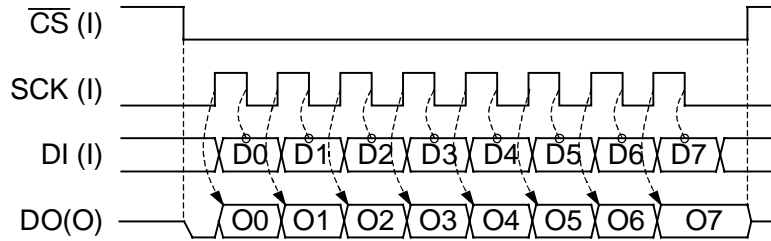
- CPOL = “L”, DIPH = “L”, DOPH = “H”



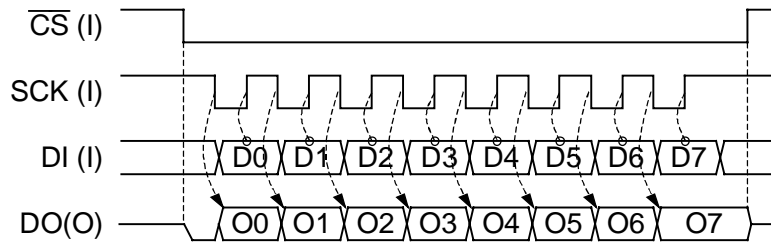
- CPOL = “L”, DIPH = “H”, DOPH = “L”



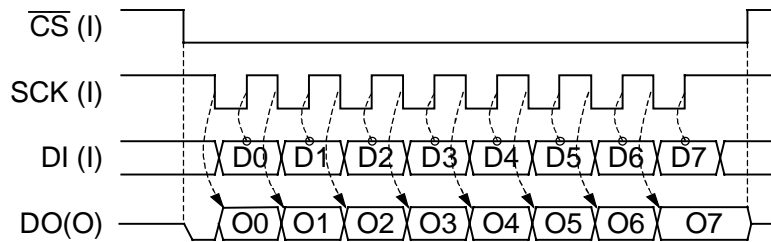
- CPOL = "L", DIPH = "H", DOPH = "H"



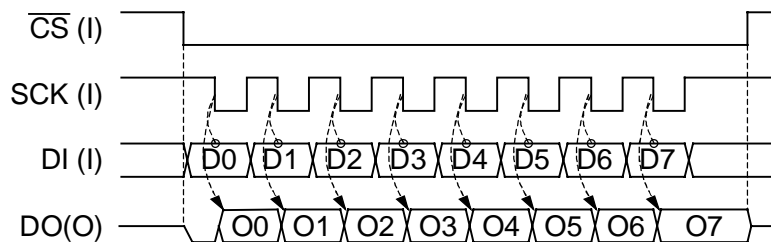
- CPOL = "H", DIPH = "L", DOPH = "L"



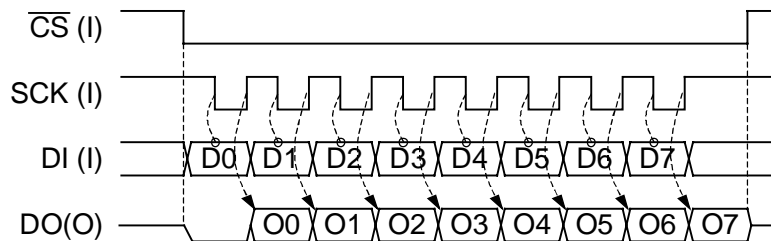
- CPOL = "H", DIPH = "L", DOPH = "H"



- CPOL = "H", DIPH = "H", DOPH = "L"



- CPOL = "H", DIPH = "H", DOPH = "H"



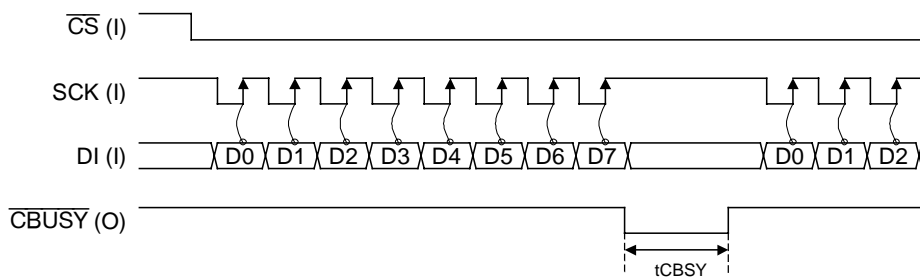
2. Command Data Write Timing

The timing for writing command data is shown below.

After “L” is input to the \overline{CS} pin, 8-bit command data is input to the DI pin serially from the LSB, synchronized with the input clock signal of the SCK pin. After 8 SCK clock signals have been input, “L” is output to the \overline{CBUSY} pin. While the \overline{CBUSY} pin is “L”, the serial interface cannot be used. It waits for the \overline{CBUSY} pin output to become “H” before inputting the next command data.

A timing diagram for the case where the CPOL pin is set at the “H” level and the DIPH pin is set at “L” level is shown below.

The “L” level output time of the \overline{CBUSY} pin, t_{CBSY} , varies depending on the operating state of the LSI.

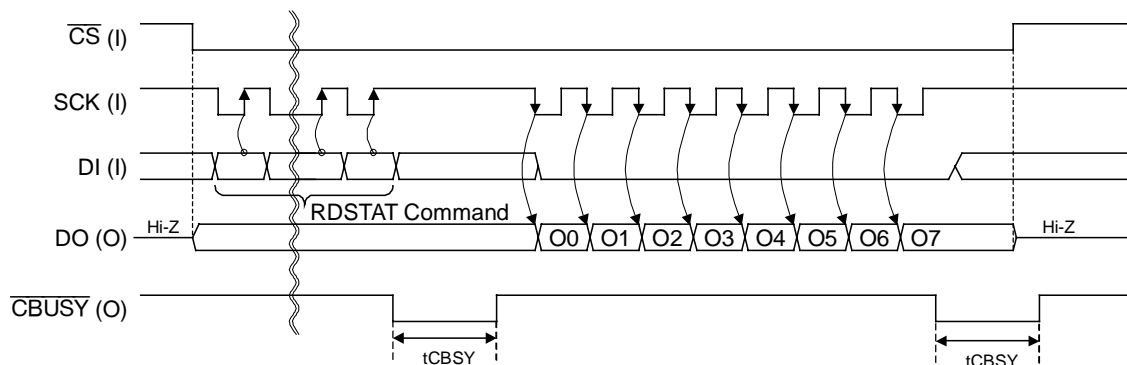


3. Status Read Timing

The timing for reading status signals is shown below.

After “L” is input to the \overline{CS} pin and the status read command (RDSTAT command) is input, 8-bit status data is output to the DO pin serially from the LSB synchronized with the falling edge of the input clock signal of the SCK pin.

A timing diagram for the case where the CPOL pin is set at the “H” level, the DIPH pin at “L” level, and the “DOPH” at the “L” level is shown below.



Audio Interface

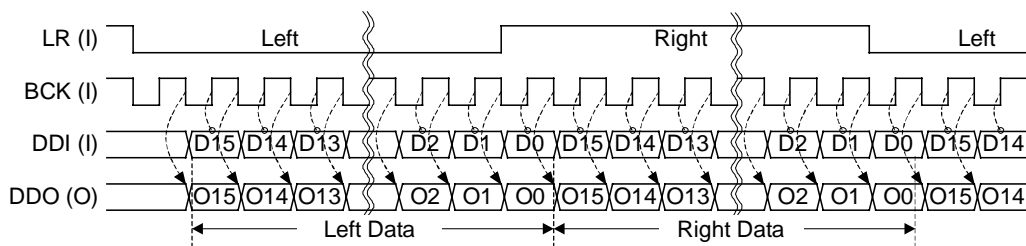
The audio interface is used to write the audio data into and read the audio data out of the buffer memory during recording and playback.

As an audio interface, the ML2308 supports two types of interface formats (I²S format and front-aligned MSB first format).

Access to the buffer memory is made from the LR pin, BCK pin, DDI pin and DDO pin regardless of the selected format.

1. At I²S Formatting

Access timing to the buffer memory with the I²S format is shown below:



During playback, the 16-bit playback data is input serially from the MSB to the DDI pin in synchronization with the clock signal of the BCK pin. The DDI pin input data is taken in the LSI at the rising edge of the BCK clock signal. The recording data is output from the DDO pin at the falling edge of the BCK clock signal during recording.

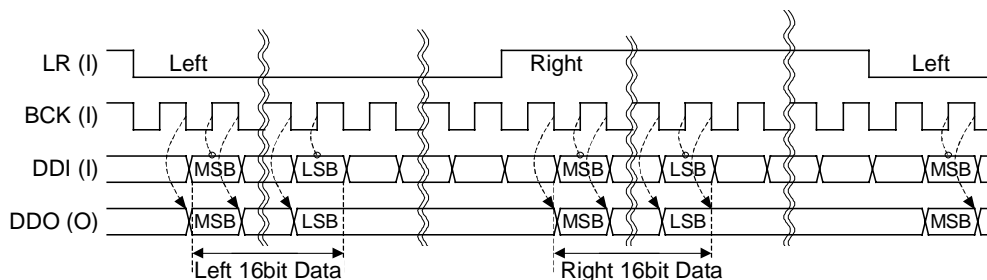
The left side data is input and output when the level of the LR pin is at “L” and the right side data is input and output when the level of the LR pin is at “H”.

The status signal output (EMP, MID and FUL) of the buffer memory is also switched according to the input level of the LR pin. The right side status data is output when the level of the LR pin is at “L” and the left side status signal is output when the level is at “H”. Note that the status of the opposite channel is output when compared with the input and output of the data.

When the buffer memory is empty, the read data will be 0000h (hexadecimal) if reading is performed.

If the BCK clock signal is input for the duration of 16 clocks or more while the LR pin is at “H” or “L”, then the 16-bit front-aligned data will become valid data.

The buffer memory access timing, when the BCK clock is 16-bit or more, is shown below:

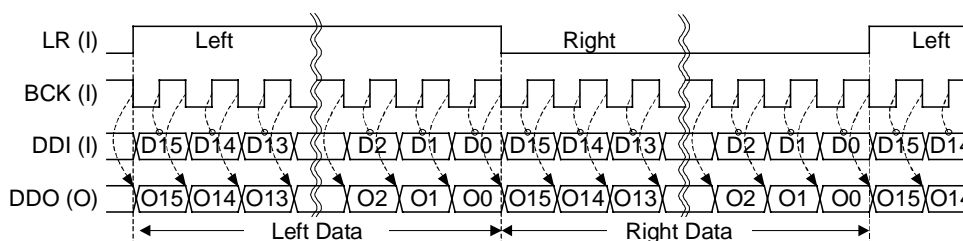


It is necessary to access both the left and right sides of the buffer memory during monaural recording and playback as well. Since buffer memory access of an unused channel will be ignored, there will be no effect to the channels that are in use. The status signal of an unused channel retains the empty state, even for the status signals of the buffer memory (EMP, MID and FUL) as well.

For example, when recording with the left side channel, the audio data read from the right side channel will be 0000h (hexadecimal). When playing back, the values written in the right side of the buffer memory will be ignored.

2. At Front-Aligned MSB First Formatting

The buffer memory access timing for the front-aligned MSB first format is shown below:



During playback, the 16-bit playback data is input serially from the MSB to the DDI pin in synchronization with the clock signal of the BCK pin. The DDI pin input data is taken in the LSI at the rising edge of the BCK clock signal. The recording data is output from the DDO pin at the falling edge of the BCK clock signal during recording.

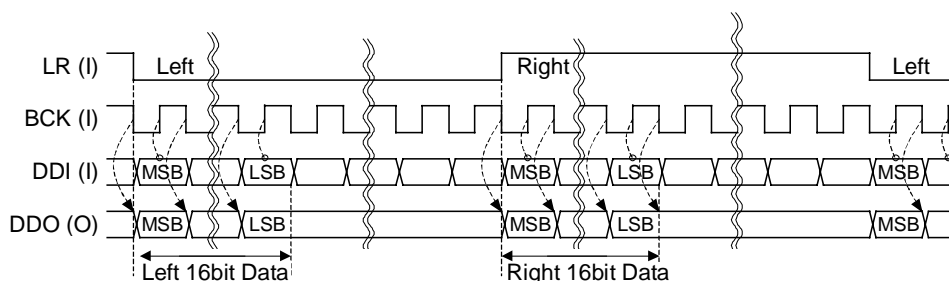
The left side data is input and output when the level of the LR pin is at “H” and the right side data is input and output when the level of the LR pin is at “L”.

The status signal output (EMP, MID and FUL) of the buffer memory is also switched according to the input level of the LR pin. The right side status data is output when the level of the LR pin is at “H” and the left side status signal is output when the level is at “L”. Note that the status of the opposite channel is output when compared with the input and output of the data.

When the buffer memory is empty, the read data will be 0000h (hexadecimal) if reading is performed.

If the BCK clock signal is input for the duration of 16 clocks or more while the LR pin is at “H” or “L”, then the 16-bit front-aligned data will become valid data.

The buffer memory access timing, when the BCK clock is 16-bit or more, is shown below:



It is necessary to access both the left and right sides of the buffer memory during monaural recording and playback as well. Since buffer memory access of an unused channel will be ignored, there will be no effect to the channels that are in use. The status signal of an unused channel retains the empty state, even for the status signals of the buffer memory (EMP, MID and FUL) as well.

For example, when recording with the left side channel, the audio data read from the right side channel will be 0000h (hexadecimal). When playing back, the values written in the right side of the buffer memory will be ignored.

3. Data Configurations for Respective Audio Synthesis Methods

The configuration of the audio data that is input to and output from the buffer memory during recording and playback, for each respective audio synthesis method, is shown in the table below:

1) 2-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	LSB1	MSB2	LSB2	MSB3	LSB3	MSB4	LSB4
D7	D6	D5	D4	D3	D2	D1	D0
MSB5	LSB5	MSB6	LSB6	MSB7	LSB7	MSB8	LSB8

2) 3-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
0	MSB1	2SB1	LSB1	MSB2	2SB2	LSB2	MSB3
D7	D6	D5	D4	D3	D2	D1	D0
2SB3	LSB3	MSB4	2SB4	LSB4	MSB5	2SB5	LSB5

3) 4-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2
D7	D6	D5	D4	D3	D2	D1	D0
MSB3	3SB3	2SB3	LSB3	MSB4	3SB4	2SB4	LSB4

4) 5-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
0	MSB1	4SB1	3SB1	2SB1	LSB1	MSB2	4SB2
D7	D6	D5	D4	D3	D2	D1	D0
3SB2	2SB2	LSB2	MSB3	4SB3	3SB3	2SB3	LSB3

5) 6-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	MSB1	5SB1	4SB1	3SB1
D7	D6	D5	D4	D3	D2	D1	D0
2SB1	LSB1	MSB2	5SB2	4SB2	3SB2	2SB2	LSB2

6) 7-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
0	0	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1
D7	D6	D5	D4	D3	D2	D1	D0
LSB1	MSB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

7) 8-bit ADPCM2, 8-bit straight PCM, 8-bit non-linear PCM, or μ -law PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
MSB2	7SB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

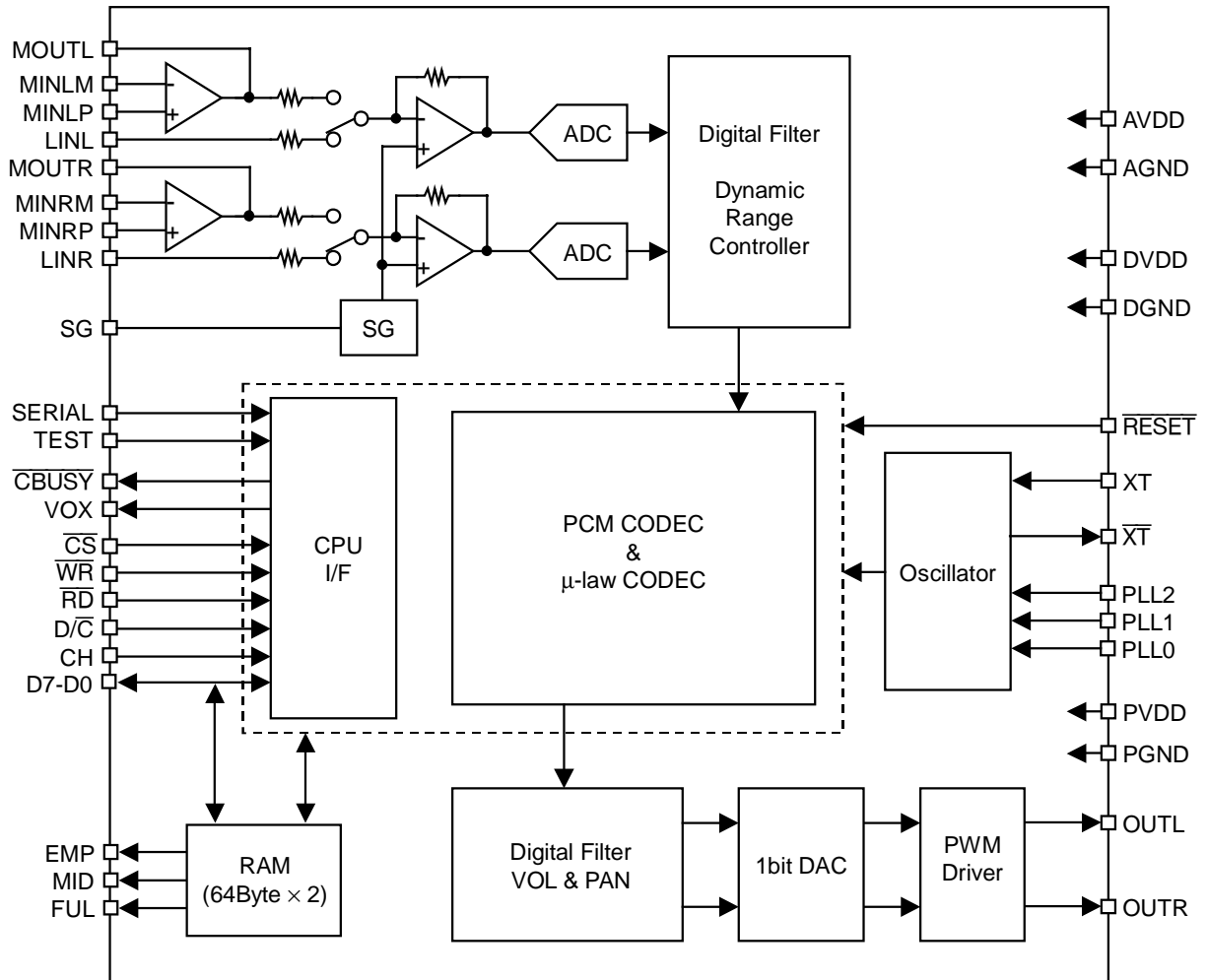
8) 16-bit straight PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1
D7	D6	D5	D4	D3	D2	D1	D0
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

This concludes the descriptions on the serial interface. Refer to Section (3) for details concerning common items, such as command lists, operation flows and examples of applied circuits.

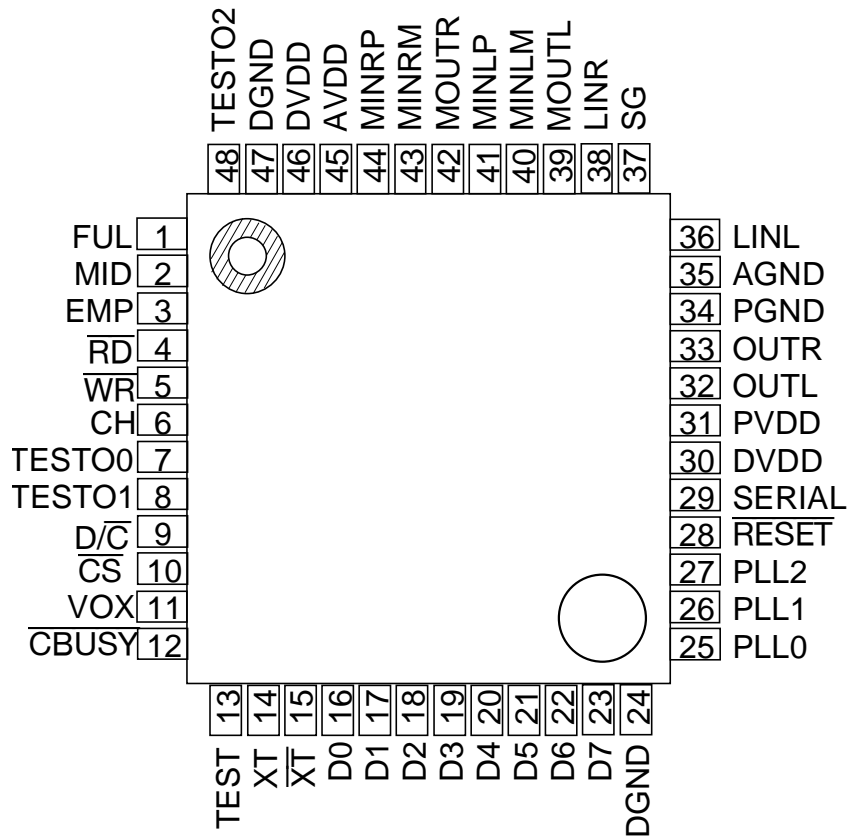
(2) PARALLEL INTERFACE

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

48-pin plastic VQFN (Parallel interface)



DESCRIPTION OF PINS

Command Interface Related Pins

Pin number	Pin name	I/O	Description
28	$\overline{\text{RESET}}$	I	The reset input pin. At "L" level input, the LSI is initialized. At that time, oscillation is stopped and the power is shut off. When turning the power on, input at the "L" level, and change to the "H" level once the supplied power voltage has been stabilized.
29	SERIAL	I	The CPU interface select pin. The level is fixed to "L" when the parallel interface is selected.
10	$\overline{\text{CS}}$	I	The select input pin for the command interface and the audio interface. The $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs are accepted at the "L" level. The $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signal inputs are ignored at the "H" level.
9	$\text{D}/\overline{\text{C}}$	I	The select input pin for the command interface and the audio interface. The level of the $\text{D}/\overline{\text{C}}$ pin is set to "L" and the "L" pulse is input to the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins when inputting a command or outputting the internal status. The audio interface becomes enabled when the level is at "H".
5	$\overline{\text{WR}}$	I	The write pulse input pin. This pin is used in common by the command interface and the audio interface. [The "L" level selected for the $\text{D}/\overline{\text{C}}$ pin] The input data of the D7 to D0 pins is taken into the LSI as command data at the rising edge of the $\overline{\text{WR}}$ pin. Once the command data is taken in, the "L" level is output to the $\overline{\text{CBUSY}}$ pin, indicating that a command process is taking place. A "L" level command input of the $\overline{\text{CBUSY}}$ pin will be ignored. The command is input while the level of the $\overline{\text{CBUSY}}$ pin is at "H".
			[The "H" level selected for the $\text{D}/\overline{\text{C}}$ pin] Refer to the descriptions on the audio interface related pins on the next page.
4	$\overline{\text{RD}}$	I	The read pulse input pin. This pin is used in common by the command interface and the audio interface. [The "L" level selected for the $\text{D}/\overline{\text{C}}$ pin] Status data is output to the D7 to D0 pins while the level of the $\overline{\text{RD}}$ pin is at "L". In order to read the internal status, the level of the $\overline{\text{RD}}$ pin is set to "L" after the input of the RDSTAT command. Note that the status data will not be updated unless the RDSTAT command has been input.
			[The "H" level selected for the $\text{D}/\overline{\text{C}}$ pin] Refer to the descriptions on the audio interface related pins on the next page.
16-23	D7-D0	I/O	Data is input or output with the bi-directional data bus. These pins are used in common by the command interface and the audio interface.
12	$\overline{\text{CBUSY}}$	O	This pin outputs data at "L" level during command processing. Commands can be input when the $\overline{\text{CBUSY}}$ pin is at the "H" level.
11	VOX	O	The audio level detect signal output pin for recording. After recording has started, this pin outputs "H" once the recording input signal amplitude reaches the prescribed level.

Audio Interface Related Pins

Pin number	Pin name	I/O	Description
10	\overline{CS}	I	The select input pin for the command interface and the audio interface. The \overline{WR} and \overline{RD} inputs are accepted when set to the "L" level. The \overline{WR} and \overline{RD} signal inputs are ignored when set to the "H" level.
9	D/\overline{C}	I	The select input pin for the command interface and the audio interface. When the audio data is input or output, the level of the D/\overline{C} pin is set to "H" and the "L" level pulse is input to the \overline{WR} and \overline{RD} pins. The command interface is enabled when the level is at "L".
6	CH	I	The select input pin for the audio interface channel. When the level is at "L", the buffer memory of the left side is selected and the buffer memory status of the left side is output as status output of the EMP, MID and FUL pins. When the level is at "H", the buffer memory of the right side is selected and the buffer memory status of the right side is output as status output of the EMP, MID and FUL pins.
5	\overline{WR}	I	The write pulse input pin. This pin is used in common by the command interface and the audio interface. [The "H" level selected for the D/\overline{C} pin] The input data of the D7 to D0 pins are written into the buffer memory, which has been selected with the CH pin, at the rising edge of the \overline{WR} pin. The state of the \overline{CS} pin is irrelevant. [The "L" level selected for the D/\overline{C} pin] Refer to the descriptions on the command interface related pins on the preceding page.
4	\overline{RD}	I	The read pulse input pin. This pin is used in common by the command interface and the audio interface. [The "H" level selected for the D/\overline{C} pin] While the level of the \overline{RD} pin is at "L", the data read from the buffer memory, which has been selected with the CH pin, is output to the D7 to D0 pins. [The "L" level selected for the D/\overline{C} pin] Refer to the descriptions on the command interface related pins on the preceding page.
16-23	D7-D0	I/O	Data is input or output with the bi-directional data bus. These pins are used in common by the command interface and the audio interface.
1	FUL	O	The status signal, indicating that the entire buffer memory is full of data, will be output. A "H" active or "L" active selection can be made with the OPT command. Recordings made after the buffer memory becomes full are not stored in the buffer memory and are discarded. Therefore, any data written after the buffer memory becomes full, will not be played back.
2	MID	O	The status signal, indicating that at least half of the buffer memory is filled with data, will be output. A "H" active or "L" active selection can be made with the OPT command. Ordinarily, access to the buffer memory is controlled by the output of the MID pin.
3	EMP	O	The status signal, indicating that there is no data in the entire buffer memory, will be output. A "H" active or "L" active selection can be made with the OPT command.

Analog, Clock or Power Supply Related Pins

Pin number	Pin name	I/O	Description
39	MOUTL	O	The output pin of the microphone amplifier on the left side.
40	MINLM	I	The inverted input pin of the microphone amplifier on the left side.
41	MINLP	I	The non-inverted input pin of the microphone amplifier on the left side.
42	MOUTR	O	The output pin of the microphone amplifier on the right side.
43	MINRM	I	The inverted input pin of the microphone amplifier on the right side.
44	MINRP	I	The non-inverted input pin of the microphone amplifier on the right side.
36	LINL	I	The input pin of the line amplifier on the left side.
38	LINR	I	The input pin of the line amplifier on the right side.
37	SG	O	The output pin for the reference voltage (signal ground) of the analog circuit.
33	OUTR	O	This is the playback output pin for the right side. An external LC filter has been configured to eliminate a high-frequency component, as the PWM pulse is output.
32	OUTL	O	This is the playback output pin for the left side. An external LC filter has been configured to eliminate a high-frequency component, as the PWM pulse is output.
14	XT	I	An oscillator connection pin. When using an external clock, input it from this pin.
15	\overline{XT}	O	An oscillator connection pin. When using an external clock, leave this open.
25, 26, 27	PLL2-0	I	The multiplication setting pins for the built-in PLL. Set them so that the PLL output does not exceed 100 MHz.
13	TEST	I	A test pin. Fix it at "L". It has a built-in pull-down resistor
7, 8, 48	TESTO2-0	O	Test pins. Leave them open when the circuit board is connected.
30, 46	DVDD	—	The digital power supply pins. Connect a bypass capacitor of 0.1 μ F or more between these pins and the DGND pin.
24, 47	DGND	—	The digital ground pins.
45	AVDD	—	The analog power supply pin. Connect a bypass capacitor of 0.1 μ F or more between this pin and the AGND pin.
35	AGND	—	The ground supply pin.
31	PVDD	—	The power supply pin for the PWM driver. Connect a bypass capacitor of 0.1 μ F or more between this pin and the PGND pin.
34	PGND	—	The ground pin for the PWM driver.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +5.0	V
Input voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Storage temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 3.6	V
Operating temperature	T_{op}	—	-20 to +70	$^\circ\text{C}$
Source clock frequency	f_{osc}	—	3.0 to 6.5	MHz

ELECTRICAL CHARACTERISTICS**DC Characteristics**

$DV_{DD} = AV_{DD} = 2.7$ to 3.6 V
 DGND = AGND = 0 V, $T_a = -20$ to $+70^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
“H” input voltage	V_{IH}	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
“L” input voltage	V_{IL}	—	-0.3	—	0.6	V
“H” output voltage	V_{OH}	$I_{OH} = -1$ mA	$V_{DD} - 0.4$	—	—	V
“L” output voltage	V_{OL}	$I_{OL} = 2$ mA	—	—	0.4	V
“H” input current (Note 1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	μA
“H” input current (Note 2)	I_{IH2}	$V_{IH} = V_{DD}$	0.3	—	20	μA
“H” input current (Note 3)	I_{IH3}	$V_{IH} = V_{DD}$	30	—	150	μA
“H” input current (Note 4)	I_{IL1}	$V_{IL} = \text{GND}$	-10	—	—	μA
“L” input current (Note 2)	I_{IL2}	$V_{IL} = \text{GND}$	-20	—	-0.3	μA
Operating current consumption	I_{DD}	$f_{osc} = 4.096$ MHz at no load	—	TBD	40	mA
Current consumption during power down	I_{DDs}	$T_a = -20$ to $+70^\circ\text{C}$	—	TBD	10	μA

- Notes:
1. Applies to input pins excluding XT and TEST pins.
 2. Applies to XT pin.
 3. Applies to TEST pin.
 4. Applies to input pins excluding XT pin.

Analog Section CharacteristicsDV_{DD} = AV_{DD} = 2.7 to 3.6 VDGND = AGND = 0 V, T_a = -20 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MIN input impedance	R _{INM}	—	100	—	—	kΩ
LINL, LINR input impedance	R _{INL}	When line input is used	22	32	42	kΩ
LIN1, LIN2 maximum input amplitude	V _{LIN}	—	—	0.6 × V _{DD}	—	V _{pp}
MOUT, LOU _{TL} , LOU _{TR} output load resistance	R _{OUTA}	—	100	—	—	kΩ
Microphone amplifier gain setting range	G _{MIC}	—	—	—	30	dB
Line amplifier voltage gain error	G _{LINE}	—	-10	0	10	%
SG output voltage	V _{SG}	—	0.48 × V _{DD}	0.5 × V _{DD}	0.52 × V _{DD}	V
SG output resistance	R _{SG}	—	12	15	18	kΩ
OUTL, OU _{TR} output power	P _{OUT}	At BTL output and R _L = 16Ω	—	—	150	mW

(3) COMMON TO SERIAL AND PARALLEL INTERFACES

DESCRIPTION OF FUNCTIONS

Setting of Master Clock Frequency

The master clock (MCLK) of the ML2308 is a clock that uses the source oscillation clock of the XT pin with the multiplication factor of 15 to 29 applied by the internal PLL. The sampling frequency is determined by the frequency division of this MCLK. Thus the multiplication factor of the internal PLL needs to be changed, depending on the frequency of the source oscillation clock of the XT pin.

The multiplication factor of the internal PLL is set at PLL2 to PLL0 pins, as shown in the table below:

PLL2 (27Pin)	PLL1 (26Pin)	PLL0 (25Pin)	PLL Multiplication Factor
0	0	0	15
0	0	1	16
0	1	0	18
0	1	1	20
1	0	0	22
1	0	1	24
1	1	0	28
1	1	1	29

Do not alter the settings for the PLL multiplication factor after the power has been turned on.

The MCLK frequency is obtained by multiplying the PLL multiplication factor with the source oscillation frequency.

Do not conduct settings that result in the MCLK's frequency exceeding 100 MHz.

The sampling frequency is selected with the S3 to S0 bits of the METHOD command. Respective sampling frequencies are determined by the relational expression with the MCLK, as shown below:

S3	S2	S1	S0	Relationship between Sampling Frequency and MCLK	Sampling Frequency When Source Oscillation Frequency = 4.096 MHz PLL Multiplication Factor = 24
0	0	0	0	Not used	Not used
0	0	0	1	MCLK/15360 (Hz)	6.4 kHz
0	0	1	0	MCLK/7680 (Hz)	12.8 kHz
0	0	1	1	MCLK/3840 (Hz)	25.6 kHz
0	1	0	0	MCLK/24576 (Hz)	4.0 kHz
0	1	0	1	MCLK/12288 (Hz)	8.0 kHz
0	1	1	0	MCLK/6144 (Hz)	16.0 kHz
0	1	1	1	MCLK/3072 (Hz)	32.0 kHz
1	0	0	0	MCLK/16384 (Hz)	6.0 kHz
1	0	0	1	MCLK/8192 (Hz)	12.0 kHz
1	0	1	0	MCLK/4096 (Hz)	24.0 kHz
1	0	1	1	MCLK/2048 (Hz)	48.0 kHz

Note: The unit of the clock frequency assigned for the MCLK is Hz.

When using a 44.1 kHz sampling frequency, set the source oscillation frequency to 3.7632 MHz, the PLL multiplication factor to the multiple factor of 24 and the S3 to S0 bits of the METHOD command to Bh (hexadecimal).

When using a 4.096 MHz source oscillation frequency, set the PLL multiplication factor to the multiple factor of 22 and the S3 to S0 bits of the METHOD command to Bh (hexadecimal). The sampling frequency in this instance will become 44 kHz, with an error of 44.1 kHz being -0.227%.

Buffer Memory Configuration

There are two buffer memories, one for the left side and the other for the right side. The capacity of the buffer memory can be selected with the OPT command from among 512 bits, 256 bits and 128 bits. However, the memory capacity that varies from one channel to another cannot be set.

Since the buffer time varies depending on the audio synthesis method and sampling frequency used, select the buffer memory capacity in proportion to the load of the CPU for the external control. The default value is set to 512 bits.

The maximum buffer time for the buffer memory of respective audio synthesis methods, with the buffer memory capacity of 512 bits and sampling frequency of 16kHz, is shown below:

Audio Synthesis Method	Maximum Buffer Time
2-bit ADPCM2	256 samples/16kHz = 16 ms
3-bit ADPCM2	160 samples/16kHz = 10 ms
4-bit ADPCM2	128 samples/16kHz = 8 ms
5/6/7/8-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 8-bit μ -law PCM	64 samples/16kHz = 4 ms
16-bit straight PCM	32 samples/16kHz = 2 ms

Audio Synthesis Methods

This LSI supports four types of audio synthesis methods to meet the needs of various audio types: 2-bit/3-bit/4-bit/5-bit/6-bit/7-bit/8-bit ADPCM2, 8-bit/16-bit straight PCM, 8-bit nonlinear PCM and μ -law PCM.

2-bit/3-bit/4-bit/5-bit/6-bit/7-bit/8-bit ADPCM2

The ADPCM2 method is an audio synthesis method that achieves higher sound quality than ADPCM (Adaptive Differential Pulse Code Modulation). This method adaptively changes the quantized width Δ for each sample and codes it as 2-bit to 8-bit data. For human voices, animal cries, or natural sounds, this method allows the audio data volume to be reduced.

8-bit/16-bit Straight PCM

This method is the best of the three methods for following audio waveforms in all audio areas. It is suitable for sounds with sudden waveform changes and waveforms in pulse forms.

8-bit Nonlinear PCM

This method is for playing back audio input in the range of $7/16 V_{DD}$ to $9/16 V_{DD}$ as 10-bit straight PCM sound quality, and for improving the sound quality of waveforms with low amplitude.

μ -law PCM

This method is for G.711 compliant playback.

Sampling Frequency

There are restrictions on the sampling frequencies that can be used, depending on the audio synthesis methods as well as the recording and playback methods (monaural, stereo or double speed playback). Respective audio synthesis methods and sampling frequencies that can be used for recording and playback modes are shown in the tables below.

• At Stereo Recording and Playback

Recording and Playback Mode Audio Synthesis Method	Sampling Frequencies Available			
	x1 Recording and Playback	x1.25 Recording and Playback	x1.5 Recording and Playback	x2 Recording and Playback
2/3/4-bit ADPCM2 method	24.0 kHz or lower	25.6 kHz or lower	16.0 kHz or lower	12.8 kHz or lower
5/6/7/8-bit ADPCM2 method	16.0 kHz or lower	16.0 kHz or lower	16.0 kHz or lower	12.0 kHz or lower
Full PCM method	All frequencies available	All frequencies available	All frequencies available	32 kHz or lower

• At Monaural Recording and Playback

Recording and Playback Mode Audio Synthesis Method	Sampling Frequencies Available			
	x1 Recording and Playback	x1.25 Recording and Playback	x1.5 Recording and Playback	x2 Recording and Playback
2/3/4-bit ADPCM2 method	All frequencies available	All frequencies available	32.0 kHz or lower	25.6 kHz or lower
5/6/7/8-bit ADPCM2 method	32.0 kHz or lower	32.0 kHz or lower	32.0 kHz or lower	24.0 kHz or lower
Full PCM method	All frequencies available	All frequencies available	All frequencies available	All frequencies available

Note: The sampling frequencies that can be used as described above represent the case where the source oscillation frequency is $f_{osc} = 4.096$ MHz and the set PLL multiplication factor is 24.

COMMAND FUNCTION

Command List

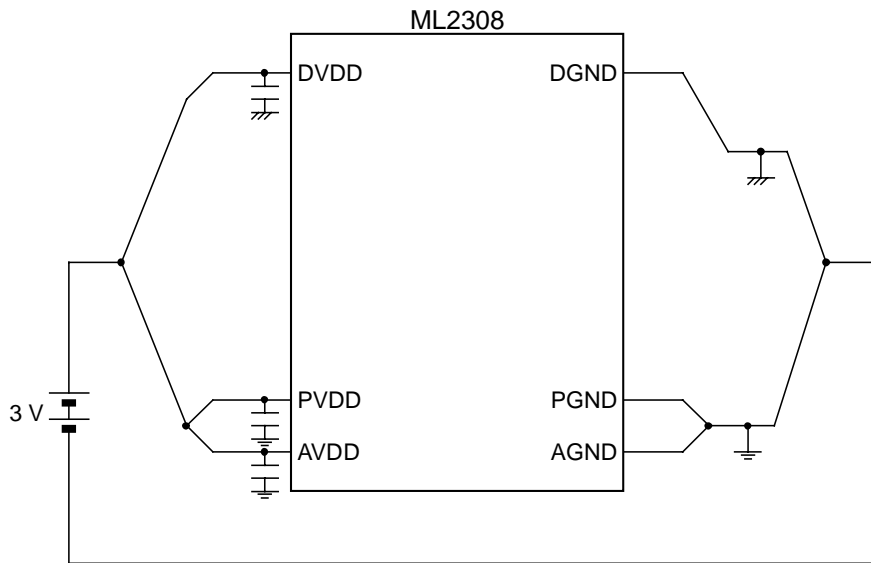
Command name	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOOP	0	0	0	0	0	0	0	0	No function
PDWN	0	0	0	1	0	0	0	1	Power down command
REC	0	0	1	0	0	0	R	L	Recording start command
PLAY	0	0	1	1	0	0	R	L	Playback start command
STOP	0	1	0	0	0	0	R	L	Recording/playback stop command
PAUSE	0	1	0	1	0	CL	R	L	Recording/playback pause command
BPLAY	0	1	1	0	0	0	R	L	Block playback start command
	0	0	0	0	0	B2	B1	B0	
SPEED	0	1	1	1	0	X2	X1	X0	Fast/slow listening setting command
METHOD	1	0	0	0	0	0	R	L	Audio synthesis method, sampling frequency setting command
	P3	P2	P1	P0	S3	S2	S1	S0	
VOL	1	0	0	1	0	0	R	L	Volume setting command
	V7	V6	V5	V4	V3	V2	V1	V0	
PAN	1	0	1	0	0	0	R	L	Panpot setting command
	R3	R2	R1	R0	L3	L2	L1	L0	
DRC	1	0	1	1	0	0	0	0	Automatic level control setting command
	0	0	0	DR4	DR3	DR2	DR1	DR0	
ATLT	1	1	0	0	0	0	0	0	ADC attack time/release time setting command
	LT3	LT2	LT1	LT0	AT3	AT2	AT1	AT0	
RDSTAT	1	1	0	1	0	0	0	0	Status read command
OPT	1	1	1	0	0	0	0	0	Buffer memory capacity/pin status/stereo/buffer memory serial interface setting
	0	0	0	ADT	AI	M1	M0	A	
MTSPD	1	1	1	0	1	0	MS1	MS0	Transition time setting command when varying volume
OPTANA	1	1	1	1	0	0	0	0	Analog option setting command
	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	

POWER SUPPLY WIRING

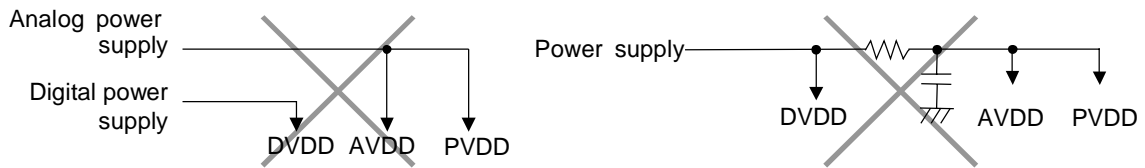
The power supply of the ML2308 is divided into the following three supplies

- Digital power supply (DVDD)
- Analog power supply for analog circuits (AVDD)
- Analog power supply for audio output driver (PVDD)

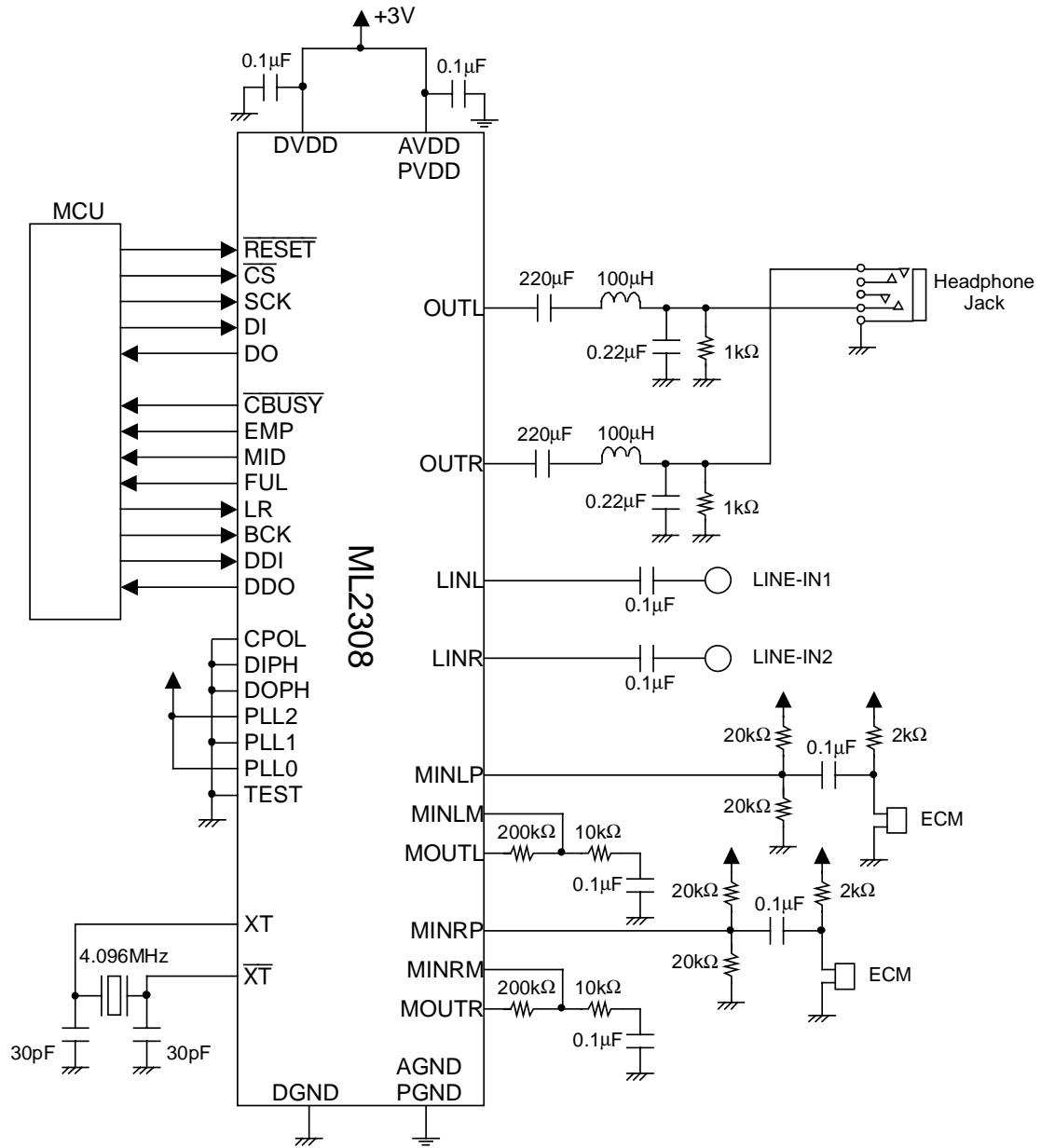
Supply DVDD, PVDD, and AVDD from the same power supply and divide the wiring for the analog and digital systems as shown below.



Do not arrange the wiring as shown below.

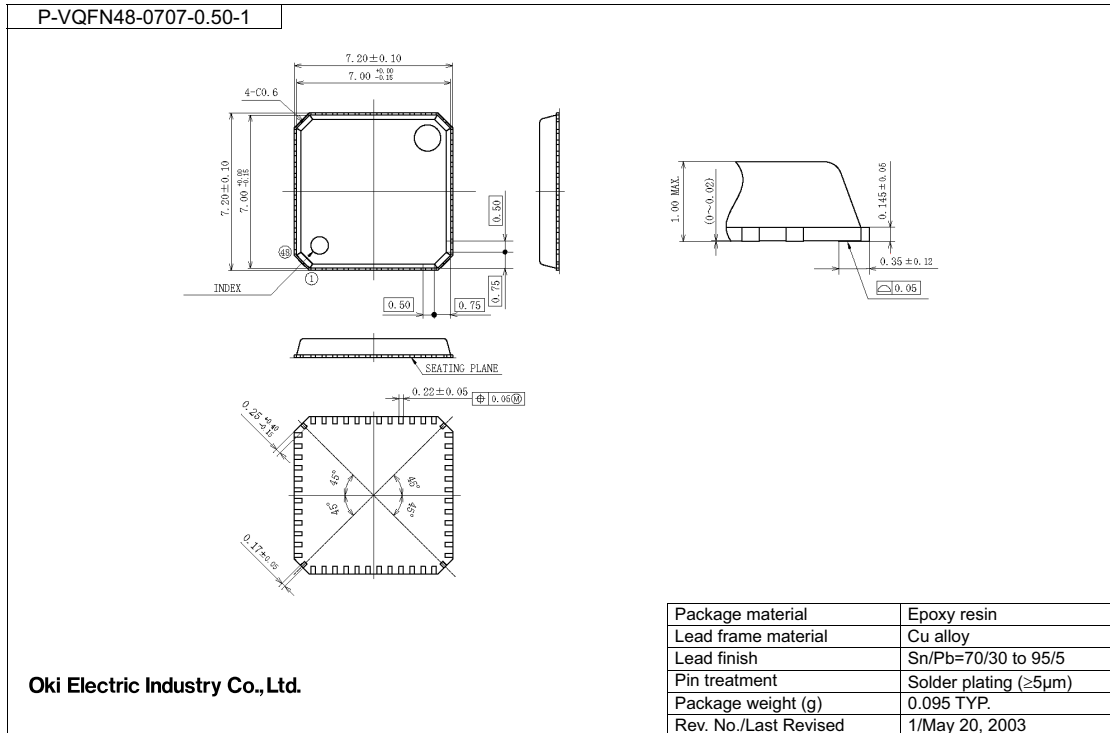


EXAMPLE OF APPLICATION CIRCUIT (WHEN SERIAL INTERFACE IS USED)



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

WHEN PLACING AN ORDER

Specify ML2308GP (Package: 48-pin plastic VQFN).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL2308DIGEST-01	Aug. 9, 2004	–	–	Preliminary edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
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