MH25609ATN-10

2359296-BIT(262144-WORD BY 9-BIT)CMOS STATIC RAM

DESCRIPTION

The MH25609ATN is a 2359296-bit CMOS static RAM module organized as 262144-word by 9-bits. It consists of two industry standard 128K × 8 static RAMs, 256K × 1 static RAM, decoder, and one logic.

The stand-by current is low enough for a battery backup application. It is mounted a flat package and SOJ on a 35-pin single in line package.

FEATURES

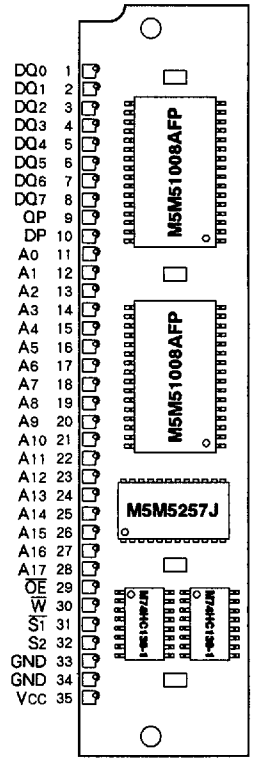
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by data retention (max)
MH25609ATN-10	100ns	213mA	300 μA

- Single +5V Power supply
- No Clock, No Refresh
- Simple Memory Expansion by $\overline{S1}$, S2
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Bit nine (DP, QP) is generally used for parity
- Solder plating contact

APPLICATION

Small Capacity Memory Unit

PIN CONFIGURATION (TOP VIEW) [Single side]



Outline 35N9B

MITSUBISHI ELECTRIC

MH25609ATN

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FUNCTION

The operation mode of the MH25609ATN is determine by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$, or S2, whichever occurs first requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and data bus contention problem in the write cycle is eliminated.

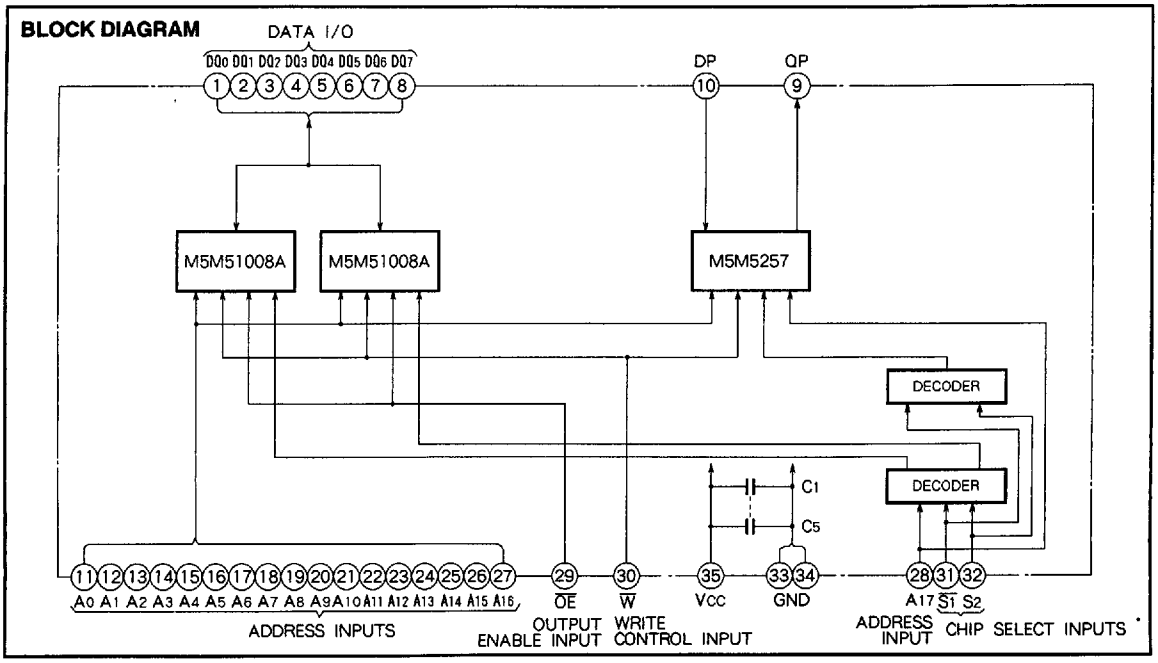
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H).

When setting $\overline{S1}$ at a high level, or S2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chip and memory expansion by $\overline{S1}$ and S2.

FUNCTION TABLE

$\overline{S1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand by
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	DIN	Active
L	H	H	L	Read	DOUT	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	− 0.3~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	1.7	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 40~125	℃

* In case of pulse width ≦ 50ns, − 3.0V.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		3.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		− 0.3*		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA	2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA			0.4	V
I_I	Input current	V_I = 0~V_{CC}			± 4	μA
I_{OZ}	Output current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0~V_{CC}			± 12	μA
I_{CC1}	Active supply current (TTL)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH} Output open Other inputs = V_{IH}			213	mA
	Active supply current (CMOS)	$\overline{S_1}$ ≦ 0.2V, S_2 ≧ V_{CC} − 0.2V Output open Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V		110	163	
I_{CC2}	Stand-by supply current	① $\overline{S_1}$, A_{17} ≦ 0.2 or ≧ V_{CC}−0.2, S_2 ≦ 0.2, Other input = 0~V_{CC} ② $\overline{S_1}$ and S_2 ≧ V_{CC}−0.2V A_{17} ≦ 0.2 or ≧ V_{CC}−0.2 Other inputs = 0~V_{CC}			300	μA
I_{CC3}	Stand-by supply current	$\overline{S_1}$ = V_{IH}, S_2 = V_{IL} Other inputs = 0~V_{CC}		6	9	mA
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz			35	pF
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz			25	pF

Note 1 : Direction for current flowing into an IC is positive (no mark).
2 : Typical value is V_{CC} = 5V, Ta = 25℃.
* In case of pulse width ≦ 50ns, − 3.0V.

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AC SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Test condition

Input pulse level ····· V_{IH} = 3.2V, V_{IL} = 0V
Input rise and fall time ····· 5ns
Reference level ····· V_{OH} = V_{OL} = 1.5V
Transition is measured ± 500mV from steady state voltage (for t_{en}, t_{dis})
Output loads (Fig. 1) ····· C_L = 30pF
C_L = 5pF (for t_{en}, t_{dis})

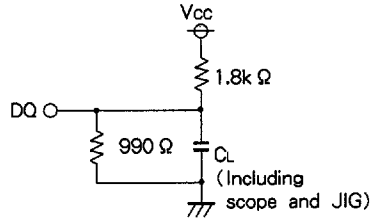

Fig. 1 Output load

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CR}	Read cycle time	100			ns
$t_{a(A)}$	Address access time			100	ns
$t_{a(\overline{ST})}$	Chip select 1 access time			100	ns
$t_{a(S2)}$	Chip select 2 access time			100	ns
$t_{a(\overline{OE})}$	Output enable access time			55	ns
$t_{dis(\overline{ST})}$	Output disable time after $\overline{S_1}$ high			45	ns
$t_{dis(S2)}$	Output disable time after S_2 low			45	ns
$t_{dis(\overline{OE})}$	Output disable time after $\overline{OE}$ high			30	ns
$t_{en(\overline{ST})}$	Output enable time after $\overline{S_1}$ low	10			ns
$t_{en(S2)}$	Output enable time after S_2 high	10			ns
$t_{en(\overline{OE})}$	Output enable time after $\overline{OE}$ low	5			ns
$t_{V(A)}$	Data valid time after address charge	10			ns

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CW}	Write cycle time	100			ns
$t_{W(\overline{W})}$	Write pulse width	65			ns
$t_{su(A)}$	Address set up time	0			ns
$t_{su(\overline{ST})}$	Chip select 1 set up time	85			ns
$t_{su(S2)}$	Chip select 2 set up time	85			ns
$t_{su(D)}$	Data set up time	35			ns
$t_{h(D)}$	Data hold time	0			ns
$t_{rec(\overline{W})}$	Write recovery time	0			ns
$t_{dis(\overline{W})}$	Output disable time after $\overline{W}$ low			30	ns
$t_{dis(\overline{OE})}$	Output disable time after $\overline{OE}$ high			30	ns
$t_{en(\overline{W})}$	Output enable time after $\overline{W}$ high	5			ns
$t_{en(\overline{OE})}$	Output enable time after $\overline{OE}$ low	5			ns

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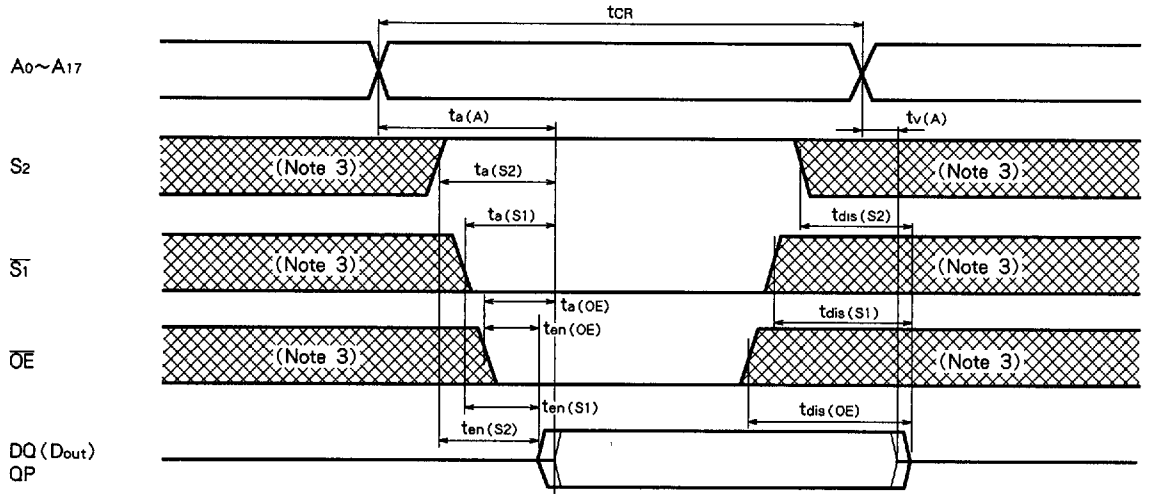
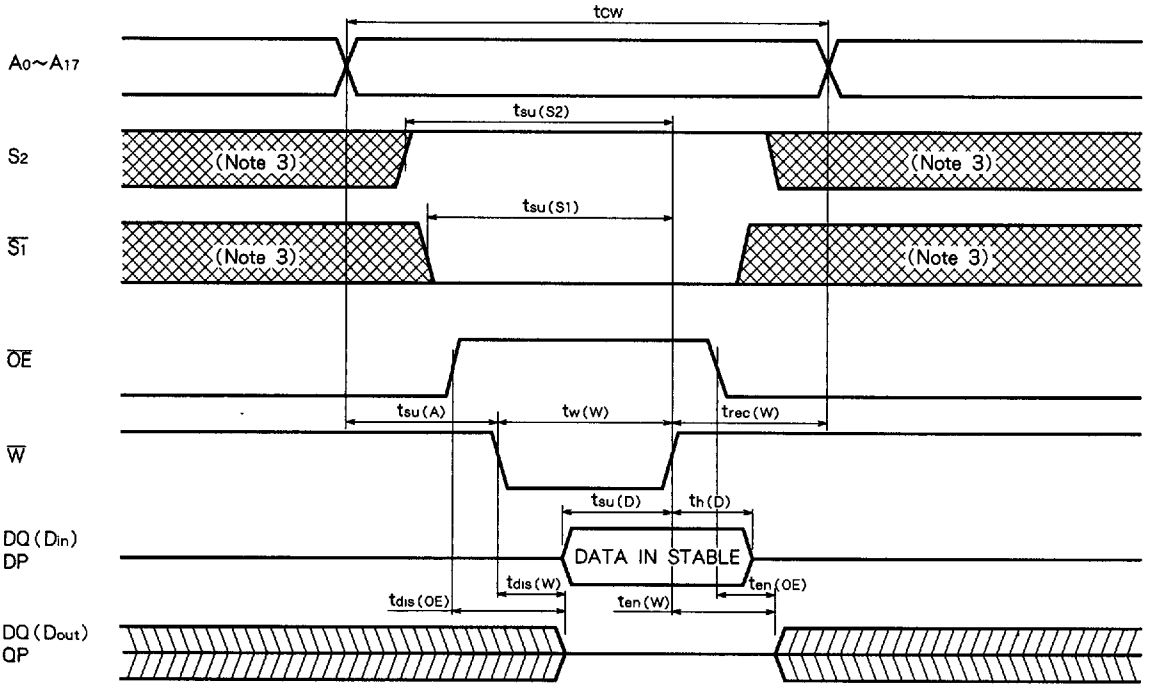
TIMING DIAGRAM

Read cycle



W = "H" level

Write cycle (W control)



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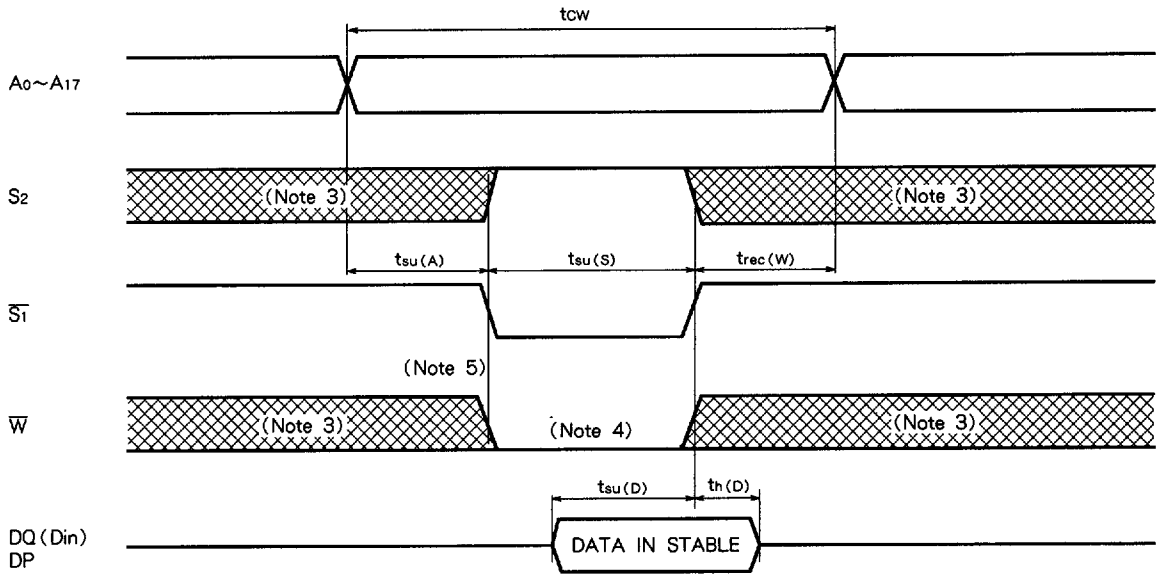
Write cycle ($\overline{S}$ control)



Note 3 : Hatching indicates the state is don't care.
4 : Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S1}$ low or S2 high, the output remains in the high-impedance state.
6 : Don't apply inverted pulse signal externally when DQ pin is in output mode.

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POWER DOWN CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2.0			V
$V_{I(\overline{ST})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$	3.2			V
		2V ≦ V_{CC} ≦ 2.2V		$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$			0.8	V
		$V_{CC(PD)}$ < 4.5V			0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, S_2 ≦ 0.2V or $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V Other inputs = 0~3V			150	μA

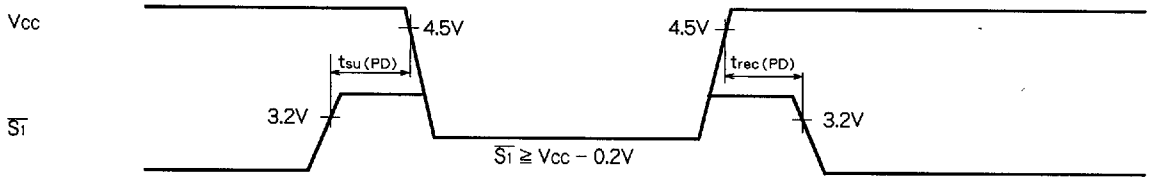
Note 7 : When $\overline{S_1}$ is operated at 2.2V (V_{IH} min) and the supply voltage is between 4.5V and 2.4V, supply current is defined as I_{CC3}.

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control



S_2 control