MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this document
by MCM29020/D

MCM29020
MCM29040
MCM29080

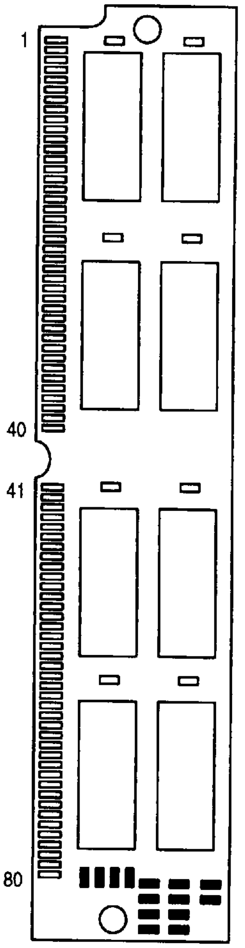
Product Preview

2, 4, and 8 MB Flash SIMM Family

The MCM290x0 is a 5 V-only, sector erase flash memory SIMM organized as either one, two, or four banks of 512K x 32 bits. The modules are JEDEC-standard 80-pin SIMMs, with each bank consisting of four 512K x 8 CMOS 5.0 V-only sector erase flash memories, mounted on a substrate along with decoupling capacitors. The MCM29020 is a 2 MB Flash SIMM, the MCM29040 is 4 MB and the MCM29080 is 8 MB.

- 5.0 V ± 10% Write and Erase Minimizes System Level Power Requirements
- JEDEC Industry Standard Pin-Out and Architecture
- Compatible with JEDEC-Standard (E^2PROM) Commands
- Minimum 100,000 Write/Erase Cycles
- Sector Erase Architecture:
  - Eight Equal Size Sectors of 64K Bytes Each
  - Any Combination of Sectors can be Concurrently Erased
  - Supports Full Chip Erase
- Embedded Erase™ Algorithms Allow Automatic Preprogram and Erase at any Sector
- Embedded Program™ Algorithms Allow Automatic Write and Verify of Data at a Specified Address
- $\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion
- Sector Protection Allows Hardware Disable of Sectors from Write or Erase Operations
- Low V_{CC} Write Inhibit ≤ 3.2 V
- Suspend Erase/Resume Feature to Allow a Read Cycle in Another Sector Within the Same Bank During an Erase Cycle
- Consists of Four, Eight, or Sixteen 512K x 8 Flash Memories, and 0.22 µF (Min) Decoupling Capacitors
- Fast Access Time: MCM290x0-90 = 90 ns (Max)
- Low Active Power Dissipation: MCM290x0-90 = 1.4 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels: MCM29020-90 = 22 mW (Max)
    - MCM29040-90 = 44 mW (Max)
    - MCM29080-90 = 88 mW (Max)
  - CMOS Levels: MCM29020-90 = 2.2 mW (Max)
    - MCM29040-90 = 4.4 mW (Max)
    - MCM29080-90 = 8.8 mW (Max)

8 MB SIMM
MCM29080S
CASE 1105–01
TOP VIEW



PIN NAMES	
A0 – A18	Address Input
$\overline{\text{CE0}}$ – $\overline{\text{CE3}}$*	Chip Enable
$\overline{\text{WE0}}$ – $\overline{\text{WE3}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ0 – DQ31	Data Input/Output
PD1 – PD7	Presence Detect
NC	No Connection
V_{CC}	Power Supply
V_{SS}	Ground

* $\overline{\text{CE1}}$ only available on 4 MB and 8 MB modules. $\overline{\text{CE2}}$ and $\overline{\text{CE3}}$ only available on 8 MB

Embedded Erase and Embedded Program are trademarks of Advanced Micro Devices, Inc.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

5/94

MOTOROLA

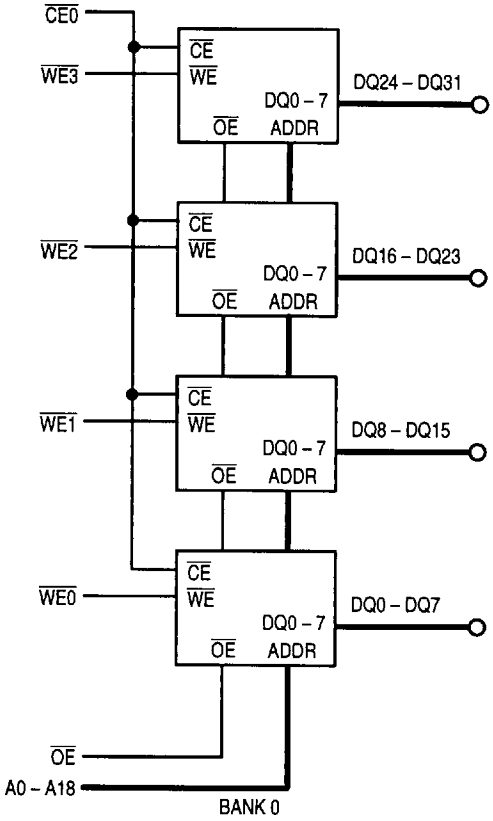
PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	21	*	41	A11	61	DQ9
2	V_{CC}	22	*	42	A10	62	DQ8
3	NC	23	*	43	A9	63	DQ7
4	$\overline{OE}$	24	$\overline{CE0}$	44	A8	64	DQ6
5	$\overline{WE0}$	25	V_{SS}	45	A7	65	DQ5
6	$\overline{WE1}$	26	DQ29	46	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	$\overline{WE2}$	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	NC
12	DQ20	32	NC	52	A0	72	V_{CC}
13	DQ21	33	NC	53	$\overline{WE3}$	73	PD1
14	DQ22	34	A18	54	V_{SS}	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	V_{SS}

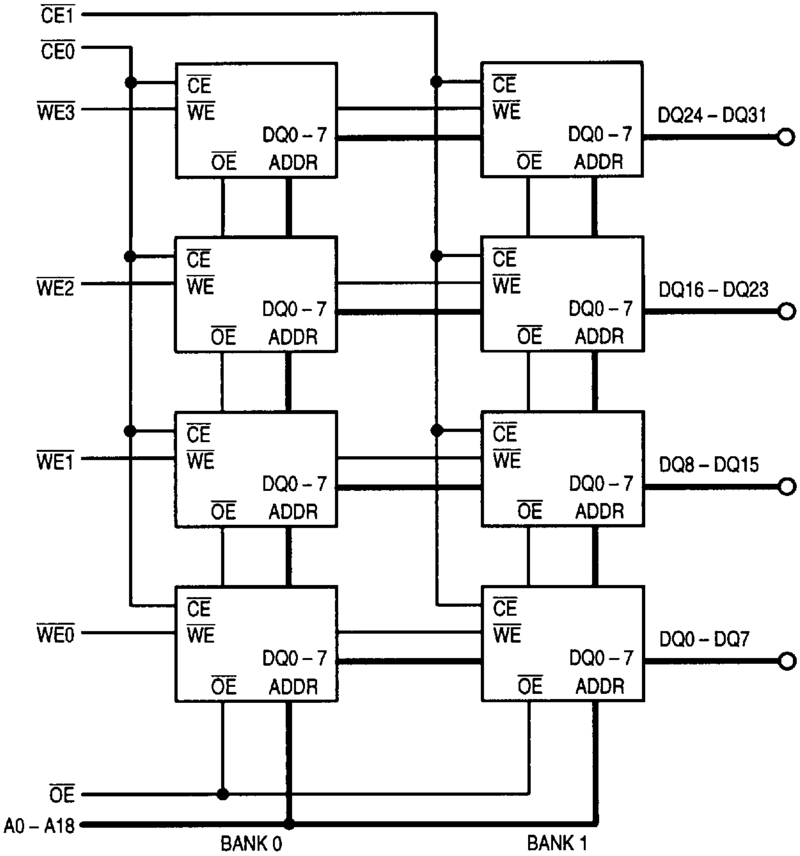
* SIMM DENSITY			
Pin No.	2 MB	4 MB	8 MB
21	NC	NC	$\overline{CE3}$
22	NC	NC	$\overline{CE2}$
23	NC	$\overline{CE1}$	$\overline{CE1}$

PRESENCE DETECT PIN OUT 90 ns SIMM			
Pin Name	2 MB	4 MB	8 MB
PD1	V_{SS}	NC	V_{SS}
PD2	V_{SS}	NC	NC
PD3	V_{SS}	NC	NC
PD4	NC	V_{SS}	V_{SS}
PD5	NC	NC	NC
PD6	NC	NC	NC
PD7	V_{SS}	V_{SS}	V_{SS}

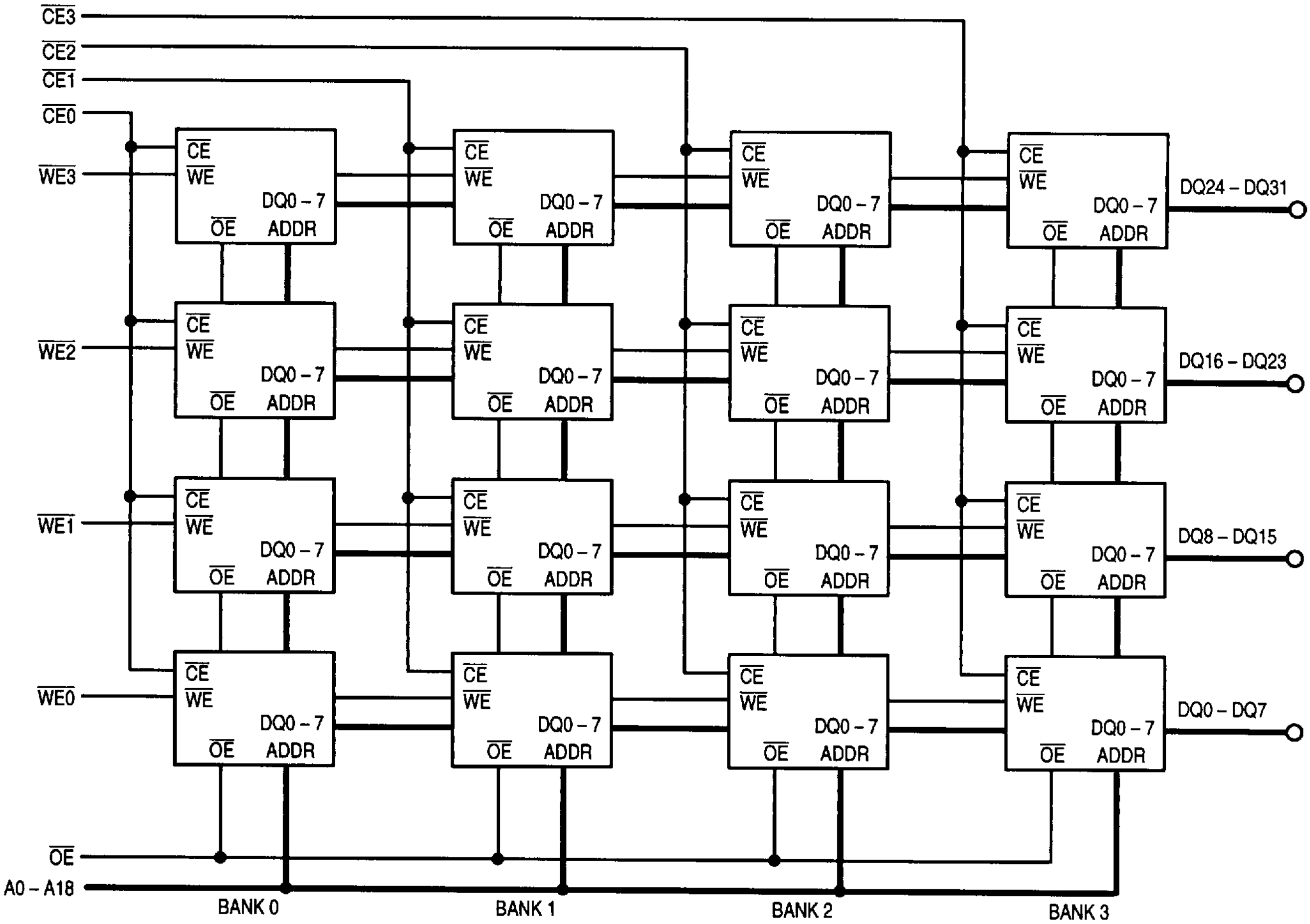
MCM29020
2 MB SIMM BLOCK DIAGRAM



MCM29040
4 MB SIMM BLOCK DIAGRAM



MCM29080
8 MB SIMM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Notes 1 through 4)

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 1)	V_{CC}	– 2.0 to + 7	V
Voltage Relative to V_{SS}: All Pins Except A9, $\overline{CE}$, and $\overline{OE}$ (Note 1) A9, $\overline{CE}$, and $\overline{OE}$ (Note 2)	V_{in}, V_{out}	 – 2.0 to + 7 – 2.0 to + 14	V
Data Output Current per DQ Pin (Note 3)	I_{out}	200	mA
Power Dissipation	P_D	1.8	W
Operating Temperature Range	T_C	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 65 to + 125	°C

NOTES:

1. Minimum dc voltage on input or I/O pins is – 0.5 V. During voltage transitions, inputs may overshoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. Minimum dc voltage on pin A9, $\overline{CE}$, or $\overline{OE}$ is – 0.5 V. During voltage transitions, inputs may overshoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on pin A9, $\overline{CE}$, or $\overline{OE}$ is + 13.5 V which may overshoot to + 14.0 V for periods of up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be longer than one second.
4. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_C = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS}, see Note)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.0	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5	—	0.8	V
Voltage for Autoselect and Sector Protect	V_{ID}	11.5	12.0	12.5	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	3.2	—	4.2	V

NOTE: Only one bank active.

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Active Current ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$)		I_{CC1}			mA	1, 2
	MCM29020F90, t_{RC} = 90 ns		—	160		
	MCM29040F90, t_{RC} = 90 ns		—	164		
	MCM29080F90, t_{RC} = 90 ns		—	172		
V_{CC} Active Current ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$)		I_{CC2}			mA	1, 3, 4
	MCM29020F90, t_{RC} = 90 ns		—	240		
	MCM29040F90, t_{RC} = 90 ns		—	244		
	MCM29080F90, t_{RC} = 90 ns		—	252		
V_{CC} Standby Current – TTL Levels ($V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$)		I_{CC3}			mA	
	MCM29020F90, t_{RC} = 90 ns		—	4		
	MCM29040F90, t_{RC} = 90 ns		—	8		
	MCM29080F90, t_{RC} = 90 ns		—	16		
V_{CC} Standby Current – CMOS Levels ($V_{CC} = V_{CC}$ max, $\overline{CE} = V_{CC} \pm 0.5$ V, $\overline{OE} = V_{IL}$)		I_{CC4}			mA	
	MCM29020F90, t_{RC} = 90 ns		—	0.4		
	MCM29040F90, t_{RC} = 90 ns		—	0.8		
	MCM29080F90, t_{RC} = 90 ns		—	1.6		
Input Load Current ($V_{SS} \le V_{in} \le V_{CC}$, $V_{CC} = V_{CC}$ max)		I_{LI}			µA	
	MCM29020F90		– 4	4		
	MCM29040F90		– 8	8		
	MCM29080F90		– 16	16		
A9 Input Load Current (A9 = 12.5 V, $V_{CC} = V_{CC}$ max)		I_{LIT}			µA	
	MCM29020F90		– 200	200		
	MCM29040F90		– 400	400		
	MCM29080F90		– 800	800		
Output Leakage Current ($V_{SS} \le V_{out} \le V_{CC}$, $V_{CC} = V_{CC}$ max)		I_{LO}			µA	
	MCM29020F90		– 1	1		
	MCM29040F90		– 2	2		
	MCM29080F90		– 4	4		
Output High Voltage (I_{OH} = – 2.5 mA, $V_{CC} = V_{CC}$ min)		V_{OH1}	2.4	—	V	
Output High Voltage (I_{OH} = – 100 µA, $V_{CC} = V_{CC}$ min)		V_{OH2}	V_{CC} – 0.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:
1. Only one bank active.
2. The I_{CC} current listed includes both the dc operating current and the frequency dependent component (at 6 MHz).
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Not 100% tested.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	2 MB Max	4 MB Max	8 MB Max	Unit
Input Capacitance	Addresses (Except A9)	C_{in}	40	70	130	pF
	$\overline{CE}$		46	46	46	
	$\overline{OE}$, A9		46	82	154	
	$\overline{WE}$		18	25	40	
Input/Output Capacitance	DQ	$C_{I/O}$	22	34	58	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

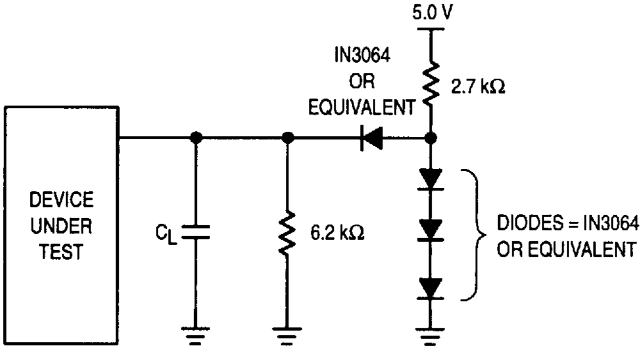
(V_{CC} = 5.0 V ± 10%, T_C = 0 to 70°C, Unless Otherwise Noted)

READ ONLY OPERATIONS CYCLE (See Note 1)

Parameter	Symbol		MCM290x0-90		Unit	Notes
	Std	Alt	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	90	—	ns	2
Address to Output Delay, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	t_{AVQV}	t_{ACC}	—	90	ns	
Chip Enable to Output Delay, $\overline{OE}$ = V_{IL}	t_{ELQV}	t_{CE}	—	90	ns	
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	35	ns	
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	20	ns	3
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	20	ns	3
Output Hold From Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	0	—	ns	
Write Recovery Time Before Read	t_{WHGL}	t_{WR}	6	—	µs	

NOTES:

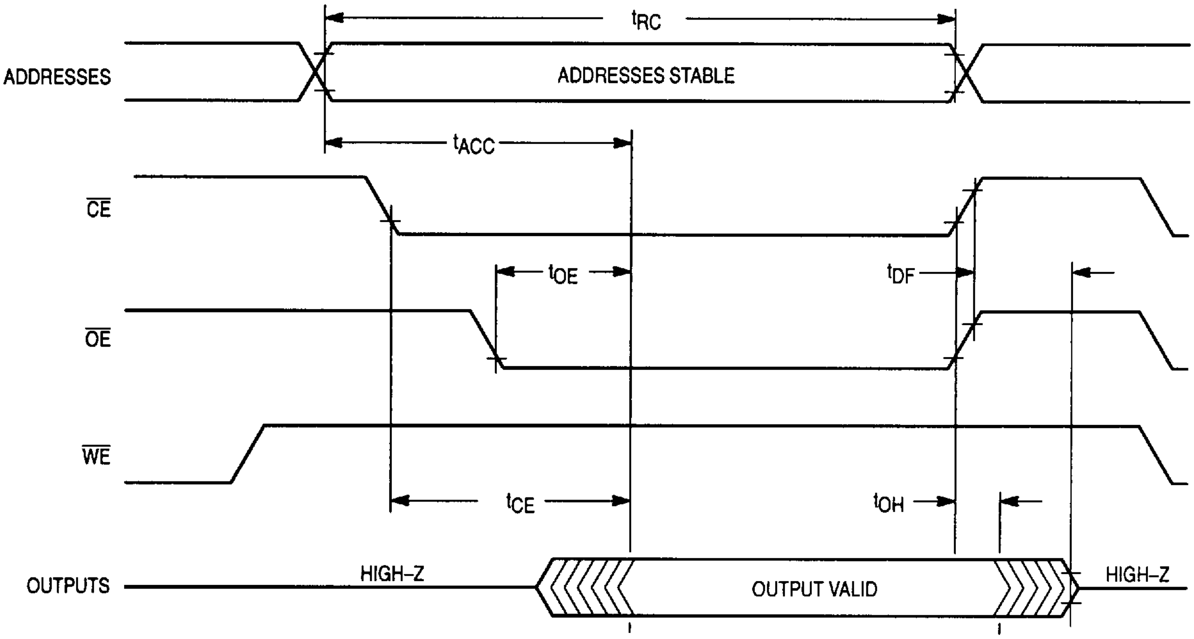
1. Test conditions — output load: one TTL gate and 100 pF; input rise and fall times: 20 ns; input pulse levels: 0.45 V to 2.4 V; timing measurement reference level: input, 0.8 and 2.0 V; output, 0.8 and 2.0 V.
2. Not 100% tested.
3. Output driver disable time.



NOTE: C_L = 100 pF including jig capacitance.

Figure 1. Test Conditions

READ CYCLE



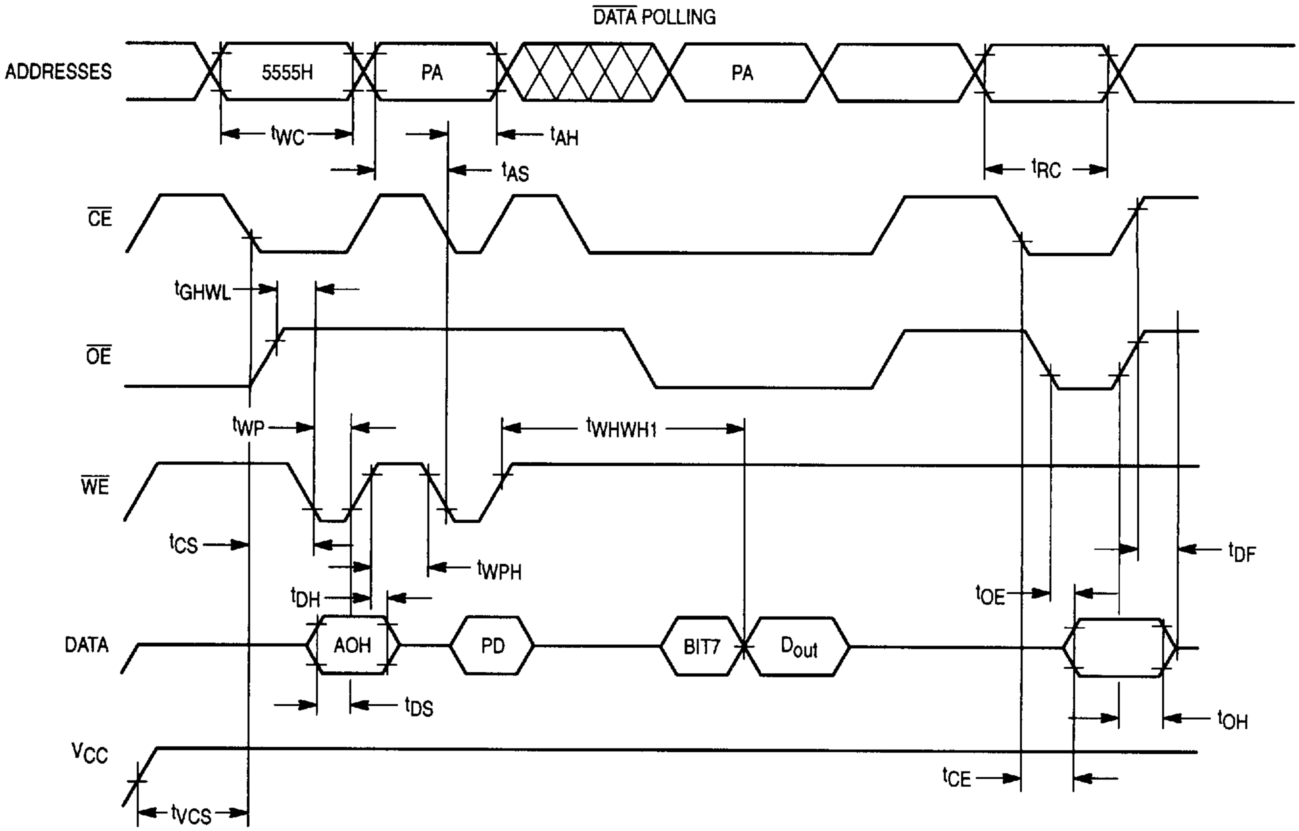
WRITE/ERASE/PROGRAM OPERATIONS

Parameter	Symbol		MCM290x0-90			Unit	Notes
	Std	Alt	Min	Typ	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	90	—	—	ns	1
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	ns	
Address Hold Time	t_{WLAX}	t_{AH}	45	—	—	ns	
Data Setup Time	t_{DVWH}	t_{DS}	45			ns	
Data Hold Time	t_{WHQX}	t_{DH}	0	—	—	ns	
Output Enable Setup Time		t_{OES}	0	—	—	ns	
Output Enable Hold Time Read Toggle and $\overline{\text{Data}}$ Polling		t_{OEH}	0 10	— —	— —	ns	1
Write Recovery Time Before Read	t_{WHGL}	t_{WR}	6	—	—	µs	
Read Recovery Time Before Write	t_{GHWL}		0	—	—	ns	
$\overline{\text{CE}}$ Setup Time	t_{ELWL}	t_{CS}	0	—	—	ns	
$\overline{\text{CE}}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	45	—	—	ns	
Write Pulse Width High	t_{WHWL}	t_{WPH}	20	—	—	ns	
Byte Programming Operation	t_{WHWH1}		—	16	—	µs	
Erase Operation	t_{WHWH2}		—	1.5	30	s	2
V_{CC} Setup Time		t_{VCS}	50	—	—	µs	1
Voltage Transition Time		t_{VLHT}	4	—	—	µs	1, 3
Write Pulse Width		t_{WPP}	100	—	—	µs	3
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{OESP}	4	—	—	µs	1, 3
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{CSP}	4	—	—	µs	1, 4

NOTES:

1. Not 100% tested.
2. This does not include the preprogramming time.
3. These timings are for Sector Protect/Unprotect operations.
4. This timing is only for Sector Unprotect.

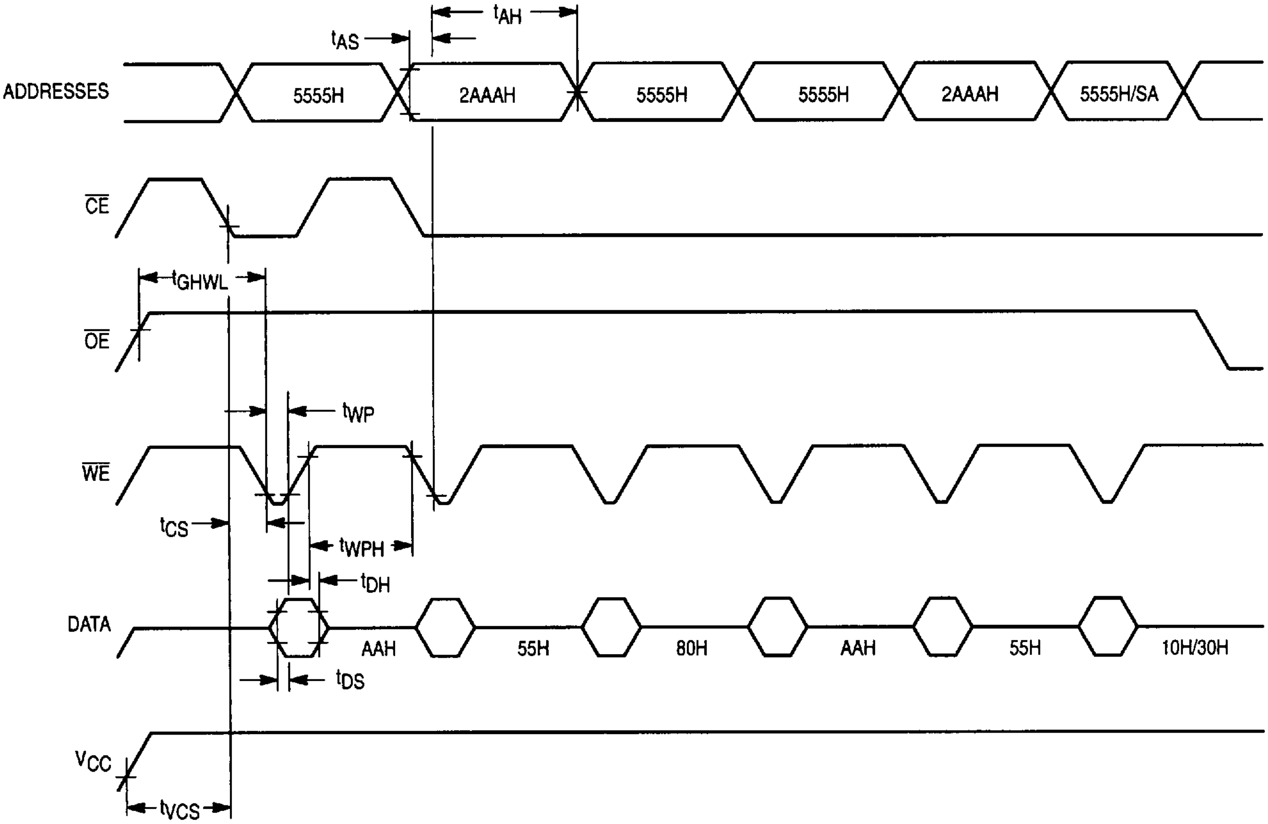
PROGRAM OPERATIONS



NOTES:

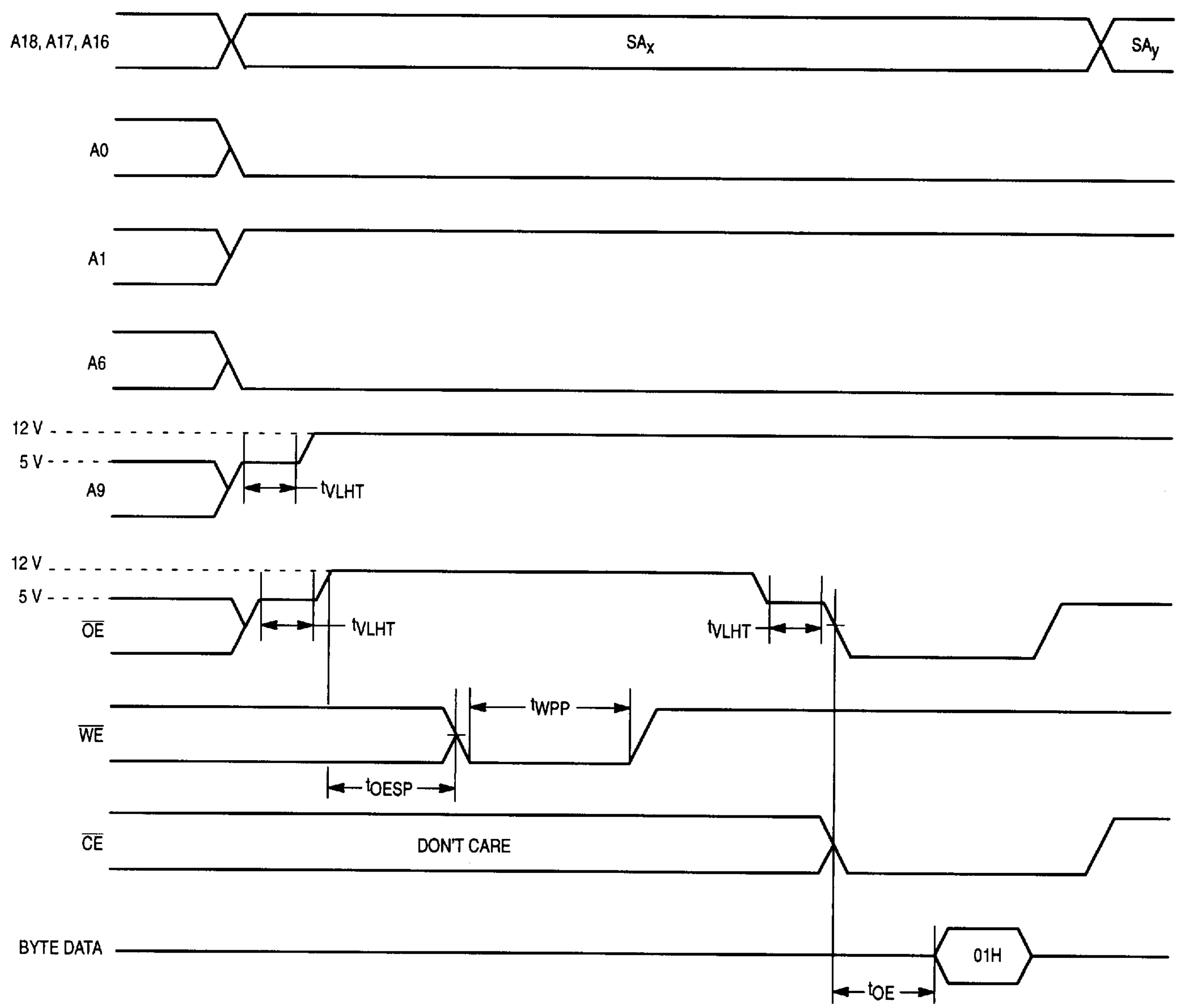
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. BIT7 is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

CHIP/SECTOR ERASE OPERATIONS



NOTE: SA is the sector address for Sector Erase.

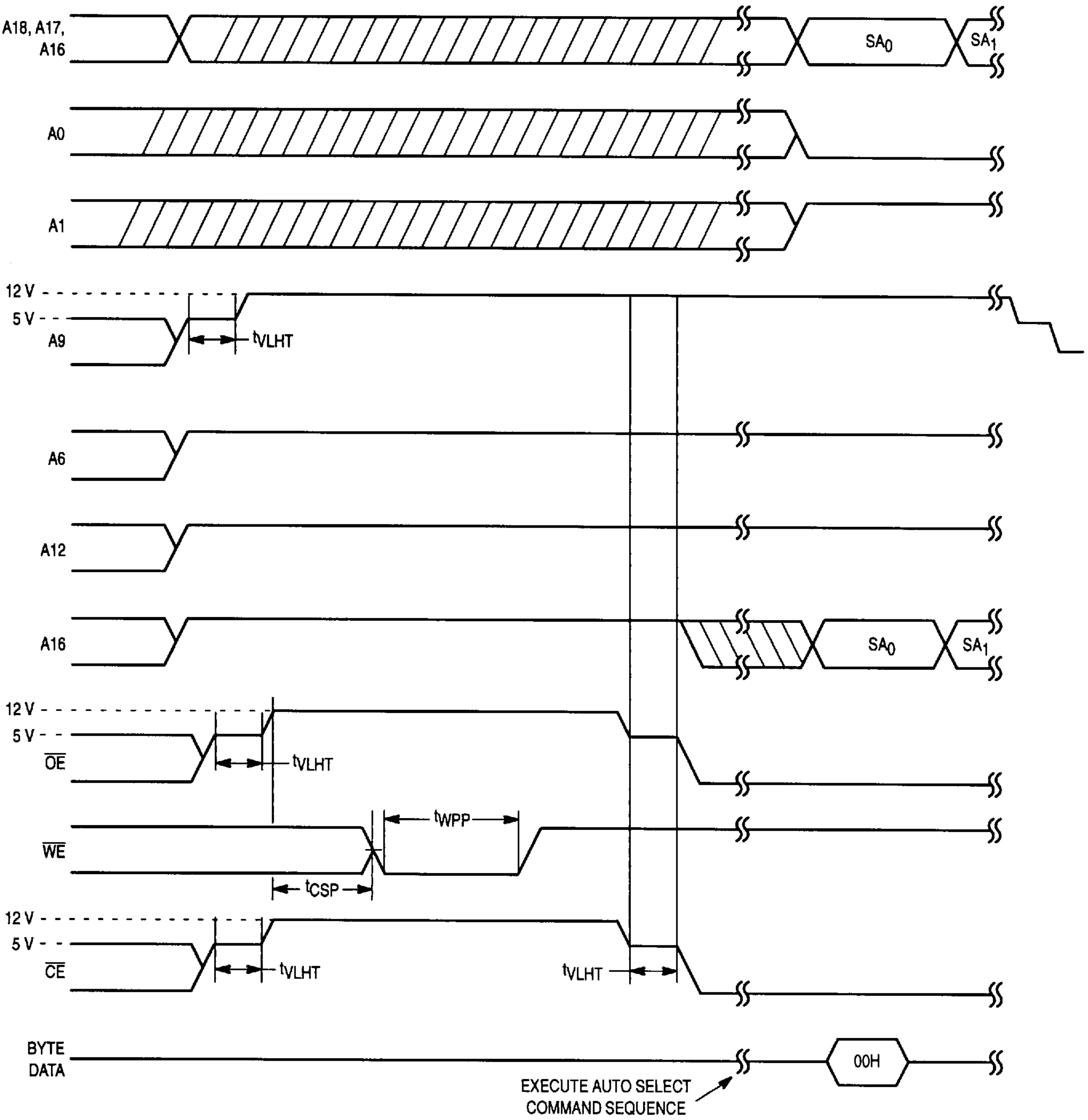
SECTOR PROTECT CYCLE



SA$_x$ = Sector Address for initial sector

SA$_y$ = Sector Address for next sector

SECTOR UNPROTECT CYCLE

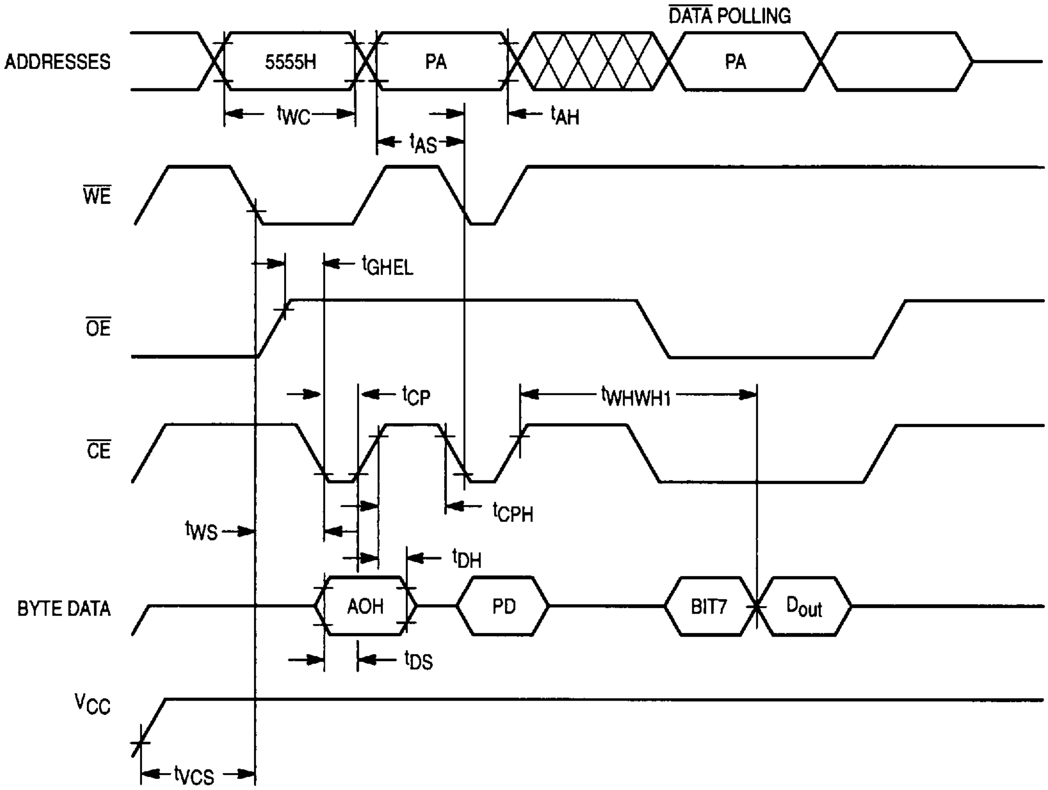


ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLES

Parameter	Symbol		MCM290x0-90			Unit	Notes
	Std	Alt	Min	Typ	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	90	—	—	ns	1
Address Setup Time	t_{AVEL}	t_{AS}	0	—	—	ns	
Address Hold Time	t_{ELAX}	t_{AH}	45	—	—	ns	
Data Setup Time	t_{DVEH}	t_{DS}	45			ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	—	ns	
Output Enable Setup Time		t_{OES}	0	—	—	ns	
Output Enable Hold Time Read Toggle and $\overline{\text{Data}}$ Polling		t_{OEH}	0 10	— —	— —	ns	1
Read Recover Time before Write		t_{GHEL}	0	—	—	ns	
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	—	ns	
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0			ns	
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	45	—	—	ns	
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	20	—	—	ns	
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	—	16	—	µs	
Erase Operation	t_{WHWH2}	t_{WHWH2}	—	1.5	30	s	2
V_{CC} Setup Time		t_{VCS}	—	50	—	µs	1

NOTES:
1. Not 100% tested.
2. This does not include the preprogramming time.

ALTERNATE $\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



NOTES:

1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. BIT7 is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

GENERAL DESCRIPTION

The Motorola MCM290x0 family of 2 MB, 4 MB, and 8 MB Flash SIMMs are designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase options.

The module family offers access time of 90 nanoseconds, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the module 512K x 32 banks are controlled through separate chip enable ($\overline{CE}$) controls. Write enable ($\overline{WE}$) controls the DQ data byte selection on the module and a common output enable ($\overline{OE}$) is accessible to control module data output.

The module family is command set compatible with the JEDEC standard 4M E^2PROM. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to a state-machine, embedded in each Flash component, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the modules is similar to reading from 12.0 V Flash or EPROM devices.

The command descriptions for this product are intended to be replicated by the end user to each of the four bytes of the modules data bus for proper and complete execution of the command. DQ data bits are to be referenced per Table 1.

Table 1. Flash SIMM Command Bit Assignments

Data Bit	Byte 0	Byte 1	Byte 2	Byte 3
Bit 0	DQ0	DQ8	DQ16	DQ24
Bit 1	DQ1	DQ9	DQ17	DQ25
Bit 2	DQ2	DQ10	DQ18	DQ26
Bit 3	DQ3	DQ11	DQ19	DQ27
Bit 4	DQ4	DQ12	DQ20	DQ28
Bit 5	DQ5	DQ13	DQ21	DQ29
Bit 6	DQ6	DQ14	DQ22	DQ30
Bit 7	DQ7	DQ15	DQ23	DQ31

As an example, $\overline{\text{Data}}$ Polling of BIT7 must be applied to module bits DQ7, DQ15, DQ23, and DQ31.

The module is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire module or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

This module also features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

The module features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of BIT7 or by the toggle bit feature on BIT6 of each data byte. Once the end of a program or erase cycle has been completed, each device internally resets to the read mode.

FLEXIBLE SECTOR-ERASE ARCHITECTURE

- 64K Bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

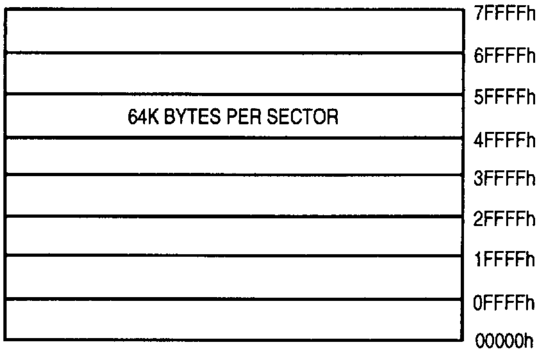


Table 2. User Bus Operations (see Note 1)

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I/O
Auto-Select Manufacturer Code (Note 2)	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code (Note 2)	L	L	H	H	L	L	V_{ID}	Code
Read (Note 3)	L	L	H	A0	A1	A6	A9	D_{out}
Standby	H	X	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	D_{in} (Note 4)
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protect (Note 5)	L	L	H	L	H	L	V_{ID}	Code

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tabes 3 and 4.
3. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. Refer to Table 5 for valid D_{in} during a write operation.
5. Refer to Sector Protection section.

READ MODE

The module has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time).

STANDBY MODE

The module has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), when the current consumed is 400 μA per module bank; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is 4 mA per module bank. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

OUTPUT DISABLE

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

AUTOSELECT

The autoselect mode allows the reading out of a binary code from the module and will identify the Flash component manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacture and device codes may also be read via the command register, when the module is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 5 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacture's code (for example, AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code (for example, Am29F040 = A4H). These two bytes are given in the table below. All identifiers for manufacturers and device will exhibit odd parity with the MSB (BIT7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 3).

Table 3. Sector Protection Verify Autoselect Codes

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
AMD Chip Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
AM29F040 Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at protected sector addresses.

Table 4. Sector Address Tables

	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

WRITE

Module erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

SECTOR PROTECTION

The flash module features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$, and $\overline{CE}$ = V_{IH}. The sector addresses (A18, A17, and A16) should be set to the sector to be protected. Table 4 defines the sector address for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A16, A17, and A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical 1 code at module BIT0 outputs for a protected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17, and A18) are the sector address, will produce a logical 1 at BIT0 outputs for a protected sector. See Table 3 for Autoselect codes.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 5 defines the valid register command sequences. Remember that register commands must be replicated for each module byte addressed. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable).

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered. There is a 6 μs write recovery time before read for the first read after a write.

The module will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Reset is needed to terminate the autoselect operation. It can be used to terminate an Erase or Sector Erase operation, but the data in the sector or device being erased would then be undefined.

AUTOSELECT COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains a command autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code A4H (see Table 3). All manufacturer and device codes will exhibit odd parity with the MSB (BIT7) defined as the parity bit.

Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical 1 at device output BIT0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Table 5. Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Reset/Read	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Bank Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

NOTES:

1. Address bits A15, A17, and A18 = X = don't care. Write Sequences may be initiated with A15, A17, and A18 in either state.
2. Address bits A16, A17, and A18 = X = don't care for all address commands except for program address (PA) and sector address (SA).
3. Bus operations are defined in Table 2.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE pulse.
   SA = Address of the sector to be erased. The combination of A18, A17, A16 will uniquely select any sector.
5. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE.

BYTE PROGRAMMING

Each Flash chip on the module is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of CE or WE, whichever happens later and the data is latched on the rising edge of CE or WE, whichever happens first. The rising edge of CE or WE (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The Flash chips will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on BIT7 of each byte is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data 0 cannot be programmed back to a 1. Attempting to do so will probably hang up the device (exceed timing limits), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still 0. Only erase operations can convert 0s to 1s.

Figure 2 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

BANK ERASE

Bank erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the bank erase command.

Bank erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. A Reset command will terminate the Erase but the data in the bank will be undefined. In that case, perform the Erase operation again and allow it to complete.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on BIT7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read the mode.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

SECTOR ERASE

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of WE, while the command (data) is latched on the rising edge of WE. A time-out of 100 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

CAUTION

Do not attempt to write an invalid command sequence during the sector erase timeout. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 100 μs (± 20%), otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 100 μs from the rising edge of the last $\overline{\text{WE}}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{\text{WE}}$ occurs within the 100 μs time-out window the timer is reset. Any command other than Sector Erase or Erase Suspend during this period will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations. A Reset command will terminate the Sector Erase but the data in the sector will be undefined. In that case, perform the Sector Erase operation again and allow it to complete.

The automatic sector erase begins after the 100 μs time out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on BIT7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read mode. $\overline{\text{Data}}$ polling must be performed at an address within any of the sectors being erased.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

ERASE SUSPEND

Erase Suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B0H) will be allowed only during the Sector Erase Operation that will include the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares in writing the erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the module will take between 0.1 μs to 10 μs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit to determine if the module has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the module is in since there is no external indication of whether the module is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the BIT5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignore. Another Erase Suspend command can be written after the module has resumed.

Table 6. Hardware Sequence Flags

	Status	BIT7	BIT6	BIT5	BIT3	BIT2 – BIT0
In Progress	Auto-Programming	$\overline{\text{BIT7}}$	Toggle	0	0	$(\overline{\text{D}})$
	Programming in Auto Erase	0	Toggle	0	1	
	Erasing in Auto-Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{\text{BIT7}}$	Toggle	1	0	$(\overline{\text{D}})$
	Programming in Auto Erase	0	Toggle	1	1	
	Erasing in Auto-Erase	0	Toggle	1	1	

NOTE: BIT0, BIT1, BIT2, BIT4 are reserve pins for future use.

WRITE OPERATION STATUS

BIT7

Data Polling

The module features Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the compliment of the data last written to BIT7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to BIT7. During the Embedded Erase Algorithm, an attempt to read the device will produce a 0 at the BIT7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a 1 at the BIT7 output. The flowchart for Data Polling (BIT7) is shown in Figure 4.

For bank erase, the Data Polling is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase WE pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the data pins (BIT7) may change asynchronously while the output enable (OE) is asserted low. This means that the device is driving status information on BIT7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the BIT7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and BIT7 has a valid data, the data outputs on BIT0 – BIT6 of each byte may be still invalid. The valid data on BIT0 – BIT7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 5 for the Data Polling timing specifications and diagrams.

BIT6

Toggle Bit

The module also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OE toggling) data from the device will result in BIT6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, BIT6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth WE pulse in the four write pulse sequence. For bank erase, the Toggle Bit is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase WE pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either CE or OE toggling will cause the BIT6 to toggle.

See Figure 6 for the Toggle Bit timing specifications and diagrams.

BIT5

Exceeded Timing Limits

BIT5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions BIT5 will produce a 1. This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The CE circuit will partially power down the device under these conditions. The OE and WE pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the bank erase operation, it specifies that the entire chip on the bank is bad or combination of sectors are bad. In which case, the bank should not be reused.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The BIT5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on BIT7 bit and BIT6 never stops toggling. Once the device has exceeded timing limits, the BIT5 bit will indicate a 1. Please note that this is not a device failure condition since the device was incorrectly used.

BIT3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. BIT3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, BIT3 may be used to determine if the sector erase timer window is still open. If BIT3 is high (1) the internally controlled erase cycle has begun; attempts to write subsequent sector erase commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If BIT3 is low (0), the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of BIT3 prior to and following each subsequent sector erase command. If BIT3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Hardware Sequence Flags.

DATA PROTECTION

The module is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

LOW V_{CC} WRITE INHIBIT

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}.

WRITE PULSE “GLITCH” PROTECTION

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

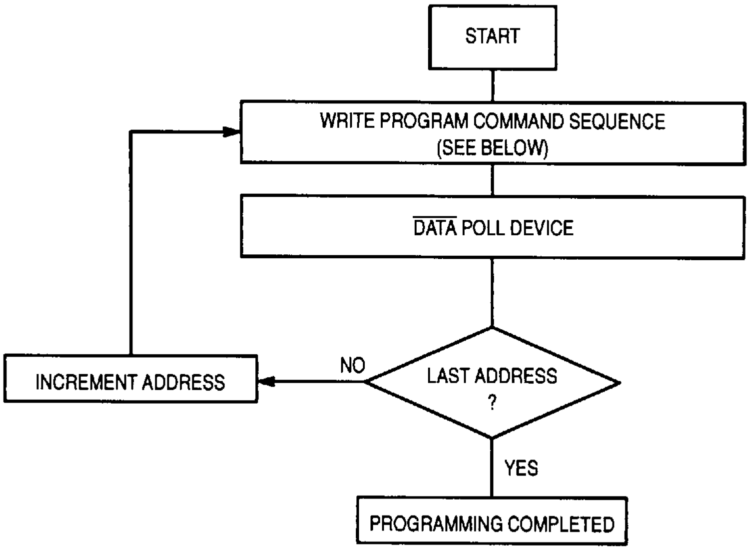
Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER-UP WRITE INHIBIT

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

SECTOR PROTECT

Sectors of the module may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.



Program Command Sequence (Address/Command):

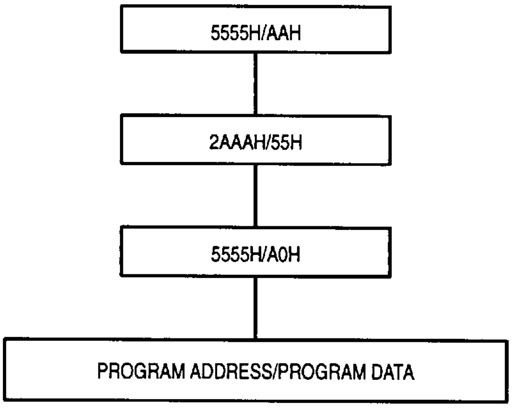


Figure 2. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby (see Note)		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Read		Compare Data Output to Data Expected

NOTE: Module is either powered-down, erase inhibit, or program inhibit.

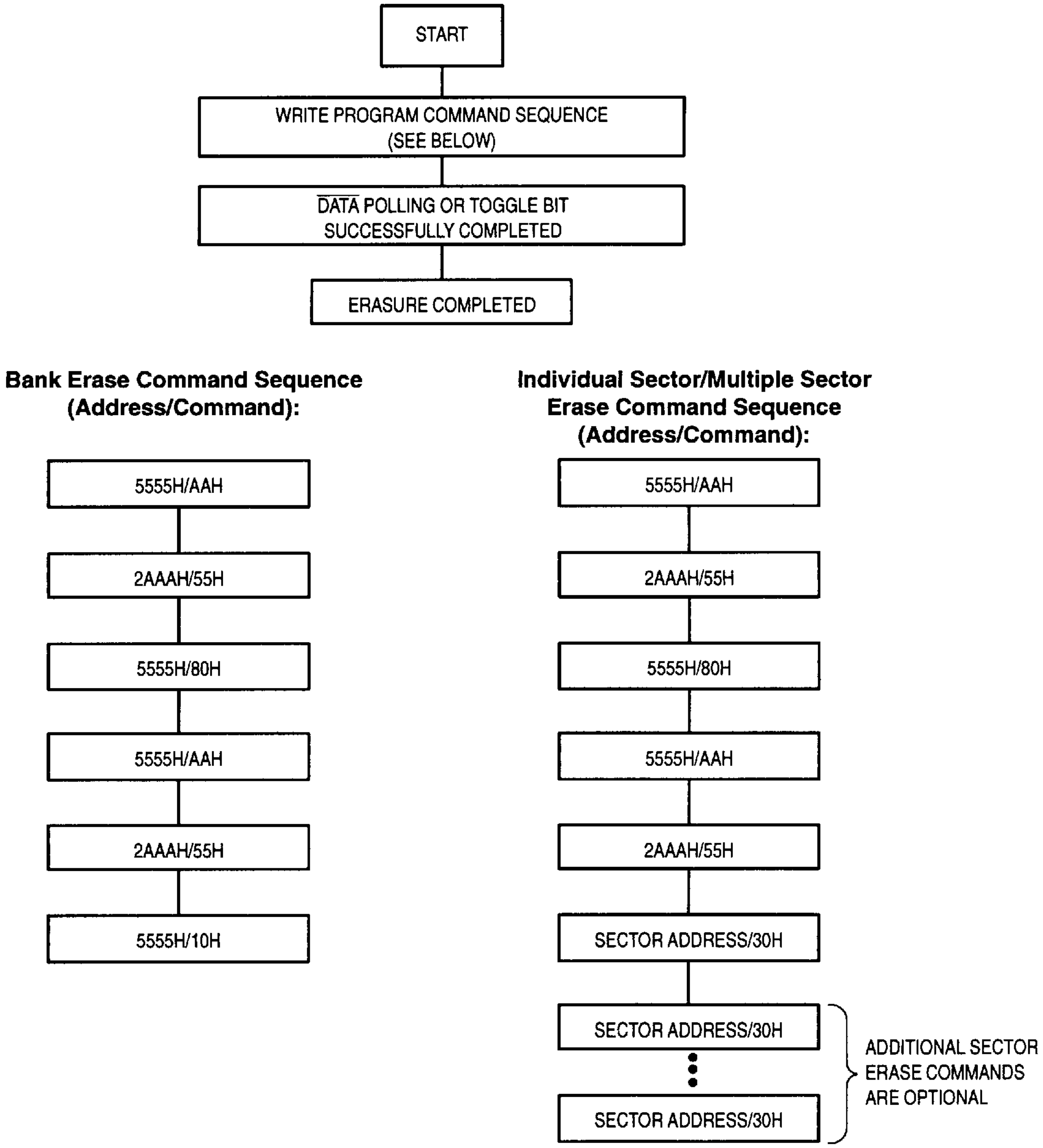
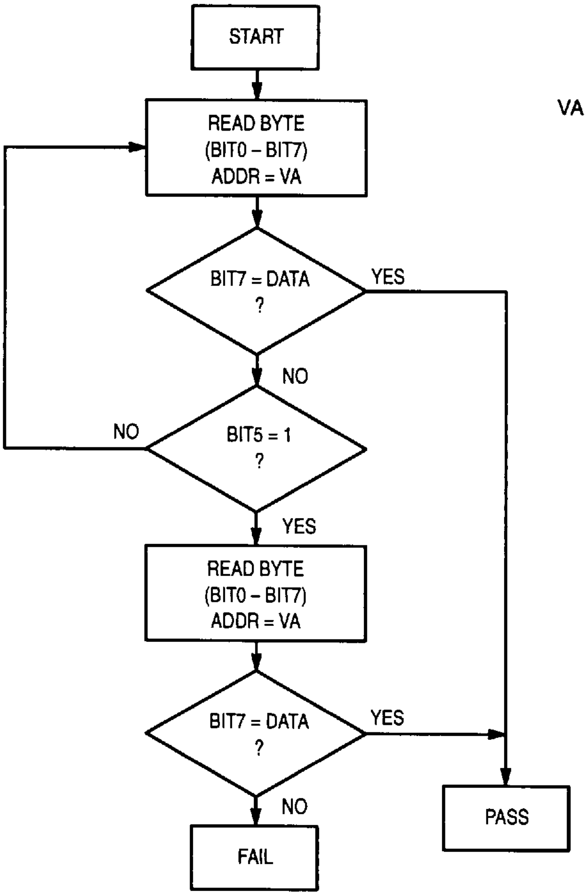


Figure 3. Embedded Erase Algorithm

Table 8. Embedded Erase Algorithm

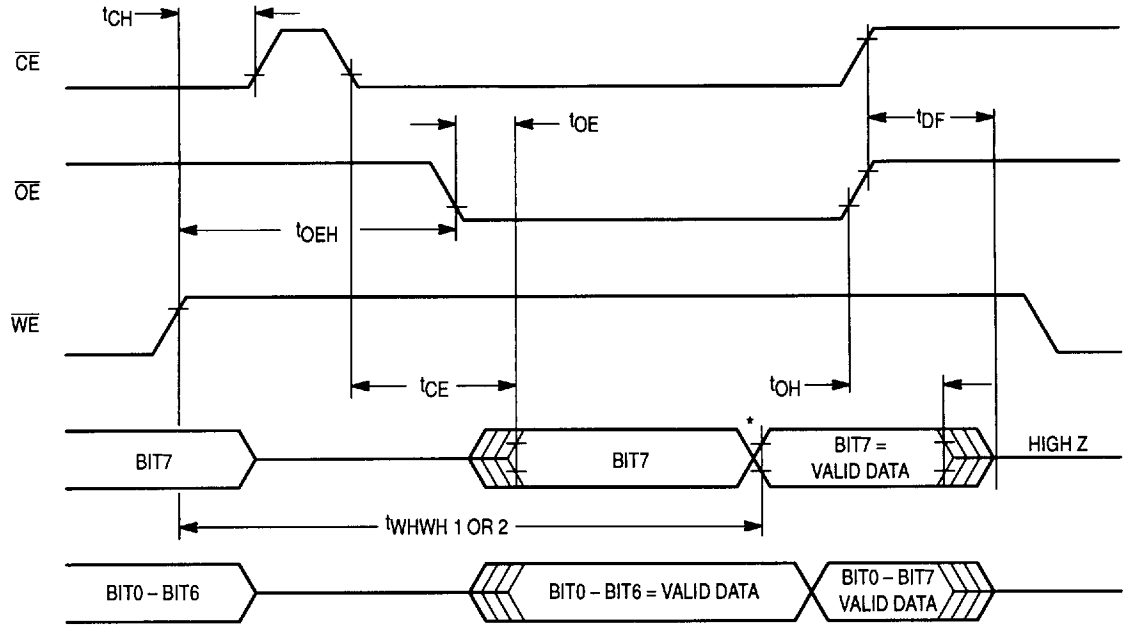
Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Read		Compare Output to FFH



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during device erase

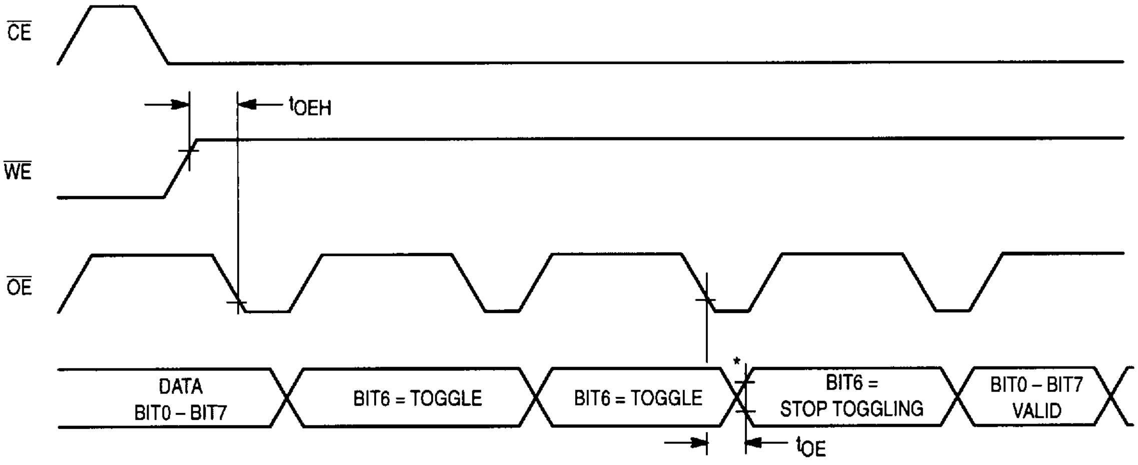
NOTE: BIT7 is rechecked even if BIT5 = 1 because BIT7 may change simultaneously with BIT5.

Figure 4. $\overline{\text{Data}}$ Polling Algorithm



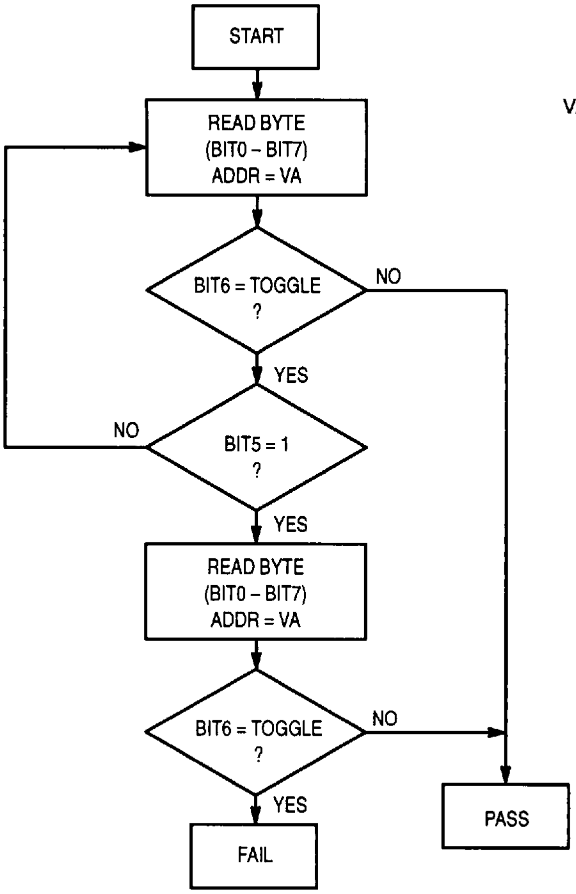
*BIT7 = Valid Data (the device has completed the embedded operation).

Figure 5. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations



*BIT6 Stops Toggling (the device has completed the embedded operation).

Figure 6. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

NOTE: BIT6 is rechecked even if BIT5 = 1 because BIT6 may stop toggling at the same time as BIT5 changing to 1.

Figure 7. Toggle Bit Algorithm

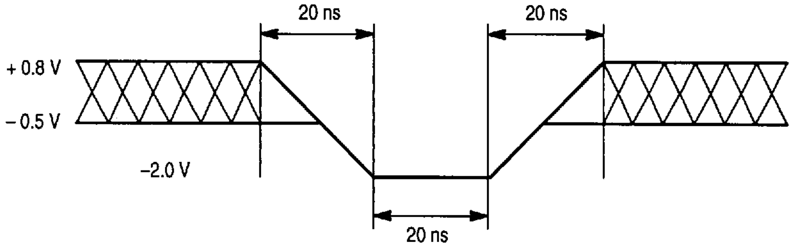


Figure 8. Maximum Negative Overshoot Waveform

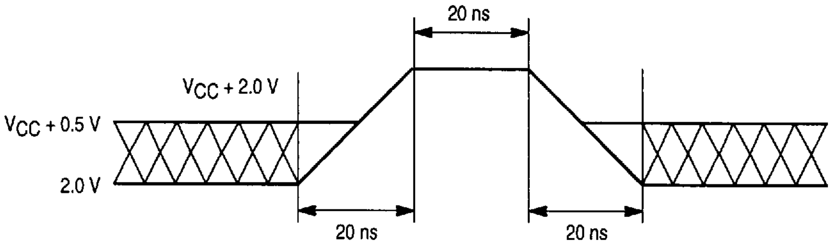


Figure 9. Maximum Positive Overshoot Waveform

SECTOR PROTECTION ALGORITHMS

SECTOR PROTECTION

The module features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A18, A17, and A16. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting A6 = $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector, will produce 01H at data outputs (BIT0 – BIT7) for a protected sector.

SECTOR UNPROTECT

The module also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A16, and A12 should be set to V_{IH}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector address, will produce 00H at data outputs (BIT0 – BIT7) for an unprotected sector.

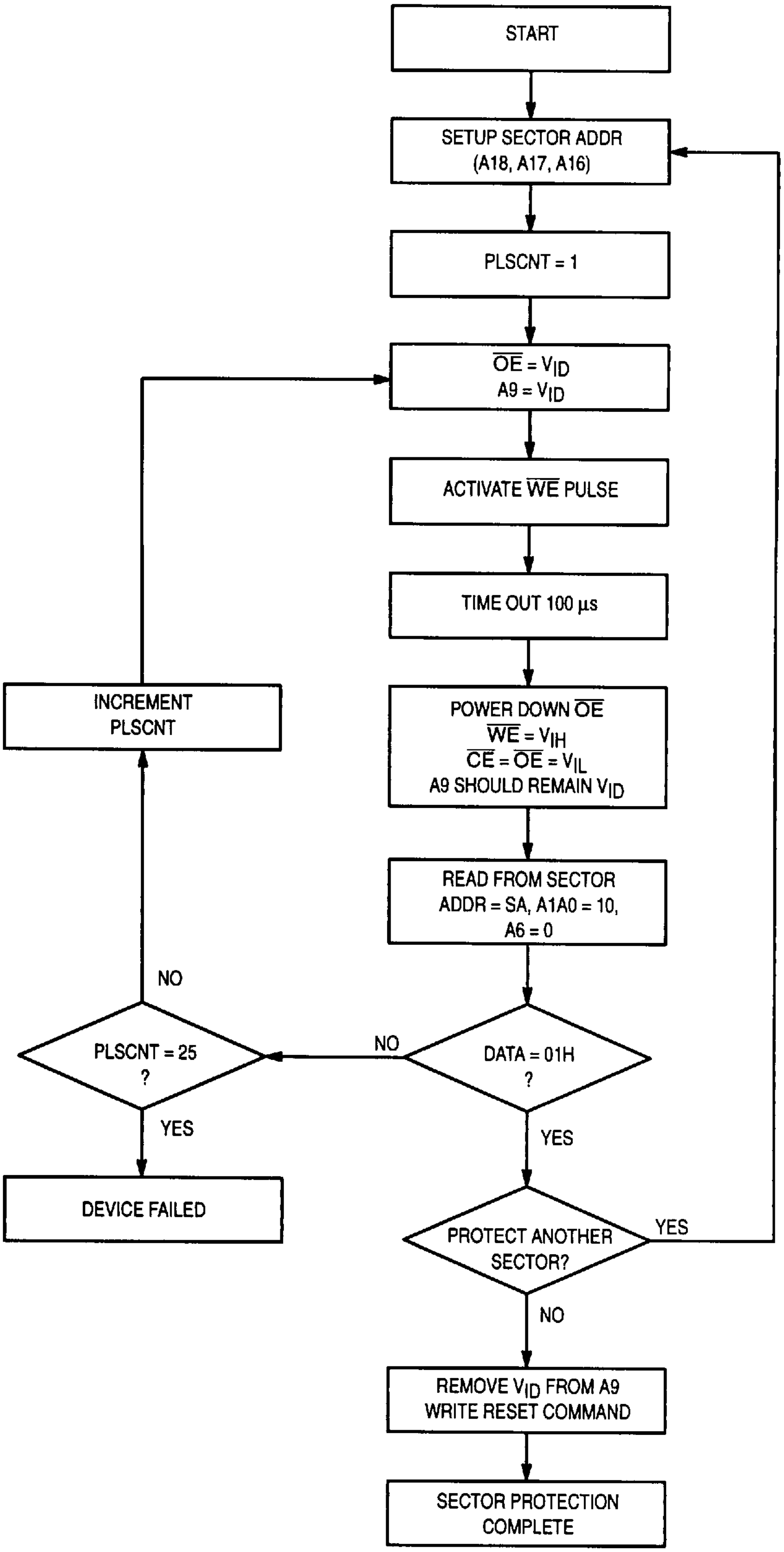
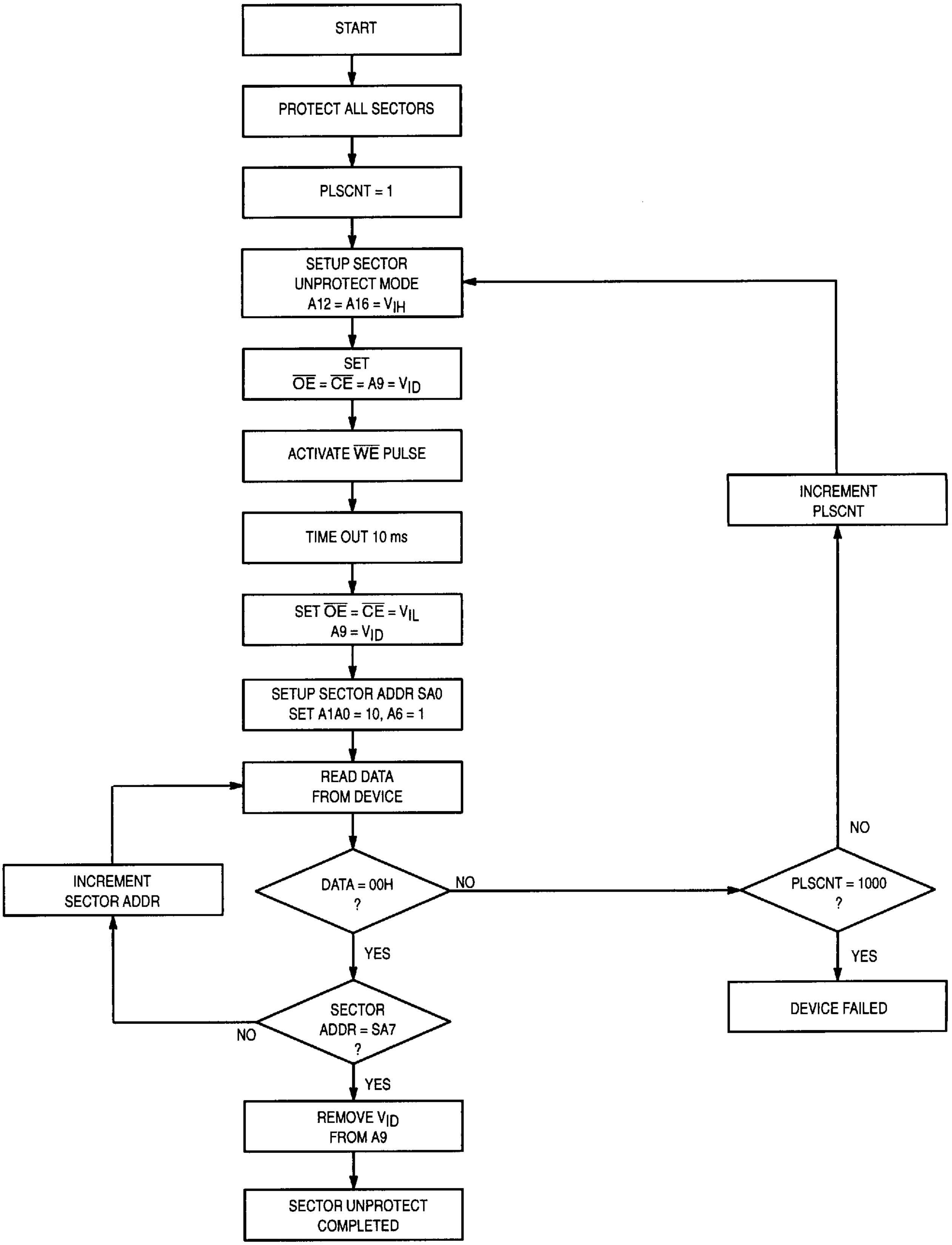


Figure 10. Sector Protection Algorithm



NOTES:
SA = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 4 for details.

Figure 11. Sector Unprotect Algorithm

ORDERING INFORMATION
(Order by Full Part Number)

MCM 290x0 X XX

Motorola Memory Prefix

Part Number (29020 = 2 MB,
29040 = 4 MB, 29080 = 8 MB)

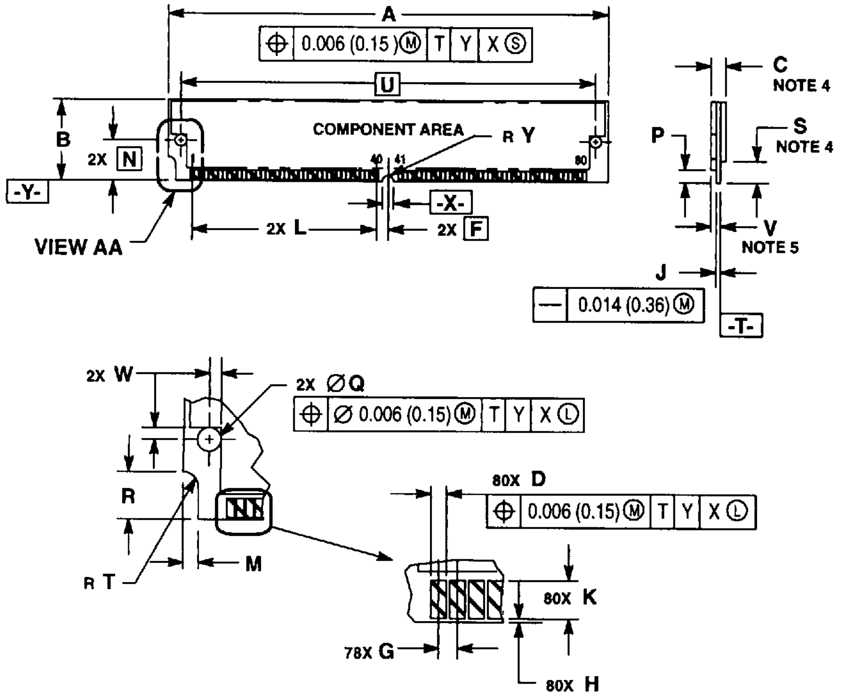
Speed (90 = 90 ns)

Package (S = 80 pin SIMM,
SG = 80 pin Gold Pad SIMM)

Full Part Numbers — MCM29020S90 MCM29020SG90
MCM29040S90 MCM29040SG90
MCM29080S90 MCM29080SG90

PACKAGE DIMENSIONS

S PACKAGE
80-PIN SIMM
CASE 1105-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. DIMENSIONS C AND S DEFINE AN OPTIONAL DOUBLE–SIDED MODULE.
5. DIMENSION V DEFINES A SINGLE–SIDED MODULE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	4.645	4.655	117.98	118.24
B	0.850 MAX		21.59 MAX	
C	—	0.156	—	3.96
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.047	0.054	1.19	1.37
K	0.100	—	2.54	—
L	1.950 REF		49.53 REF	
M	0.075	0.085	1.91	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	4.384 BSC		111.35 BSC	
V	—	0.105	—	2.67
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.