54F/74F524

8-Bit Registered Comparator

Description

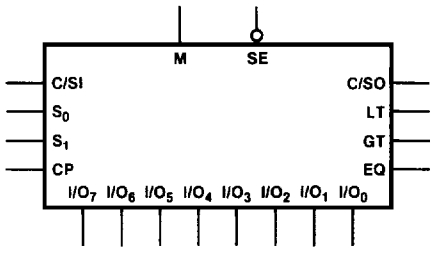
The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow twos complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

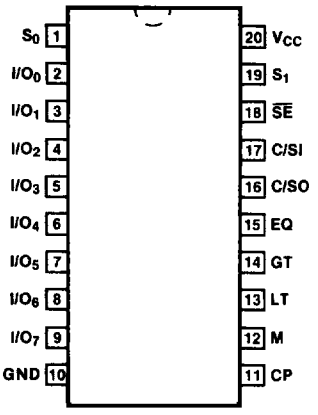
- **8-Bit Bidirectional Register with Bus-Oriented Input-Output**
- **Independent Serial Input-Output to Register**
- **Register Bus Comparator with 'Equal to', 'Greater then' and 'Less than' Outputs**
- **Cascadable in Groups of Eight Bits**
- **Open-Collector Comparator Outputs for AND-Wired Expansion**
- **Twos Complement or Magnitude Compare**

Ordering Code: See Section 5

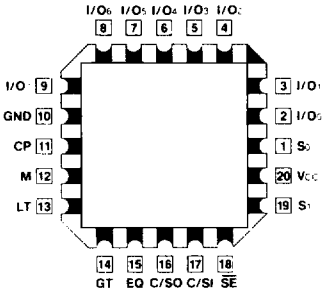
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	0.5/0.375
C/SI	Status Priority or Serial Data Input	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{SE}$	Status Enable Input (Active LOW)	0.5/0.375
M	Compare Mode Select Input	0.5/0.375
I/O_0-I/O_7	Parallel Data Inputs or	1.75/0.406
	3-State Parallel Data Outputs	75/15 (12.5)
C/SO	Status Priority or Serial Data Output	25/12.5
LT	Register Less Than Bus Output	OC*/12.5
EQ	Register Equal Bus Output	OC*/12.5
GT	Register Greater Than Bus Output	OC*/12.5

*OC = Open Collector

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Functional Description

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals S_0 and S_1 according to the Select Truth Table. The 3-state parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word length greater than eight bits.

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure a). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case

propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6(n-2) ns.

Select Truth Table

S_0	S_1	Operation
L	L	Hold—Retains data in shift register
L	H	Read—Read contents in register onto data bus
H	L	Shift—Allows serial shifting on next rising clock edge
H	H	Load—Load data on bus into register

Number Representation Select Table

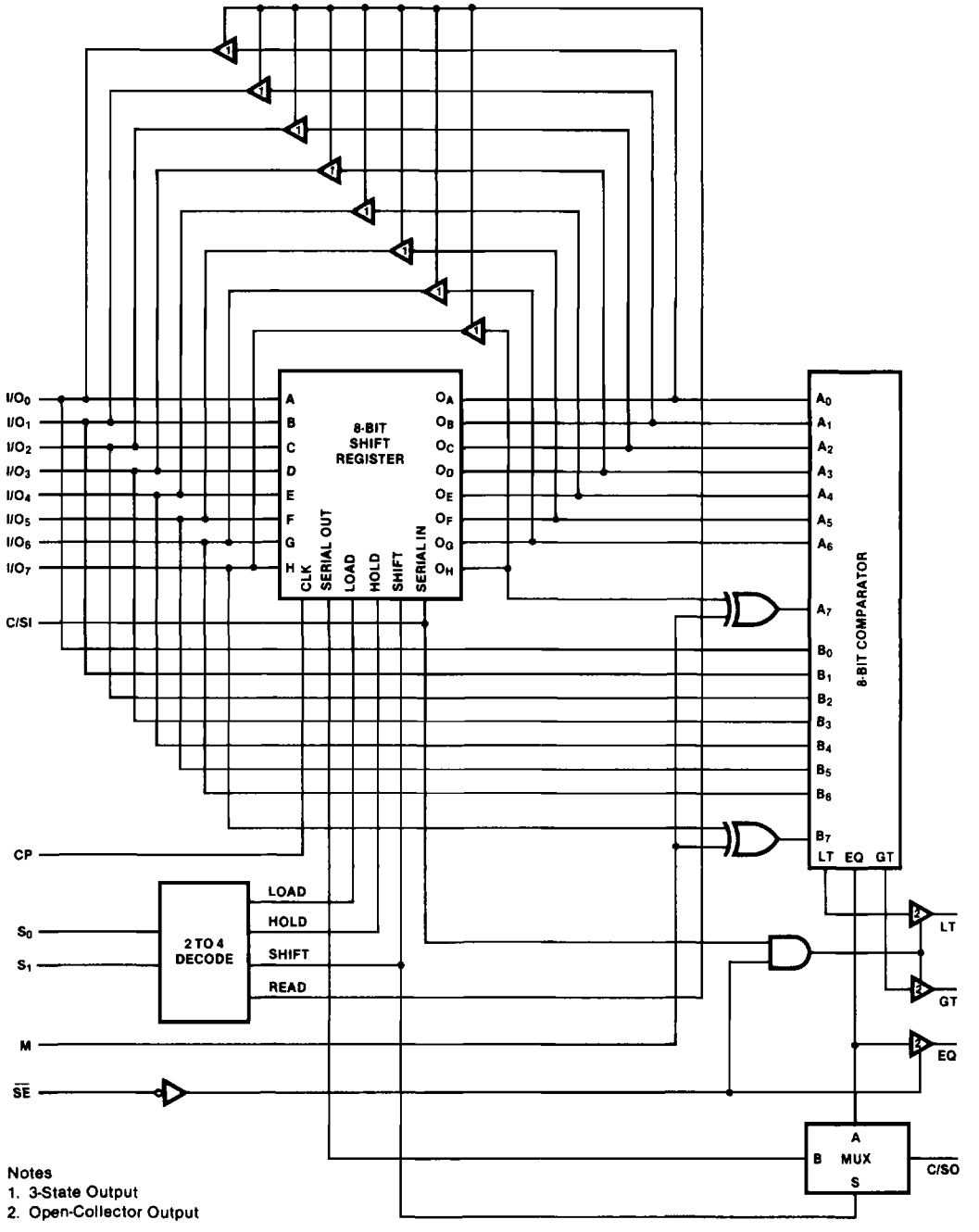
M	Operation
L	Magnitude compare
H	Twos complement compare

Status Truth Table (Hold Mode)

Inputs			Outputs			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	1
L	L	O_A-O_H > I/O_0-I/O_7	L	H	H	L
L	L	O_A-O_H = I/O_0-I/O_7	H	H	H	L
L	L	O_A-O_H < I/O_0-I/O_7	L	H	H	L
L	H	O_A-O_H > I/O_0-I/O_7	L	H	L	L
L	H	O_A-O_H = I/O_0-I/O_7	H	L	L	H
L	H	O_A-O_H < I/O_0-I/O_7	L	L	H	L

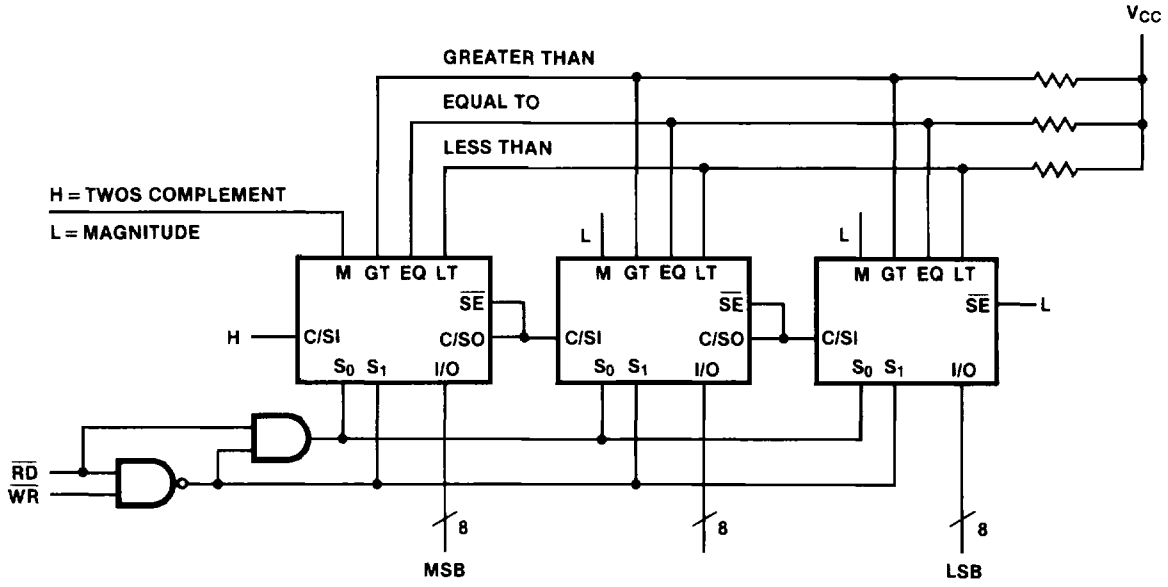
1 = HIGH if data are equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Notes
1. 3-State Output
2. Open-Collector Output

Fig. a Cascading 'F524s for Comparing Longer Words



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		128	180	mA	S_0, S_1, $\overline{SE}$, C/SI = HIGH CP, I/O_0-I/O_7, Register = LOW

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	50	75				50		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay I/O_n to EQ	9.0 5.0	16.5 9.5	20.0 12.0			9.0 5.0	21.0 13.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay I/O_n to GT	8.5 6.5	14.1 13.0	19.0 16.5			8.5 6.5	20.0 17.5		
t_{PLH} t_{PHL}	Propagation Delay I/O_n to LT	7.0 4.5	15.5 10.0	20.0 14.0			7.0 4.5	21.0 15.0		
t_{PLH} t_{PHL}	Propagation Delay I/O_n to C/SO	8.0 6.0	15.2 12.5	19.5 16.0			8.0 6.0	20.5 17.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay CP to EQ	10.0 4.0	20.0 8.5	25.0 16.5			10.0 4.0	26.0 17.5	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to GT	10.0 8.5	16.5 17.0	21.0 22.0			10.0 8.5	22.0 23.0		
t_{PLH} t_{PHL}	Propagation Delay CP to LT	9.0 5.5	20.0 13.5	25.0 17.0			9.0 5.5	26.0 18.0		
t_{PLH}	Propagation Delay CP to C/SO (Compare)	8.5	16.5	21.0			8.5	22.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to C/SO (Serial Shift)	5.0 4.5	10.0 9.0	13.0 11.5			5.0 4.5	14.0 12.5		
t_{PLH} t_{PHL}	Propagation Delay C/SI to GT	9.0 3.0	15.0 6.5	19.0 8.5			9.0 3.0	20.0 9.5	ns	3-1, 3-3
t_{PLH} t_{PHL}	Propagation Delay C/SI to LT	8.0 3.5	15.5 6.5	20.0 8.5			8.0 3.5	21.0 9.5		

AC Characteristics (Cont'd)

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$			T_A, V_{CC} = Mil $C_L = 50\,pF$		T_A, V_{CC} = Com $C_L = 50\,pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to EQ	15.0 9.0	25.0 15.0	33.0 19.0			15.0 9.0	35.0 20.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to GT	10.5 10.5	18.0 18.0	23.0 23.0			10.5 10.5	24.0 24.0		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to LT	13.0 12.0	22.0 19.0	28.0 24.0			13.0 12.0	30.0 25.0		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to C/SO	6.5 5.5	11.5 14.0	14.5 18.0			6.5 5.5	15.5 19.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to EQ	3.5 2.5	8.0 6.0	10.5 8.0			3.5 2.5	11.5 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to GT	6.5 3.5	12.5 6.5	16.0 8.0			6.5 3.5	17.0 9.0		
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to LT	5.0 3.5	10.5 6.0	13.5 8.0			5.0 3.5	14.5 9.0		
t_{PLH} t_{PHL}	Propagation Delay C/SI to C/SO	4.0 4.0	8.5 8.5	11.0 11.0			4.0 4.0	12.0 12.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay M to GT	8.0 6.0	15.0 12.0	19.5 15.5			8.0 6.0	20.5 16.5	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay M to LT	8.0 5.5	17.0 9.5	22.0 12.0			8.0 4.5	23.0 13.0		
t_{PZH} t_{PZL}	Output Enable Time S_0, S_1 to I/O_n	4.5 5.5	10.0 11.0	13.0 15.0			4.5 5.5	14.0 16.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time S_0, S_1 to I/O_n	3.5 4.5	8.0 9.6	12.0 12.5			3.5 4.5	13.0 13.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O_n to CP	6.0 6.0					6.0 6.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O_n to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_0 or S_1 to CP	10.0 10.0					10.0 10.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW C/SI to CP	7.0 7.0					7.0 7.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW C/SI to CP	0 0					0 0			
$t_w(H)$	Clock Pulse Width, HIGH	5.0					5.0		ns	3-7