New

EPSON

High Frequency Clock Oscillator

EG - 2001CA

Preliminary

- Generates high frequency clock from a high stability SAW (surface acoustic wave) resonator.
- Very low jitter / low phase noise.
- High oscillation stability through fundamental mode resonation.
- Low operating voltage, Typical =3.3V.
- Small SMD in 7x5mm,1.2mm height, ceramic package.

Specifications

1. Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Maximum supply voltage	V_{DD}	- 0.5		7.0	V	
Maximum input voltage	V_{IN}	- 0.5		V_{DD}+0.5	V	
Storage Temperature	T_{STG}	- 55		+ 100	°C	Stored as bare product
Soldering condition	T_{SOL}	Twice at under + 260 °C within 10 s				

2. Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	3.0	3.3	3.6	V	
Input voltage	V_{IN}	GND		V_{DD}	V	
Operating Temperature	T_{OPR}	0		+ 70	°C	
Output load condition	CL			25	pF	($f_0 \leq$ 135.000 MHz)
				15	pF	($f_0 \geq$ 135.001 MHz)

3. Frequency Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Output frequency range	f_0	106.250		166.000	MHz	V_{DD}= 3.0 V to 3.6 V
Frequency stability[$\times 10^{-6}$]	$\Delta f / f_0$	- 100		+ 100	-	Ta = 0 °C to + 70 °C

*Note 1 : Frequency stability is including calibration tolerance, reflow soldering drift, operating temperature range (Ta), operating voltage range, load change (CL) and 10 years Aging.

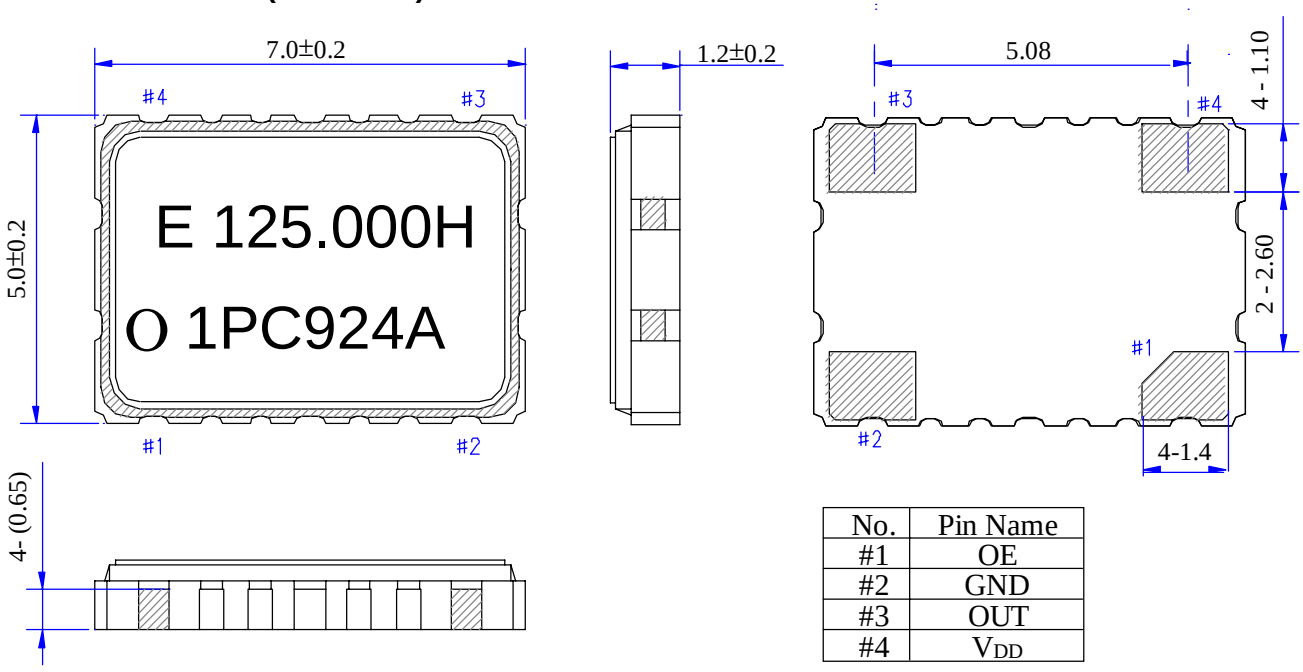
*Note 2 : Please contact to EPSON about Standard Frequency.

4. Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Current consumption	I_{DD1}		27	50	mA	fo = 125 MHz , No Load
OE input voltage	V_{IH}	70% V_{DD}			V	
	V_{IL}			30% V_{DD}	V	
OE input current	I_{IH}			5	µA	OE = V_{DD}
	I_{IL}			10	µA	OE =GND
Duty	tw / t	45		55	%	50%V_{DD}, CL ≤ Max.pF
		40		60		1.4 V Level, CL ≤ Max.pF
Output voltage	V_{OH}	V_{DD}-0.4			V	I_{OH}= -8mA
	V_{OL}			0.4	V	I_{OL}= 8mA
Output rise time	tr			2.0	ns	20% to 80%V_{DD} ,CL ≤ Max.pF
				1.0		0.8 V to 2.0 V, CL ≤ Max.pF
Output fall time	tf			2.0	ns	80% to 20%V_{DD} ,CL ≤ Max.pF
				1.0		2.0 V to 0.8 V, CL ≤ Max.pF
Oscillation start up time	tOSC			10	ms	t=0 at V_{DD}= 3.0 V
Accumulative Jitter	tjacc		3	4	ps	rms , fo = 125 MHz
Absolute Jitter	tjab		25	40	ps	Peak to peak , fo = 125 MHz
SSB phase noise	f_{CN}		-105		dBc/Hz	1 kHz offset
			-115			10 kHz offset
			-120			100 kHz offset

*Note 1 : Please place a 0.01 to 0.1 µF capacitor closely between V_{DD} and GND to obtain stable operation and protest against power line ripple.

5. External Dimensions (Unit : mm)



No.	Pin Name
#1	OE
#2	GND
#3	OUT
#4	V_{DD}

■ **Numbering Information**

E 125.000 H
A B C

1PC 924A
D E

A : Symbol B : Output Frequency (MHz) C : Design Code

D : Parts Name E : Product number

Part Numbering System

Ultra Low Jitter - SAW Oscillator