NEC

Preliminary User's Manual

V850E/IA1™

32/16-Bit Single-Chip Microcontrollers

Hardware

μPD70F3116
μPD703117

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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INTRODUCTION

Readers

This manual is intended for users who understand the functions of the V850E/IA1 (μPD70F3116, 703117) and design application systems using it.

Purpose

This manual introduces the hardware functions of the V850E/IA1 shown below for user's understanding.

Organization

This manual is divided into two parts: Hardware (this manual) and Architecture **(V850E1 Architecture User's Manual).**

Hardware	Architecture
• Pin functions	• Data type
• CPU function	• Register set
• Internal peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupt and exception
	• Pipeline operation

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

- To find the details of a register where the name is known
  →Refer to **APPENDIX A REGISTER INDEX**.

- To find the details of a function, etc. where the name is known
  →Refer to **APPENDIX C INDEX**.

- To understand the details of an instruction function
  →Refer to the **V850E1 Architecture User's Manual**.

- To understand the overall functions of the V850E/IA1
  →Read this manual according to the CONTENTS.

When the register format of each register describes 0 or 1, other values are prohibited to be specified.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Top: higher, bottom: lower
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data Type:	Word ... 32 bits
	Halfword ... 16 bits
	Byte ... 8 bits

Related documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

V850E/IA1-related documents

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IA1 Hardware User's Manual	This manual

Development tool-related documents (User's Manuals)

Document Name			Document No.
IE-V850E-MC (In-circuit Emulator for V850E/IA1), IE-V850E-MC-A (In-circuit Emulator for V850E1 and V850E/MA1)			U14487E
IE-703116-MC-EM1 (In-circuit Emulator Option Board)			To be prepared
CA850 (C Compiler Package)		Operation	U13998E
		Assembly Language	U13828E
		C Language	U13997E
		Project Manager	U13996E
RX850 Pro (Real-Time OS)		Fundamental	U13773E
		Installation	U13774E
ID850 (Integrated Debugger)	Ver. 2.20 or Later	Operation Windows™ Based	U14580E
RD850 Pro (Task Debugger)	Ver. 3.0		U13916E
AZ850 (System Performance Analyzer)			U11181E
PG-FP3 (Flash memory Programmer)			U13502E

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[MEMO]

CHAPTER 1 INTRODUCTION

The V850E/IA1 is a product in the V850 Family™ of NEC Corporation single-chip microcontrollers. This chapter provides an overview of the V850E/IA1.

1.1 Outline

The V850E/IA1 is a 32-/16-bit single-chip microcontroller that realizes high-precision inverter control of a motor due to high-speed operation. It uses the V850E1 (NB85E) CPU of the V850 Family and has on-chip ROM, RAM, bus interface, DMA controller, a variety of timers including a 3-phase sine wave PWM timer for a motor, various serial interfaces including FCAN, and peripheral facilities such as A/D converters.

(1) Implementation of V850E1 (NB85E) CPU

The V850E1 (NB85E) CPU supports a RISC instruction set in which instruction execution speeds are increased greatly through the use of basic instructions that execute one instruction per clock and optimized pipelines. Moreover, it supports multiply instructions using a 32-bit hardware multiplier, saturated product-sum operation instructions, and bit manipulation instructions as optimum instructions for digital servo control applications.

Object code efficiency is increased in the C compiler by using 2-byte length basic instructions and instructions corresponding to high-level languages, which makes a program compact.

Furthermore, since interrupt response time including processing by the on-chip interrupt controller also is fast, this CPU is suited to the realm of advanced real-time control.

(2) External bus interface function

As the external bus interface, there is a multiplex bus configuration that is an address bus (24 bits) and data bus (select 8 bits or 16 bits) suitable for compact system design. SRAM and ROM memories can be connected.

In the DMA controller, a transfer is started using software and transfers between external memories can be made concurrent with internal CPU operations or data transfers. Real-time control such as motor control or communication control also can be realized simultaneously due to high speed, high-performance CPU instruction execution.

(3) On-chip flash memory (μPD70F3116)

The on-chip flash memory version (μPD70F3116), which has a quickly accessible flash memory on-chip, can shorten system development time since it is possible to rewrite a program with the V850E/IA1 mounted in an application system. Moreover, it can greatly improve maintainability after a system ships.

(4) Complete middleware, development environment products

The V850E/IA1 can execute JPEG, JBIG, MH/MR/MMR and other middleware fast. Moreover, since middleware for realizing speech recognition, speech synthesis, and other processing also is provided, multimedia systems can be realized easily by combining with this middleware.

A development environment that integrates an optimizing C compiler, debugger, in-circuit emulator, simulator, and system performance analyzer also is provided.

1.2 Features

○ Number of instructions 83

○ Minimum instruction execution time
20 ns (@ internal 50 MHz operation)

○ General-purpose registers 32 bits × 32 registers

○ Instruction set
V850E1 (NB85E) CPU
Signed multiplication (32 bits × 32 bits → 64 bits): 1 or 2 clocks
Saturated operation instructions (with overflow/underflow detection function)
32-bit shift instruction: 1 clock
Bit manipulation instructions
Long/short format load/store instructions
Signed load instructions

○ Memory space
256 MB linear address space (shared by program and data)
Chip select output function: 8 spaces
Memory block division function: 2, 4, or 8 MB/block
Programmable wait function
Idle state insertion function

○ External bus interface
16-bit data bus (address/data multiplex)
16-/8-bit bus sizing function
Bus hold function
External wait function

○ On-chip memory

Product name	Internal ROM	Internal RAM
μPD70F3116	256 KB (flash memory)	10 KB
μPD703117	128 KB (mask ROM)	6 KB

○ Interrupts/exceptions
External interrupts: 20 (including NMI)
Internal interrupts: 45 sources
Exceptions: 1 cause
8 levels of priority definable

○ DMA controller
4-channel configuration
Transfer unit: 8 bits/16 bits
Maximum transfer count: 65,536 (2^{16})
Transfer type: 2-cycle transfer
Transfer modes: Single transfer, single-step transfer, block transfer
Transfer subjects: Memory ↔ Memory, Memory ↔ I/O, I/O ↔ I/O
Transfer requests: External request, on-chip peripheral I/O, software
DMA transfer termination (terminal count) output signal
Next address setting function

○ I/O lines	Input ports: 8 I/O ports: 75
○ Real-time pulse unit	16-bit timer for 3-phase sine wave PWM inverter control: 2 channels 16-bit up/down counter/timer for 2-phase encoder input: 2 channels General-purpose 16-bit timer/counter: 2 channels General-purpose 16-bit timer/event counter: 1 channel 16-bit interval timer: 1 channel
○ Serial interface (SIO)	Asynchronous serial interface (UART): 3 channels Clocked serial interface (CSI): 2 channels FCAN (Full Controller Area Network): 1 channel
○ NBD (Non Break Debug) function: 1 channel (μPD70F3116 only)	RAM monitoring Event detection
○ A/D converter	10-bit resolution A/D converter: 8 channels × 2 units
○ Clock generator	Multiplication function (×1, ×2.5, ×5, ×10) using PLL clock synthesizer Divide-by-2 function using external clock input
○ Power-saving function	HALT, IDLE, and software STOP modes
○ Package	144-pin plastic LQFP (fine pitch) (20×20)
○ CMOS technology	Full static circuits

1.3 Fields of Application

- Consumer equipment (inverter air conditioner)
- Industrial equipment (motor control, general-purpose inverter)
- Automobile applications (electrical power steering, electric car control)

1.4 Ordering Information

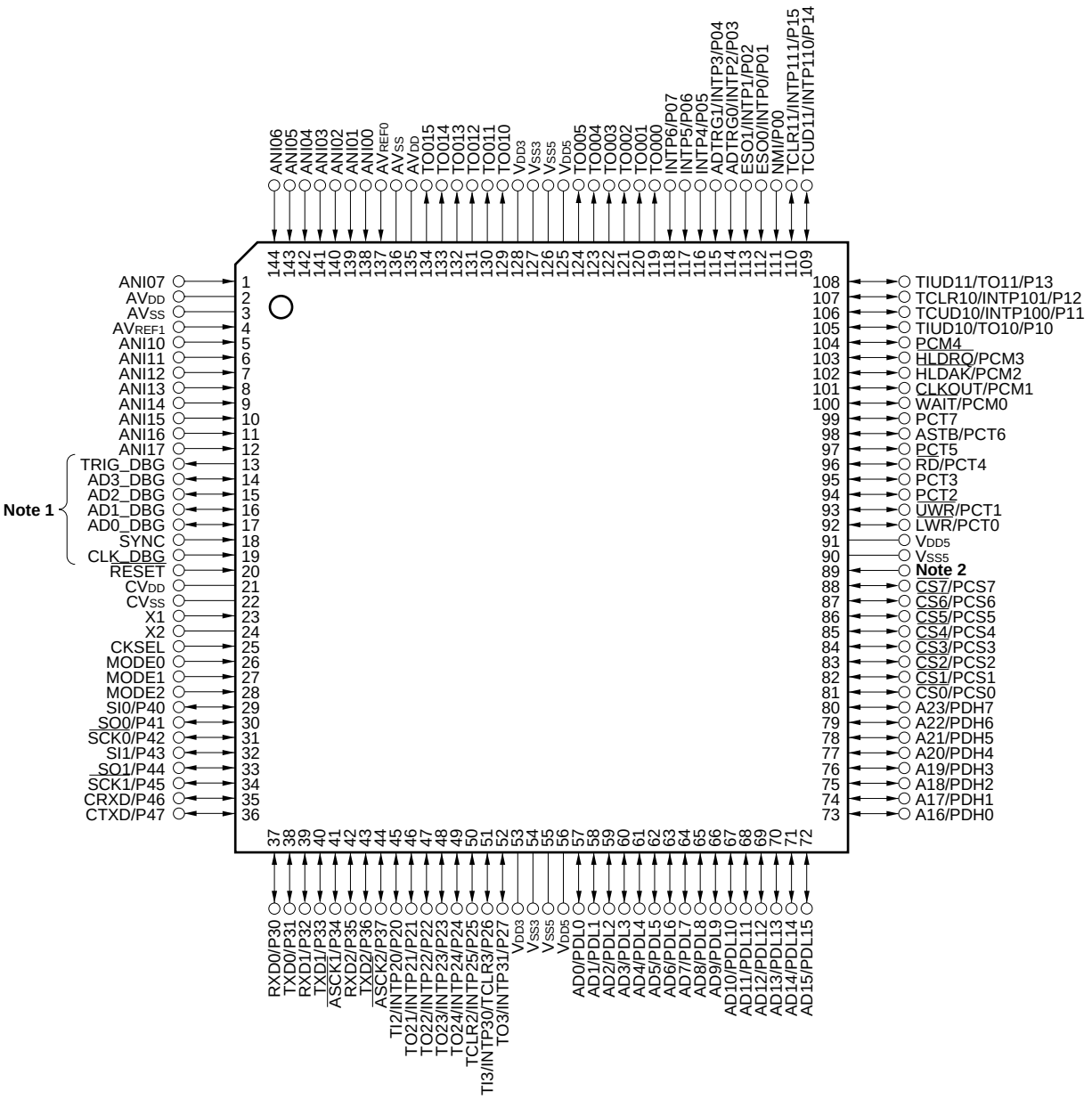
Part No.	Package	Internal ROM
μPD70F3116GJ-UEN[Note]	144-pin plastic LQFP (fine pitch) (20x20)	Flash memory
μPD703117GJ-×××-UEN[Note]	144-pin plastic LQFP (fine pitch) (20x20)	Mask ROM

Note Under development

Remark ××× indicates ROM code suffix.

1.5 Pin Configuration (Top View)

- **144-pin plastic LQFP (fine pitch) (20×20)**
  μPD70F3116GJ-UEN
  μPD703117GJ-×××-UEN



Notes 1. On-chip in μPD70F3116 only.
μPD703117 is as follows.
TRIG_DBG: IC1, AD0_DBG to AD3_DBG: IC2, SYNC: IC3, CLK_DBG: IC4

2. μPD703117: IC5
μPD70F3116: V_{PP}

Cautions 1. When using the μPD70F3116 in normal mode, connect the V_{PP} pin to V_{SS5}.

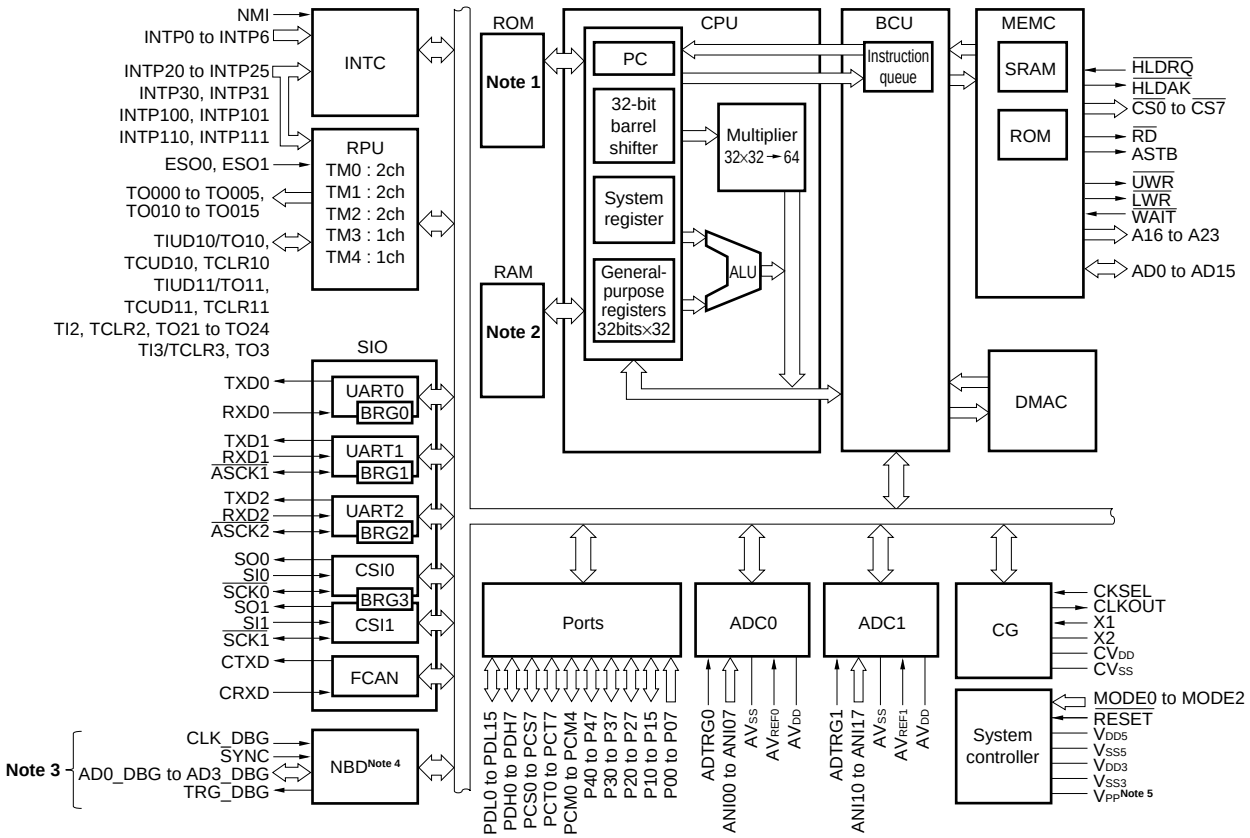
2. The processing of pins IC1 to IC5 is the same as the processing when the corresponding pins in the μPD70F3116 are unused (see 2.4 Types of Pin I/O Circuit and Connection of Unused Pins for details).

Pin Identification

A16 to A23:	Address Bus	P20 to P27:	Port 2
AD0 to AD15:	Address/Data Bus	P30 to P37:	Port 3
AD0_DBG to AD3_DBG:	Debug Address/Data Bus	P40 to P47:	Port 4
ADTRG0, ADTRG1:	AD Trigger Input	PCM0 to PCM4:	Port CM
ANI00 to ANI07,	Analog Input	PCS0 to PCS7:	Port CS
ANI10 to ANI17:		PCT0 to PCT7:	Port CT
$\overline{\text{ASCK1}}$, $\overline{\text{ASCK2}}$:	Asynchronous Serial Clock	PDH0 to PDH7:	Port DH
ASTB:	Address Strobe	PDL0 to PLD15:	Port DL
AV_{DD}:	Analog Power Supply	$\overline{\text{RD}}$:	Read
AV_{REF0}, AV_{REF1}:	Analog Reference Voltage	$\overline{\text{RESET}}$:	Reset
AV_{SS}:	Analog Ground	RXD0 to RXD2:	Receive Data
CKSEL:	Clock Generator Operating Mode Select	$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$:	Serial Clock
CLK_DBG:	Debug Clock	SI0, SI1:	Serial Input
CLKOUT:	Clock Output	SO0, SO1:	Serial Output
CRXD:	Receive Data for Controller Area Network	SYNC:	Sync
$\overline{\text{CS0}}$ to $\overline{\text{CS7}}$:	Chip Select	TCLR10, TCLR11,	Timer Clear
CTXD:	Transmit Data for Controller Area Network	TCLR2, TCLR3:	
CV_{DD}:	Clock Generator Power Supply	TCUD10, TCUD11:	Timer Control Pulse Input
CV_{SS}:	Clock Generator Ground	TI2, TI3:	Timer Input
ESO0, ESO1:	Emergency Shut Off	TIUD10, TIUD11:	Timer Count Pulse Input
$\overline{\text{HLDAK}}$:	Hold Acknowledge	TO000 to TO005,	Timer Output
$\overline{\text{HLDRQ}}$:	Hold Request	TO010 to TO015,	
IC1 to IC5:	Internally Connected	TO10, TO11,	
INTP0 to INTP6,	Interrupt Request from Peripherals	TO21 to TO24, TO3:	
INTP100, INTP101,		TRIG_DBG:	Debug Trigger
INTP110, INTP111,		TXD0 to TXD2:	Transmit Data
INTP20 to INTP25,		$\overline{\text{UWR}}$:	Upper Write Strobe
INTP30, INTP31:		V_{DD3}, V_{DD5}:	Power Supply
$\overline{\text{LWR}}$:	Lower Write Strobe	V_{PP}:	Programming Power Supply
MODE0 to MODE2:	Mode	V_{SS3}, V_{SS5}:	Ground
NMI:	Non-maskable Interrupt Request	$\overline{\text{WAIT}}$:	Wait
P00 to P07:	Port 0	X1, X2:	Crystal
P10 to P15:	Port 1		

1.6 Configuration of Function Block

1.6.1 Internal block diagram



Notes 1. μPD70F3116: 256 KB (flash memory)
μPD703117: 128 KB (mask ROM)

2. μPD70F3116: 10 KB
μPD703117: 6 KB

3. Incorporated in μPD70F3116 only.
μPD703117 is as follows.
TRIG_DBG: IC1, AD0_DBG to AD3_DBG: IC2, SYNC: IC3, CLK_DBG: IC4

4. μPD70F3116 only.

5. μPD70F3116 only.
In the μPD703117, the V_{PP} pin is assigned as the IC5 pin.

1.6.2 Internal units

(1) CPU

The CPU uses 5-stage pipeline control to execute address calculation, arithmetic and logical operation, data transfer, and most other instruction processing in one clock.

A multiplier (16 bits × 16 bits → 32 bits or 32 bits × 32 bits → 64 bits), barrel shifter (32-bit), and other dedicated hardware are on-chip to accelerate complex instruction processing.

(2) Bus control unit (BCU)

The BCU starts a required external bus cycle based on a physical address obtained from the CPU. If there is no bus cycle start request from the CPU when fetching an instruction from an external memory area, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is fetched into the internal instruction queue of the CPU.

(3) Memory controller (MEMC)

The MEMC controls SRAM, ROM, and various I/O for external memory expansion.

(4) DMA controller (DMAC)

The DMA transfers data between memory and I/O in place of the CPU.

The address mode is two-cycle transfer. The three bus modes are single transfer, single-step transfer, and block transfer.

(5) ROM

There is on-chip flash memory (256 KB) in the μPD70F3116, and mask ROM (128 KB) in the μPD703117.

On an instruction fetch, the ROM can be accessed by the CPU in one clock.

When single-chip mode 0 or flash memory programming mode is set, ROM is mapped starting from address 00000000H.

When single-chip mode 1 is set, it is mapped starting from address 00100000H.

ROM cannot be accessed if ROM-less mode 0 or 1 is set.

(6) RAM

RAM is mapped starting from address FFFFC000H.

It can be accessed by the CPU in one clock on an instruction fetch or data access.

(7) Interrupt controller (INTC)

The INTC services hardware interrupt requests from on-chip peripheral I/O and external sources (NMI, INTP0 to INTP6, INTP20 to INTP25, INTP30, INTP31, INTP100, INTP101, INTP110, INTP111). For these interrupt requests, eight levels of interrupt priority can be defined and multiprocessing controls against the interrupt sources can be performed.

(8) Clock generator (CG)

The CG provides a frequency that is 1, 2.5, 5, or 10 times (using the on-chip PLL) or 1/2 times (not using the on-chip PLL) the input clock (f_{XX}) as the internal system clock (ϕ). As the input clock, connect an external resonator to pins X1 and X2 (only when using the on-chip PLL synthesizer) or input an external clock from the X1 pin.

(9) Real-time pulse unit (RPU)

The RPU has a 2-channel 16-bit timer (TM0) for 3-phase sine wave PWM inverter control, a 2-channel 16-bit up/down counter (TM1) that can be used for 2-phase encoder input or as a general-purpose timer, a 2-channel 16-bit general-purpose timer unit (TM2), a 1-channel 16-bit timer/event counter (TM3), and a 1-channel 16-bit interval timer (TM4) on-chip. The RPU can measure the pulse interval or frequency and can output a programmable pulse.

(10) Serial interface (SIO)

A 3-channel asynchronous serial interface (UART), 2-channel clocked serial interface (CSI), and 1-channel FCAN are provided as serial interfaces.

The UART performs data transfer using pins TXDn and RXDn (n = 0 to 2).

The CSI performs data transfer using pins SOm, SIm, and $\overline{\text{SCKm}}$ (m = 0, 1).

FCAN performs data transfer using pins CTXD and CRXD.

(11) NBD function

There is a 1-channel NBD on-chip as a debugging interface (μPD70F3116 only).

(12) A/D converter (ADC)

Two units of a high-speed, high-resolution 10-bit A/D converter having eight analog input pins are implemented. The ADC converts using a successive approximation method.

(13) Ports

As shown in the table below, ports function as general-purpose ports and as control pins.

Port	I/O	Control Functions
Port 0	8-bit input	NMI input Real-time pulse unit output stop signal input External interrupt input A/D converter external trigger input
Port 1	6-bit I/O	Real-time pulse unit I/O External interrupt input
Port 2	8-bit I/O	Real-time pulse unit I/O External interrupt input
Port 3	8-bit I/O	Serial interface I/O (UART0 to UART2)
Port 4	8-bit I/O	Serial interface I/O (CSI0, CSI1, FCAN)
Port DH	8-bit I/O	External address bus (A16 to A23)
Port DL	16-bit I/O	External address/data bus (AD0 to AD15)
Port CS	8-bit I/O	External bus interface control signal output
Port CT	8-bit I/O	External bus interface control signal output
Port CM	5-bit I/O	Wait insertion signal input Internal system clock output External bus interface control signal I/O

CHAPTER 2 PIN FUNCTIONS

The names and functions of the V850E/IA1 pins are shown below. These pins can be divided by function into port pins and non-port pins.

2.1 List of Pin Functions

(1) Port pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	I	Port 0 8-bit input-only port	NMI
P01			ESO0/INTP0
P02			ESO1/INTP1
P03			ADTRG0/INTP2
P04			ADTRG1/INTP3
P05			INTP4
P06			INTP5
P07			INTP6
P10	I/O	Port 1 6-bit input/output port Input or output can be specified in 1-bit units	TIUD10/TO10
P11			TCUD10/INTP100
P12			TCLR10/INTP101
P13			TIUD11/TO11
P14			TCUD11/INTP110
P15			TCLR11/INTP111
P20	I/O	Port 2 8-bit input/output port Input or output can be specified in 1-bit units	TI2/INTP20
P21			TO21/INTP21
P22			TO22/INTP22
P23			TO23/INTP23
P24			TO24/INTP24
P25			TCLR2/INTP25
P26			TI3/TCLR3/INTP30
P27			TO3/INTP31
P30	I/O	Port 3 8-bit input/output port Input or output can be specified in 1-bit units	RXD0
P31			TXD0
P32			RXD1
P33			TXD1
P34			$\overline{\text{ASCK1}}$
P35			RXD2
P36			TXD2
P37			$\overline{\text{ASCK2}}$

(2/3)

Pin Name	I/O	Function	Alternate Function
P40	I/O	Port 4 8-bit input/output port Input or output can be specified in 1-bit units	SI0
P41			SO0
P42			$\overline{\text{SCK0}}$
P43			SI1
P44			SO1
P45			$\overline{\text{SCK1}}$
P46			CRXD
P47			CTXD
PCM0	I/O	Port CM 5-bit input/output port Input or output can be specified in 1-bit units	$\overline{\text{WAIT}}$
PCM1			CLKOUT
PCM2			$\overline{\text{HLDAK}}$
PCM3			$\overline{\text{HLDRQ}}$
PCM4			–
PCT0	I/O	Port CT 8-bit input/output port Input or output can be specified in 1-bit units	$\overline{\text{LWR}}$
PCT1			$\overline{\text{UWR}}$
PCT2			–
PCT3			–
PCT4			$\overline{\text{RD}}$
PCT5			–
PCT6			ASTB
PCT7			–
PCS0	I/O	Port CS 8-bit input/output port Input or output can be specified in 1-bit units	$\overline{\text{CS0}}$
PCS1			$\overline{\text{CS1}}$
PCS2			$\overline{\text{CS2}}$
PCS3			$\overline{\text{CS3}}$
PCS4			$\overline{\text{CS4}}$
PCS5			$\overline{\text{CS5}}$
PCS6			$\overline{\text{CS6}}$
PCS7			$\overline{\text{CS7}}$
PDH0	I/O	Port DH 8-bit input/output port Input or output can be specified in 1-bit units	A16
PDH1			A17
PDH2			A18
PDH3			A19
PDH4			A20
PDH5			A21
PDH6			A22
PDH7			A23

(3/3)

Pin Name	I/O	Function	Alternate Function
PDL0	I/O	Port DL	AD0
PDL1		8-/16-bit input/output port	AD1
PDL2		Input or output can be specified in 1-bit units	AD2
PDL3			AD3
PDL4			AD4
PDL5			AD5
PDL6			AD6
PDL7			AD7
PDL8			AD8
PDL9			AD9
PDL10			AD10
PDL11			AD11
PDL12			AD12
PDL13			AD13
PDL14			AD14
PDL15			AD15

(2) Non-port pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO000	O	Timer 00 pulse signal output	–
TO001			–
TO002			–
TO003			–
TO004			–
TO005			–
TO010	O	Timer 01 pulse signal output	–
TO011			–
TO012			–
TO013			–
TO014			–
TO015			–
TO10	O	Timer 10 or 11 pulse signal output	P10/TIUD10
TO11			P13/TIUD11
TO21	O	Timer 2 pulse signal output	P21/INTP21
TO22			P22/INTP22
TO23			P23/INTP23
TO24			P24/INTP24
TO3	O	Timer 3 pulse signal output	P27/INTP31
ESO0	I	Timer 00 or 01 output stop signal input	P01/INTP0
ESO1			P02/INTP1
TIUD10	I	External count clock input to up/down counter (timer 10 or 11)	P10/TO10
TIUD11			P13/TO11
TCUD10	I	Count operation switching signal to up/down counter (timer 10 or 11)	P11/INTP100
TCUD11			P14/INTP110
TCLR10	I	Clear signal input to up/down counter (timer 10 or 11)	P12/INTP101
TCLR11			P15/INTP111
TI2	I	Timer 2 or 3 external count input	P20/INTP20
TI3			P26/INTP30/TCLR3
TCLR2	I	Timer 2 or 3 clear signal input	P25/INTP25
TCLR3			P26/INTP31/TI3
INTP0	I	External maskable interrupt request input	P01/ESO0
INTP1			P02/ESO1
INTP2			P03/ADTRG0
INTP3			P04/ADTRG1
INTP4			P05
INTP5			P06
INTP6			P07

(2/3)

Pin Name	I/O	Function	Alternate Function
INTP100	I	External maskable interrupt request input and timer 10 external capture trigger input	P11/TCUD10
INTP101			P12/TCLR10
INTP110	I	External maskable interrupt request input and timer 11 external capture trigger input	P14/TCUD11
INTP111			P15/TCLR11
INTP20	I	External maskable interrupt request input and timer 2 external capture trigger input	P20/TI2
INTP21			P21/TO21
INTP22			P22/TO22
INTP23			P23/TO23
INTP24			P24/TO24
INTP25			P25/TCLR2
INTP30	I	External maskable interrupt request input and timer 3 external capture trigger input	P26/TI3/TCLR3
INTP31			P27/TO3
SO0	O	Serial transmit data output (3-wire) to CSI0 and CSI1	P41
SO1			P44
SI0	I	Serial transmit data input (3-wire) to CSI0 and CSI1	P40
SI1			P43
$\overline{SCK0}$	I/O	Serial clock I/O (3-wire) to CSI0 and CSI1	P42
$\overline{SCK1}$			P45
TXD0	O	Serial transmit data output to UART0 to UART2	P31
TXD1			P33
TXD2			P36
RXD0	I	Serial receive data input to UART0 to UART2	P30
RXD1			P32
RXD2			P35
$\overline{ASCK1}$	I/O	UART1 and UART2 serial clock input/output	P34
$\overline{ASCK2}$			P37
CTXD	O	FCAN serial transmit data output	P47
CRXD	I	FCAN serial receive data input	P46
ANI00 to ANIC7	I	Analog input to A/D converter	–
ANI11 to ANI17			–
ADTRG0	I	External trigger input to A/D converter	P03/INTP2
ADTRG1			P04/INTP4
NMI	I	Non-maskable interrupt request input	P00
MODE0	I	Specifies V850E/IA1 operation mode	–
MODE1			–
MODE2			–
V_{PP} Note 1	–	Power application input for flash memory write	–
IC1 to IC5 Note 2	–	Internal connection pins	–

Notes 1. μPD70F3116 only

2. μPD703117 only

(3/3)

Pin Name	I/O	Function	Alternate Function
$\overline{WAIT}$	I	Control signal input to insert wait in bus cycl e	PCM0
$\overline{HLDAK}$	O	Bus hold acknowledge output	PCM2
$\overline{HLDRQ}$	I	Bus hold request input	PCM3
$\overline{LWR}$	O	External data lower byte write enable signal output	PCT0
$\overline{UWR}$	O	External data upper byte write enable signal output	PCT1
$\overline{RD}$	O	External data bus read strobe signal output	PCT4
ASTB	O	External data bus address strobe signal output	PCT6
$\overline{CS0}$	O	Chip select signal output	PCS0
$\overline{CS1}$			PCS1
$\overline{CS2}$			PCS2
$\overline{CS3}$			PCS3
$\overline{CS4}$			PCS4
$\overline{CS5}$			PCS5
$\overline{CS6}$			PCS6
$\overline{CS7}$			PCS7
AD0 to AD15	I/O	16-bit address/data bus for external memory	PDL0 to PDL15
A16 to A23	O	Upper 8-bit address bus for external memory	PLH0 to PLH7
$\overline{RESET}$	I	System reset input	–
X1	I	Crystal resonator connection pin for system clock generation Input to X1 pin when providing clocks from outside.	–
X2	–		–
CLKOUT	O	System clock output	PCM1
CKSEL	I	Input specifying clock generator operation mode	–
AV_{REF0}	I	Reference voltage input for A/D converter 0	–
AV_{REF1}	I	Reference voltage input for A/D converter 1	–
AV_{DD}	–	Positive power supply for A/D converter	–
AV_{SS}	–	Ground potential for A/D converter	–
CV_{DD}	–	Positive power supply for dedicated clock generator	–
CV_{SS}	–	Ground potential for dedicated clock generator	–
V_{DD5}	–	Positive power supply for peripheral interface	–
V_{SS5}	–	Ground potential for peripheral interface	–
V_{DD3}	–	3 V positive power supply pin for Internal CPU	–
V_{SS3}	–	Ground potential for Internal CPU	–
CLK_DBG[Note]	I	Debugging interface clock input (3 V interface)	–
SYNC[Note]	I	Debugging interface command synchronization input (3 V interface)	–
AD0_DBG[Note]	I/O	Command interface input for debugging (3 V interface)	–
AD1_DBG[Note]			–
AD2_DBG[Note]			–
AD3_DBG[Note]			–
TRIG_DBG[Note]	O	Address match trigger signal output for debugging (3 V interface)	–

Note μPD70F3116 only

2.2 Pin Status

The following table shows the status of each pin after a reset, in power-saving mode (software STOP mode, IDLE, HALT), on a DMA transfer, and on a bus hold.

Pin \ Operating Status	Reset (Single-Chip Mode 0)	Reset (Single-Chip Mode 1, ROM-Less Mode 0 or 1)	IDLE Mode/ Software STOP Mode	HALT Mode/ During DMA Transfer	Bus Hold
A16 to A23 (PDH0 to PDH7)	Hi-Z	Hi-Z	Hi-Z	Operating	Hi-Z
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	Hi-Z	Hi-Z	Operating	Hi-Z
$\overline{CS0}$ to $\overline{CS7}$ (PCS0 to PCS7)	Hi-Z	Hi-Z	H	Operating	Hi-Z
$\overline{LWR}$, $\overline{UWR}$ (PCT0, PCT1)	Hi-Z	Hi-Z	H	Operating	Hi-Z
$\overline{RD}$ (PCT4)	Hi-Z	Hi-Z	H	Operating	Hi-Z
ASTB (PCT6)	Hi-Z	Hi-Z	L	Operating	Hi-Z
$\overline{WAIT}$ (PCM0)	Hi-Z	Hi-Z	–	Operating	–
CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating
$\overline{HLDAK}$ (PCM2)	Hi-Z	Hi-Z	H	Operating	L
$\overline{HLDRQ}$ (PCM3)	Hi-Z	–	–	Operating	Operating

Caution When controlling the external bus using an ASIC or the like in standby mode, provide a separate control circuit.

Remarks Hi-Z: High impedance
H: High-level output
L: Low-level output
–: No input sampling

2.3 Description of Pin Functions

(1) P00 to P07 (Port 0) … Input

Port 0 is an 8-bit input-only port in which all pins are fixed for input.

Besides functioning as an input port, in control mode, P00 to P07 operate as NMI input, real-time pulse unit (RPU) output stop signal input, external interrupt request input, and A/D converter (ADC) external trigger input. Normally, if function pins also serve as ports, one mode or the other is selected using a port mode control register. However, there is no such register for P00 to P07. Therefore, the input port cannot be switched with the NMI input pin, RPU output stop signal input pin, external interrupt request input pin, and A/D converter (ADC) external trigger input pin. Read the status of each pin by reading the port.

(a) Port mode

P00 to P07 are input-only.

(b) Control mode

P00 to P07 also serve as NMI, ESO0, ESO1, ADTRG0, ADTRG1, and INTP0 to INTP6 pins, but they cannot be switched.

(i) NMI (Non-maskable interrupt request) … Input

This is non-maskable interrupt request input.

(ii) ESO0, ESO1 (Emergency shut off) … Input

These pins input timer 00 and timer 01 output stop signals.

(iii) INTP0 to INTP6 (Interrupt request from peripherals) … Input

These are external interrupt request input pins.

(iv) ADTRG0, ADTRG1 (AD trigger input) … Input

These are A/D converter external trigger input pins.

(2) P10 to P15 (Port 1) … Input/output

Port 1 is a 6-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as an input/output port, in control mode, P10 to P15 operate as RPU input/output and external interrupt request input.

An operation mode of port or control mode can be selected for each bit and specified by the port 1 mode control register (PMC1).

(a) Port mode

P10 to P15 can be set to input or output in 1-bit units using the port 1 mode register (PM1).

(b) Control mode

P10 to P15 can be set to port or control mode in 1-bit units using PMC1.

(i) TO10, TO11 (Timer output) … Output

These pins output timer 10 and timer 11 pulse signals.

(ii) TIUD10, TIUD11 (Timer count pulse input) … Input

These are external counter clock input pins to the up/down counter (timer 10, timer 11).

(iii) TCUD10, TCUD11 (Timer control pulse input) … Input

These pins input count operation switching signals to the up/down counter (timer 10, timer 11).

(iv) TCLR10, TCLR11 (Timer clear) … Input

These are clear signal input pins to the up/down counter (timer 10, timer 11).

(v) INTP100, INTP101 (Interrupt request from peripherals) … Input

These are external interrupt request input pins and timer 10 external capture trigger input pins.

(vi) INTP110, INTP111 (Interrupt request from peripherals) … Input

These are external interrupt request input pins and timer 11 external capture trigger input pins.

(3) P20 to P27 (Port 2) … Input/output

Port 2 is an 8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as an input/output port, in control mode, P20 to P27 operate as RPU input/output and external interrupt request input.

An operation mode of port or control mode can be selected for each bit and specified by the port 2 mode control register (PMC2).

(a) Port mode

P20 to P27 can be set to input or output in 1-bit units using the port 2 mode register (PM2).

(b) Control mode

P20 to P27 can be set to port or control mode in 1-bit units using PMC2.

(i) TO21 to TO24 (Timer output) … Output

These pins output a timer 2 pulse signal.

(ii) TO3 (Timer output) … Output

This pin outputs a timer 3 pulse signal.

(iii) TI2, TI3 (Timer input) … Input

These are timer 2 and timer 3 external counter clock input pins.

(iv) TCLR2, TCLR3 (Timer clear) … Input

These are timer 2 and timer 3 clear signal input pins.

(v) INPT20 to INTP25 (Interrupt request from peripherals) … Input

These are external interrupt request input pins and timer 2 external capture trigger input pins.

(vi) INTP30, INPT31 (Interrupt request from peripherals) … Input

These are external interrupt request input pins and timer 3 external capture trigger input pins.

(4) P30 to P37 (Port 3) … Input/output

Port 3 is an 8-bit input/output that can be set to input or output in 1-bit units.

Besides functioning as an input/output port, in control mode, P30 to P37 operate as serial interface (UART0 to UART2) input/output.

An operation mode of port or control mode can be selected for each bit and specified by the port 3 mode control register (PMC3).

(a) Port mode

P30 to P37 can be set to input or output in 1-bit units using the port 3 mode register (PM3).

(b) Control mode

P30 to P37 can be set to port or control mode in 1-bit units using PMC3.

(i) TXD0 to TXD2 (Transmit data) … Output

These pins output serial transmit data of UART0 to UART2.

(ii) RXD0 to RXD2 (Receive data) … Input

These pins input serial receive data of UART0 to UART2.

(iii) $\overline{\text{ASCK1}}$, $\overline{\text{ASCK2}}$ (Asynchronous serial clock) … Input/output

These are UART1 and UART2 serial clock input/output pins.

(5) P40 to P47 (Port 4) … Input/output

Port 4 is an 8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as an input/output port, in control mode, P40 to P47 operate as serial interface (CSI0, CSI1, FCAN) input/output.

An operation mode of port or control mode can be selected for each bit and specified by the port 4 mode control register (PMC4).

(a) Port mode

P40 to P47 can be set to input or output in 1-bit units using the port 4 mode register (PM4).

(b) Control mode

P40 to P47 can be set to port or control mode in 1-bit units using PMC4.

(i) SO0, SO1 (Serial output) … Output

These pins output CSI0 and CSI1 serial transmit data.

(ii) SI0, SI1 (Serial input) … Input

These pins input CSI0 and CSI1 serial receive data.

(iii) $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$ (Serial clock) … Input/output

These are CSI0 and CSI1 serial clock input/output pins.

(iv) CTXD (Transmit data for controller area network) … Output

This pin outputs FCAN serial transmit data.

(v) CRXD (Receive data for controller area network) … Input

This pin inputs FCAN serial receive data.

(6) PCM0 to PCM4 (Port CM) … Input/output

Port CM is a 5-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as a port, in control mode, PCM0 to PCM4 operate as wait insertion signal input, internal system clock output, and bus hold control signal output.

An operation mode of port or control mode can be selected for each bit and specified by the port CM mode control register (PMCCM).

(a) Port mode

PCM0 to PCM4 can be set to input or output in 1-bit units using the port CM mode register (PMCM).

(b) Control mode

PCM0 to PCM4 can be set to port or control mode in 1-bit units using PMCCM.

(i) $\overline{\text{WAIT}}$ (Wait) … Input

This control signal input pin, which inserts a data wait in a bus cycle, can input asynchronously with respect to a CLKOUT signal. Sampling is done at the falling edge of a CLKOUT signal in a bus cycle in a T1 or TW state. If the setup or hold time is not secured in the sampling timing, wait insertion may not be performed.

(ii) CLKOUT (Clock output) … Output

This is an internal system clock output pin. In single-chip mode 1 and ROM-less mode 0 or 1, output is not performed by the CLKOUT pin because it is in port mode during the reset period. To perform CLKOUT output, set this pin to control mode using the port CM mode control register (PMCCM).

(iii) $\overline{\text{HLDAK}}$ (Hold acknowledge) … Output

This is an acknowledge signal output pin that shows that the V850E/IA1 received a bus hold request and that the external address/data bus and various strobe pins entered in a high-impedance state.

While this signal is active, the external address/data bus and various strobe pins become high-impedance and transfer the bus mastership to the external bus master.

(iv) $\overline{\text{HLDRQ}}$ (Hold request) … Input

This is the input pin by which an external device requests that the V850E/IA1 release the external address/data bus and various strobe pins. The signal via this pin can be input asynchronously with respect to the CLKOUT signal. When this pin becomes active, the V850E/IA1 makes the external address/data bus and various strobe pins high-impedance after the executing bus cycle terminates (or immediately if there is none) and releases the bus by making the $\overline{\text{HLDAK}}$ signal active.

To reliably set bus hold status, keep the $\overline{\text{HLDRQ}}$ signal active until a $\overline{\text{HLDAK}}$ signal is output.

(7) PCT0 to PCT7 (Port CT) … Input/output

Port CT is an 8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as a port, in control mode, it operates as control signal output for when memory is expanded externally.

An operation mode of port or control mode can be selected for each bit and specified by the port CT mode control register (PMCCT).

(a) Port mode

PCT0 to PCT7 can be set to input or output in 1-bit units using the port CT mode register (PMCT).

(b) Control mode

PCT0 to PCT7 can be set to port or control mode in 1-bit units using PMCCT.

(i) $\overline{\text{LWR}}$ (Lower byte write strobe) … Output

This is a strobe signal that shows that the executing bus cycle is a write cycle for SRAM, external ROM, or an external peripheral I/O area.

In the data bus, the lower byte is in effect. If the bus cycle is a lower memory write, it becomes active at the falling edge of a T1 state CLKOUT signal and becomes inactive at the falling edge of a T2 state CLKOUT signal.

(ii) $\overline{\text{UWR}}$ (Upper byte write strobe) … Output

This is a strobe signal that shows that the executing bus cycle is a write cycle for SRAM, external ROM, or an external peripheral I/O area.

In the data bus, the upper byte is in effect. If the bus cycle is an upper memory write, it becomes active at the falling edge of a T1 state CLKOUT signal and becomes inactive at the falling edge of a T2 state CLKOUT signal.

(iii) $\overline{\text{RD}}$ (Read strobe) … Output

This is a strobe signal that shows that the executing bus cycle is a read cycle for SRAM, external ROM, or external peripheral I/O. It is inactive in an idle state (TI).

(iv) ASTB (Address strobe) … Output

This is the external address bus latch strobe signal output pin.

Output becomes low level in synchronous with the falling edge of the clock in a T1 state bus cycle, and high level in synchronous with the falling edge of the clock in a T3 state.

(8) PCS0 to PCS7 (Port CS) … Input/output

Port CS is an 8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as a port, in control mode, these operate as chip select signal output for when memory is expanded externally.

An operation mode of port or control can be selected for each bit and specified by the port CS mode control register (PMCCS).

(a) Port mode

PCS0 to PCS7 can be set to input or output in 1-bit units using the port CS mode register (PMCS).

(b) Control mode

PCS0 to PCS7 can be set to port or control mode in 1-bit units using PMCCS.

(i) $\overline{\text{CS0}}$ to $\overline{\text{CS7}}$ (Chip select) … Output

This is the chip select signal for external SRAM, external ROM, or external peripheral I/O.

The signal $\overline{\text{CSn}}$ is assigned to memory block n (n = 0 to 7).

This is active for the period during which a bus cycle that accesses the corresponding memory block is activated.

It is inactive in an idle state (TI).

(9) PDH0 to PDH7 (Port DH) … Input/output

Port DH is an 8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as a port, in control mode (external expansion mode), these operate as the address bus (A16 to A23) for when memory is expanded externally.

An operation mode of port or control mode can be selected for each bit and specified by the port DH mode control register (PMCDH).

(a) Port mode

PDH0 to PDH7 can be set to input or output in 1-bit units using the port DH mode register (PMDH).

(b) Control mode

PDH0 to PDH7 can be used as A16 to A23 by using PMCDH.

(i) A16 to A23 (Address) … Output

This pin outputs the upper 8-bit address of the 24-bit address in the address bus on an external access.

(10) PDL0 to PDL7 (Port DL) … Input/output

Port DL is a 16-/8-bit input/output port in which input or output can be set in 1-bit units.

Besides functioning as a port, in control mode (external expansion mode), these operate as the address/data bus (AD0 to AD15) for when memory is expanded externally.

An operation mode of port or control mode can be selected for each bit and specified by the port DL mode control register (PMCDL).

(a) Port mode

PDL0 to PDL15 can be set to input or output in 1-bit units using the port DL mode register (PMDL).

(b) Control mode

PDL0 to PDL15 can be used as AD0 to AD15 by using PMCDL.

(i) AD0 to AD15 (Address/data bus) … Input/output

This is a multiplexed bus for an address or data on an external access. When used for an address (T1 state) they are 24-bit address output pins A0 to A15, and when used for data (T2, TW, T3) they are 16-bit data input/output bus pins.

(11) TO000 to TO005 (Timer output) … Output

These pins output the pulse signal of timer 00.

(12) TO010 to TO015 (Timer output) … Output

These pins output the pulse signal of timer 01.

(13) ANI00 to ANI07, ANI10 to ANI17 (Analog input) … Input

These are analog input pins to the A/D converter.

(14) CKSEL (Clock generator operating mode select) … Input

This is the input pin that specifies the operation mode of the clock generator. Fix it so that the input level does not change during operation.

(15) MODE0 to MODE2 (Mode) … Input

These are the input pins that specify the operation mode. Operation modes are broadly divided into normal operation modes and flash memory programming mode. The normal operation modes are single-chip modes 0 and 1 and ROM-less modes 0 and 1 (see **3.3 Operation Mode** for details). The operation mode is determined by sampling the status of each of pins MODE0 to MODE2 on a reset.

Fix these so that the input level does not change during operation.

(a) μPD70F3116

V_{PP}	MODE2	MODE1	MODE0	Operation Mode	
0 V	L	L	L	Normal operation mode	ROM-less mode 0
0 V	L	L	H		ROM-less mode 1
0 V	L	H	L		Single-chip mode 0
0 V	L	H	H		Single-chip mode 1
7.8 V	L	H	×	Flash memory programming mode	
Other than above				Setting prohibited	

(b) μPD703117

MODE2	MODE1	MODE0	Operation Mode	
L	L	L	Normal operation mode	ROM-less mode 0
L	L	H		ROM-less mode 1
L	H	L		Single-chip mode 0
L	H	H		Single-chip mode 1
Other than above			Setting prohibited	

Remark L : Low-level input
H : High-level input
× : don't care

(16) $\overline{\text{RESET}}$ (Reset) … Input

$\overline{\text{RESET}}$ input is asynchronous input. When a signal having a certain low level width is input in asynchronous with the operation clock, a system reset that takes precedence over all operations occurs.

Besides a normal initialize or start, this signal is also used to release a standby mode (HALT, IDLE, software STOP).

(17) X1, X2 (Crystal)

These pins connect a resonator for system clock generation.

They also can input external clocks. For external clock input, connect to the X1 pin and leave the X2 pin open.

(18) CV_{DD} (Power supply for clock generator)

This is the positive power supply pin for the clock generator.

(19) CV_{SS} (Ground for clock generator)

This is the ground pin for the clock generator.

(20) V_{DD5} (Power supply)

This is the positive power supply pin for the peripheral interface.

(21) V_{SS5} (Ground)

This is the ground pin for the peripheral interface.

(22) V_{DD3} (Power supply)

This is the positive power supply pin for the internal CPU.

(23) V_{SS3} (Ground)

This is the ground pin for the internal CPU.

(24) CLK_DBG (Debug clock) … Input

This is the clock input pin for the debug interface (3 V interface)

(25) SYNC (Sync) … Input

This is the command synchronization input pin for debugging (3 V interface).

(26) AD0_DBG to AD3_DBG (Debug address/data bus) … Input/output

These are command interface pins for debugging (3 V interface).

(27) TRIG_DBG (Debug trigger) … Output

This is the address match trigger signal output pin for debugging (3 V interface).

(28) AV_{DD} (Analog power supply)

This is the analog positive power supply pin for the A/D converter.

(29) AV_{SS} (Analog ground)

This is the ground pin for the A/D converter.

(30) AV_{REF0}, AV_{REF1} (Analog reference voltage) … Input

These are the reference voltage supply pins for the A/D converter.

2.4 Types of Pin I/O Circuit and Connection of Unused Pins

Connection of a 1 to 10 kΩ resistor is recommended when connecting to V_{DD5}, V_{SS5}, CV_{DD}, or CV_{SS} via a resistor.

(1/2)

Pin	I/O Circuit Type	Recommended Connection
P00/NMI	2	Connect directly to V_{SS5}.
P01/ESO0/INTP0 P02/ESO1/INTP1		
P03/ADTRG0/INTP2 P04/ADTRG1/INTP3		
P05/INTP4 to P07/INTP6		
P10/TIUD10/TO10	5-K	Input status: Independently connect to V_{DD5} or V_{SS5} via a resistor. Output status: Leave open.
P11/TCUD10/INTP100		
P12/TCLR10/INTP101		
P13/TIUD11/TO11		
P14/TCUD11/INTP110		
P15/TCLR11/INTP111		
P20/TI2/INTP20		
P21/TO21/INTP21 to P24/TO24/INTP24		
P25/TCLR2/INTP25		
P26/TI3/TCLR3/INTP30		
P27/TO3/INTP31		
P30/RXD0		
P31/TXD0	5	
P32/RXD1	5-K	
P33/TXD1	5	
P34/$\overline{\text{ASCK1}}$	5-K	
P35/RXD2		
P36/TXD2	5	
P37/$\overline{\text{ASCK2}}$	5-K	
P40/SI0		
P41/SO0	5	
P42/$\overline{\text{SCK0}}$	5-K	
P43/SI1		
P44/SO1	5	
P45/$\overline{\text{SCK1}}$	5-K	
P46/CRXD		
P47/CTXD	5	

(2/2)

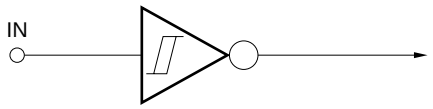
Pin	I/O Circuit Type	Recommended Connection
PCM0/$\overline{\text{WAIT}}$	5	Input status: Independently connect to V_{DD5} or V_{SS5} via a resistor. Output status: Leave open.
PCM1/CLKOUT		
PCM2/$\overline{\text{HLDAK}}$		
PCM3/$\overline{\text{HLDRQ}}$		
PCM4		
PCT0/$\overline{\text{LWR}}$		
PCT1/$\overline{\text{UWR}}$		
PCT2		
PCT3		
PCT4/$\overline{\text{RD}}$		
PCT5		
PCT6/ASTB		
PCT7		
PCS0/$\overline{\text{CS0}}$		
PCS1/$\overline{\text{CS1}}$		
PCS2/$\overline{\text{CS2}}$		
PCS3/$\overline{\text{CS3}}$		
PCS4/$\overline{\text{CS4}}$		
PCS5/$\overline{\text{CS5}}$		
PCS6/$\overline{\text{CS6}}$		
PCS7/$\overline{\text{CS7}}$		
PDH0/A16 to PDH7/A23		
PDL0/AD0 to PDL15/AD15		
AD0_DBG to AD3_DBG[Note 1]	5-K	Independently connect to CV_{DD} or CV_{SS} via a resistor.
TRIG_DBG[Note 1]	3	Leave open (low-level output).
CLK_DBG[Note 1]	2	Independently connect to CV_{SS} via a resistor.
SYNC[Note 1]		Independently connect to CV_{DD} via a resistor.
ANI00 to ANI07, ANI10 to ANI17	7	Connect to V_{SS5}.
TO000 to TO005, TO010 to TO015	4	Leave open.
MODE0 to MODE2	2	–
V_{PP}[Note 1]/IC5[Note 2]		Connect to V_{SS5}.
$\overline{\text{RESET}}$		–
CKSEL		–
X2	–	Leave open.
AV_{SS}	–	Connect to V_{SS5}.
AV_{REF0}, AV_{REF1}	–	Connect to V_{SS5}.
AV_{DD}	–	Connect to V_{SS5}.

Notes 1. μPD70F3116 only

2. μPD703117 only

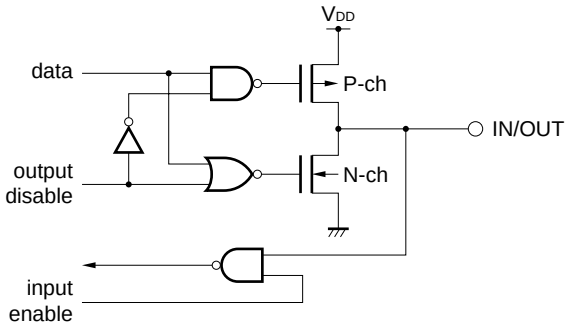
2.5 Pin I/O Circuits

Type 2

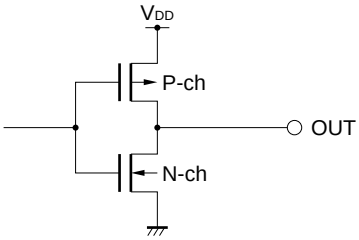


Schmitt Triggered input with hysteresis characteristics

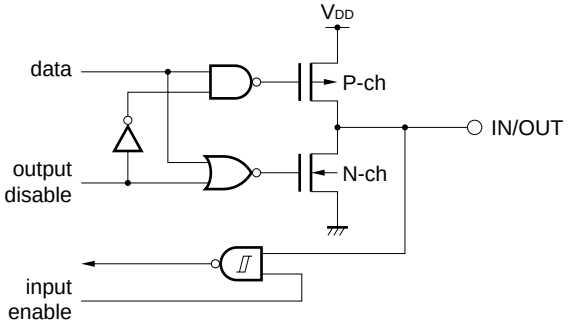
Type 5



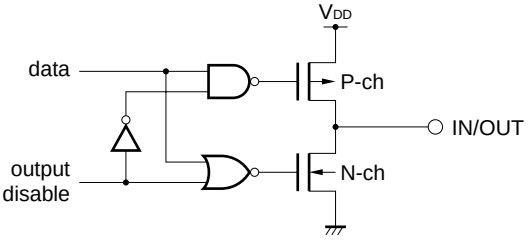
Type 3



Type 5-K

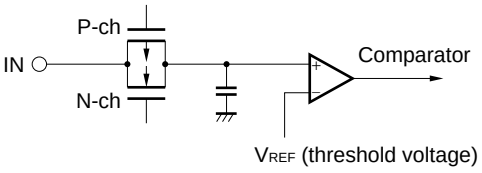


Type 4



Push-pull output with possible high-impedance output (P-ch, N-ch both off)

Type 7



[MEMO]

CHAPTER 3 CPU FUNCTION

The CPU of the V850E/IA1 is based on RISC architecture and executes almost all instructions in one clock cycle, using 5-stage pipeline control.

3.1 Features

- Minimum instruction execution time: 20 ns (@ internal 50 MHz operation)
- Memory space Program space: 64 MB Linear
  Data space: 4 GB Linear
- Thirty-two 32-bit general-purpose registers
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiplication/division instructions
- Saturated operation instructions
- One-clock 32-bit shift instruction
- Long/short instruction format
- Four types of bit manipulation instructions
  - Set
  - Clear
  - Not
  - Test

3.2 CPU Register Set

The registers of the V850E/IA1 can be classified into two categories: a general-purpose program register set and a dedicated system register set. All the registers are 32-bit width.

For details, refer to **V850E1 User's Manual Architecture**.

(1) Program register set

31	0
r0	(Zero register)
r1	(Assembler-reserved register)
r2	
r3	(Stack pointer (SP))
r4	(Global pointer (GP))
r5	(Text pointer (TP))
r6	
r7	
r8	
r9	
r10	
r11	
r12	
r13	
r14	
r15	
r16	
r17	
r18	
r19	
r20	
r21	
r22	
r23	
r24	
r25	
r26	
r27	
r28	
r29	
r30	(Element pointer (EP))
r31	(Link pointer (LP))

31	0
PC	(Program counter)

(2) System register set

31	0
EIPC	(Status saving register during interrupt)
EIPSW	(Status saving register during interrupt)
FEPC	(Status saving register during NMI)
FEPSW	(Status saving register during NMI)
ECR	(Interrrupt source register)
PSW	(Program status word)
CTPC	(Status saving register during CALLT execution)
CTPSW	(Status saving register during CALLT execution)
DBPC	(Status saving register during exception/debug trap)
DBPSW	(Status saving register during exception/debug trap)
CTBP	(CALLT base pointer)

3.2.1 Program register set

The program register set includes general-purpose registers and a program counter.

(1) General-purpose registers

Thirty-two general-purpose registers, r0 to r31, are available. Any of these registers can be used as a data variable or address variable.

However, r0 and r30 are implicitly used by instructions, and care must be exercised when using these registers. r0 is a register that always holds 0, and is used for operations using 0 and offset 0 addressing. r30 is used, by means of the SLD and SST instructions, as a base pointer for when memory is accessed. Also, r1, r3 to r5, and r31 are implicitly used by the assembler and C compiler. Therefore, before using these registers, their contents must be saved so that they are not lost. The contents must be restored to these registers after they have been used. r2 is sometimes used by a real-time OS. r2 can be used as a register for variables when it is not being used by the real-time OS.

Table 3-1. Program Registers

Name	Usage	Operation
r0	Zero register	Always holds 0
r1	Assembler-reserved register	Working register for generating address
r2	Address/data variable register (when not being used by the real-time OS)	
r3	Stack pointer	Used to generate stack frame when function is called
r4	Global pointer	Used to access global variable in data area
r5	Text pointer	Register to indicate the start of the text area (where program code is located)
r6 to r29	Address/data variable registers	
r30	Element pointer	Base pointer for generating address when memory is accessed
r31	Link pointer	Used by compiler when calling function
PC	Program counter	Holds instruction address during program execution

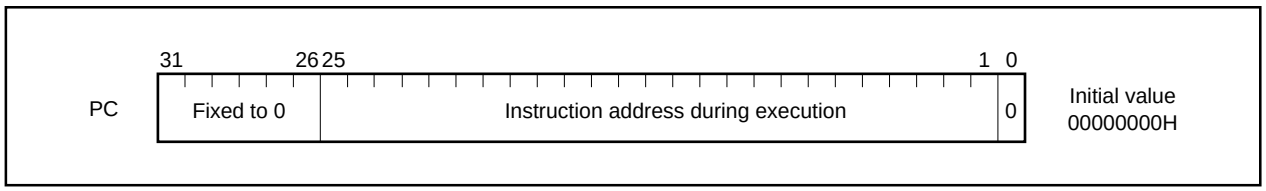
Remark For detailed descriptions about r1, r3, r4, r5, and r31, which are used by the assembler and C compiler, refer to **CA850 (C Compiler Package) User's Manual Assembly Language (U10543E)**.

(2) Program counter

This register holds the instruction address during program execution. The lower 26 bits of this register are valid, and bits 31 to 26 are fixed to 0. If a carry occurs from bit 25 to 26, it is ignored.

Bit 0 is fixed to 0, and branching to an odd address cannot be performed.

Figure 3-1. Program Counter (PC)



3.2.2 System register set

System registers control the status of the CPU and hold interrupt information.

To read/write these system registers, specify a system register number indicated below using the system register load/store instruction (LDSR or STSR instruction).

Table 3-2. System Register Numbers

No.	System Register Name	Operand Specification	
		LDSR Instruction	STSR Instruction
0	Status saving register during interrupt (EIPC)[Note 1]	○	○
1	Status saving register during interrupt (EIPSW)	○	○
2	Status saving register during NMI (FEPC)	○	○
3	Status saving register during NMI (FEPSW)	○	○
4	Interrupt source register (ECR)	×	○
5	Program status word (PSW)	○	○
6 to 15	Reserved number for future function expansion (operations that access these register numbers cannot be guaranteed).	×	×
16	Status saving register during CALLT execution (CTPC)	○	○
17	Status saving register during CALLT execution (CTPSW)	○	○
18	Status saving register during exception/debug trap (DBPC)	○[Note 2]	○
19	Status saving register during exception/debug trap (DBPSW)	○[Note 2]	○
20	CALLT base pointer (CTBP)	○	○
21 to 31	Reserved number for future function expansion (operations that access these register numbers cannot be guaranteed).	×	×

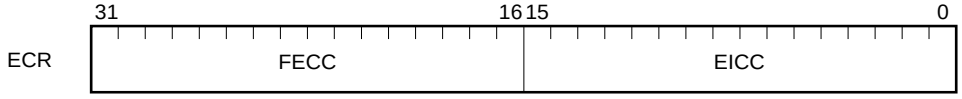
Notes 1. Because this register has only one set, to allow multiple interrupts, it is necessary to save this register by program.

2. Access is only possible when the DBTRAP instruction is executed.

Caution Even if bit 0 of EIPC, FEPC, or CTPC is set to 1 with the LDSR instruction, bit 0 will be ignored when the program is returned by the RETI instruction after interrupt servicing (because bit 0 of the PC is fixed to 0). When setting the value of EIPC, FEPC, or CTPC, use an even value (bit 0 = 0).

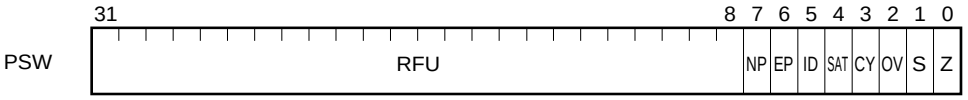
Remark ○: Access allowed
×: Access prohibited

Figure 3-2. Interrupt Source Register (ECR)



Bit Position	Bit Name	Function
31 to 16	FECC	Exception code of non-maskable interrupt (NMI)
15 to 0	EICC	Exception code of exception/maskable interrupt

Figure 3-3. Program Status Word (PSW)



Bit Position	Flag	Function
31 to 8	RFU	Reserved field (fixed to 0).
7	NP	Indicates that non-maskable interrupt (NMI) servicing is in progress. This flag is set when an NMI is acknowledged, and disables multiple interrupts. 0: NMI servicing not under execution. 1: NMI servicing under execution.
6	EP	Indicates that exception processing is in progress. This flag is set when an exception is generated. Moreover, interrupt requests can be acknowledged when this bit is set. 0: Exception processing not under execution. 1: Exception processing under execution.
5	ID	Displays whether a maskable interrupt request can be acknowledged or not. 0: Interrupt enabled. 1: Interrupt disabled.
4	SAT[Note]	Displays that the operation result of a saturated operation processing instruction is saturated due to overflow. Due to the cumulative flag, if the operation result is saturated by the saturation operation instruction, this bit is set (1), but is not cleared (0) even if the operation results of subsequent instructions are not saturated. To clear (0) this bit, load the data in PSW. Note that in a general arithmetic operation, this bit is neither set (1) nor cleared (0). 0: Not saturated. 1: Saturated.
3	CY	This flag is set if carry or borrow occurs as result of an operation (if carry or borrow does not occur, it is reset). 0: Carry or borrow does not occur. 1: Carry or borrow occurs.
2	OV[Note]	This flag is set if an overflow occurs during operation (if overflow does not occur, it is reset). 0: Overflow does not occur. 1: Overflow occurs.
1	S[Note]	This flag is set if the result of an operation is negative (it is reset if the result is positive). 0: The operation result was positive or 0. 1: The operation result was negative.
0	Z	This flag is set if the result of an operation is zero (if the result is not zero, it is reset). 0: The operation result was not 0. 1: The operation result was 0.

Note The result of a saturation-processed operation is determined by the contents of the OV and S flags in the saturation operation. Simply setting the OV flag (1) will set the SAT flag (1) in a saturation operation.

Status of Operation Result	Flag Status			Saturation-Processed Operation Result
	S	OV	SAT	
Maximum positive value exceeded	1	1	0	7FFFFFFFH
Maximum negative value exceeded	1	1	1	80000000H
Positive (not exceeding the maximum)	Retain the value before operation	0	0	Operation result itself
Negative (not exceed the maximum)			1	

3.3 Operation Modes

3.3.1 Operation modes

The V850E/IA1 has the following operations modes. Mode specification is carried out by the MODE0 to MODE2 pins.

(1) Normal operation mode

(a) Single-chip modes 0, 1

Access to the internal ROM is enabled.

In single-chip mode 0, after the system reset is cleared, each pin related to the bus interface enters the port mode, program execution branches to the reset entry address of the internal ROM, and instruction processing starts. By setting the PMCDH, PMCDL, PMCCS, PMCCT, and PMCCM registers to control mode by instruction, an external device can be connected to the external memory area.

In single-chip mode 1, after the system reset is cleared, each pin related to the bus interface enters the control mode, program execution branches to the external device's (memory) reset entry address, and instruction processing starts.

The internal ROM area is mapped from address 100000H.

(b) ROM-less modes 0, 1

After the system reset is cleared, each pin related to the bus interface enters the control mode, program execution branches to the external device's (memory) reset entry address, and instruction processing starts. Fetching of instructions and data access for internal ROM becomes impossible.

In ROM-less mode 0, the data bus is a 16-bit data bus and in ROM-less mode 1, the data bus is an 8-bit data bus.

(2) Flash memory programming mode (μPD70F3116 only)

If this mode is specified, it becomes possible for the flash programmer to run a program to the internal flash memory.

The initial values of the registers differ depending on the mode.

Operation Mode		PMCDH	PMCDL	PMCCS	PMCCT	PMCCM	BSC
Normal operation mode	ROM-less mode 0	FFH	FFFFH	FFH	53H	0FH	5555H
	ROM-less mode 1	FFH	FFFFH	FFH	53H	0FH	0000H
	Single-chip mode 0	00H	0000H	00H	00H	00H	5555H
	Single-chip mode 1	FFH	FFFFH	FFH	53H	0FH	5555H

3.3.2 Operation mode specification

The operation mode is specified according to the status of pins MODE0 to MODE2. In an application system fix the specification of these pins and do not change them during operation. Operation is not guaranteed if these pins are changed during operation.

(a) μPD70F3116

V_{PP}	MODE2	MODE1	MODE0	Operation Mode		Remark
0 V	L	L	L	Normal operation mode	ROM-less mode 0	16-bit data bus
0 V	L	L	H		ROM-less mode 1	8-bit data bus
0 V	L	H	L		Single-chip mode 0	Internal ROM area is allocated from address 000000H.
0 V	L	H	H		Single-chip mode 1	Internal ROM area is allocated from address 100000H.
7.8 V	L	H	H/L	Flash memory programming mode		—
Other than above				Setting prohibited		

(b) μPD703117

MODE2	MODE1	MODE0	Operation Mode		Remark
L	L	L	Normal operation mode	ROM-less mode 0	16-bit data bus
L	L	H		ROM-less mode 1	8-bit data bus
L	H	L		Single-chip mode 0	Internal ROM area is allocated from address 000000H.
L	H	H		Single-chip mode 1	Internal ROM area is allocated from address 100000H.
Other than above			Setting prohibited		

Remarks L: Low-level input
H: High-level input

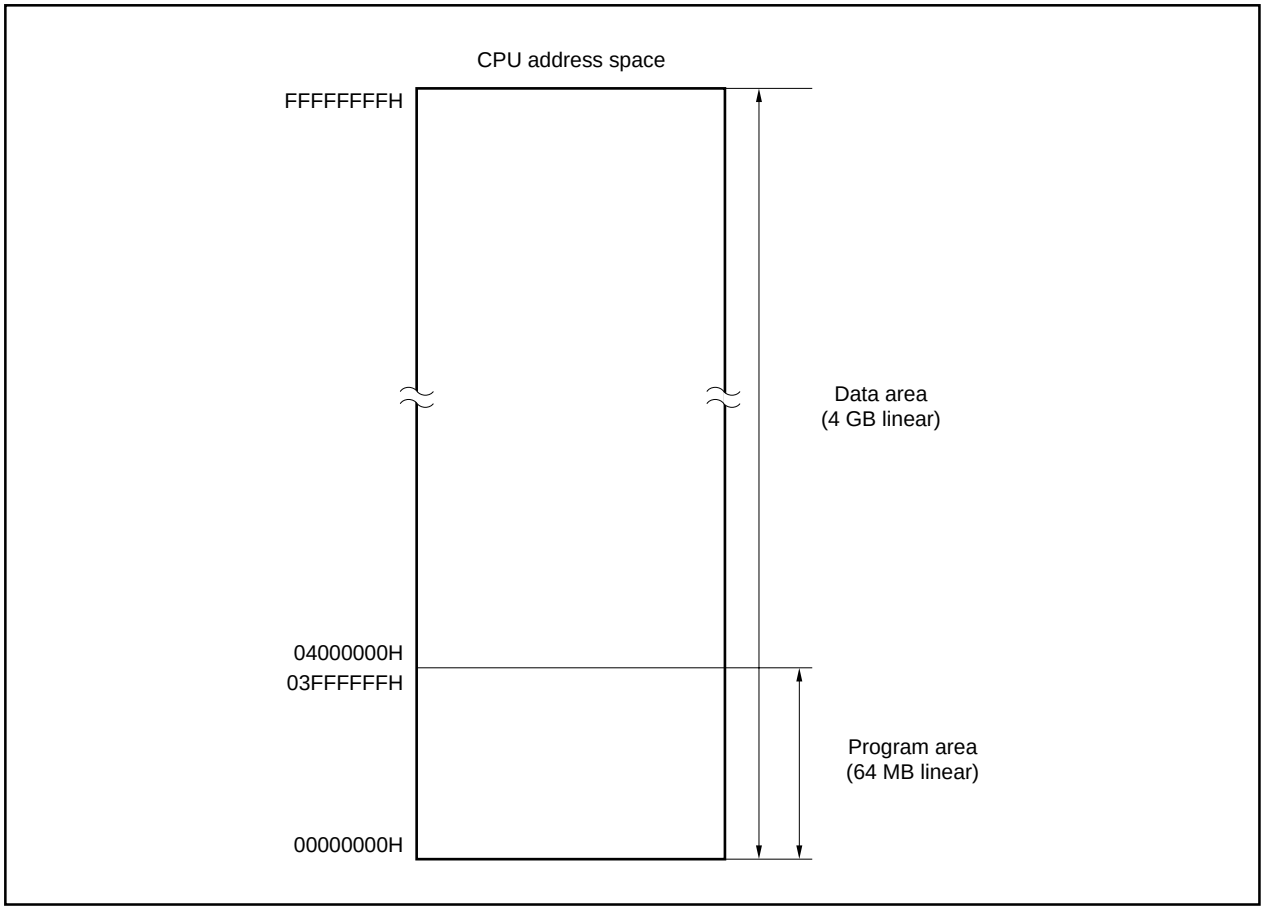
3.4 Address Space

3.4.1 CPU address space

The CPU of the V850E/IA1 is of 32-bit architecture and supports up to 4 GB of linear address space (data space) during operand addressing (data access). Also, in instruction address addressing, a maximum of 64 MB of linear address space (program space) is supported.

Figure 3-4 shows the CPU address space.

Figure 3-4. CPU Address Space

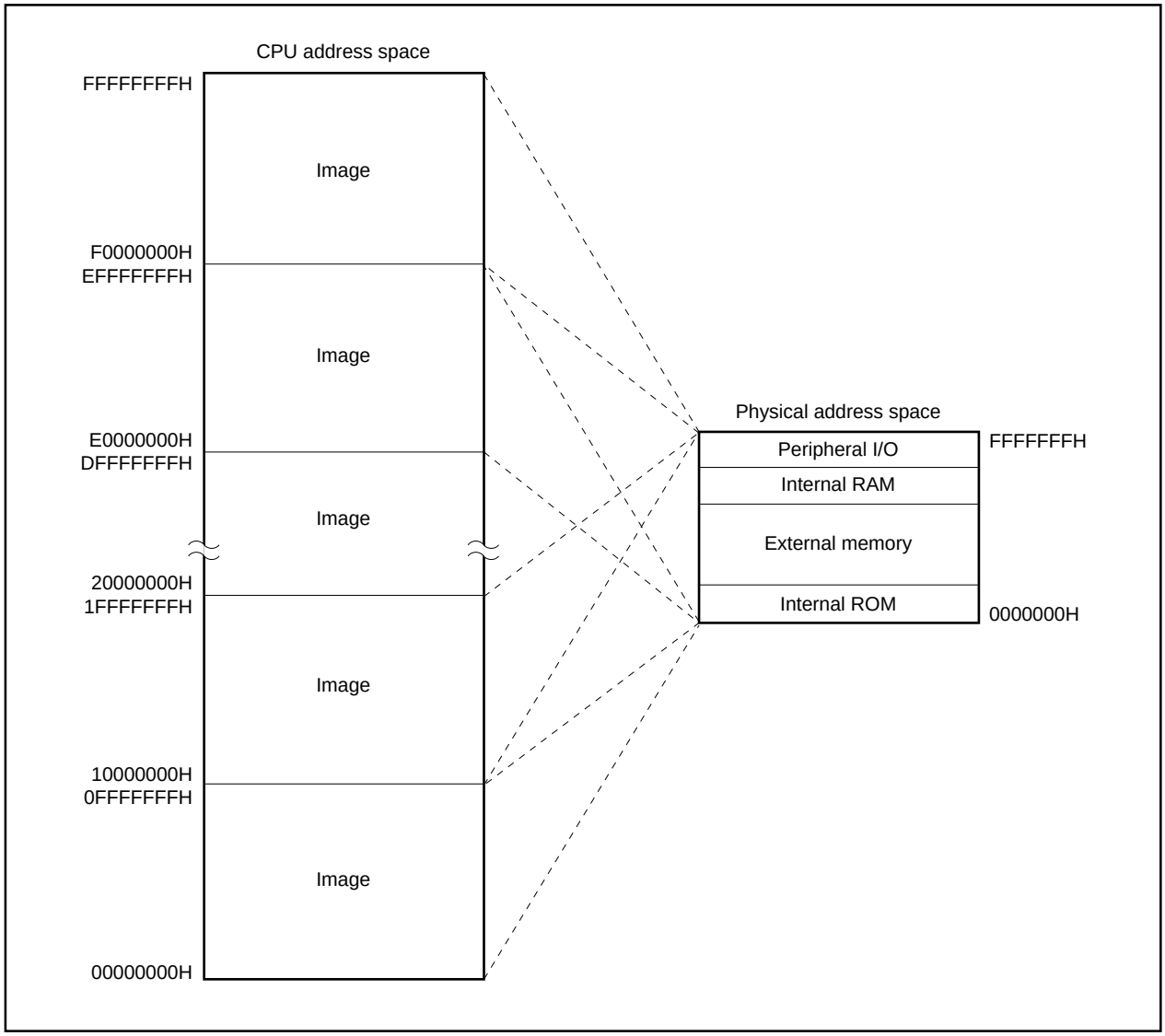


3.4.2 Image

16 images, each containing a 256 MB physical address space, are seen in the 4 GB CPU address space. In actuality, the same 256 MB physical address space is accessed regardless of the values of bits 31 to 28 of the CPU address. Figure 3-5 shows the image of the virtual addressing space.

Physical address x0000000H can be seen as CPU address 00000000H, and in addition, can be seen as address 10000000H, address 20000000H, … , address E0000000H, or address F0000000H.

Figure 3-5. Image on Address Space



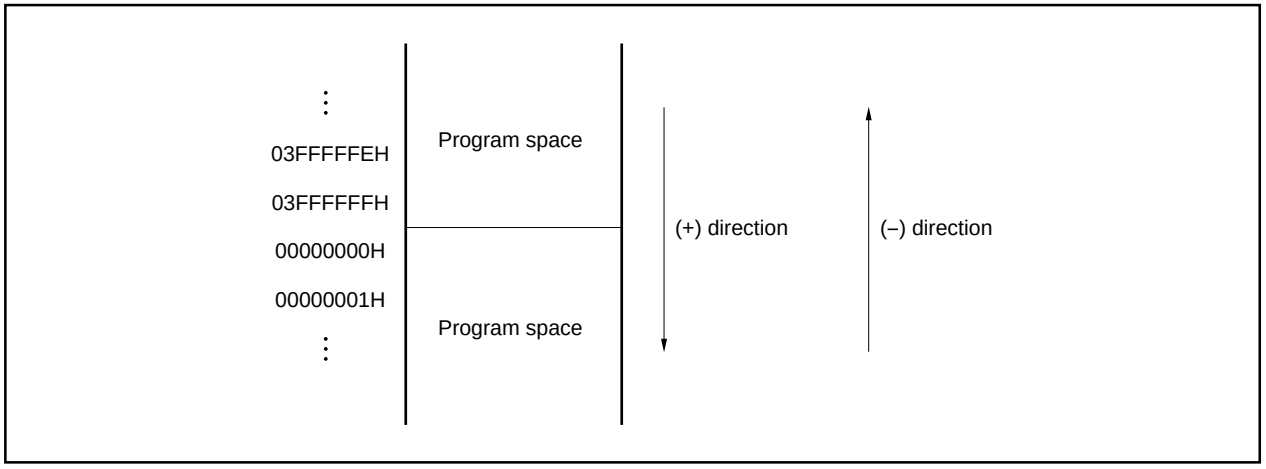
3.4.3 Wrap-around of CPU address space

(1) Program space

Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0, and only the lower 26 bits are valid. Even if a carry or borrow occurs from bit 25 to 26 as a result of branch address calculation, the higher 6 bits ignore the carry or borrow.

Therefore, the lower-limit address of the program space, address 00000000H, and the upper-limit address 03FFFFFFH become contiguous addresses. Wrap-around refers to a situation like this whereby the lower-limit address and upper-limit address become contiguous.

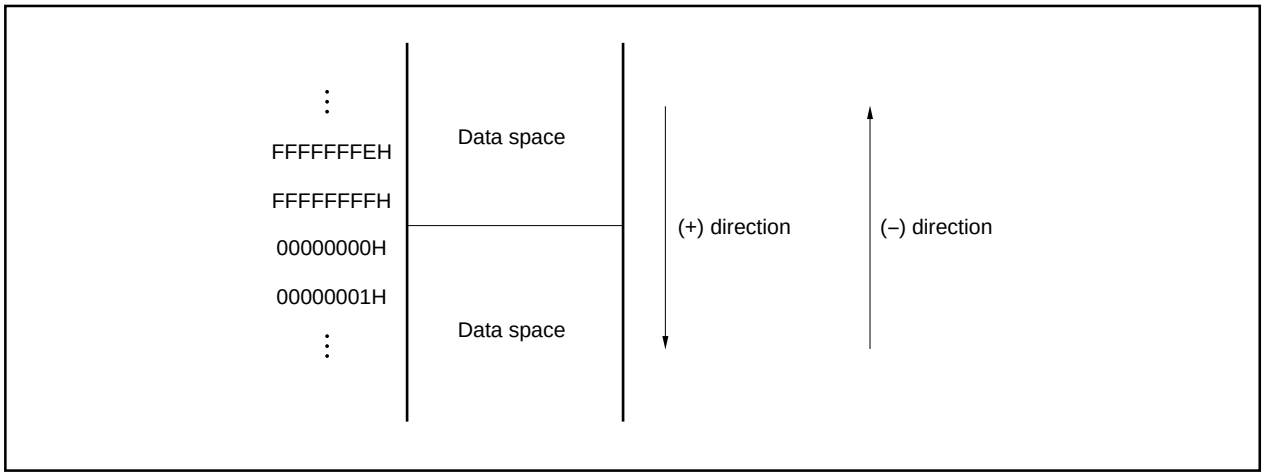
Caution The 4 KB area of 03FFF000H to 03FFFFFFH can be seen as an image of 0FFFF000H to 0FFFFFFFH. No instruction can be fetched from this area because this area is defined as peripheral I/O area. Therefore, do not execute any branch address calculation in which the result will reside in any part of this area.



(2) Data space

The result of an operand address calculation that exceeds 32 bits is ignored.

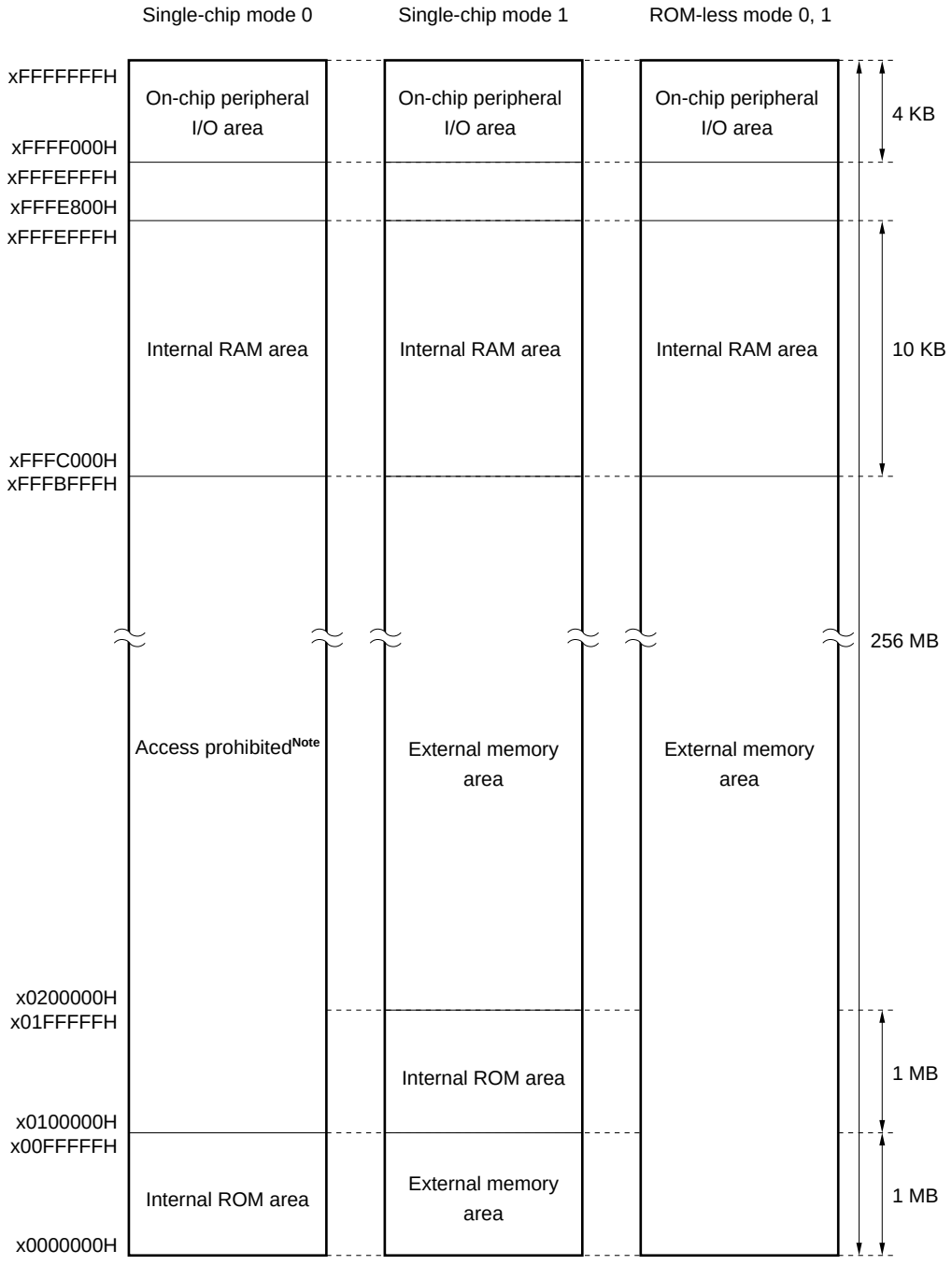
Therefore, the lower-limit address of the program space, address 00000000H, and the upper-limit address FFFFFFFFH are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



3.4.4 Memory map

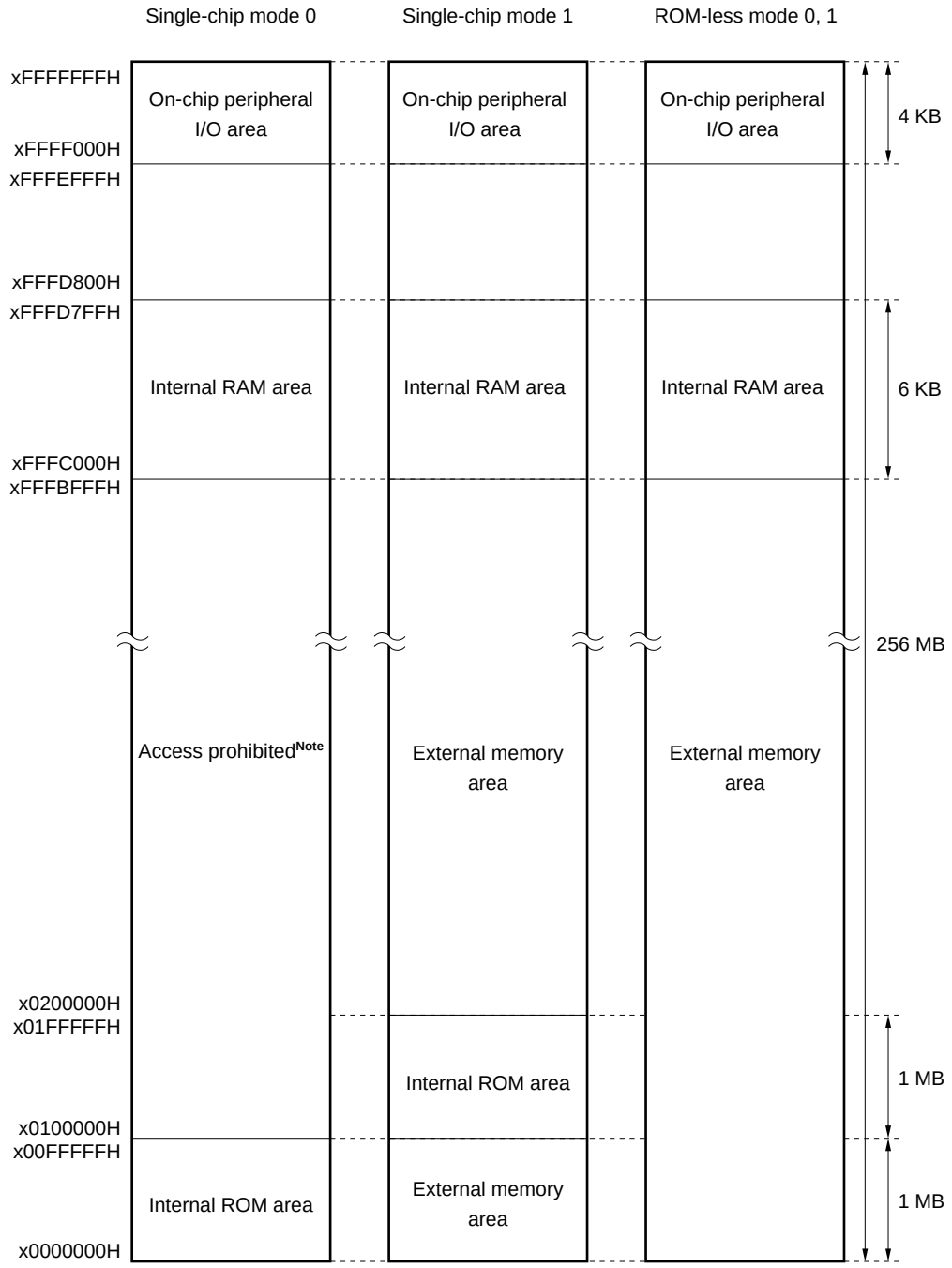
The V850E/IA1 reserves areas as shown in Figures 3-6 and 3-7. Each mode is specified by the MODE0 to MODE2 pins.

Figure 3-6. Memory Map (μPD70F3116)



Note By setting the PMCDH, PMCDL, PMCCS, PMCCT, and PMCCM registers to control mode, this area can be used as external memory area.

Figure 3-7. Memory Map (μPD703117)



Note By setting the PMCDH, PMCDL, PMCCS, PMCCT, and PMCCM registers to control mode, this area can be used as external memory area.

3.4.5 Area

(1) Internal ROM area

(a) Memory map (μPD70F3116, 703117)

1 MB of internal ROM area, addresses 00000H to FFFFFH, is reserved.

<1> μPD70F3116

256 KB are provided in the following addresses as physical internal ROM (flash memory).

- In single-chip mode 0: Addresses 000000H to 03FFFFH
- In single-chip mode 1: Addresses 100000H to 13FFFFH

<2> μPD703117

128 KB are provided in the following addresses as physical internal ROM (mask ROM).

- In single-chip mode 0: Addresses 000000H to 01FFFFH
- In single-chip mode 1: Addresses 100000H to 11FFFFH

(b) Interrupt/exception table

The V850E/IA1 increases the interrupt response speed by assigning handler addresses corresponding to interrupts/exceptions.

The collection of these handler addresses is called an interrupt/exception table, which is located in the internal ROM area. When an interrupt/exception request is acknowledged, execution jumps to the handler address, and the program written at that memory is executed. Table 3-3 shows the sources of interrupts/exceptions, and the corresponding addresses.

Remark When in ROM-less modes 0, 1, or in single-chip mode 1, in order to resume correct operation after reset, provide a handler address to the reset routine in address 0 of the external memory.

Table 3-3. Interrupt/Exception Table (1/2)

Start Address of Interrupt/Exception Table	Interrupt/Exception Source
00000000H	RESET
00000010H	NMI
00000040H	TRAP0n (n = 0 to F)
00000050H	TRAP1n (n = 0 to F)
00000060H	ILGOP/DBTRAP
00000080H	INTP0
00000090H	INTP1
000000A0H	INTP2
000000B0H	INTP3
000000C0H	INTP4
000000D0H	INTP5
000000E0H	INTP6
000000F0H	INTDET0
00000100H	INTDET1
00000110H	INTTM00
00000120H	INTCM003
00000130H	INTTM01
00000140H	INTCM013
00000150H	INTP100/INTCC100
00000160H	INTP101/INTCC101
00000170H	INTCM100
00000180H	INTCM101
00000190H	INTP110/INTCC110
000001A0H	INTP111/INTCC111
000001B0H	INTCM110
000001C0H	INTCM111
000001D0H	INTTM20
000001E0H	INTTM21
000001F0H	INTP20/INTCC20
00000200H	INTP21/INTCC21
00000210H	INTP22/INTCC22
00000220H	INTP23/INTCC23
00000230H	INTP24/INTCC24
00000240H	INTP25/INTCC25
00000250H	INTTM3
00000260H	INTP30/INTCC30
00000270H	INTP31/INTCC31

Table 3-3. Interrupt/Exception Table (2/2)

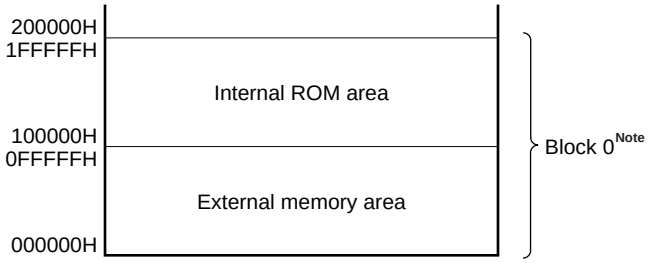
Start Address of Interrupt/Exception Table	Interrupt/Exception Source
00000280H	INTCM4
00000290H	INTDMA0
000002A0H	INTDMA1
000002B0H	INTDMA2
000002C0H	INTDMA3
000002D0H	INTCREC
000002E0H	INTCTRX
000002F0H	INTCERR
00000300H	INTCMAC
00000310H	INTCSI0
00000320H	INTCSI1
00000330H	INTSR0
00000340H	INTST0
00000350H	INTSER0
00000360H	INTSR1
00000370H	INTST1
00000380H	INTSR2
00000390H	INTST2
000003A0H	INTAD0
000003B0H	INTAD1

(c) Internal ROM area relocation function

If set in single-chip mode 1, the internal ROM area is located beginning from address 100000H, so booting from external memory becomes possible.

Therefore, in order to resume correct operation after reset, provide a handler address to the reset routine in address 0 of the external memory.

Figure 3-8. Internal ROM Area in Single-Chip Mode 1



Note See **4.3 Memory Block Function**.

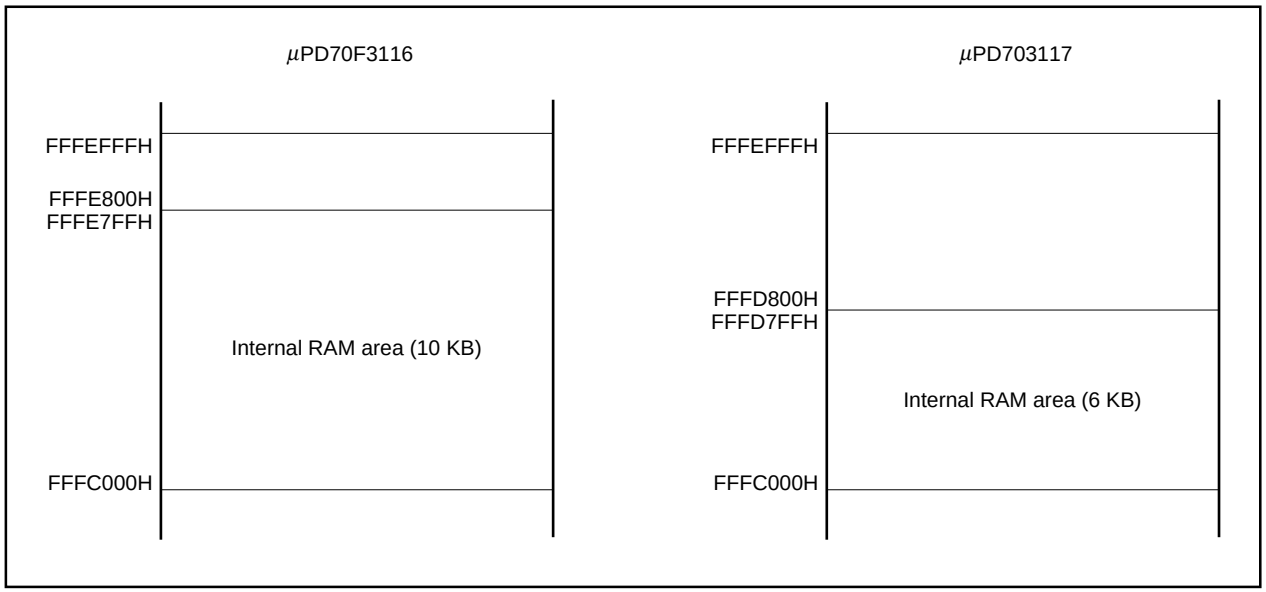
(2) Internal RAM area

12 KB of memory, addresses FFFC000H to FFFEFFFH, is reserved for the internal RAM area.

The 12 KB area of 3FFC000H to 3FFEFFFH can be seen as an image of FFFC000H to FFFEFFFH. When the internal RAM area is used as the program space, access addresses 3FFC000H to 3FFEFFFH.

In the μPD70F3116, 10 KB of memory, addresses FFFC000H to FFFE7FFH, is provided as physical internal RAM.

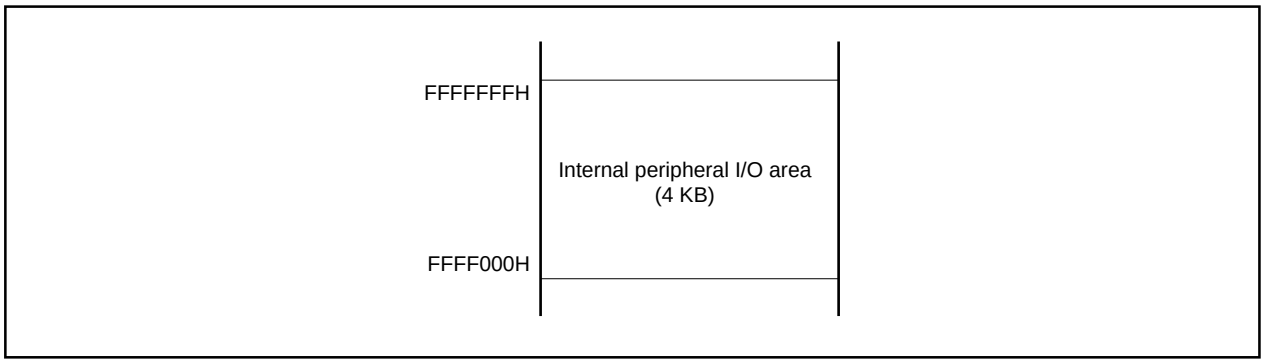
In the μPD703117, 6 KB of memory, addresses FFFC000H to FFFEDFFH, is provided as physical internal RAM.



(3) On-chip peripheral I/O area

4 KB of memory, addresses FFFF000H to FFFFFFFH, is provided as an on-chip peripheral I/O area.

An image of addresses FFFF000H to FFFFFFFH can be seen in the area between addresses 3FFF000H and 3FFFFFFH.



Peripheral I/O registers associated with the operation mode specification and the state monitoring for the on-chip peripherals I/O are all memory-mapped to the on-chip peripheral I/O area. Program fetches cannot be executed from this area.

Cautions 1. The least significant bit of an address is not decoded. Therefore, if byte access is executed in the register at an odd address (2n + 1), the register at the even address (2n) will be accessed because of the hardware specification.

2. In the V850E/IA1, no registers exist that are capable of word access, but if a register is word accessed, halfword access is performed twice in the order of lower address, then higher address of the word area, ignoring the lower 2 bits of the address.

3. For registers in which byte access is possible, if halfword access is executed, the higher 8 bits become undefined during the read operation, and the lower 8 bits of data are written to the register during the write operation.

4. Addresses that are not defined as registers are reserved for future expansion. If these addresses are accessed, the operation is undefined and not guaranteed.

5. Addresses 3FFF000H to 3FFFFFFH cannot be specified as the source/destination address of DMA transfer. Be sure to use addresses FFFF000H to FFFFFFFH for the source/destination address of DMA transfer.

In the on-chip peripheral I/O area, a 16 KB area of addresses from x0000H to 3FFFH is provided as a programmable peripheral I/O area. Within this area, the area between x2000H and x2FFFH is used exclusively for the FCAN controller (see **3.4.9 Programmable peripheral I/O registers**).

(4) External memory area

256 MB are available for external memory area. The lower 64 MB can be used as program/data area and the higher 192 MB as data area.

(a) μPD70F3116

When in single-chip mode 0: x0100000H to xFFFBFFFH
When in single-chip mode 1: x0000000H to x00FFFFFH, x0200000H to xFFFBFFFH
When in ROM-less modes 0 and 1: x0000000H to xFFFBFFFH

(b) μPD703117

When in single-chip mode 0: x0100000H to xFFFBFFFH
When in single-chip mode 1: x0000000H to x00FFFFFH, x0200000H to xFFFBFFFH
When in ROM-less modes 0 and 1: x0000000H to xFFFBFFFH

Access to the external memory area uses the chip-select signal assigned to each memory block (which is carried out in the CS unit set by chip area selection control registers 0 and 1 (CSC0, CSC1)).
Note that, the internal ROM, internal RAM, on-chip peripheral I/O, and programmable peripheral I/O areas cannot be accessed as external memory areas.

3.4.6 External memory expansion

By setting the port n mode control register (PMCn) to control mode, an external device can be connected to the external memory space using each pin of ports DH, DL, CS, CT, and CM. Each register is set by selecting control mode for each pin of these ports using PMCn (n = DH, DL, CS, CT, CM).

Note that the status after reset differs as shown below in accordance with the operating mode specification set by pins MODE0 to MODE2 (refer to **3.3 Operation Modes** for details of the operation modes).

(a) In the case of ROM-less mode 0

Because each pin of ports DH, DL, CS, CT, and CM enters control mode following a reset, external memory can be used without making changes to the port n mode control register (PMCn) (the external data bus width is 16 bits).

(b) In the case of ROM-less mode 1

Because each pin of ports DH, DL, CS, CT, and CM enters control mode following a reset, external memory can be used without making changes to the port n mode control register (PMCn) (the external data bus width is 8 bits).

(c) In the case of single-chip mode 0

Since the internal ROM area is accessed after a, reset, each pin of ports DH, DL, CS, CT, and CM enters the port mode, and external devices cannot be used.

To use external memory, set the port n mode control register (PMCn).

(d) In the case of single-chip mode 1

The internal ROM area is allocated from address 100000H. As a result, because each pin of ports DH, DL, CS, CT, and CM enters control mode following a reset, external memory can be used without making changes to the port n mode control register (PMCn) (the external data bus width is 16 bits).

Remark n = DH, DL, CS, CT, CM

3.4.7 Recommended use of address space

The architecture of the V850E/IA1 requires that a register that serves as a pointer be secured for address generation when accessing operand data in the data space. Operand data access from instruction can be directly executed at the address in this pointer register ±32 KB. However, because there is a limit to which general-purpose registers are used as a pointer register, by minimizing the deterioration of address calculation performance when changing the pointer value, the number of usable general-purpose registers for handling variables is maximized, and the program size can be saved.

To enhance the efficiency of using the pointer in connection with of the memory map of the V850E/IA1, the following points are recommended:

(1) Program space

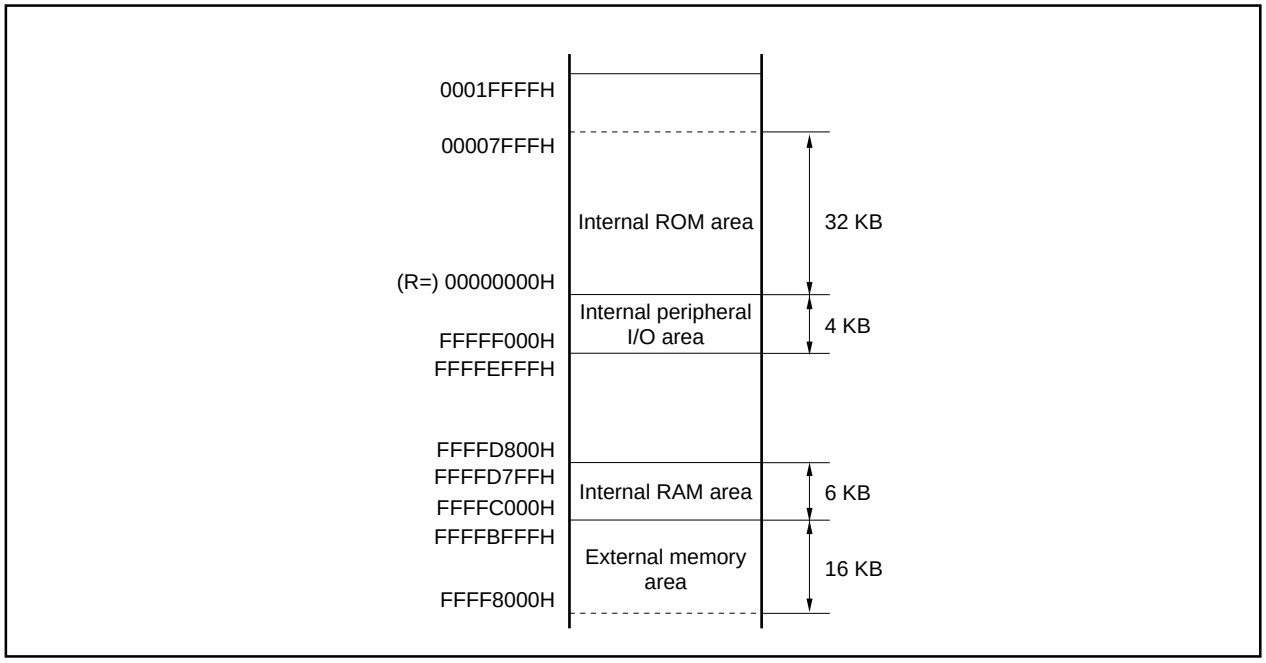
Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0, and only the lower 26 bits are valid. Therefore, a contiguous 64 MB space, starting from address 00000000H, unconditionally corresponds to the memory map of the program space.

When the internal RAM area is used as the program space, access addresses 3FFC000H to 3FFEFFFH.

(2) Data space

For the efficient use of resources that make use of the wrap-around feature of the data space, the continuous 16 MB address spaces 00000000H to 00FFFFFFH and FF000000H to FFFFFFFFH of the 4 GB CPU are used as the data space. With the V850E/IA1, a 256 MB physical address space is seen as 16 images in the 4 GB CPU address space. The highest bit (bit 25) of this 26-bit address is assigned as address sign-extended to 32 bits.

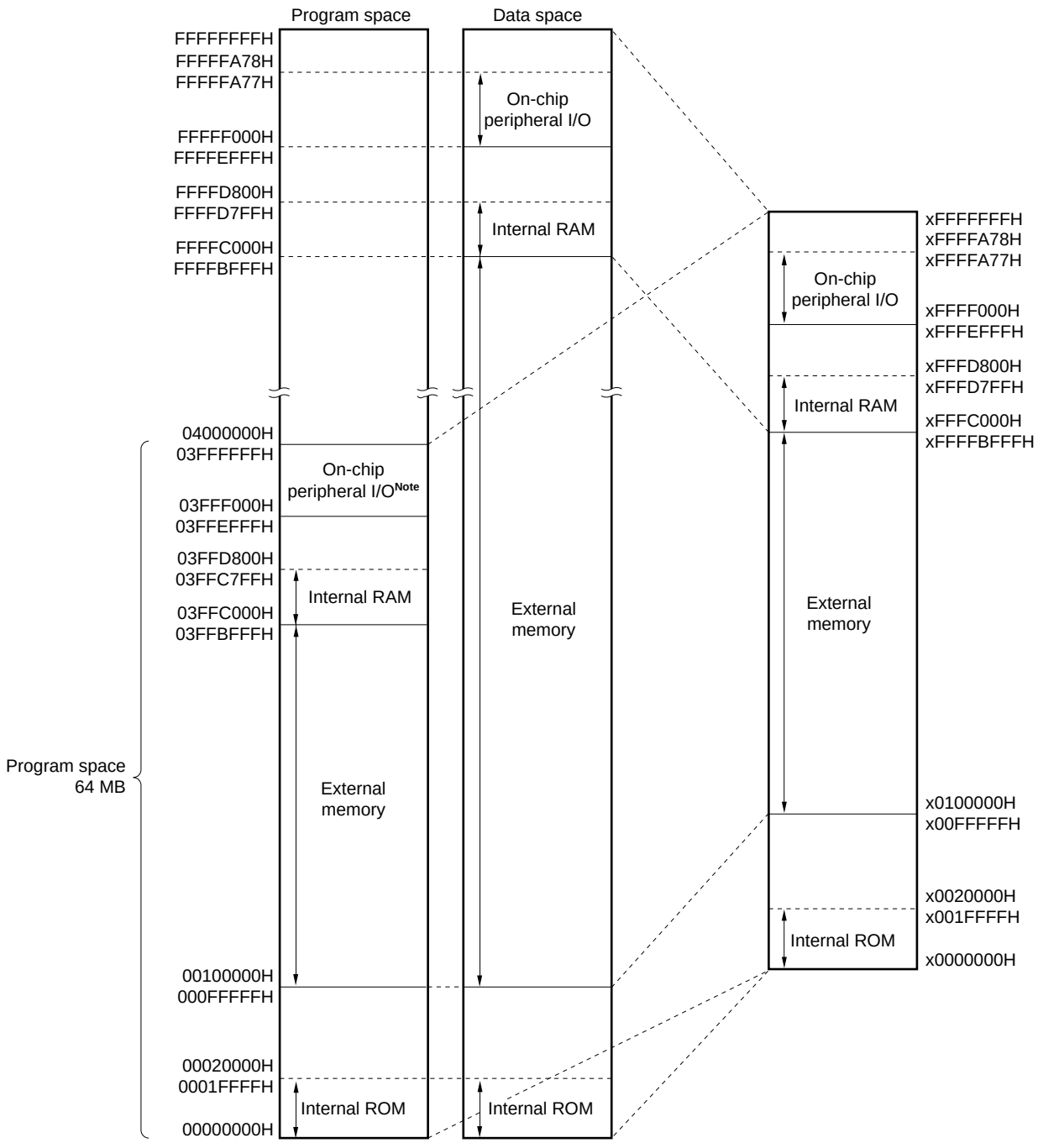
Example Application of wrap-around (μPD703117)



When R = r0 (zero register) is specified with the LD/ST disp16 [R] instruction, an addressing range of 00000000H ±32 KB can be referenced with the sign-extended disp 16. By mapping the external memory in the 16 KB area in the figure, all resources including internal hardware can be accessed with one pointer.

The zero register (r0) is a register set to 0 by the hardware, and eliminates the need for additional registers for the pointer.

Figure 3-9. Recommended Memory Map



Note This area cannot be used as a program area.

Remarks 1. The arrows indicate the recommended area.

2. This is a recommended memory map when the μPD703117 is set to single-chip mode 0, and used in external expansion mode.

3.4.8 Peripheral I/O registers

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF004H	Port DL	PDL	R/W			√	Undefined
FFFFF004H	Port DLL	PDLL	R/W	√	√		Undefined
FFFFF005H	Port DLH	PDLH	R/W	√	√		Undefined
FFFFF006H	Port DH	PDH	R/W	√	√		Undefined
FFFFF008H	Port CS	PCS	R/W	√	√		Undefined
FFFFF00AH	Port CT	PCT	R/W	√	√		Undefined
FFFFF00CH	Port CM	PCM	R/W	√	√		Undefined
FFFFF024H	Port DL mode register	PMDL	R/W			√	FFFFH
FFFFF024H	Port DL mode register L	PMDLL	R/W	√	√		FFH
FFFFF025H	Port DL mode register H	PMDLH	R/W	√	√		FFH
FFFFF026H	Port DH mode register	PMDH	R/W	√	√		FFH
FFFFF028H	Port CS mode register	PMCS	R/W	√	√		FFH
FFFFF02AH	Port CT mode register	PMCT	R/W	√	√		FFH
FFFFF02CH	Port CM mode register	PMCM	R/W	√	√		FFH
FFFFF044H	Port DL mode control register	PMCDL	R/W			√	0000H/FFFFH
FFFFF044H	Port DL mode control register L	PMCDLL	R/W	√	√		00H/FFH
FFFFF045H	Port DL mode control register H	PMCDLH	R/W	√	√		00H/FFH
FFFFF046H	Port DH mode control register	PMCDH	R/W	√	√		00H/FFH
FFFFF048H	Port CS mode control register	PMCCS	R/W	√	√		00H/FFH
FFFFF04AH	Port CT mode control register	PMCCT	R/W	√	√		00H/53H
FFFFF04CH	Port CM mode control register	PMCCM	R/W	√	√		00H/0FH
FFFFF060H	Chip area select control register 0	CSC0	R/W			√	2C11H
FFFFF062H	Chip area select control register 1	CSC1	R/W			√	2C11H
FFFFF064H	Peripheral area selection control register	BPC	R/W			√	0000H
FFFFF066H	Bus size configuration register	BSC	R/W			√	0000H/5555H
FFFFF06EH	System wait control register	VSWC	R/W	√	√		77H
FFFFF080H	DMA source address register 0L	DSA0L	R/W			√	Undefined
FFFFF082H	DMA source address register 0H	DSA0H	R/W			√	Undefined
FFFFF084H	DMA destination address register 0L	DDA0L	R/W			√	Undefined
FFFFF086H	DMA destination address register 0H	DDA0H	R/W			√	Undefined
FFFFF088H	DMA source address register 1L	DSA1L	R/W			√	Undefined
FFFFF08AH	DMA source address register 1H	DSA1H	R/W			√	Undefined
FFFFF08CH	DMA destination address register 1L	DDA1L	R/W			√	Undefined
FFFFF08EH	DMA destination address register 1H	DDA1H	R/W			√	Undefined
FFFFF090H	DMA source address register 2L	DSA2L	R/W			√	Undefined
FFFFF092H	DMA source address register 2H	DSA2H	R/W			√	Undefined

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF094H	DMA destination address register 2L	DDA2L	R/W			√	Undefined
FFFFF096H	DMA destination address register 2H	DDA2H	R/W			√	Undefined
FFFFF098H	DMA source address register 3L	DSA3L	R/W			√	Undefined
FFFFF09AH	DMA source address register 3H	DSA3H	R/W			√	Undefined
FFFFF09CH	DMA destination address register 3L	DDA3L	R/W			√	Undefined
FFFFF09EH	DMA destination address register 3H	DDA3H	R/W			√	Undefined
FFFFF0C0H	DMA transfer count register 0	DBC0	R/W			√	Undefined
FFFFF0C2H	DMA transfer count register 1	DBC1	R/W			√	Undefined
FFFFF0C4H	DMA transfer count register 2	DBC2	R/W			√	Undefined
FFFFF0C6H	DMA transfer count register 3	DBC3	R/W			√	Undefined
FFFFF0D0H	DMA addressing control register 0	DADC0	R/W			√	0000H
FFFFF0D2H	DMA addressing control register 1	DADC1	R/W			√	0000H
FFFFF0D4H	DMA addressing control register 2	DADC2	R/W			√	0000H
FFFFF0D6H	DMA addressing control register 3	DADC3	R/W			√	0000H
FFFFF0E0H	DMA channel control register 0	DCHC0	R/W	√	√		00H
FFFFF0E2H	DMA channel control register 1	DCHC1	R/W	√	√		00H
FFFFF0E4H	DMA channel control register 2	DCHC2	R/W	√	√		00H
FFFFF0E6H	DMA channel control register 3	DCHC3	R/W	√	√		00H
FFFFF0F0H	DMA disable status register	DDIS	R	√	√		00H
FFFFF0F2H	DMA restart register	DRST	R/W	√	√		00H
FFFFF100H	Interrupt mask register 0	IMR0	R/W			√	FFFFH
FFFFF100H	Interrupt mask register 0L	IMR0L	R/W	√	√		FFH
FFFFF101H	Interrupt mask register 0H	IMR0H	R/W	√	√		FFH
FFFFF102H	Interrupt mask register 1	IMR1	R/W			√	FFFFH
FFFFF102H	Interrupt mask register 1L	IMR1L	R/W	√	√		FFH
FFFFF103H	Interrupt mask register 1H	IMR1H	R/W	√	√		FFH
FFFFF104H	Interrupt mask register 2	IMR2	R/W			√	FFFFH
FFFFF104H	Interrupt mask register 2L	IMR2L	R/W	√	√		FFH
FFFFF105H	Interrupt mask register 2H	IMR2H	R/W	√	√		FFH
FFFFF106H	Interrupt mask register 3	IMR3	R/W			√	FFFFH
FFFFF106H	Interrupt mask register 3L	IMR3L	R/W	√	√		FFH
FFFFF107H	Interrupt mask register 3H	IMR3H	R/W	√	√		FFH
FFFFF110H	Interrupt control register	P0IC0	R/W	√	√		47H
FFFFF112H	Interrupt control register	P0IC1	R/W	√	√		47H
FFFFF114H	Interrupt control register	P0IC2	R/W	√	√		47H
FFFFF116H	Interrupt control register	P0IC3	R/W	√	√		47H
FFFFF118H	Interrupt control register	P0IC4	R/W	√	√		47H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF11AH	Interrupt control register	P0IC5	R/W	√	√		47H
FFFFF11CH	Interrupt control register	P0IC6	R/W	√	√		47H
FFFFF11EH	Interrupt control register	DETIC0	R/W	√	√		47H
FFFFF120H	Interrupt control register	DETIC1	R/W	√	√		47H
FFFFF122H	Interrupt control register	TM0IC0	R/W	√	√		47H
FFFFF124H	Interrupt control register	CM03IC0	R/W	√	√		47H
FFFFF126H	Interrupt control register	TM0IC1	R/W	√	√		47H
FFFFF128H	Interrupt control register	CM03IC1	R/W	√	√		47H
FFFFF12AH	Interrupt control register	CC10IC0	R/W	√	√		47H
FFFFF12CH	Interrupt control register	CC10IC1	R/W	√	√		47H
FFFFF12EH	Interrupt control register	CM10IC0	R/W	√	√		47H
FFFFF130H	Interrupt control register	CM10IC1	R/W	√	√		47H
FFFFF132H	Interrupt control register	CC11IC0	R/W	√	√		47H
FFFFF134H	Interrupt control register	CC11IC1	R/W	√	√		47H
FFFFF136H	Interrupt control register	CM11IC0	R/W	√	√		47H
FFFFF138H	Interrupt control register	CM11IC1	R/W	√	√		47H
FFFFF13AH	Interrupt control register	TM2IC0	R/W	√	√		47H
FFFFF13CH	Interrupt control register	TM2IC1	R/W	√	√		47H
FFFFF13EH	Interrupt control register	CC2IC0	R/W	√	√		47H
FFFFF140H	Interrupt control register	CC2IC1	R/W	√	√		47H
FFFFF142H	Interrupt control register	CC2IC2	R/W	√	√		47H
FFFFF144H	Interrupt control register	CC2IC3	R/W	√	√		47H
FFFFF146H	Interrupt control register	CC2IC4	R/W	√	√		47H
FFFFF148H	Interrupt control register	CC2IC5	R/W	√	√		47H
FFFFF14AH	Interrupt control register	TM3IC0	R/W	√	√		47H
FFFFF14CH	Interrupt control register	CC3IC0	R/W	√	√		47H
FFFFF14EH	Interrupt control register	CC3IC1	R/W	√	√		47H
FFFFF150H	Interrupt control register	CM4IC0	R/W	√	√		47H
FFFFF152H	Interrupt control register	DMAIC0	R/W	√	√		47H
FFFFF154H	Interrupt control register	DMAIC1	R/W	√	√		47H
FFFFF156H	Interrupt control register	DMAIC2	R/W	√	√		47H
FFFFF158H	Interrupt control register	DMAIC3	R/W	√	√		47H
FFFFF15AH	Interrupt control register	CANIC0	R/W	√	√		47H
FFFFF15CH	Interrupt control register	CANIC1	R/W	√	√		47H
FFFFF15EH	Interrupt control register	CANIC2	R/W	√	√		47H
FFFFF160H	Interrupt control register	CANIC3	R/W	√	√		47H
FFFFF162H	Interrupt control register	CSIIC0	R/W	√	√		47H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF164H	Interrupt control register	CSIIC1	R/W	√	√		47H
FFFFF166H	Interrupt control register	SRIC0	R/W	√	√		47H
FFFFF168H	Interrupt control register	STIC0	R/W	√	√		47H
FFFFF16AH	Interrupt control register	SEIC0	R/W	√	√		47H
FFFFF16CH	Interrupt control register	SRIC1	R/W	√	√		47H
FFFFF16EH	Interrupt control register	STIC1	R/W	√	√		47H
FFFFF170H	Interrupt control register	SRIC2	R/W	√	√		47H
FFFFF172H	Interrupt control register	STIC2	R/W	√	√		47H
FFFFF174H	Interrupt control register	ADIC0	R/W	√	√		47H
FFFFF176H	Interrupt control register	ADIC1	R/W	√	√		47H
FFFFF1FAH	In-service priority register	ISPR	R	√	√		00H
FFFFF1FCH	Command register	PRCMD	W		√		Undefined
FFFFF1FEH	Power-saving control register	PSC	R/W	√	√		00H
FFFFF200H	A/D scan mode register 00	ADSCM00	R/W	√	√	√	0000H
FFFFF202H	A/D scan mode register 01	ADSCM01	R/W	√	√	√	0000H
FFFFF204H	A/D voltage detection mode register 0	ADETM0	R/W	√	√	√	0000H
FFFFF210H	A/D conversion result register 00	ADCR00	R			√	0000H
FFFFF212H	A/D conversion result register 01	ADCR01	R			√	0000H
FFFFF214H	A/D conversion result register 02	ADCR02	R			√	0000H
FFFFF216H	A/D conversion result register 03	ADCR03	R			√	0000H
FFFFF218H	A/D conversion result register 04	ADCR04	R			√	0000H
FFFFF21AH	A/D conversion result register 05	ADCR05	R			√	0000H
FFFFF21CH	A/D conversion result register 06	ADCR06	R			√	0000H
FFFFF21EH	A/D conversion result register 07	ADCR07	R			√	0000H
FFFFF240H	A/D scan mode register 10	ADSCM10	R/W	√	√	√	0000H
FFFFF242H	A/D scan mode register 11	ADSCM11	R/W	√	√	√	0000H
FFFFF244H	A/D voltage detection mode register 1	ADETM1	R/W	√	√	√	0000H
FFFFF250H	A/D conversion result register 10	ADCR10	R			√	0000H
FFFFF252H	A/D conversion result register 11	ADCR11	R			√	0000H
FFFFF254H	A/D conversion result register 12	ADCR12	R			√	0000H
FFFFF256H	A/D conversion result register 13	ADCR13	R			√	0000H
FFFFF258H	A/D conversion result register 14	ADCR14	R			√	0000H
FFFFF25AH	A/D conversion result register 15	ADCR15	R			√	0000H
FFFFF25CH	A/D conversion result register 16	ADCR16	R			√	0000H
FFFFF25EH	A/D conversion result register 17	ADCR17	R			√	0000H
FFFFF280H	A/D internal trigger select register	ITRG0	R/W	√	√		00H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF400H	Port 0	P0	R/W	√	√		Undefined
FFFFF402H	Port 1	P1	R/W	√	√		Undefined
FFFFF404H	Port 2	P2	R/W	√	√		Undefined
FFFFF406H	Port 3	P3	R/W	√	√		Undefined
FFFFF408H	Port 4	P4	R/W	√	√		Undefined
FFFFF422H	Port 1 mode register	PM1	R/W	√	√		FFH
FFFFF424H	Port 2 mode register	PM2	R/W	√	√		FFH
FFFFF426H	Port 3 mode register	PM3	R/W	√	√		FFH
FFFFF428H	Port 4 mode register	PM4	R/W	√	√		FFH
FFFFF442H	Port 1 mode control register	PMC1	R/W	√	√		00H
FFFFF444H	Port 2 mode control register	PMC2	R/W	√	√		00H
FFFFF446H	Port 3 mode control register	PMC3	R/W	√	√		00H
FFFFF448H	Port 4 mode control register	PMC4	R/W	√	√		00H
FFFFF462H	Port 1 function control register	PFC1	R/W	√	√		00H
FFFFF464H	Port 2 function control register	PFC2	R/W	√	√		00H
FFFFF480H	Bus cycle type configuration register 0	BCT0	R/W			√	CCCCH
FFFFF482H	Bus cycle type configuration register 1	BCT1	R/W			√	CCCCH
FFFFF484H	Data wait control register 0	DWC0	R/W			√	3333H
FFFFF486H	Data wait control register 1	DWC1	R/W			√	3333H
FFFFF488H	Address wait control register	AWC	R/W			√	0000H
FFFFF48AH	Bus cycle control register	BCC	R/W			√	AAAAH
FFFFF540H	Timer 4	TM4	R			√	0000H
FFFFF542H	Compare register 4	CM4	R/W			√	0000H
FFFFF544H	Timer control register 4	TMC4	R/W	√	√		00H
FFFFF570H	Dead time timer reload register 0	DTRR0	R/W			√	FFFH
FFFFF572H	Buffer register CM00	BFCM00	R/W			√	FFFFH
FFFFF574H	Buffer register CM01	BFCM01	R/W			√	FFFFH
FFFFF576H	Buffer register CM02	BFCM02	R/W			√	FFFFH
FFFFF578H	Buffer register CM03	BFCM03	R/W			√	FFFFH
FFFFF57AH	Timer control register 00	TMC00	R/W			√	0508H
FFFFF57AH	Timer control register 00L	TMC00L	R/W	√	√		08H
FFFFF57BH	Timer control register 00H	TMC00H	R/W	√	√		05H
FFFFF57CH	Timer unit control register 00	TUC00	R/W	√	√		01H
FFFFF57DH	Timer output mode register 0	TOMR0	R/W		√		00H
FFFFF57EH	PWM software timing output register 0	PSTO0	R/W	√	√		00H
FFFFF57FH	PWM output enable register 0	POER0	R/W	√	√		00H
FFFFF580H	TOMR write enable register 0	SPEC0	R/W			√	0000H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF5B0H	Dead time timer reload register 1	DTRR1	R/W			√	FFFH
FFFFF5B2H	Buffer register CM10	BFCM10	R/W			√	FFFFH
FFFFF5B4H	Buffer register CM11	BFCM11	R/W			√	FFFFH
FFFFF5B6H	Buffer register CM12	BFCM12	R/W			√	FFFFH
FFFFF5B8H	Buffer register CM13	BFCM13	R/W			√	FFFFH
FFFFF5BAH	Timer control register 01	TMC01	R/W			√	0508H
FFFFF5BAH	Timer control register 01L	TMC01L	R/W	√	√		08H
FFFFF5BBH	Timer control register 01H	TMC01H	R/W	√	√		05H
FFFFF5BCH	Timer unit control register 01	TUC01	R/W	√	√		01H
FFFFF5BDH	Timer output mode register 1	TOMR1	R/W		√		00H
FFFFF5BEH	PWM software timing output register 1	PSTO1	R/W	√	√		00H
FFFFF5BFH	PWM output enable register 1	POER1	R/W	√	√		00H
FFFFF5C0H	TOMR write enable register 1	SPEC1	R/W			√	0000H
FFFFF5D0H	Timer 0n clock select register	PRM01	R/W	√	√		00H
FFFFF5D8H	Timer 1n/Timer 2n clock select register	PRM02	R/W	√	√		00H
FFFFF5E0H	Timer 10	TM10	R/W			√	0000H
FFFFF5E2H	Compare register 100	CM100	R/W			√	0000H
FFFFF5E4H	Compare register 101	CM101	R/W			√	0000H
FFFFF5E6H	Capture/compare register 100	CC100	R/W			√	0000H
FFFFF5E8H	Capture/compare register 101	CC101	R/W			√	0000H
FFFFF5EAH	Capture/compare control register 0	CCR0	R/W	√	√		00H
FFFFF5EBH	Timer unit mode register 0	TUM0	R/W	√	√		00H
FFFFF5ECH	Timer control register 10	TMC10	R/W	√	√		00H
FFFFF5EDH	Signal edge select register 10	SESA10	R/W	√	√		00H
FFFFF5EEH	Prescaler mode register 10	PRM10	R/W	√	√		07H
FFFFF5EFH	Status register 0	STATUS0	R	√	√		00H
FFFFF5F6H	CC101 capture input select register	CSL10	R/W	√	√		00H
FFFFF5F8H	Timer 10 noise elimination time select register	NRC10	R/W	√	√		00H
FFFFF600H	Timer 11	TM11	R/W			√	0000H
FFFFF602H	Compare register 110	CM110	R/W			√	0000H
FFFFF604H	Compare register 111	CM111	R/W			√	0000H
FFFFF606H	Capture/compare register 110	CC110	R/W			√	0000H
FFFFF608H	Capture/compare register 111	CC111	R/W			√	0000H
FFFFF60AH	Capture/compare control register 1	CCR1	R/W	√	√		00H
FFFFF60BH	Timer unit mode register 1	TUM1	R/W	√	√		00H
FFFFF60CH	Timer control register 11	TMC11	R/W	√	√		00H
FFFFF60DH	Signal edge select register 11	SESA11	R/W	√	√		00H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF60EH	Prescaler mode register 11	PRM11	R/W	√	√		07H
FFFFF60FH	Status register 1	STATUS1	R	√	√		00H
FFFFF616H	CC111 capture input select register	CSL11	R/W	√	√		00H
FFFFF618H	Timer 11 noise elimination time select register	NRC11	R/W	√	√		00H
FFFFF620H	Timer connection select register 0	TMIC0	R/W	√	√		00H
FFFFF630H	Timer 2 input filter mode register 0	FEM0	R/W	√	√		00H
FFFFF631H	Timer 2 input filter mode register 1	FEM1	R/W	√	√		00H
FFFFF632H	Timer 2 input filter mode register 2	FEM2	R/W	√	√		00H
FFFFF633H	Timer 2 input filter mode register 3	FEM3	R/W	√	√		00H
FFFFF634H	Timer 2 input filter mode register 4	FEM4	R/W	√	√		00H
FFFFF635H	Timer 2 input filter mode register 5	FEM5	R/W	√	√		00H
FFFFF640H	Timer 2 clock stop register	STOPTE0	R/W	√	√	√	0000H
FFFFF642H	Timer 2 count clock/control edge select register	CSE0	R/W	√	√	√	0000H
FFFFF644H	Timer 2 subchannel input event edge select register	SESE0	R/W	√	√	√	0000H
FFFFF646H	Timer 2 time base control register	TCRE0	R/W	√	√	√	0000H
FFFFF648H	Timer 2 output control register	OCTLE0	R/W	√	√	√	0000H
FFFFF64AH	Timer 2 subchannel 0, 5 capture/compare control register	CMSE050	R/W			√	0000H
FFFFF64CH	Timer 2 subchannel 1, 2 capture/compare control register	CMSE120	R/W			√	0000H
FFFFF64EH	Timer 2 subchannel 3, 4 capture/compare control register	CMSE340	R/W			√	0000H
FFFFF650H	Timer 2 subchannel 1 sub capture/compare register	CVSE10	R/W			√	0000H
FFFFF652H	Timer 2 subchannel 1 main capture/compare register	CVPE10	R			√	0000H
FFFFF654H	Timer 2 subchannel 2 sub capture/compare register	CVSE20	R/W			√	0000H
FFFFF656H	Timer 2 subchannel 2 main capture/compare register	CVPE20	R			√	0000H
FFFFF658H	Timer 2 subchannel 3 sub capture/compare register	CVSE30	R/W			√	0000H
FFFFF65AH	Timer 2 subchannel 3 main capture/compare register	CVPE30	R			√	0000H
FFFFF65CH	Timer 2 subchannel 4 sub capture/compare register	CVSE40	R/W			√	0000H
FFFFF65EH	Timer 2 subchannel 4 main capture/compare register	CVPE40	R			√	0000H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF660H	Timer 2 subchannel 0 capture/compare register	CVSE00	R/W			√	0000H
FFFFF662H	Timer 2 subchannel 5 capture/compare register	CVSE50	R/W			√	0000H
FFFFF664H	Timer 2 time base status register	TBSTATE0	R/W	√	√	√	0000H
FFFFF666H	Timer 2 capture/compare 1 to 4 status register	CCSTATE0	R/W	√	√	√	0000H
FFFFF668H	Timer 2 output delay register	ODELE0	R/W	√	√	√	0000H
FFFFF66AH	Timer 2 software event capture register	OSCE0	R/W			√	0000H
FFFFF680H	Timer 3	TM3	R			√	0000H
FFFFF682H	Capture/compare register 30	CC30	R/W			√	0000H
FFFFF684H	Capture/compare register 31	CC31	R/W			√	0000H
FFFFF686H	Timer control register 30	TMC30	R/W	√	√		00H
FFFFF688H	Timer control register 31	TMC31	R/W	√	√		20H
FFFFF689H	Valid edge select register	SESC	R/W	√	√		00H
FFFFF690H	Timer 3 clock select register	PRM03	R/W	√	√		00H
FFFFF698H	Timer 3 noise elimination time select register	NRC3	R/W	√	√		00H
FFFFF800H	Peripheral command register	PHCMD	W		√		Undefined
FFFFF802H	Peripheral status register	PHS	R/W	√	√		00H
FFFFF810H	DMA trigger factor register 0	DTFR0	R/W	√	√		00H
FFFFF812H	DMA trigger factor register 1	DTFR1	R/W	√	√		00H
FFFFF814H	DMA trigger factor register 2	DTFR2	R/W	√	√		00H
FFFFF816H	DMA trigger factor register 3	DTFR3	R/W	√	√		00H
FFFFF820H	Power-saving mode register	PSMR	R/W	√	√		00H
FFFFF822H	Clock control register	CKC	R/W	√	√		00H
FFFFF824H	Lock register	LOCK	R	√	√		Undefined
FFFFF880H	External interrupt mode register 0	INTM0	R/W	√	√		00H
FFFFF882H	External interrupt mode register 1	INTM1	R/W	√	√		00H
FFFFF884H	External interrupt mode register 2	INTM2	R/W	√	√		00H
FFFFF8D4H	Flash programming mode control register	FLPMC	R/W	√	√		08H/0CH
FFFFF900H	Clocked serial interface mode register 0	CSIM0	R/W	√	√		00H
FFFFF901H	Clocked serial interface clock select register 0	CSIC0	R/W	√	√		00H
FFFFF902H	Clocked serial interface receive buffer register 0	SIRB0	R			√	0000H
FFFFF904H	Clocked serial interface transmit buffer register 0	SOTB0	R/W			√	0000H
FFFFF906H	Clocked serial interface read-only receive buffer register 0	SIRBE0	R			√	0000H
FFFFF908H	Clocked serial interface first transmit buffer register 0	SOTBF0	R/W			√	0000H

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFF90AH	Serial I/O shift register 0	SIO0	R			√	0000H
FFFFF910H	Clocked serial interface mode register 1	CSIM1	R/W	√	√		00H
FFFFF911H	Clocked serial interface clock select register 1	CSIC1	R/W	√	√		00H
FFFFF912H	Clocked serial interface receive buffer register 1	SIRB1	R			√	0000H
FFFFF914H	Clocked serial interface transmit buffer register 1	SOTB1	R/W			√	0000H
FFFFF916H	Clocked serial interface read-only receive buffer register 1	SIRBE1	R			√	0000H
FFFFF918H	Clocked serial interface first transmit buffer register 1	SOTBF1	R/W			√	0000H
FFFFF91AH	Serial I/O shift register 1	SIO1	R			√	0000H
FFFFF920H	Prescaler mode register 3	PRSM3	R/W	√	√		00H
FFFFF922H	Prescaler compare register 3	PRSCM3	R/W	√	√		00H
FFFFF930H	FCAN clock select register	PRM04	R/W	√	√		00H
FFFFFA00H	Asynchronous serial interface mode register 0	ASIM0	R/W	√	√		01H
FFFFFA02H	Receive buffer register 0	RXB0	R	√	√		FFH
FFFFFA03H	Asynchronous serial interface status register 0	ASIS0	R	√	√		00H
FFFFFA04H	Transmit buffer register 0	TXB0	R/W	√	√		FFH
FFFFFA05H	Asynchronous serial interface transmit status register 0	ASIF0	R	√	√		00H
FFFFFA06H	Clock select register 0	CKSR0	R/W	√	√		00H
FFFFFA07H	Baud rate generator control register 0	BRGC0	R/W	√	√		FFH
FFFFFA20H	2-frame successive receive buffer register 1	RXB1	R/W			√	Undefined
FFFFFA22H	Receive buffer register L1	RXBL1	R/W	√	√		Undefined
FFFFFA24H	2-frame successive transmit shift register 1	TXS1	W			√	Undefined
FFFFFA26H	Transmit shift register L1	TXSL1	W		√		Undefined
FFFFFA28H	Asynchronous serial interface mode register 10	ASIM10	R/W	√	√		81H
FFFFFA2AH	Asynchronous serial interface mode register 11	ASIM11	R/W	√	√		00H
FFFFFA2CH	Asynchronous serial interface status register 1	ASIS1	R	√	√		00H
FFFFFA2EH	Prescaler mode register 1	PRSM1	R/W	√	√		00H
FFFFFA30H	Prescaler compare register 1	PRSCM1	R/W	√	√		00H
FFFFFA40H	2-frame successive receive buffer register 2	RXB2	R/W			√	Undefined
FFFFFA42H	Receive buffer register L2	RXBL2	R/W	√	√		Undefined
FFFFFA44H	2-frame successive transmit shift register 2	TXS2	W			√	Undefined
FFFFFA46H	Transmit shift register L2	TXSL2	W		√		Undefined
FFFFFA48H	Asynchronous serial interface mode register 20	ASIM20	R/W	√	√		81H
FFFFFA4AH	Asynchronous serial interface mode register 21	ASIM21	R/W	√	√		00H
FFFFFA4CH	Asynchronous serial interface status register 2	ASIS2	R	√	√		00H

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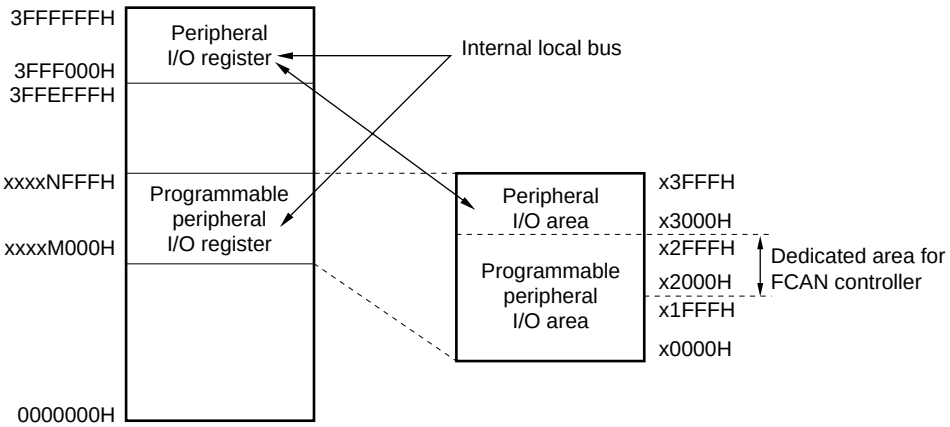
Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
FFFFFA4EH	Prescaler mode register 2	PRSM2	R/W	√	√		00H
FFFFFA50H	Prescaler compare register 2	PRSCM2	R/W	√	√		00H
FFFFFA60H	RAM access data buffer L	NBDL	R/W		√	√	0000H
FFFFFA61H	RAM access data buffer LU	NBDLU	R/W		√		00H
FFFFFA62H	RAM access data buffer H	NBDH	R/W		√	√	0000H
FFFFFA63H	RAM access data buffer HU	NBDHU	R/W		√		00H
FFFFFA64H	DMA source address setting register SL	NBDMSL	R			√	Undefined
FFFFFA66H	DMA source address setting register SH	NBDMSH	R			√	Undefined
FFFFFA68H	DMA destination address setting register DL	NBDMDL	R			√	Undefined
FFFFFA6AH	DMA destination address setting register DH	NBDMDH	R			√	Undefined
FFFFFA70H	RAM address alternate register L	ISL_RAML	R/W			√	0000H
FFFFFA72H	RAM address alternate register H	ISL_RAMH	R/W			√	0000H
FFFFFA74H	ROM address alternate register L	ISL_ROML	R/W			√	0000H
FFFFFA76H	ROM address alternate register H	ISL_ROMH	R/W			√	0000H

3.4.9 Programmable peripheral I/O registers

In the V850E/IA1, the 16 KB area of x0000H to x3FFFH is provided as a programmable peripheral I/O area. In this area, the area between x2000H and x2FFFH is used exclusively for the FCAN controller.

The internal bus of the V850E/IA1 becomes active when the peripheral I/O register area (FFFF000H to FFFFFFFH) or the programmable peripheral I/O register area (xxxxm000H to xxxxnFFFH) is accessed (m = xx00B, n = xx11B). Note that when data is written to the peripheral I/O register area, the written contents is reflected on the peripheral I/O register since peripheral I/O register area is allocated to the last 4 KB of the programmable peripheral I/O register area.

Figure 3-10. Programmable Peripheral I/O Register (Outline)



Caution The CAN message buffer register can allocate address xxxx freely as a programmable peripheral I/O register. But once the address xxxx is set, it cannot be changed.

Remark M = xx00B
N = xx11B

The peripheral area selection control register (BPC) is used for programmable peripheral I/O register area selection.

(1) Peripheral area selection control register (BPC)

This register can be read/written in 16-bit units.

Figure 3-11. Peripheral Area Selection Control Register (BPC)

BPC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
	PA15	0	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	FFFFF064H	0000H

Bit Position	Bit Name	Function
15	PA15	Enables/disables usage of programmable peripheral I/O area PA15: 0 = Disables usage of programmable peripheral I/O area; 1 = Enables usage of programmable peripheral I/O area
13 to 0	PA13 to PA0	Specifies an address in programmable peripheral I/O area (corresponds to A27 to A14, respectively).

A list of the programmable peripheral I/O registers is shown below.

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn804H	CAN message data length register 00	M_DLC00	R/W		√		Undefined
xxxxn805H	CAN message control register 00	M_CTRL00	R/W		√		Undefined
xxxxn806H	CAN message time stamp register 00	M_TIME00	R/W			√	Undefined
xxxxn808H	CAN message data register 000	M_DATA000	R/W		√		Undefined
xxxxn809H	CAN message data register 001	M_DATA001	R/W		√		Undefined
xxxxn80AH	CAN message data register 002	M_DATA002	R/W		√		Undefined
xxxxn80BH	CAN message data register 003	M_DATA003	R/W		√		Undefined
xxxxn80CH	CAN message data register 004	M_DATA004	R/W		√		Undefined
xxxxn80DH	CAN message data register 005	M_DATA005	R/W		√		Undefined
xxxxn80EH	CAN message data register 006	MDATA006	R/W		√		Undefined
xxxxn80FH	CAN message data register 007	M_DATA007	R/W		√		Undefined
xxxxn810H	CAN message ID register L00	M_IDL00	R/W			√	Undefined
xxxxn812H	CAN message ID register H00	M_IDH00	R/W			√	Undefined
xxxxn814H	CAN message configuration register 00	M_CONF00	R/W		√		Undefined
xxxxn815H	CAN message status register 00	M_STAT00	R		√		Undefined
xxxxn816H	CAN status set/cancel register 00	SC_STAT00	W			√	0000H
xxxxn824H	CAN message data length register 01	M_DLC01	R/W		√		Undefined
xxxxn825H	CAN message control register 01	M_CTRL01	R/W		√		Undefined
xxxxn826H	CAN message time stamp register 01	M_TIME01	R/W			√	Undefined
xxxxn828H	CAN message data register 010	M_DATA010	R/W		√		Undefined
xxxxn829H	CAN message data register 011	M_DATA011	R/W		√		Undefined
xxxxn82AH	CAN message data register 012	M_DATA012	R/W		√		Undefined
xxxxn82BH	CAN message data register 013	M_DATA013	R/W		√		Undefined
xxxxn82CH	CAN message data register 014	M_DATA014	R/W		√		Undefined
xxxxn82DH	CAN message data register 015	M_DATA015	R/W		√		Undefined
xxxxn82EH	CAN message data register 016	M_DATA016	R/W		√		Undefined
xxxxn82FH	CAN message data register 017	M_DATA017	R/W		√		Undefined
xxxxn830H	CAN message ID register L01	M_IDL01	R/W			√	Undefined
xxxxn832H	CAN message ID register H01	M_IDH01	R/W			√	Undefined
xxxxn834H	CAN message configuration register 01	M_CONF01	R/W		√		Undefined
xxxxn835H	CAN message status register 01	M_STAT01	R		√		Undefined
xxxxn836H	CAN status set/cancel register 01	SC_STAT01	W			√	0000H
xxxxn844H	CAN message data length register 02	M_DLC02	R/W		√		Undefined
xxxxn845H	CAN message control register 02	M_CTRL02	R/W		√		Undefined
xxxxn846H	CAN message time stamp register 02	M_TIME02	R/W			√	Undefined
xxxxn848H	CAN message data register 020	M_DATA020	R/W		√		Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
Xxxxn849H	CAN message data register 021	M_DATA021	R/W		√		Undefined
xxxxn84AH	CAN message data register 022	M_DATA022	R/W		√		Undefined
Xxxxn84BH	CAN message data register 023	M_DATA023	R/W		√		Undefined
xxxxn84CH	CAN message data register 024	M_DATA024	R/W		√		Undefined
xxxxn84DH	CAN message data register 025	M_DATA025	R/W		√		Undefined
xxxxn84EH	CAN message data register 026	M_DATA026	R/W		√		Undefined
xxxxn84FH	CAN message data register 027	M_DATA027	R/W		√		Undefined
xxxxn850H	CAN message ID register L02	M_IDL02	R/W			√	Undefined
xxxxn852H	CAN message ID register H02	M_IDH02	R/W			√	Undefined
xxxxn854H	CAN message configuration register 02	M_CONF02	R/W		√		Undefined
xxxxn855H	CAN message status register 02	M_STAT02	R		√		Undefined
xxxxn856H	CAN status set/cancel register 02	SC_STAT02	W			√	0000H
xxxxn864H	CAN message data length register 03	M_DLC03	R/W		√		Undefined
xxxxn865H	CAN message control register 03	M_CTRL03	R/W		√		Undefined
xxxxn866H	CAN message time stamp register 03	M_TIME03	R/W			√	Undefined
xxxxn868H	CAN message data register 030	M_DATA030	R/W		√		Undefined
xxxxn869H	CAN message data register 031	M_DATA031	R/W		√		Undefined
xxxxn86AH	CAN message data register 032	M_DATA032	R/W		√		Undefined
xxxxn86BH	CAN message data register 033	M_DATA033	R/W		√		Undefined
xxxxn86CH	CAN message data register 034	M_DATA034	R/W		√		Undefined
xxxxn86DH	CAN message data register 035	M_DATA035	R/W		√		Undefined
xxxxn86EH	CAN message data register 036	M_DATA036	R/W		√		Undefined
xxxxn86FH	CAN message data register 037	M_DATA037	R/W		√		Undefined
xxxxn870H	CAN message ID register L03	M_IDL03	R/W			√	Undefined
xxxxn872H	CAN message ID register H03	M_IDH03	R/W			√	Undefined
xxxxn874H	CAN message configuration register 03	M_CONF03	R/W		√		Undefined
xxxxn875H	CAN message status register 03	M_STAT03	R		√		Undefined
xxxxn876H	CAN status set/cancel register 03	SC_STAT03	W			√	0000H
xxxxn884H	CAN message data length register 04	M_DLC04	R/W		√		Undefined
xxxxn885H	CAN message control register 04	M_CTRL04	R/W		√		Undefined
xxxxn886H	CAN message time stamp register 04	M_TIME04	R/W			√	Undefined
xxxxn888H	CAN message data register 040	M_DATA040	R/W		√		Undefined
xxxxn889H	CAN message data register 041	M_DATA041	R/W		√		Undefined
xxxxn88AH	CAN message data register 042	M_DATA042	R/W		√		Undefined
xxxxn88BH	CAN message data register 043	M_DATA043	R/W		√		Undefined
xxxxn88CH	CAN message data register 044	M_DATA044	R/W		√		Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn88DH	CAN message data register 045	M_DATA045	R/W		√		Undefined
xxxxn88EH	CAN message data register 046	M_DATA046	R/W		√		Undefined
xxxxn88FH	CAN message data register 047	M_DATA047	R/W		√		Undefined
Xxxxn890H	CAN message ID register L04	M_IDL04	R/W			√	Undefined
xxxxn882H	CAN message ID register H04	M_IDH04	R/W			√	Undefined
xxxxn894H	CAN message configuration register 04	M_CONF04	R/W		√		Undefined
xxxxn895H	CAN message status register 04	M_STAT04	R		√		Undefined
xxxxn896H	CAN status set/cancel register 04	M_STAT04	W			√	0000H
xxxxn8A4H	CAN message data length register 05	M_DLC05	R/W		√		Undefined
xxxxn8A5H	CAN message control register 05	M_DTRL05	R/W		√		Undefined
xxxxn8A6H	CAN message time stamp register 05	M_TIME05	R/W			√	Undefined
xxxxn8A8H	CAN message data register 050	M_DATA050	R/W		√		Undefined
xxxxn8A9H	CAN message data register 051	M_DATA051	R/W		√		Undefined
xxxxn8AAH	CAN message data register 052	M_DATA052	R/W		√		Undefined
xxxxn8ABH	CAN message data register 053	M_DATA053	R/W		√		Undefined
xxxxn8ACH	CAN message data register 054	M_DATA054	R/W		√		Undefined
xxxxn8ADH	CAN message data register 055	M_DATA055	R/W		v		Undefined
xxxxn8AEH	CAN message data register 056	M_DATA056	R/W		√		Undefined
xxxxn8AFH	CAN message data register 057	M_DATA057	R/W		√		Undefined
xxxxn8BCH	CAN message ID register L05	M_IDL05	R/W			√	Undefined
xxxxn8B2H	CAN message ID register H05	M_IDH05	R/W			√	Undefined
xxxxn8B4H	CAN message configuration register 05	M_CONF05	R/W		√		Undefined
xxxxn8B5H	CAN message status register 05	M_STAT05	R		√		Undefined
xxxxn8B6H	CAN status set/cancel register 05	SC_STAT05	W			√	0000H
xxxxn8C4H	CAN message data length register 06	M_DLC06	R/W		√		Undefined
xxxxn8C5H	CAN message control register 06	M_DTRL06	R/W		√		Undefined
xxxxn8C6H	CAN message time stamp register 06	M_TIME06	R/W			√	Undefined
xxxxn8C8H	CAN message data register 060	M_DATA060	R/W		√		Undefined
xxxxn8C9H	CAN message data register 061	M_DATA061	R/W		√		Undefined
xxxxn8CAH	CAN message data register 062	M_DATA062	R/W		√		Undefined
xxxxn8CBH	CAN message data register 063	M_DATA063	R/W		√		Undefined
xxxxn8CCH	CAN message data register 064	M_DATA064	R/W		√		Undefined
xxxxn8CDH	CAN message data register 065	M_DATA065	R/W		√		Undefined
xxxxn8CEH	CAN message data register 066	M_DATA066	R/W		√		Undefined
xxxxn8CFH	CAN message data register 067	M_DATA067	R/W		√		Undefined
xxxxn8DCH	CAN message ID register L06	M_IDL06	R/W			√	Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn8D2H	CAN message ID register H06	M_IDH06	R/W			√	Undefined
xxxxn8D4H	CAN message configuration register 06	M_CONF06	R/W		√		Undefined
xxxxn8D5H	CAN message status register 06	M_STAT06	R		√		Undefined
xxxxn8D6H	CAN status set/cancel register 06	SC_STAT06	W			√	0000H
xxxxn8E4H	CAN message data length register 07	M_DLC07	R/W		√		Undefined
xxxxn8E5H	CAN message control register 07	M_CTRL07	R/W		√		Undefined
xxxxn8E6H	CAN message time stamp register 07	M_TIME07	R/W			√	Undefined
xxxxn8E8H	CAN message data register 070	M_DATA070	R/W		√		Undefined
xxxxn8E9H	CAN message data register 071	M_DATA071	R/W		√		Undefined
xxxxn8EAH	CAN message data register 072	M_DATA072	R/W		√		Undefined
xxxxn8EBH	CAN message data register 073	M_DATA073	R/W		√		Undefined
xxxxn8ECH	CAN message data register 074	M_DATA074	R/W		√		Undefined
xxxxn8EDH	CAN message data register 075	M_DATA075	R/W		√		Undefined
xxxxn8EEH	CAN message data register 076	M_DATA076	R/W		√		Undefined
xxxxn8EFH	CAN message data register 077	M_DATA077	R/W		√		Undefined
xxxxn8F0H	CAN message ID register L07	M_IDL07	R/W			√	Undefined
xxxxn8F2H	CAN message ID register H07	M_IDH07	R/W			√	Undefined
xxxxn8F4H	CAN message configuration register 07	M_CONF07	R/W		√		Undefined
xxxxn8F5H	CAN message status register 07	M_STAT07	R		√		Undefined
xxxxn8F6H	CAN status set/cancel register 07	SC_STAT07	W			√	0000H
xxxxn904H	CAN message data length register 08	M_DLC08	R/W		√		Undefined
xxxxn905H	CAN message control register 08	M_CTRL08	R/W		√		Undefined
xxxxn906H	CAN message time stamp register 08	M_TIME08	R/W			√	Undefined
xxxxn908H	CAN message data register 080	M_DATA080	R/W		√		Undefined
xxxxn909H	CAN message data register 081	M_DATA081	R/W		√		Undefined
xxxxn90AH	CAN message data register 082	M_DATA082	R/W		√		Undefined
xxxxn90BH	CAN message data register 083	M_DATA083	R/W		√		Undefined
xxxxn90CH	CAN message data register 084	M_DATA084	R/W		√		Undefined
xxxxn90DH	CAN message data register 085	M_DATA085	R/W		√		Undefined
xxxxn90EH	CAN message data register 086	M_DATA086	R/W		√		Undefined
xxxxn90FH	CAN message data register 087	M_DATA087	R/W		√		Undefined
xxxxn910H	CAN message ID register L08	M_IDL08	R/W			√	Undefined
xxxxn912H	CAN message ID register H08	M_IDH08	R/W			√	Undefined
xxxxn914H	CAN message configuration register 08	M_CONF08	R/W		√		Undefined
xxxxn915H	CAN message status register 08	M_STAT08	R		√		Undefined
xxxxn916H	CAN status set/cancel register 08	SC_STAT08	W			√	0000H

Remark n = 2, 6, A, or E

(5/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn924H	CAN message data length register 09	M_DLC09	R/W		√		Undefined
xxxxn925H	CAN message control register 09	M_CTRL09	R/W		√		Undefined
xxxxn926H	CAN message time stamp register 09	M_TIME09	R/W			√	Undefined
xxxxn928H	CAN message data register 090	M_DATA090	R/W		√		Undefined
xxxxn929H	CAN message data register 091	M_DATA091	R/W		√		Undefined
xxxxn92AH	CAN message data register 092	M_DATA092	R/W		√		Undefined
xxxxn92BH	CAN message data register 093	M_DATA093	R/W		√		Undefined
xxxxn92CH	CAN message data register 094	M_DATA094	R/W		√		Undefined
xxxxn92DH	CAN message data register 095	M_DATA095	R/W		√		Undefined
xxxxn92EH	CAN message data register 096	M_DATA096	R/W		√		Undefined
xxxxn92FH	CAN message data register 097	M_DATA097	R/W		√		Undefined
xxxxn930H	CAN message ID register L09	M_IDL09	R/W			√	Undefined
xxxxn932H	CAN message ID register H09	M_IDH09	R/W			√	Undefined
xxxxn934H	CAN message configuration register 09	M_CONF09	R/W		√		Undefined
xxxxn935H	CAN message status register 09	M_STAT09	R		√		Undefined
xxxxn936H	CAN status set/cancel register 09	SC_STAT09	W			√	0000H
xxxxn944H	CAN message data length register 10	M_DLC10	R/W		√		Undefined
xxxxn945H	CAN message control register 10	M_CTRL10	R/W		√		Undefined
xxxxn946H	CAN message time stamp register 10	M_TIME10	R/W			√	Undefined
xxxxn948H	CAN message data register 100	M_DATA100	R/W		√		Undefined
xxxxn949H	CAN message data register 101	M_DATA101	R/W		√		Undefined
xxxxn94AH	CAN message data register 102	M_DATA102	R/W		√		Undefined
xxxxn94BH	CAN message data register 103	M_DATA103	R/W		√		Undefined
xxxxn94CH	CAN message data register 104	M_DATA104	R/W		√		Undefined
xxxxn94DH	CAN message data register 105	M_DATA105	R/W		√		Undefined
xxxxn94EH	CAN message data register 106	M_DATA106	R/W		√		Undefined
xxxxn94FH	CAN message data register 107	M_DATA107	R/W		√		Undefined
xxxxn950H	CAN message ID register L10	M_IDL10	R/W			√	Undefined
xxxxn952H	CAN message ID register H10	M_IDH10	R/W			√	Undefined
xxxxn954H	CAN message configuration register 10	M_CONF10	R/W		√		Undefined
xxxxn955H	CAN message status register 10	M_STAT10	R		√		Undefined
xxxxn956H	CAN status set/cancel register 10	SC_STAT10	W			√	0000H
xxxxn964H	CAN message data length register 11	M_DLC11	R/W		√		Undefined
xxxxn965H	CAN message control register 11	M_CTRL11	R/W		√		Undefined
xxxxn966H	CAN message time stamp register 11	M_TIME11	R/W			√	Undefined
xxxxn968H	CAN message data register 110	M_DATA110	R/W		√		Undefined

Remark n = 2, 6, A, or E

(6/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn969H	CAN message data register 111	M_DATA111	R/W		√		Undefined
xxxxn96AH	CAN message data register 112	M_DATA112	R/W		√		Undefined
xxxxn96BH	CAN message data register 113	M_DATA113	R/W		√		Undefined
xxxxn96CH	CAN message data register 114	M_DATA114	R/W		√		Undefined
xxxxn96DH	CAN message data register 115	M_DATA115	R/W		√		Undefined
xxxxn96EH	CAN message data register 116	M_DATA116	R/W		√		Undefined
xxxxn96FH	CAN message data register 117	M_DATA117	R/W		√		Undefined
xxxxn970H	CAN message ID register L11	M_IDL11	R/W			√	Undefined
xxxxn972H	CAN message ID register H11	M_IDH11	R/W			√	Undefined
xxxxn974H	CAN message configuration register 11	M_CONF11	R/W		√		Undefined
xxxxn975H	CAN message status register 11	M_STAT11	R		√		Undefined
xxxxn976H	CAN status set/cancel register 11	SC_STAT11	W			√	0000H
xxxxn984H	CAN message data length register 12	M_DLC12	R/W		√		Undefined
xxxxn985H	CAN message control register 12	M_CTRL12	R/W		√		Undefined
xxxxn986H	CAN message time stamp register 12	M_TIME12	R/W			√	Undefined
xxxxn988H	CAN message data register 120	M_DATA120	R/W		√		Undefined
xxxxn989H	CAN message data register 121	M_DATA121	R/W		√		Undefined
xxxxn98AH	CAN message data register 122	M_DATA122	R/W		√		Undefined
xxxxn98BH	CAN message data register 123	M_DATA123	R/W		√		Undefined
xxxxn98CH	CAN message data register 124	M_DATA124	R/W		√		Undefined
xxxxn98DH	CAN message data register 125	M_DATA125	R/W		√		Undefined
xxxxn98EH	CAN message data register 126	M_DATA126	R/W		√		Undefined
xxxxn98FH	CAN message data register 127	M_DATA127	R/W		√		Undefined
xxxxn990H	CAN message ID register L12	M_IDL12	R/W			√	Undefined
xxxxn992H	CAN message ID register H12	M_IDH12	R/W			√	Undefined
xxxxn994H	CAN message configuration register 12	M_CONF12	R/W		√		Undefined
xxxxn995H	CAN message status register 12	M_STAT12	R		√		Undefined
xxxxn996H	CAN status set/cancel register 12	SC_STAT12	W			√	0000H
xxxxn9A4H	CAN message data length register 13	M_DLC13	R/W		√		Undefined
xxxxn9A5H	CAN message control register 13	M_CTRL13	R/W		√		Undefined
xxxxn9A6H	CAN message time stamp register 13	M_TIME13	R/W			√	Undefined
xxxxn9A8H	CAN message data register 130	M_DATA130	R/W		√		Undefined
xxxxn9A9H	CAN message data register 131	M_DATA131	R/W		√		Undefined
xxxxn9AAH	CAN message data register 132	M_DATA132	R/W		√		Undefined
xxxxn9ABH	CAN message data register 133	M_DATA133	R/W		√		Undefined
xxxxn9ACH	CAN message data register 134	M_DATA134	R/W		√		Undefined

Remark n = 2, 6, A, or E

(7/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn9ADH	CAN message data register 135	M_DATA135	R/W		√		Undefined
xxxxn9AEH	CAN message data register 136	M_DATA136	R/W		√		Undefined
xxxxn9AFH	CAN message data register 137	M_DATA137	R/W		√		Undefined
xxxxn9B0H	CAN message ID register L13	M_IDL13	R/W			√	Undefined
xxxxn9B2H	CAN message ID register H13	M_IDH13	R/W			√	Undefined
xxxxn9B4H	CAN message configuration register 13	M_CONF13	R/W		√		Undefined
xxxxn9B5H	CAN message status register 13	M_STAT13	R		√		Undefined
xxxxn9B6H	CAN status set/cancel register 13	SC_STAT13	W			√	0000H
xxxxn9C4H	CAN message data length register 14	M_DLC14	R/W		√		Undefined
xxxxn9C5H	CAN message control register 14	M_CTRL14	R/W		√		Undefined
xxxxn9C6H	CAN message time stamp register 14	M_TIME14	R/W			√	Undefined
xxxxn9C8H	CAN message data register 140	M_DATA140	R/W		√		Undefined
xxxxn9C9H	CAN message data register 141	M_DATA141	R/W		√		Undefined
xxxxn9CAH	CAN message data register 142	M_DATA142	R/W		√		Undefined
xxxxn9CBH	CAN message data register 143	M_DATA143	R/W		√		Undefined
xxxxn9CCH	CAN message data register 144	M_DATA144	R/W		√		Undefined
xxxxn9CDH	CAN message data register 145	M_DATA145	R/W		√		Undefined
xxxxn9CEH	CAN message data register 146	M_DATA146	R/W		√		Undefined
xxxxn9CFH	CAN message data register 147	M_DATA147	R/W		√		Undefined
xxxxn9D0H	CAN message ID register L14	M_IDL14	R/W			√	Undefined
xxxxn9D2H	CAN message ID register H14	M_IDH14	R/W			√	Undefined
xxxxn9D4H	CAN message configuration register 14	M_CONF14	R/W		√		Undefined
xxxxn9D5H	CAN message status register 14	M_STAT14	R		√		Undefined
xxxxn9D6H	CAN status set/cancel register 14	SC_STAT14	W			√	0000H
xxxxn9E4H	CAN message data length register 15	M_DLC15	R/W		√		Undefined
Xxxxn9E5H	CAN message control register 15	M_CTRL15	R/W		√		Undefined
Xxxxn9E6H	CAN message time stamp register 15	M_TIME15	R/W			√	Undefined
xxxxn9E8H	CAN message data register 150	M_DATA150	R/W		√		Undefined
xxxxn9E9H	CAN message data register 151	M_DATA151	R/W		√		Undefined
xxxxn9EAH	CAN message data register 152	M_DATA152	R/W		√		Undefined
xxxxn9EBH	CAN message data register 153	M_DATA153	R/W		√		Undefined
xxxxn9ECH	CAN message data register 154	M_DATA154	R/W		√		Undefined
xxxxn9EDH	CAN message data register 155	M_DATA155	R/W		√		Undefined
xxxxn9EEH	CAN message data register 156	M_DATA156	R/W		√		Undefined
xxxxn9EFH	CAN message data register 157	M_DATA157	R/W		√		Undefined
xxxxn9F0H	CAN message ID register L15	M_IDL15	R/W			√	Undefined

Remark n = 2, 6, A, or E

(8/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxn9F2H	CAN message ID register H15	M_IDH15	R/W			√	Undefined
xxxxn9F4H	CAN message configuration register 15	M_CONF15	R/W		√		Undefined
xxxxn9F5H	CAN message status register 15	M_STAT15	R		√		Undefined
xxxxn9F6H	CAN status set/cancel register 15	SC_STAT15	W			√	0000H
xxxxnA04H	CAN message data length register 16	M_DLC16	R/W		√		Undefined
xxxxnA05H	CAN message control register 16	M_CTRL16	R/W		√		Undefined
xxxxnA06H	CAN message time stamp register 16	M_TIME16	R/W			√	Undefined
xxxxnA08H	CAN message data register 160	M_DATA160	R/W		√		Undefined
xxxxnA09H	CAN message data register 161	M_DATA161	R/W		√		Undefined
xxxxnA0AH	CAN message data register 162	M_DATA162	R/W		√		Undefined
xxxxnA0BH	CAN message data register 163	M_DATA163	R/W		√		Undefined
xxxxnA0CH	CAN message data register 164	M_DATA164	R/W		√		Undefined
xxxxnA0DH	CAN message data register 165	M_DATA165	R/W		√		Undefined
xxxxnA0EH	CAN message data register 166	M_DATA166	R/W		√		Undefined
xxxxnA0FH	CAN message data register 167	M_DATA167	R/W		√		Undefined
xxxxnA10H	CAN message ID register L16	M_IDL16	R/W			√	Undefined
xxxxnA12H	CAN message ID register H16	M_IDH16	R/W			√	Undefined
xxxxnA14H	CAN message configuration register 16	M_CONF16	R/W		√		Undefined
xxxxnA15H	CAN message status register 16	M_STAT16	R		√		Undefined
xxxxnA16H	CAN status set/cancel register 16	SC_STAT16	W			√	0000H
xxxxnA24H	CAN message data length register 17	M_DLC17	R/W		√		Undefined
xxxxnA25H	CAN message control register 17	M_CTRL17	R/W		√		Undefined
xxxxnA26H	CAN message time stamp register 17	M_TIME17	R/W			√	Undefined
xxxxnA28H	CAN message data register 170	M_DATA170	R/W		√		Undefined
xxxxnA29H	CAN message data register 171	M_DATA171	R/W		√		Undefined
xxxxnA2AH	CAN message data register 172	M_DATA172	R/W		√		Undefined
xxxxnA2BH	CAN message data register 173	M_DATA173	R/W		√		Undefined
xxxxnA2CH	CAN message data register 174	M_DATA174	R/W		√		Undefined
xxxxnA2DH	CAN message data register 175	M_DATA175	R/W		√		Undefined
xxxxnA2EH	CAN message data register 176	M_DATA176	R/W		√		Undefined
xxxxnA2FH	CAN message data register 177	M_DATA177	R/W		√		Undefined
xxxxnA30H	CAN message ID register L17	M_IDL17	R/W			√	Undefined
xxxxnA32H	CAN message ID register H17	M_IDH17	R/W			√	Undefined
xxxxnA34H	CAN message configuration register 17	M_CONF17	R/W		√		Undefined
xxxxnA35H	CAN message status register 17	M_STAT17	R		√		Undefined
xxxxnA36H	CAN status set/cancel register 17	SC_STAT17	W			√	0000H

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnA44H	CAN message data length register 18	M_DLC18	R/W		√		Undefined
xxxxnA45H	CAN message control register 18	M_CTRL18	R/W		√		Undefined
xxxxnA46H	CAN message time stamp register 18	M_TIME18	R/W			√	Undefined
xxxxnA48H	CAN message data register 180	M_DATA180	R/W		√		Undefined
xxxxnA49H	CAN message data register 181	M_DATA181	R/W		√		Undefined
xxxxnA4AH	CAN message data register 182	M_DATA182	R/W		√		Undefined
xxxxnA4BH	CAN message data register 183	M_DATA183	R/W		√		Undefined
xxxxnA4CH	CAN message data register 184	M_DATA184	R/W		√		Undefined
xxxxnA4DH	CAN message data register 185	M_DATA185	R/W		√		Undefined
xxxxnA4EH	CAN message data register 186	M_DATA186	R/W		√		Undefined
xxxxnA4FH	CAN message data register 187	M_DATA187	R/W		√		Undefined
xxxxnA50H	CAN message ID register L18	M_IDL18	R/W			√	Undefined
xxxxnA52H	CAN message ID register H18	M_IDH18	R/W			√	Undefined
xxxxnA54H	CAN message configuration register 18	M_CONF18	R/W		√		Undefined
xxxxnA55H	CAN message status register 18	M_STAT18	R		√		Undefined
xxxxnA56H	CAN status set/cancel register 18	SC_STAT18	W			√	0000H
xxxxnA64H	CAN message data length register 19	M_DLC19	R/W		√		Undefined
xxxxnA65H	CAN message control register 19	M_CTRL19	R/W		√		Undefined
xxxxnA66H	CAN message time stamp register 19	M_TIME19	R/W			√	Undefined
xxxxnA68H	CAN message data register 190	M_DATA190	R/W		√		Undefined
xxxxnA69H	CAN message data register 191	M_DATA191	R/W		√		Undefined
xxxxnA6AH	CAN message data register 192	M_DATA192	R/W		√		Undefined
xxxxnA6BH	CAN message data register 193	M_DATA193	R/W		√		Undefined
xxxxnA6CH	CAN message data register 194	M_DATA194	R/W		√		Undefined
xxxxnA6DH	CAN message data register 195	M_DATA195	R/W		√		Undefined
xxxxnA6EH	CAN message data register 196	M_DATA196	R/W		√		Undefined
xxxxnA6FH	CAN message data register 197	M_DATA197	R/W		√		Undefined
xxxxnA70H	CAN message ID register L19	M_IDL19	R/W			√	Undefined
xxxxnA72H	CAN message ID register H19	M_IDH19	R/W			√	Undefined
xxxxnA74H	CAN message configuration register 19	M_CONF19	R/W		√		Undefined
xxxxnA75H	CAN message status register 19	M_STAT19	R		√		Undefined
xxxxnA76H	CAN status set/cancel register 19	SC_STAT19	W			√	0000H
xxxxnA84H	CAN message data length register 20	M_DLC20	R/W		√		Undefined
xxxxnA85H	CAN message control register 20	M_CTRL20	R/W		√		Undefined
xxxxnA86H	CAN message time stamp register 20	M_TIME20	R/W			√	Undefined
xxxxnA88H	CAN message data register 200	M_DATA200	R/W		√		Undefined

Remark n = 2, 6, A, or E

(10/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnA89H	CAN message data register 201	M_DATA201	R/W		√		Undefined
xxxxnA8AH	CAN message data register 202	M_DATA202	R/W		√		Undefined
xxxxnA8BH	CAN message data register 203	M_DATA203	R/W		√		Undefined
xxxxnA8CH	CAN message data register 204	M_DATA204	R/W		√		Undefined
xxxxnA8DH	CAN message data register 205	M_DATA205	R/W		√		Undefined
xxxxnA8EH	CAN message data register 206	M_DATA206	R/W		√		Undefined
xxxxnA8FH	CAN message data register 207	M_DATA207	R/W		√		Undefined
xxxxnA90H	CAN message ID register L20	M_IDL20	R/W			√	Undefined
xxxxnA92H	CAN message ID register H20	M_IDH20	R/W			√	Undefined
xxxxnA94H	CAN message configuration register 20	M_CONF20	R/W		√		Undefined
xxxxnA95H	CAN message status register 20	M_STAT20	R		√		Undefined
xxxxnA96H	CAN status set/cancel register 20	SC_STAT20	W			√	0000H
xxxxnAA4H	CAN message data length register 21	M_DLC21	R/W		√		Undefined
xxxxnAA5H	CAN message control register 21	M_CTRL21	R/W		√		Undefined
xxxxnAA6H	CAN message time stamp register 21	M_TIME21	R/W			√	Undefined
xxxxnAA8H	CAN message data register 210	M_DATA210	R/W		√		Undefined
xxxxnAA9H	CAN message data register 211	M_DATA211	R/W		√		Undefined
xxxxnAAAH	CAN message data register 212	M_DATA212	R/W		√		Undefined
xxxxnAABH	CAN message data register 213	M_DATA213	R/W		√		Undefined
xxxxnAACH	CAN message data register 214	M_DATA214	R/W		√		Undefined
xxxxnAADH	CAN message data register 215	M_DATA215	R/W		√		Undefined
xxxxnAAEH	CAN message data register 216	M_DATA216	R/W		√		Undefined
xxxxnAAFH	CAN message data register 217	M_DATA217	R/W		√		Undefined
xxxxnAB0H	CAN message ID register L21	M_IDL21	R/W			√	Undefined
xxxxnAB2H	CAN message ID register H21	M_IDH21	R/W			√	Undefined
xxxxnAB4H	CAN message configuration register 21	M_CONF21	R/W		√		Undefined
xxxxnAB5H	CAN message status register 21	M_STAT21	R		√		Undefined
xxxxnAB6H	CAN status set/cancel register 21	SC_STAT21	W			√	0000H
xxxxnAC4H	CAN message data length register 22	M_DLC22	R/W		√		Undefined
xxxxnAC5H	CAN message control register 22	M_CTRL22	R/W		√		Undefined
xxxxnAC6H	CAN message time stamp register 22	M_TIME22	R/W			√	Undefined
xxxxnAC8H	CAN message data register 220	M_DATA220	R/W		√		Undefined
xxxxnAC9H	CAN message data register 221	M_DATA221	R/W		√		Undefined
xxxxnACAH	CAN message data register 222	M_DATA222	R/W		√		Undefined
xxxxnACBH	CAN message data register 223	M_DATA223	R/W		√		Undefined
xxxxnACCH	CAN message data register 224	M_DATA224	R/W		√		Undefined

Remark n = 2, 6, A, or E

(11/15)

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnACDH	CAN message data register 225	M_DATA225	R/W		√		Undefined
xxxxnACEH	CAN message data register 226	M_DATA226	R/W		√		Undefined
xxxxnACFH	CAN message data register 227	M_DATA227	R/W		√		Undefined
xxxxnAD0H	CAN message ID register L22	M_IDL22	R/W			√	Undefined
xxxxnAD2H	CAN message ID register H22	M_IDH22	R/W			√	Undefined
xxxxnAD4H	CAN message configuration register 22	M_CONF22	R/W		√		Undefined
xxxxnAD5H	CAN message status register 22	M_STAT22	R		√		Undefined
xxxxnAD6H	CAN status set/cancel register 22	SC_STAT22	W			√	0000H
xxxxnAE4H	CAN message data length register 23	M_DLC23	R/W		√		Undefined
xxxxnAE5H	CAN message control register 23	M_CTRL23	R/W		√		Undefined
xxxxnAE6H	CAN message time stamp register 23	M_TIME23	R/W			√	Undefined
xxxxnAE8H	CAN message data register 230	M_DATA230	R/W		√		Undefined
xxxxnAE9H	CAN message data register 231	M_DATA231	R/W		√		Undefined
xxxxnAEAH	CAN message data register 232	M_DATA232	R/W		√		Undefined
xxxxnAEBH	CAN message data register 233	M_DATA233	R/W		√		Undefined
xxxxnAECH	CAN message data register 234	M_DATA234	R/W		√		Undefined
xxxxnAEDH	CAN message data register 235	M_DATA235	R/W		√		Undefined
xxxxnAEEH	CAN message data register 236	M_DATA236	R/W		√		Undefined
xxxxnAEFH	CAN message data register 237	M_DATA237	R/W		√		Undefined
xxxxnAF0H	CAN message ID register L23	M_IDL23	R/W			√	Undefined
xxxxnAF2H	CAN message ID register H23	M_IDH23	R/W			√	Undefined
xxxxnAF4H	CAN message configuration register 23	M_CONF23	R/W		√		Undefined
xxxxnAF5H	CAN message status register 23	M_STAT23	R		√		Undefined
xxxxnAF6H	CAN status set/cancel register 23	SC_STAT23	W			√	0000H
xxxxnB04H	CAN message data length register 24	M_DLC24	R/W		√		Undefined
xxxxnB05H	CAN message control register 24	M_CTRL24	R/W		√		Undefined
xxxxnB06H	CAN message time stamp register 24	M_TIME24	R/W			√	Undefined
xxxxnB08H	CAN message data register 240	M_DATA240	R/W		√		Undefined
xxxxnB09H	CAN message data register 241	M_DATA241	R/W		√		Undefined
xxxxnB0AH	CAN message data register 242	M_DATA242	R/W		√		Undefined
xxxxnB0BH	CAN message data register 243	M_DATA243	R/W		√		Undefined
xxxxnB0CH	CAN message data register 244	M_DATA244	R/W		√		Undefined
xxxxnB0DH	CAN message data register 245	M_DATA245	R/W		√		Undefined
xxxxnB0EH	CAN message data register 246	M_DATA246	R/W		√		Undefined
xxxxnB0FH	CAN message data register 247	M_DATA247	R/W		√		Undefined
xxxxnB10H	CAN message ID register L24	M_IDL24	R/W			√	Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnB12H	CAN message ID register H24	M_IDH24	R/W			√	Undefined
xxxxnB14H	CAN message configuration register 24	M_CONF24	R/W		√		Undefined
xxxxnB15H	CAN message status register 24	M_STAT24	R		√		Undefined
xxxxnB16H	CAN status set/cancel register 24	SC_STAT24	W			√	0000H
xxxxnB24H	CAN message data length register 25	M_DLC25	R/W		√		Undefined
xxxxnB25H	CAN message control register 25	M_CTRL25	R/W		√		Undefined
xxxxnB26H	CAN message time stamp register 25	M_TIME25	R/W			√	Undefined
xxxxnB28H	CAN message data register 250	M_DATA250	R/W		√		Undefined
xxxxnB29H	CAN message data register 251	M_DATA251	R/W		√		Undefined
xxxxnB2AH	CAN message data register 252	M_DATA252	R/W		√		Undefined
xxxxnB2BH	CAN message data register 253	M_DATA253	R/W		√		Undefined
xxxxnB2CH	CAN message data register 254	M_DATA254	R/W		√		Undefined
xxxxnB2DH	CAN message data register 255	M_DATA255	R/W		√		Undefined
xxxxnB2EH	CAN message data register 256	M_DATA256	R/W		√		Undefined
xxxxnB2FH	CAN message data register 257	M_DATA257	R/W		√		Undefined
xxxxnB30H	CAN message ID register L25	M_IDL25	R/W			√	Undefined
xxxxnB32H	CAN message ID register H25	M_IDH25	R/W			√	Undefined
xxxxnB34H	CAN message configuration register 25	M_CONF25	R/W		√		Undefined
xxxxnB35H	CAN message status register 25	M_STAT25	R		√		Undefined
xxxxnB36H	CAN status set/cancel register 25	SC_STAT25	W			√	0000H
xxxxnB44H	CAN message data length register 26	M_DLC26	R/W		√		Undefined
xxxxnB45H	CAN message control register 26	M_CTRL26	R/W		√		Undefined
xxxxnB46H	CAN message time stamp register 26	M_TIME26	R/W			√	Undefined
xxxxnB48H	CAN message data register 260	M_DATA260	R/W		√		Undefined
xxxxnB49H	CAN message data register 261	M_DATA261	R/W		√		Undefined
xxxxnB4AH	CAN message data register 262	M_DATA262	R/W		√		Undefined
xxxxnB4BH	CAN message data register 263	M_DATA263	R/W		√		Undefined
xxxxnB4CH	CAN message data register 264	M_DATA264	R/W		√		Undefined
xxxxnB4DH	CAN message data register 265	M_DATA265	R/W		√		Undefined
xxxxnB4EH	CAN message data register 266	M_DATA266	R/W		√		Undefined
xxxxnB4FH	CAN message data register 267	M_DATA267	R/W		√		Undefined
xxxxnB50H	CAN message ID register L26	M_IDL26	R/W			√	Undefined
xxxxnB52H	CAN message ID register H26	M_IDH26	R/W			√	Undefined
xxxxnB54H	CAN message configuration register 26	M_CONF26	R/W		√		Undefined
xxxxnB55H	CAN message status register 26	M_STAT26	R		√		Undefined
xxxxnB56H	CAN status set/cancel register 26	SC_STAT26	W			√	0000H

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnB64H	CAN message data length register 27	M_DLC27	R/W		√		Undefined
xxxxnB65H	CAN message control register 27	M_CTRL27	R/W		√		Undefined
xxxxnB66H	CAN message time stamp register 27	M_TIME27	R/W			√	Undefined
xxxxnB68H	CAN message data register 270	M_DATA270	R/W		√		Undefined
xxxxnB69H	CAN message data register 271	M_DATA271	R/W		√		Undefined
xxxxnB6AH	CAN message data register 272	M_DATA272	R/W		√		Undefined
xxxxnB6BH	CAN message data register 273	M_DATA273	R/W		√		Undefined
xxxxnB6CH	CAN message data register 274	M_DATA274	R/W		√		Undefined
xxxxnB6DH	CAN message data register 275	M_DATA275	R/W		√		Undefined
xxxxnB6EH	CAN message data register 276	M_DATA276	R/W		√		Undefined
xxxxnB6FH	CAN message data register 277	M_DATA277	R/W		√		Undefined
xxxxnB70H	CAN message ID register L27	M_IDL27	R/W			√	Undefined
xxxxnB72H	CAN message ID register H27	M_IDH27	R/W			√	Undefined
xxxxnB74H	CAN message configuration register 27	M_CONF27	R/W		√		Undefined
xxxxnB75H	CAN message status register 27	M_STAT27	R		√		Undefined
xxxxnB76H	CAN status set/cancel register 27	SC_STAT27	W			√	Undefined
xxxxnB84H	CAN message data length register 28	M_DLC28	R/W		√		Undefined
xxxxnB85H	CAN message control register 28	M_CTRL28	R/W		√		Undefined
xxxxnB86H	CAN message time stamp register 28	M_TIME28	R/W			√	Undefined
xxxxnB88H	CAN message data register 280	M_DATA280	R/W		√		Undefined
xxxxnB89H	CAN message data register 281	M_DATA281	R/W		√		Undefined
xxxxnB8AH	CAN message data register 282	M_DATA282	R/W		√		Undefined
xxxxnB8BH	CAN message data register 283	M_DATA283	R/W		√		Undefined
xxxxnB8CH	CAN message data register 284	M_DATA284	R/W		√		Undefined
xxxxnB8DH	CAN message data register 285	M_DATA285	R/W		√		Undefined
xxxxnB8EH	CAN message data register 286	M_DATA286	R/W		√		Undefined
xxxxnB8FH	CAN message data register 287	M_DATA287	R/W		√		Undefined
xxxxnB90H	CAN message ID register L28	M_IDL28	R/W			√	Undefined
xxxxnB92H	CAN message ID register H28	M_IDH28	R/W			√	Undefined
xxxxnB94H	CAN message configuration register 28	M_CONF28	R/W		√		Undefined
xxxxnB95H	CAN message status register 28	M_STAT28	R		√		Undefined
xxxxnB96H	CAN status set/cancel register 28	SC_STAT28	W			√	0000H
xxxxnBA4H	CAN message data length register 29	M_DLC29	R/W		√		Undefined
xxxxnBA5H	CAN message control register 29	M_CTRL29	R/W		√		Undefined
xxxxnBA6H	CAN message time stamp register 29	M_TIME29	R/W			√	Undefined
xxxxnBA8H	CAN message data register 290	M_DATA290	R/W		√		Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnBA9H	CAN message data register 291	M_DATA291	R/W		√		Undefined
xxxxnBAAH	CAN message data register 292	M_DATA292	R/W		√		Undefined
xxxxnBABH	CAN message data register 293	M_DATA293	R/W		√		Undefined
xxxxnBACH	CAN message data register 294	M_DATA294	R/W		√		Undefined
xxxxnBADH	CAN message data register 295	M_DATA295	R/W		√		Undefined
xxxxnBAEH	CAN message data register 296	M_DATA296	R/W		√		Undefined
xxxxnBAFH	CAN message data register 297	M_DATA297	R/W		√		Undefined
xxxxnBB0H	CAN message ID register L29	M_IDL29	R/W			√	Undefined
xxxxnBB2H	CAN message ID register H29	M_IDH29	R/W			√	Undefined
xxxxnBB4H	CAN message configuration register 29	M_CONF29	R/W		√		Undefined
xxxxnBB5H	CAN message status register 29	M_STAT29	R		√		Undefined
xxxxnBB6H	CAN status set/cancel register 29	SC_STAT29	W			√	0000H
xxxxnBC4H	CAN message data length register 30	M_DLC30	R/W		√		Undefined
xxxxnBC5H	CAN message control register 30	M_CTRL30	R/W		√		Undefined
xxxxnBC6H	CAN message time stamp register 30	M_TIME30	R/W			√	Undefined
xxxxnBC8H	CAN message data register 300	M_DATA300	R/W		√		Undefined
xxxxnBC9H	CAN message data register 301	M_DATA301	R/W		√		Undefined
xxxxnBCAH	CAN message data register 302	M_DATA302	R/W		√		Undefined
xxxxnBCBH	CAN message data register 303	M_DATA303	R/W		√		Undefined
xxxxnBCCH	CAN message data register 304	M_DATA304	R/W		√		Undefined
xxxxnBCDH	CAN message data register 305	M_DATA305	R/W		√		Undefined
xxxxnBCEH	CAN message data register 306	M_DATA306	R/W		√		Undefined
xxxxnBCFH	CAN message data register 307	M_DATA307	R/W		√		Undefined
xxxxnBD0H	CAN message ID register L30	M_IDL30	R/W			√	Undefined
xxxxnBD2H	CAN message ID register H30	M_IDH30	R/W			√	Undefined
xxxxnBD4H	CAN message configuration register 30	M_CONF30	R/W		√		Undefined
xxxxnBD5H	CAN message status register 30	M_STAT30	R		√		Undefined
xxxxnBD6H	CAN status set/cancel register 30	SC_STAT30	W			√	0000H
xxxxnBE4H	CAN message data length register 31	M_DLC31	R/W		√		Undefined
xxxxnBE5H	CAN message control register 31	M_CTRL31	R/W		√		Undefined
xxxxnBE6H	CAN message time stamp register 31	M_TIME31	R/W			√	Undefined
xxxxnBE8H	CAN message data register 310	M_DATA310	R/W		√		Undefined
xxxxnBE9H	CAN message data register 311	M_DATA311	R/W		√		Undefined
xxxxnBEAH	CAN message data register 312	M_DATA312	R/W		√		Undefined
xxxxnBEBH	CAN message data register 313	M_DATA313	R/W		√		Undefined
xxxxnBECH	CAN message data register 314	M_DATA314	R/W		√		Undefined

Remark n = 2, 6, A, or E

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation			Initial Value
				1 bit	8 bits	16 bits	
xxxxnBEDH	CAN message data register 315	M_DATA315	R/W		√		Undefined
xxxxnBEEH	CAN message data register 316	M_DATA316	R/W		√		Undefined
xxxxnBEFH	CAN message data register 317	M_DATA317	R/W		√		Undefined
xxxxnBFCH	CAN message ID register L31	M_IDL31	R/W			√	Undefined
xxxxnBF2H	CAN message ID register H31	M_IDH31	R/W			√	Undefined
xxxxnBF4H	CAN message configuration register 31	M_CONF31	R/W		√		Undefined
xxxxnBF5H	CAN message status register 31	M_STAT31	R		√		Undefined
xxxxnBF6H	CAN status set/cancel register 31	SC_STAT31	W			√	0000H
xxxxnC00H	CAN interrupt pending register	CCINTP	R			√	0000H
xxxxnC02H	CAN global interrupt pending register	CGINTP	R/W		√		00H
xxxxnC04H	CAN1 local interrupt pending register	C1INTP	R/W		√		00H
xxxxnC0CH	CAN stop register	CSTOP	R/W			√	0000H
xxxxnC10H	CAN global register Note	CGST	R/W		√	√	0100H
xxxxnC12H	CAN global interrupt enable register Note	CGIE	R/W		√	√	0A00H
xxxxnC14H	CAN main clock select register	CGCS	R/W			√	7F05H
xxxxnC18H	CAN time stop count register	CGTSC	R			√	0000H
xxxxnC1AH	CAN message find start register	CGMSS	W			√	0000H
	CAN message find result register	CGMSR	R			√	0000H
xxxxnC40H	CAN1 address mask register L0	C1MASKL0	R/W			√	Undefined
xxxxnC42H	CAN1 address mask register H0	C1MASKH0	R/W			√	Undefined
xxxxnC44H	CAN1 address mask register L1	C1MASKL1	R/W			√	Undefined
xxxxnC46H	CAN1 address mask register H1	C1MASKH1	R/W			√	Undefined
xxxxnC48H	CAN1 address mask register L2	C1MASKL2	R/W			√	Undefined
xxxxnC4AH	CAN1 address mask register H2	C1MASKH2	R/W			√	Undefined
xxxxnC4CH	CAN1 address mask register L3	C1MASKL3	R/W			√	Undefined
xxxxnC4EH	CAN1 address mask register H3	C1MASKH3	R/W			√	Undefined
xxxxnC50H	CAN1 control register	C1CTRL	R/W			√	0101H
xxxxnC52H	CAN1 definition register Note	C1DEF	R/W		√	√	0000H
xxxxnC54H	CAN1 information register	C1LAST	R			√	00FFH
xxxxnC56H	CAN1 error counter register	C1ERC	R			√	0000H
xxxxnC58H	CAN1 interrupt enable register Note	C1IE	R/W		√	√	0900H
xxxxnC5AH	CAN1 bus active register	C1BA	R			√	00FFH
xxxxnC5CH	CAN1 bit rate prescaler register	C1BRP	R/W			√	0000H
	CAN1 bus diagnostic information register	C1DINF	R			√	0000H
xxxxnC5EH	CAN1 synchronization control register	C1SYNC	R/W			√	0218H

Note This is register can be accessed in 16-bit or 8-bit units during read, and in 16-bit units during write.

Remark n = 2, 6, A, or E

3.4.10 Specific registers

Specific registers are registers that are protected from being written with illegal data due to inadvertent program loop (runaway), etc. The V850E/IA1 has three specific registers, the power save control register (PSC) (refer to **8.5.2 Control registers**), clock control register (CKC) (refer to **8.3.4 Clock control register (CKC)**), and flash programming mode control register (FLPMC).

3.4.11 System wait control register (VSWC)

Set the following values to this register according to the operating frequency used.

This register can be read/written in 8-bit or 1-bit units (address: FFFFF06EH, initial value: 77H).

Operating Frequency (ϕ)	Initial Value of VSWC
4 MHz ≤ ϕ < 25 MHz	11H
25 MHz ≤ ϕ < 33 MHz	12H
33 MHz ≤ ϕ ≤ 50 MHz	14H

3.4.12 Cautions

When using the V850E/IA1, the following registers must be set from the beginning.

- System wait control register (VSWC)
  (See **3.4.11 System wait control register (VSWC)**)
- Clock control register (CKC)
  (See **8.3.4 Clock control register (CKC)**)

After setting VSWC and CKC, set other registers as required.

[MEMO]

CHAPTER 4 BUS CONTROL FUNCTION

The V850E/IA1 is provided with an external bus interface function by which external I/O and memories, such as ROM and RAM, can be connected.

4.1 Features

- 16-bit/8-bit data bus sizing function
- 8-space chip select function
- Wait function
  - Programmable wait function, through which up to 7 wait states can be inserted for each memory block
  - External wait function via $\overline{\text{WAIT}}$ pin
- Idle state insertion function
- Bus mastership arbitration function
- Bus hold function
- External device connection enabled via bus control/port alternate function pins

4.2 Bus Control Pins

The following pins are used for connection to external devices.

Bus Control Pin (Function When in Control Mode)	Function When in Port Mode	Register for Port/Control Mode Switching
Address data bus (AD0 to AD15)	PDL0 to PDL15 (Port DL)	PMCDL
Address bus (A16 to A23)	PDH0 to PDH7 (Port DH)	PMCDH
Chip select ($\overline{\text{CS0}}$ to $\overline{\text{CS7}}$)	PCS0 to PCS7 (Port CS)	PMCCS
Read/write control ($\overline{\text{LWR}}$/$\overline{\text{UWR}}$, $\overline{\text{RD}}$, ASTB)	PCT0, PCT1, PCT4, PCT6 (Port CT)	PMCCT
External wait control ($\overline{\text{WAIT}}$)	PCM0 (Port CM)	PMCCM
Internal system clock (CLKOUT)	PCM1 (Port CM)	
Bus hold control ($\overline{\text{HLDRQ}}$, $\overline{\text{HLDAK}}$)	PCM2, PCM3 (Port CM)	

Remark In the case of single-chip mode 1 and ROM-less modes 0 and 1, when the system is reset, each bus control pin becomes unconditionally valid.

4.2.1 Pin status during internal ROM, internal RAM, and peripheral I/O access

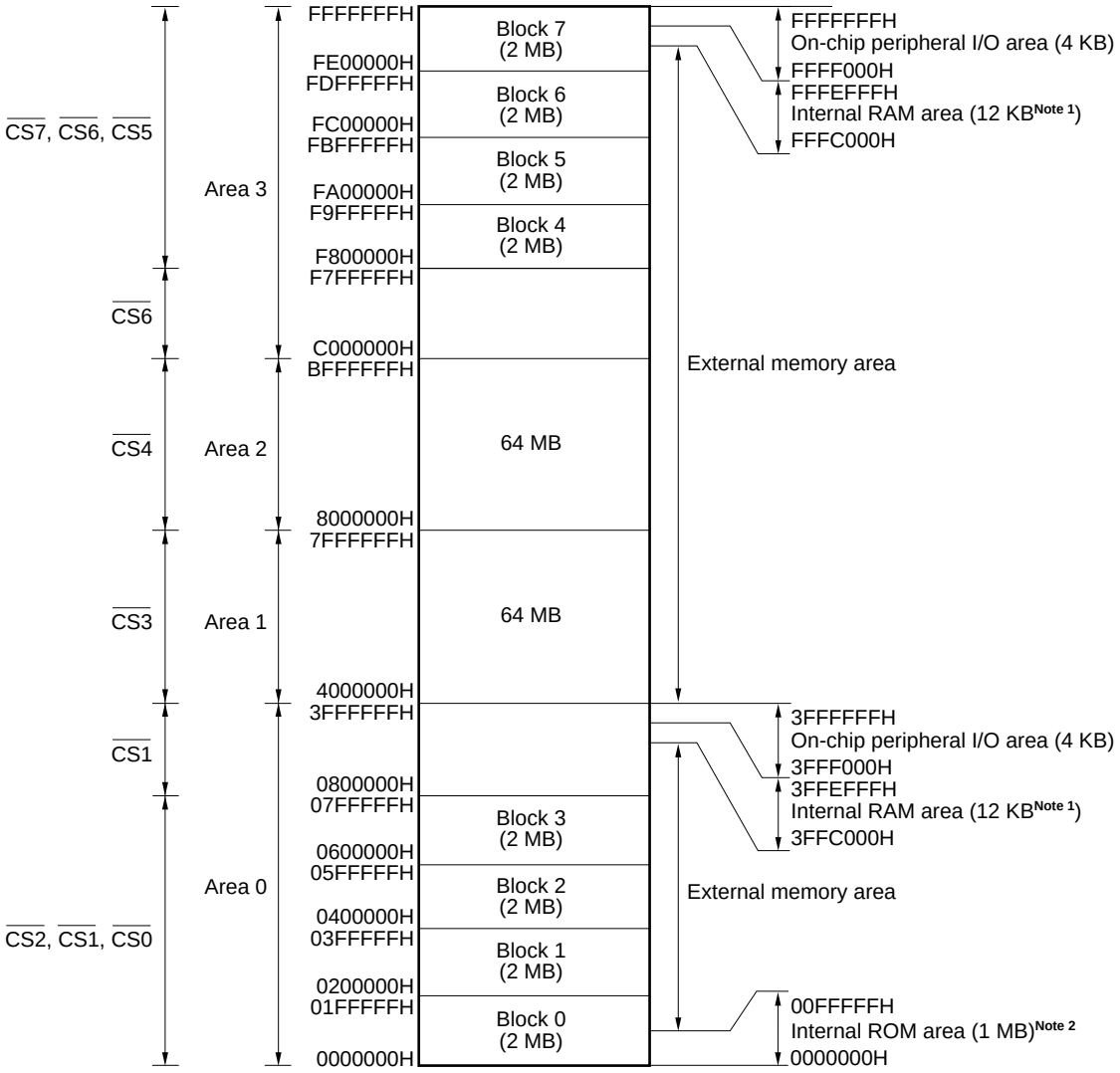
While accessing internal ROM and RAM, the address bus becomes undefined, and the data bus and external bus control signals are not output and enter the high-impedance state.

While accessing peripheral I/O, the address bus outputs the address data of the on-chip peripheral I/O currently being accessed, and the data bus and external bus control signals are not output and enter the high-impedance state.

4.3 Memory Block Function

The 256 MB memory space is divided into memory blocks of 2 MB and 64 MB units. The programmable wait function and bus cycle operation mode can be independently controlled for each block.

The area that can be used as program area is the 64 MB space of addresses 0000000H to 3FFFFFFH.



Notes 1. μPD70F3116: 10 KB
μPD703117: 6 KB

2. When in single-chip mode 1 and ROM-less modes 0 and 1, this becomes an external memory area. When in single-chip mode 1, addresses 0100000H to 01FFFFFH become an internal ROM area.

4.3.1 Chip select control function

Of the 256 MB memory area, the lower 8 MB (0000000H to 07FFFFH) and the higher 8 MB (F800000H to FFFFFFFH) can be divided into 2 MB memory blocks by chip area selection control registers 0 and 1 (CSC0, CSC1) to control the chip select signal.

The memory area can be effectively used by dividing it into memory blocks using the chip select control function. The priority order is described below.

(1) Chip area selection control registers 0, 1 (CSC0, CSC1)

These registers can be read/written in 16-bit units and become valid by setting each bit to 1.

If different chip select signal outputs are set to the same block, the priority order is controlled as follows.

CSC0: Peripheral I/O area: $\overline{CS0}$ > $\overline{CS2}$ > $\overline{CS1}$

CSC1: Peripheral I/O area: $\overline{CS7}$ > $\overline{CS5}$ > $\overline{CS6}$

If both the CS0n and CS2n bits of the CSC0 register are set to 0, $\overline{CS1}$ is output to the corresponding block (n = 0 to 3).

Similarly, if both the CS5n and CS7n bits of the CSC1 register are set to 0, $\overline{CS6}$ is output to the corresponding block (n = 0 to 3).

Figure 4-1. Chip Area Selection Control Registers 0, 1 (CSC0, CSC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CSC0	CS33	CS32	CS31	CS30	CS23	CS22	CS21	CS20	CS13	CS12	CS11	CS10	CS03	CS02	CS01	CS00	FFFFF060H	2C11H
CSC1	CS43	CS42	CS41	CS40	CS53	CS52	CS51	CS50	CS63	CS62	CS61	CS60	CS73	CS72	CS71	CS70	FFFFF062H	2C11H

Bit Position	Bit Name	Function
15 to 0	CSnm (n = 0 to 7) (m = 0 to 3)	Chip select enabled by setting CSnm bit to 1.

CSnm	CS operation
CS00	$\overline{CS0}$ output during block 0 access
CS01	$\overline{CS0}$ output during block 1 access.
CS02	$\overline{CS0}$ output during block 2 access.
CS03	$\overline{CS0}$ output during block 3 access.
CS10 to CS13	**Note 1**
CS20	$\overline{CS2}$ output during block 0 access.
CS21	$\overline{CS2}$ output during block 1 access.
CS22	$\overline{CS2}$ output during block 2 access.
CS23	$\overline{CS2}$ output during block 3 access.
CS30 to CS33	**Note 2**
CS40 to CS43	**Note 3**
CS50	$\overline{CS5}$ output during block 7 access.
CS51	$\overline{CS5}$ output during block 6 access.
CS52	$\overline{CS5}$ output during block 5 access.
CS53	$\overline{CS5}$ output during block 4 access.
CS60 to CS63	**Note 4**
CS70	$\overline{CS7}$ output during block 7 access.
CS71	$\overline{CS7}$ output during block 6 access.
CS72	$\overline{CS7}$ output during block 5 access.
CS73	$\overline{CS7}$ output during block 4 access.

Notes 1. If both the CS0n and CS2n bits have been set to 0, if area 0 is accessed, $\overline{CS1}$ will be output regardless of the setting of the CS1n bit.

2. When area 1 is accessed, $\overline{CS3}$ will be output regardless of the setting of the CS3n bit.

3. When area 2 is accessed, $\overline{CS4}$ will be output regardless of the setting of the CS4n bit.

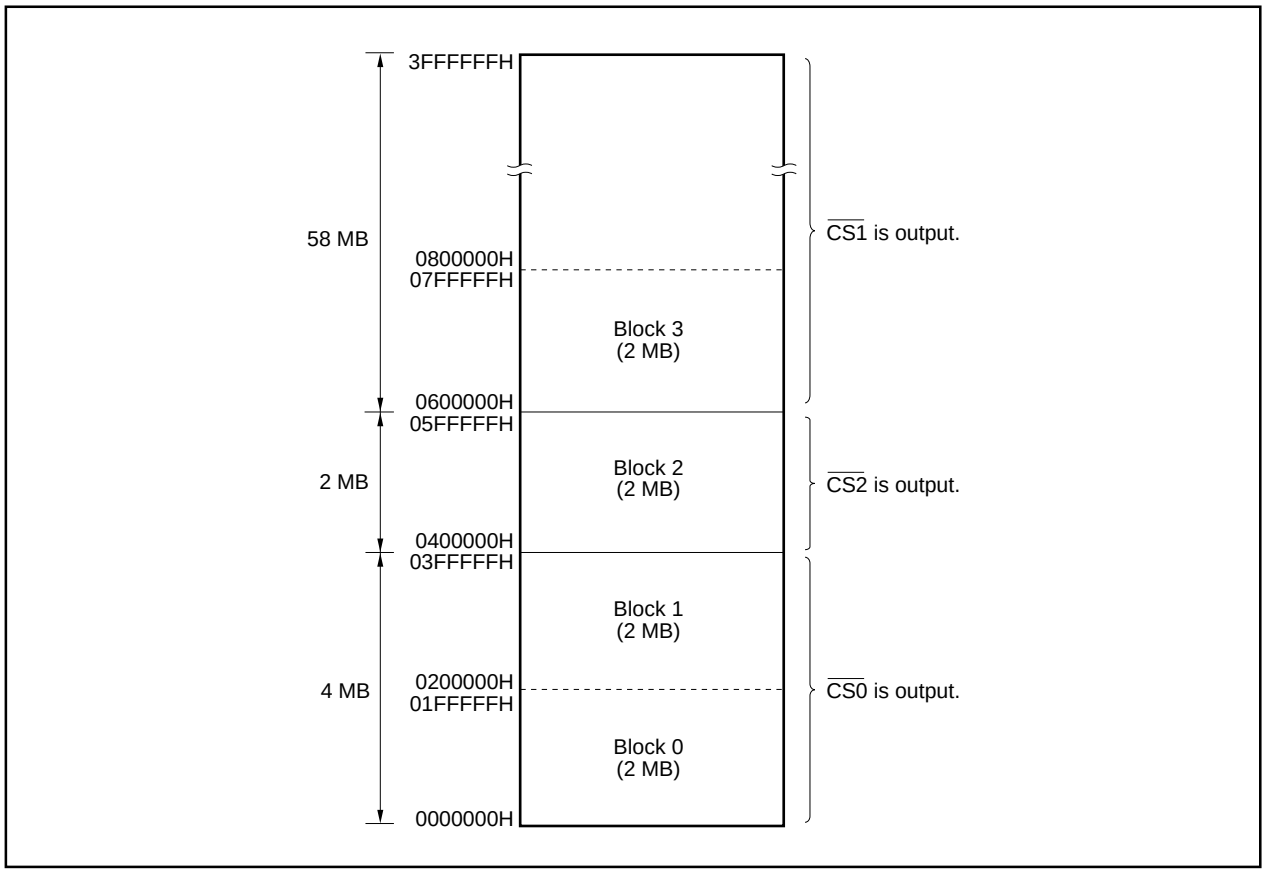
4. If both the CS5n and CS7n bits have been set to 0, if area 3 is accessed, $\overline{CS6}$ will be output regardless of the setting of the CS6n bit.

The following diagram shows the $\overline{CS}$ signal, which is enabled for area 0 when the CSC0 register is set to 0703H.

When the CSC0 register is set to 0703H, $\overline{CS0}$ and $\overline{CS2}$ are output to block 0 and block 1, but since $\overline{CS0}$ has priority over $\overline{CS2}$, $\overline{CS0}$ is output if the addresses of block 0 and block 1 are accessed.

If the address of block 3 is accessed, both the CS03 and CS23 bits of the CSC0 register are 0, and $\overline{CS1}$ is output.

Figure 4-2. Example When CSC0 Register Is Set to 0703H



4.4 Bus Cycle Type Control Function

In the V850E/IA1, the following external devices can be connected directly to each memory block.

- SRAM, external ROM, external I/O

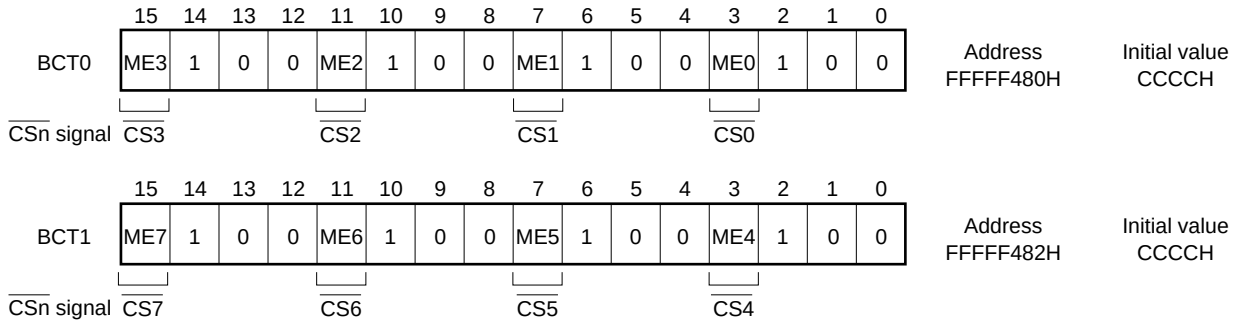
Connected external devices are specified by bus cycle type configuration registers 0, 1 (BCT0, BCT1).

4.4.1 Bus cycle type configuration registers 0, 1 (BCT0, BCT1)

(1) Bus cycle type configuration registers 0, 1 (BCT0, BCT1)

These registers can be read/written in 16-bit units.

Figure 4-3. Bus Cycle Type Configuration Registers 0, 1 (BCT0, BCT1)



Bit Position	Bit Name	Function
15, 11, 7, 3 (BCT0), 15, 11, 7, 3 (BCT1)	MEn (n = 0 to 7)	Sets memory controller operation enable for each chip select.

MEn	Memory controller operation enable
0	Operation disabled
1	Operation enabled

Caution Write to the BCT0 and BCT1 registers after reset, and then do not change the set values. Also, do not access an external memory area other than the one for this initialization routine until the initial setting of the BCT0 and BCT1 registers is complete. However, it is possible to access external memory areas whose initial settings are complete.

4.5 Bus Access

4.5.1 Number of access clocks

The number of basic clocks required to access each resource is shown below.

Bus Cycle Status \ Resource (Bus Width)		Peripheral I/O (Bus Width)				
		Internal ROM (32 Bits)	Internal RAM (32 Bits)	Peripheral I/O (16 Bits)	Programmable Peripheral I/O (16 Bits)	External Memory (16 Bits)
Instruction fetch	Normal access	1	1 Note 1	–	–	2 Note 2
	Branch	2	1	–	–	2 Note 2
	Sequential access	–	–	–	–	1 Note 2
Operand data access	Normal access	5	1	3 Note 2	3 Note 2	2 Note 2
	Sequential access	–	–	–	–	1 Note 2

Notes 1. This value is 2 if there is contention with data access.

2. MIN value

Remarks 1. Unit: Clock/access

2. n: Wait insertion count

4.5.2 Bus sizing function

The bus sizing function controls the data bus width for each CS space. The data bus width is specified by using the bus size configuration register (BSC).

(1) Bus size configuration register (BSC)

This register can be read/written in 16-bit units.

Figure 4-4. Bus Size Configuration Register (BSC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value[Note]
BSC	0	BS70	0	BS60	0	BS50	0	BS40	0	BS30	0	BS20	0	BS10	0	BS00	FFFFF066H	0000H/5555H
$\overline{\text{CS}}$n signal		$\overline{\text{CS7}}$		$\overline{\text{CS6}}$		$\overline{\text{CS5}}$		$\overline{\text{CS4}}$		$\overline{\text{CS3}}$		$\overline{\text{CS2}}$		$\overline{\text{CS1}}$		$\overline{\text{CS0}}$		

Note When in single-chip mode 0, 1: 5555H
When in ROM-less mode 0: 5555H
When in ROM-less mode 1: 0000H

Bit Position	Bit Name	Function
14, 12, 10, 8, 6, 4, 2, 0	BSn0 (n = 0 to 7)	Sets the data bus width of CSn space.

BSn0	Data Bus Width of CSn Space
0	8 bits
1	16 bits

Cautions 1. Write to the BSC register after reset, and then do not change the set values. Also, do not access an external memory area other than the one for this initialization routine until the initial setting of the BSC register is complete. However, it is possible to access external memory areas whose initial settings are complete.

2. When the data bus width is specified as 8 bits, only the signals shown below become active.

$\overline{\text{LWR}}$: When accessing SRAM, external ROM, or external I/O (write cycle)

4.5.3 Endian control function

The endian control function can be used to set processing of word data in memory using the little endian method for CS space selected with a chip select signal ($\overline{\text{CS0}}$ to $\overline{\text{CS7}}$).

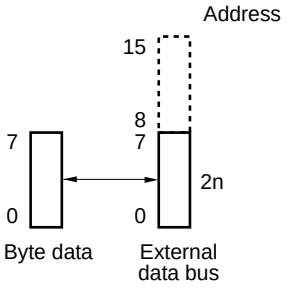
4.5.4 Bus width

The V850E/IA1 accesses peripheral I/O and external memory in 8-bit, 16-bit, or 32-bit units. The following shows the operation for each type of access. Access all data in order starting from the lower side.

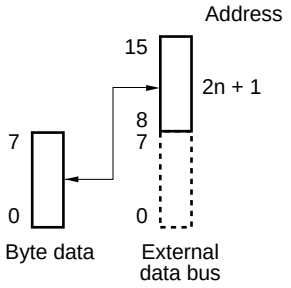
(1) Byte access (8 bits)

(a) When the data bus width is 16 bits (little endian)

<1> Access to even address (2n)

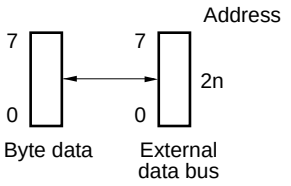


<2> Access to odd address (2n + 1)

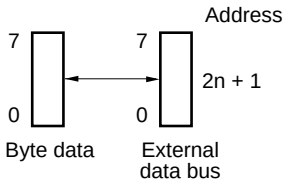


(b) When the data bus width is 8 bits (little endian)

<1> Access to even address (2n)

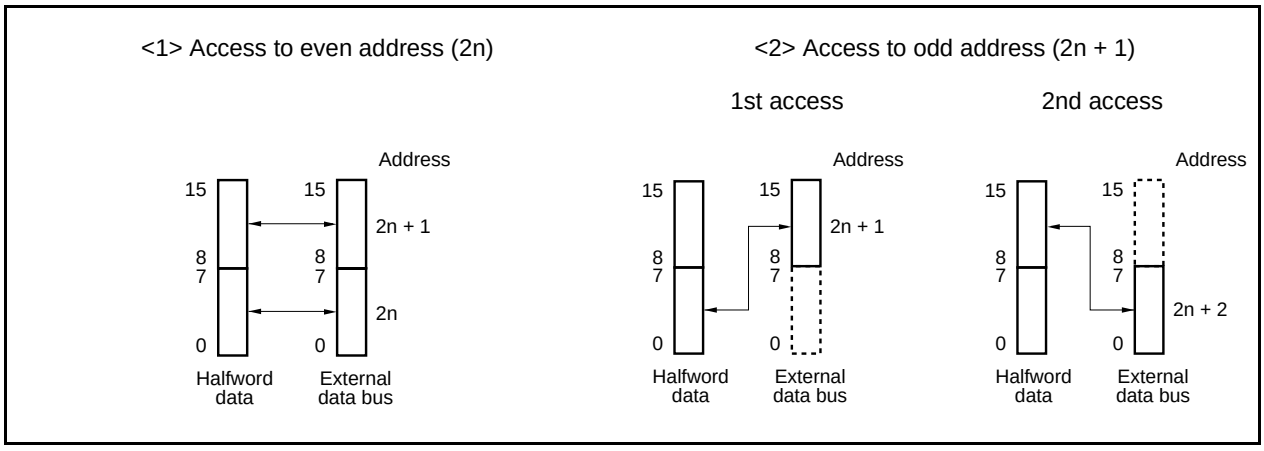


<2> Access to odd address (2n + 1)

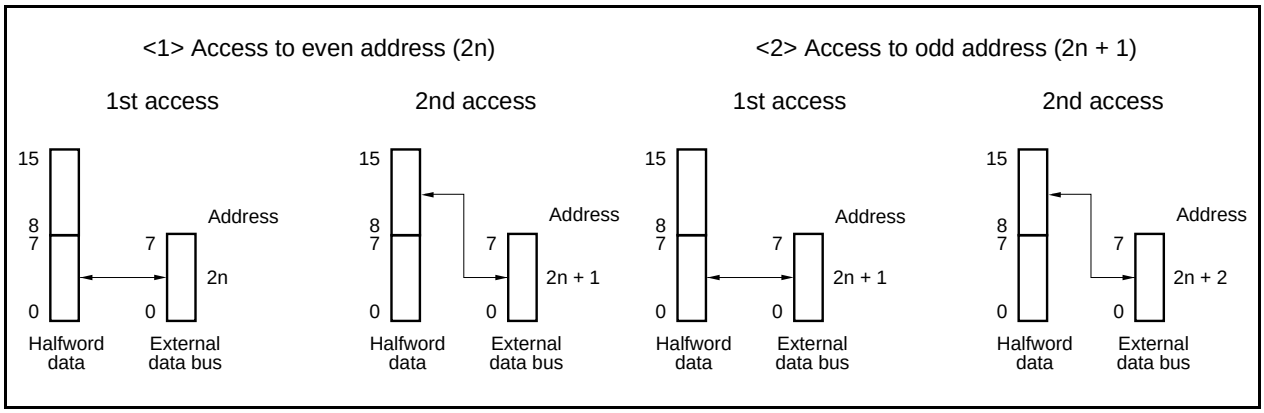


(2) Halfword access (16 bits)

(a) When the bus width is 16 bits (little endian)



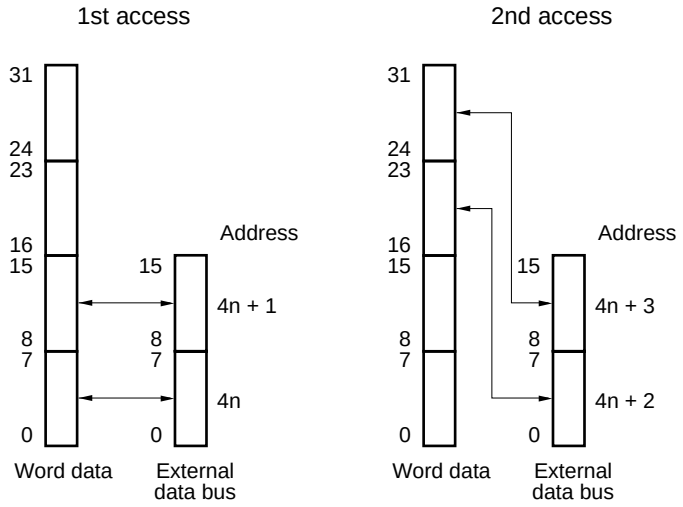
(b) When the data bus width is 8 bits (little endian)



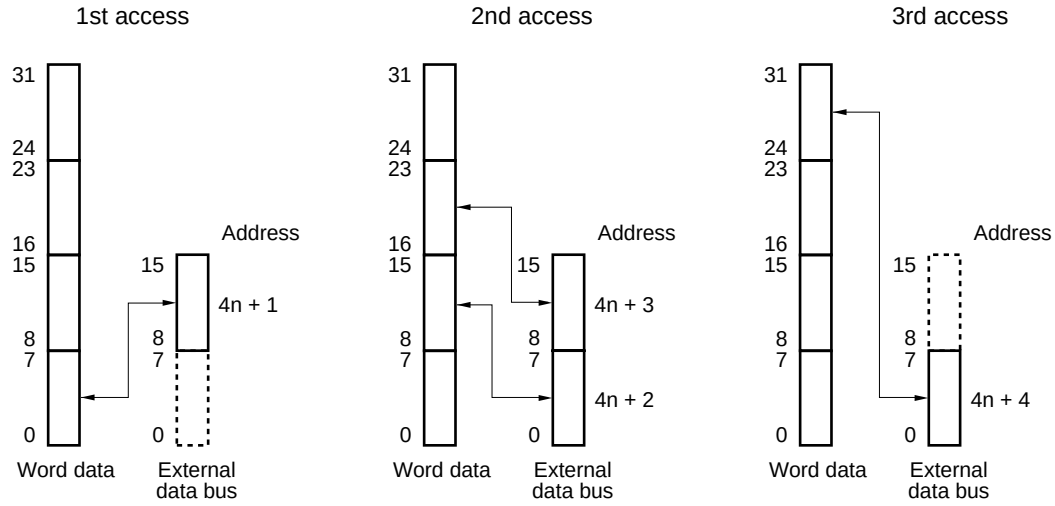
(3) Word access (32 bits)

(a) When the bus width is 16 bits (little endian) (1/2)

<1> Access to address 4n

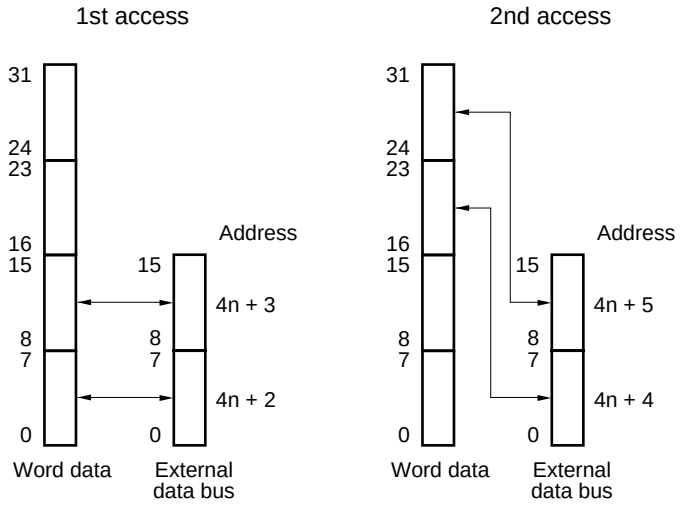


<2> Access to address 4n + 1

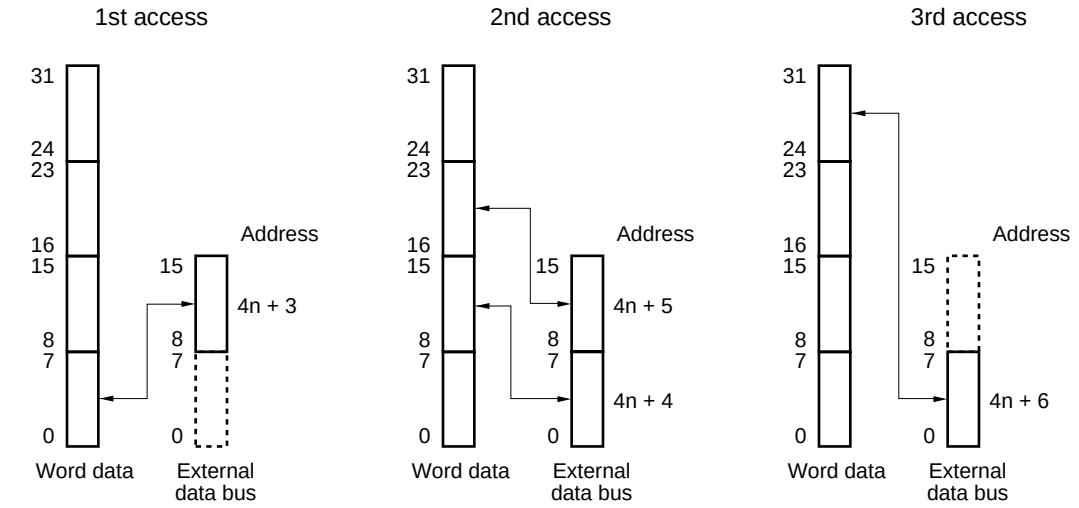


(a) When the bus width is 16 bits (little endian) (2/2)

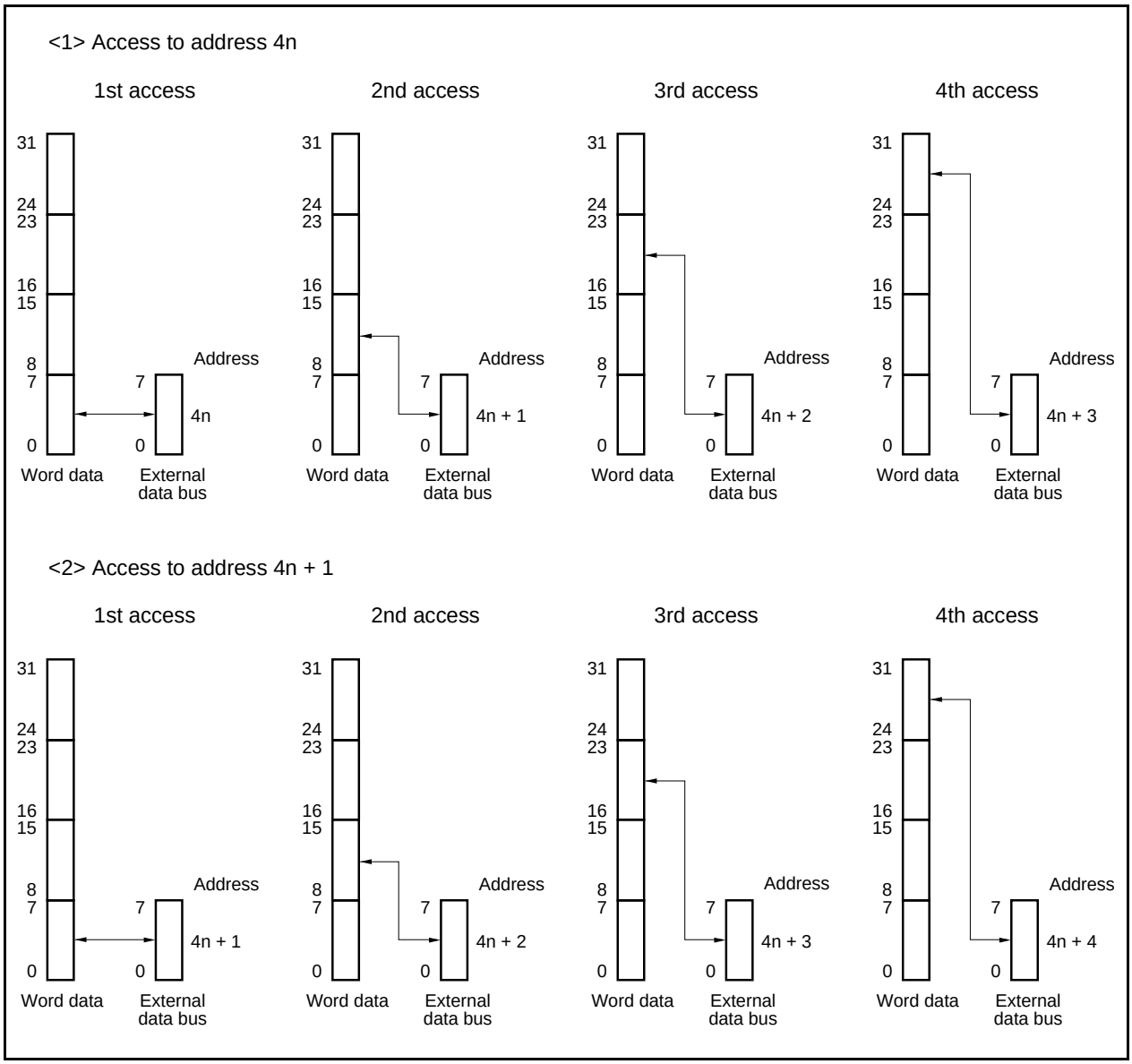
<3> Access to address 4n + 2



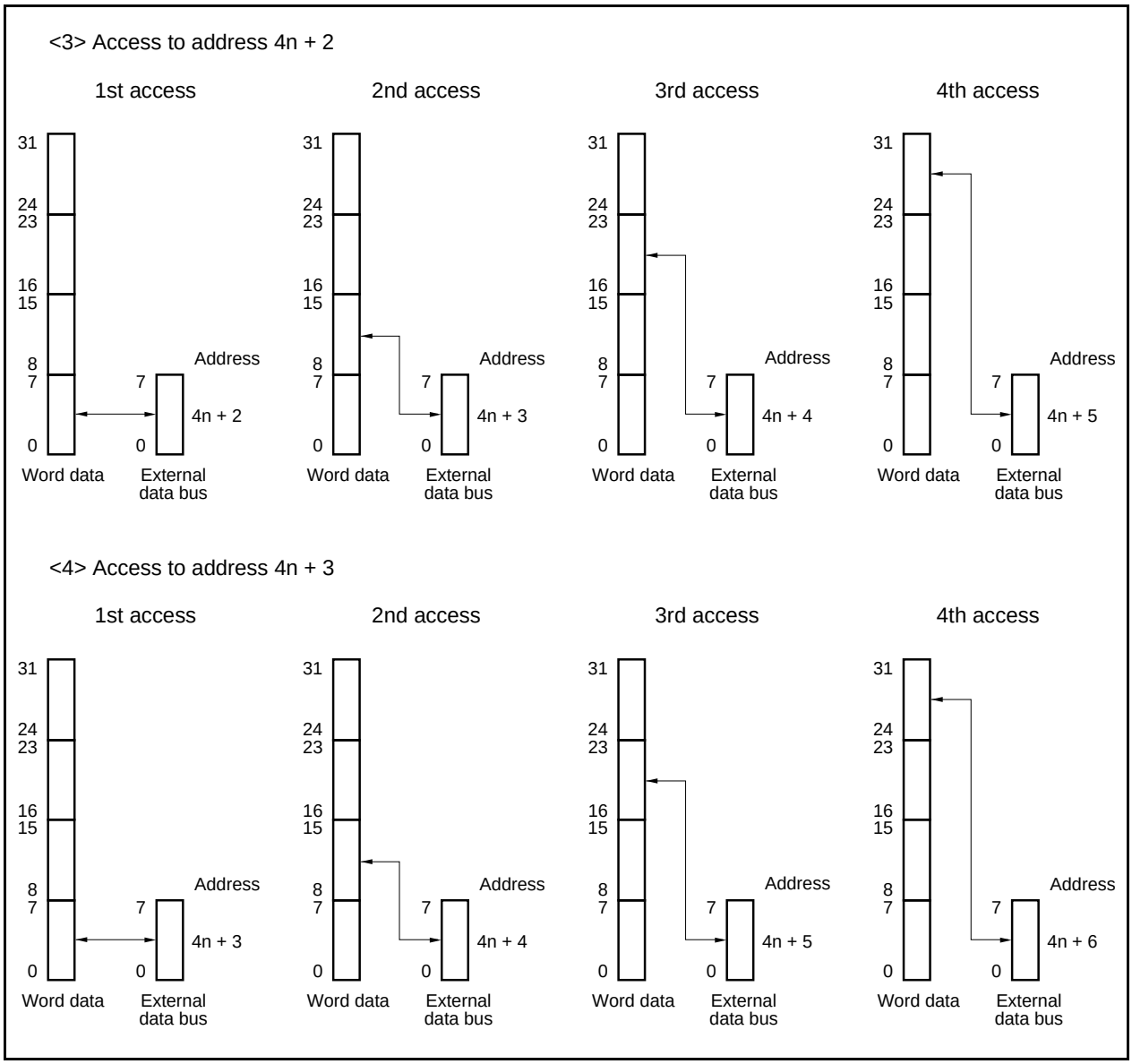
<4> Access to address 4n + 3



(b) When the data bus width is 8 bits (little endian) (1/2)



(b) When the data bus width is 8 bits (little endian) (2/2)



4.6 Wait Function

4.6.1 Programmable wait function

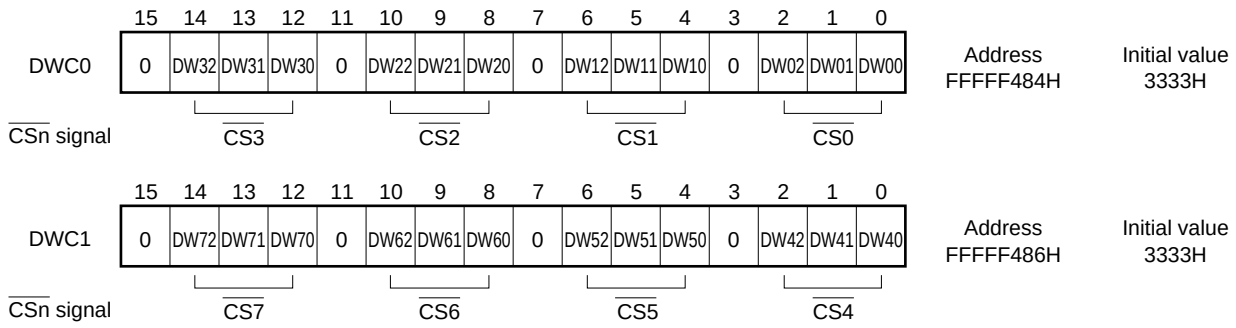
(1) Data wait control registers 0, 1 (DWC0, DWC1)

To facilitate interfacing with low-speed memory or with I/Os, it is possible to insert up to 7 data wait states in the starting bus cycle for each CS space.

The number of wait states can be specified by program using data wait control registers 0 and 1 (DWC0, DWC1). Just after system reset, all blocks have 7 data wait states inserted.

These registers can be read/written in 16-bit units.

Figure 4-5. Data Wait Control Registers 0, 1 (DWC0, DWC1)



Bit Position	Bit Name	Function
14 to 12, 10 to 8, 6 to 4, 2 to 0	DWn2 to DWn0 (n = 0 to 7)	Specifies the number of wait states inserted in the CSn space.

DWn2	DWn1	DWn0	Number of Wait States Inserted in CSn Space
0	0	0	Not inserted
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Cautions 1. The internal ROM area and internal RAM area are not subject to programmable waits and ordinarily no wait access is carried out. The on-chip peripheral I/O area is also not subject to programmable wait states, with wait control performed by each peripheral function only.

2. Write to the DWC0 and DWC1 registers after reset, and then do not change the set values. Also, do not access an external memory area other than the one for this initialization routine until the initial setting of the DWC0 and DWC1 registers is complete. However, it is possible to access external memory areas whose initial settings are complete.

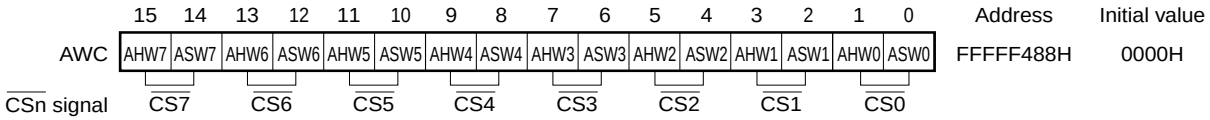
(2) Address wait control register (AWC)

In the V850E/IA1, address setup wait and address hold wait states can be inserted before and after the T1 cycle, respectively.

These wait states can be set for each CS space via the AWC register.

This register can be read/written in 16-bit units.

Figure 4-6. Address Wait Control Register (AWC)



Bit Position	Bit Name	Function
15, 13, 11, 9, 7, 5, 3, 1	AHWn (n = 0 to 7)	Sets the insertion of an address hold wait state in each CSn space after the T1 cycle. 0: Address hold wait state not inserted 1: Address hold wait state inserted
14, 12, 10, 8, 6, 4, 2, 0	ASWn (n = 0 to 7)	Sets the insertion of an address setup wait state in each CSn space before the T1 cycle. 0: Address setup wait state not inserted 1: Address setup wait state inserted

4.6.2 External wait function

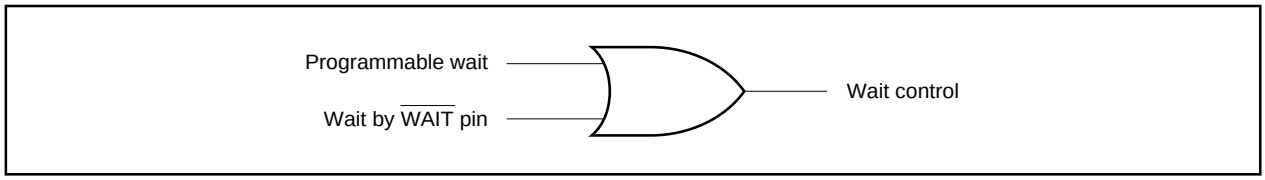
When an extremely slow device, I/O, or asynchronous system is connected, an arbitrary number of wait states can be inserted in the bus cycle by the external wait pin ($\overline{\text{WAIT}}$) for synchronization with the external device.

Just as with programmable waits, accessing internal ROM, internal RAM, and on-chip peripheral I/O areas cannot be controlled by external waits.

The external $\overline{\text{WAIT}}$ signal can be input asynchronously to CLKOUT and is sampled at the falling edge of the clock in the T2 and TW states of a bus cycle. If the setup/hold time in the sampling timing is not satisfied, the wait state may or may not be inserted in the next state.

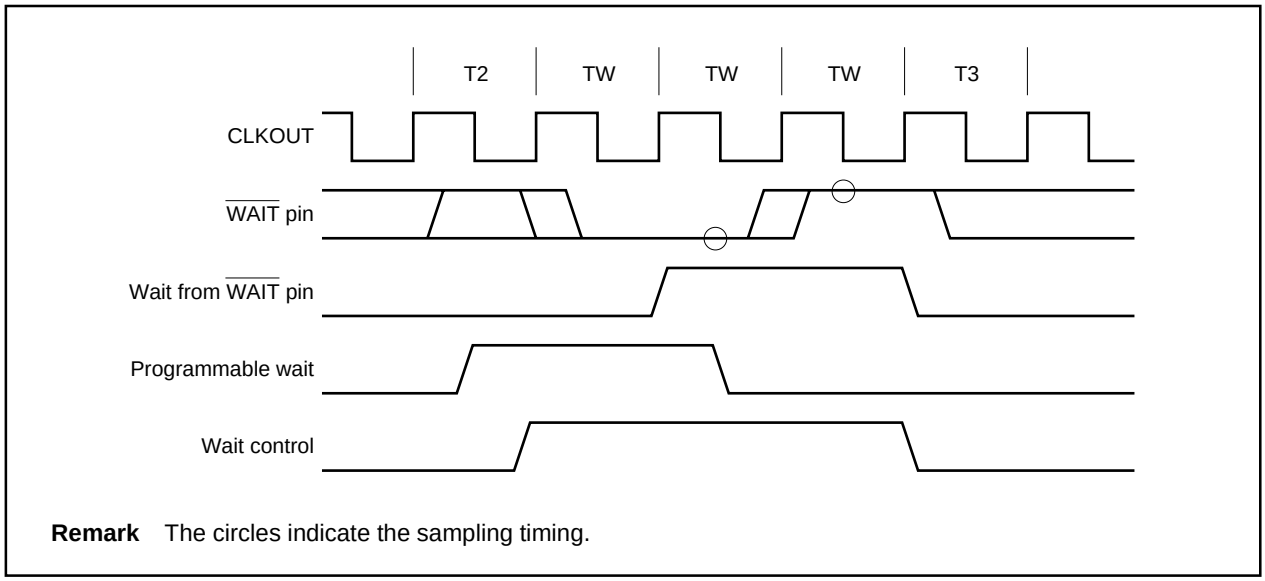
4.6.3 Relationship between programmable wait and external wait

A wait cycle is inserted as the result of an OR operation between the wait cycle specified by the set value of the programmable wait and the wait cycle controlled by the $\overline{\text{WAIT}}$ pin. In other words, the number of wait cycles is determined by the side with the greatest number of cycles.



For example, if the timings of the programmable wait and the $\overline{\text{WAIT}}$ pin signal are as illustrated below, three wait states will be inserted in the bus cycle.

Figure 4-7. Example of Wait Insertion



Remark The circles indicate the sampling timing.

4.7 Idle State Insertion Function

To facilitate interfacing with low-speed memory devices, a set number of idle states (T1) can be inserted into the starting bus cycle after the T3 state to secure the data output float delay time (t_{DF}) of the memory when each CS space is read accessed. The bus cycle following the T3 starts after the inserted idle state(s).

Idle states are inserted at the following timing.

- After the read cycle for SRAM, external I/O, or external ROM.

The idle state insertion setting can be specified using the bus cycle control register (BCC). Idle state insertion is automatically programmed for all memory blocks immediately after a system reset.

(1) Bus cycle control register (BCC)

This register can be read/written in 16-bit units.

Figure 4-8. Bus Cycle Control Register (BCC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
BCC	BC71	0	BC61	0	BC51	0	BC41	0	BC31	0	BC21	0	BC11	0	BC01	0	FFFFF48AH	AAAAH
$\overline{CS}$n signal	$\overline{CS7}$		$\overline{CS6}$		$\overline{CS5}$		$\overline{CS4}$		$\overline{CS3}$		$\overline{CS2}$		$\overline{CS1}$		$\overline{CS0}$			

Bit Position	Bit Name	Function
15, 13, 11, 9, 7, 5, 3, 1	BCn1 (n = 0 to 7)	Specifies the insertion of idle states after the T3 state in each CSn space. 0: Idle state not inserted 1: Idle state inserted

Cautions 1. Idle states cannot be inserted in internal ROM, internal RAM, on-chip peripheral I/O, or programmable peripheral I/O areas.

2. Write to the BCC register after reset, and then do not change the set values. Also, do not access an external memory area other than the one for this initialization routine until the initial setting for this register is complete. However, it is possible to access external memory areas whose initial settings are complete.

4.8 Bus Hold Function

4.8.1 Function outline

If pins PCM2 and PCM3 are specified in the control mode, the $\overline{\text{HLDAK}}$ and $\overline{\text{HLDRQ}}$ functions become valid.

If it is determined that the $\overline{\text{HLDRQ}}$ pin has become active (low level) as a bus mastership request from another bus master, the external address/data bus and each strobe pin are shifted to high impedance and then released (bus hold state). If the $\overline{\text{HLDRQ}}$ pin becomes inactive (high level) and the bus mastership request is canceled, driving of these pins begins again.

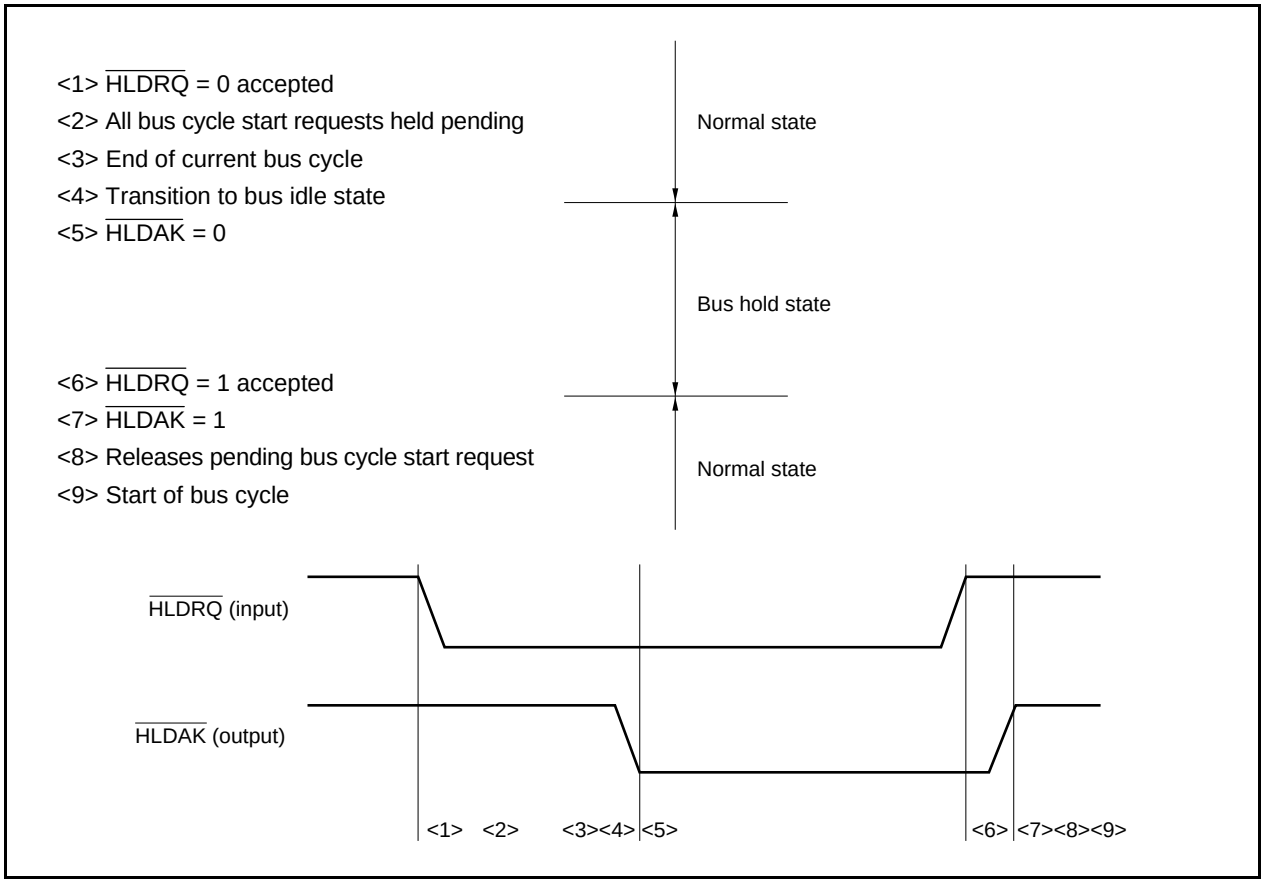
During the bus hold period, the internal operations of the V850E/IA1 continue until the external memory is accessed.

The bus hold state can be known by the HLDAK pin becoming active (low level). The period from when the $\overline{\text{HLDRQ}}$ pin becomes active (low level) to when the $\overline{\text{HLDAK}}$ pin becomes active (low level) is at least 2 clocks.

In a multiprocessor configuration, etc., a system with multiple bus masters can be configured.

4.8.2 Bus hold procedure

The procedure of the bus hold function is illustrated below.

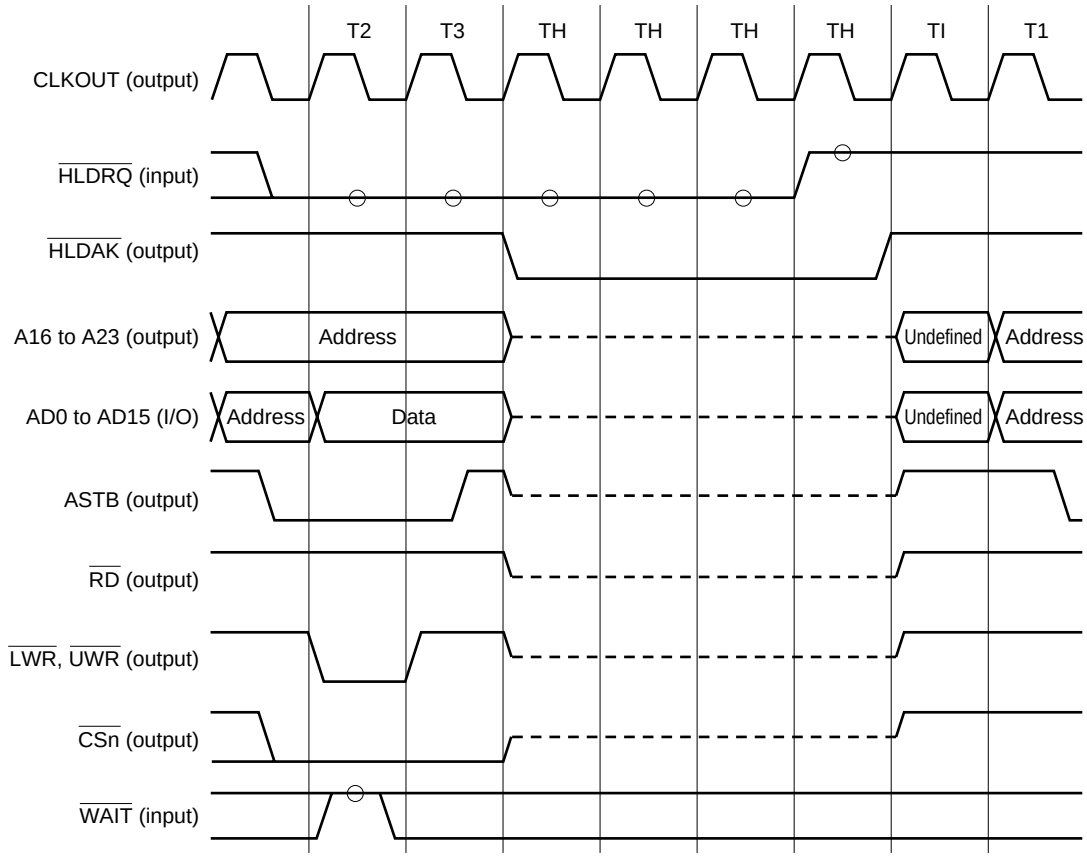


4.8.3 Operation in power save mode

In the software STOP or IDLE mode, the internal system clock is stopped. Consequently, the bus hold state is not accepted and set since the $\overline{\text{HLDRQ}}$ pin cannot be accepted even if it becomes active.

In the HALT mode, the $\overline{\text{HLDAK}}$ pin immediately becomes active when the $\overline{\text{HLDRQ}}$ pin becomes active, and the bus hold state is set. When the $\overline{\text{HLDRQ}}$ pin becomes inactive after that, the $\overline{\text{HLDAK}}$ pin also becomes inactive. As a result, the bus hold state is cleared and the HALT mode is set again.

4.8.4 Bus hold timing



Remarks 1. The circle ○ indicates the sampling timing.

2. The broken lines indicate the high-impedance state.

3. n = 0 to 7

4.9 Bus Priority Order

There are four external bus cycles: bus hold, instruction fetch, operand data access, and DMA cycle.

In order of priority, bus hold is the highest, followed by DMA cycle, instruction fetch, and operand data access, in that order.

An instruction fetch may be inserted between a read access and write access during a read modify write access.

Also, an instruction fetch may be inserted between bus accesses when a CPU bus clock is used.

Table 4-1. Bus Priority Order

Priority Order	External Bus Cycle	Bus Master
High ↕ Low	Bus hold	External device
	DMA cycle	DMA controller
	Operand data access	CPU
	Instruction fetch	CPU

4.10 Boundary Operation Conditions

4.10.1 Program space

(1) Branching to the on-chip peripheral I/O area or successive fetches from the internal RAM area to the on-chip peripheral I/O area are prohibited. If the above is performed (branching or successive fetch), an undefined data is fetched, and fetching from the external memory is not performed.

(2) If a branch instruction exists at the upper limit of the internal RAM area, a pre-fetch operation (invalid fetch) that straddles over the on-chip peripheral I/O area does not occur.

(3) If a burst fetch is performed for contiguous memory blocks, it is terminated at the upper limit of a block, and the start-up cycle is started at the lower limit of the next block.

(4) Burst fetch is valid only in the external memory area. In memory block 7, it is terminated when the internal address count value has reached the upper limit of the external memory area.

4.10.2 Data space

The V850E/IA1 is provided with an address misalign function.

Through this function, regardless of the data format (word data, halfword data, or byte data), data can be allocated to all addresses. However, in the case of word data and halfword data, if the data is not subject to boundary alignment, the bus cycle will be generated at least 2 times and bus efficiency will drop.

(1) In the case of halfword-length data access

When the address's LSB is 1, the byte-length bus cycle will be generated 2 times.

(2) In the case of word-length data access

(a) When the address's LSB is 1, bus cycles will be generated in the order of byte-length bus cycle, halfword-length bus cycle, and byte-length bus cycle.

(b) When the address's lowest 2 bits are 10, the halfword-length bus cycle will be generated 2 times.

[MEMO]

CHAPTER 5 MEMORY ACCESS CONTROL FUNCTION

5.1 SRAM, External ROM, External I/O Interface

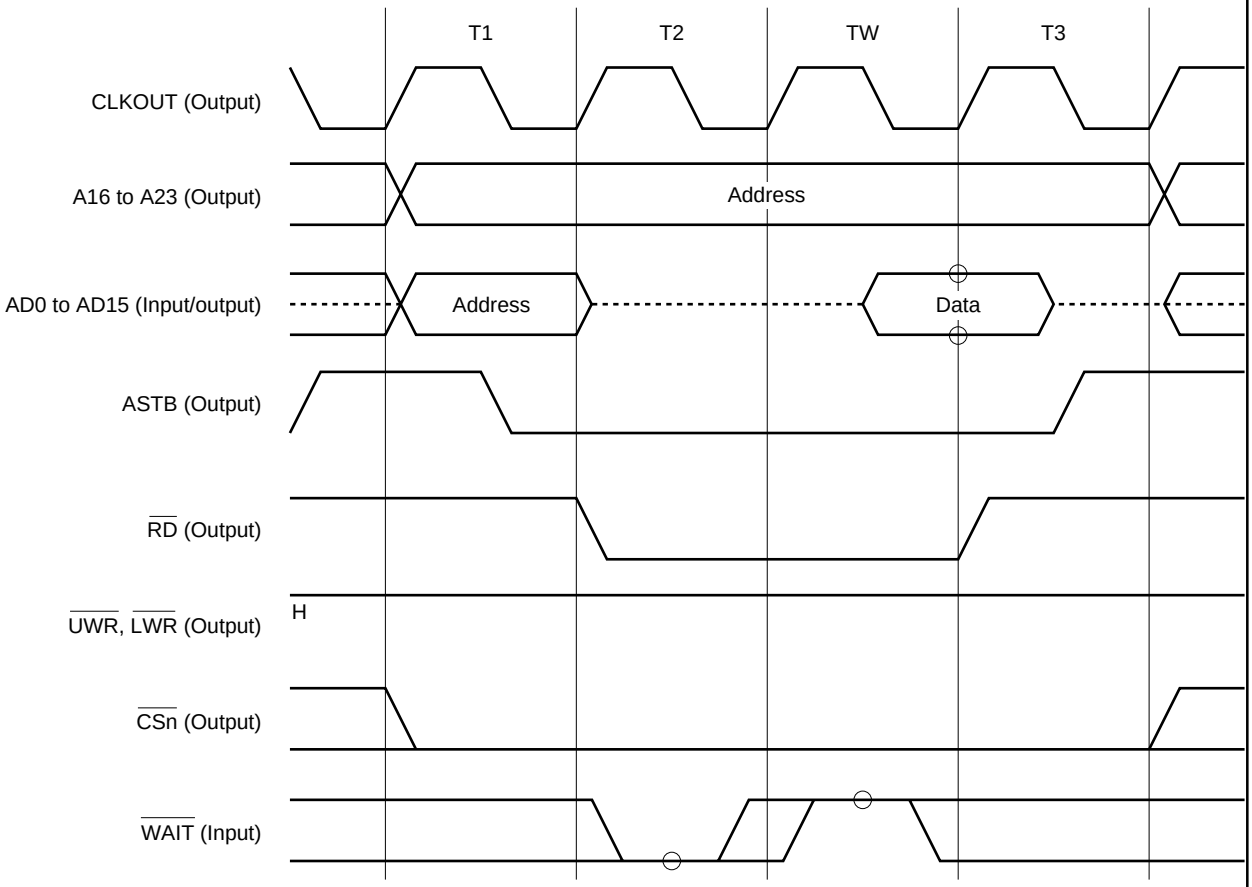
5.1.1 Features

- SRAM is accessed in a minimum of 2 states.
- A maximum of 7 programmable data wait states can be inserted according to DWC0 and DWC1 register settings.
- Data waits can be controlled by $\overline{\text{WAIT}}$ pin input.
- An idle state (1 state) can be inserted after a read/write cycle by setting the BCC register.
- An address hold wait state or address setup wait state can be inserted by setting the AWC register.

5.1.2 SRAM, external ROM, external I/O access

Figure 5-1. SRAM, External ROM, External I/O Access Timing (1/5)

(a) On a read (1 wait insertion)



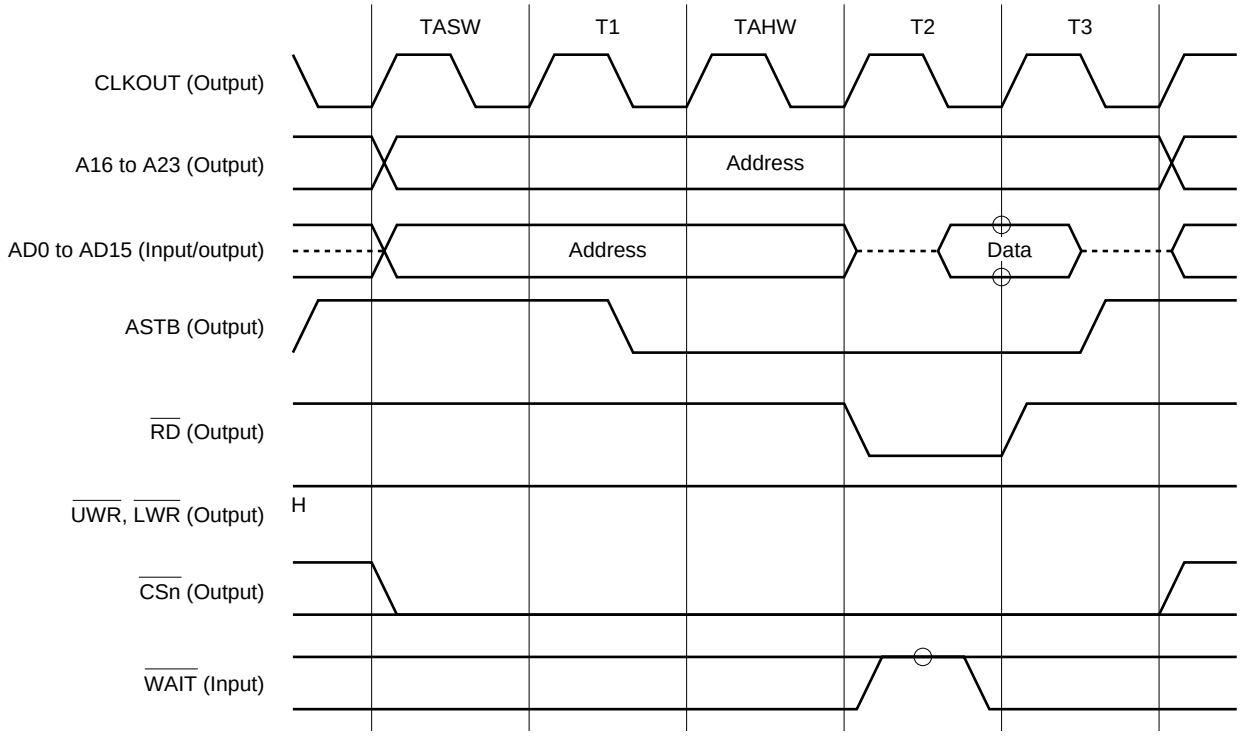
Remarks 1. The circles indicate the sampling timing.

2. Broken lines indicate high impedance.

3. n = 0 to 7

Figure 5-1. SRAM, External ROM, External I/O Access Timing (2/5)

(b) On a read (0 wait, address setup wait, address hold wait state insertion)



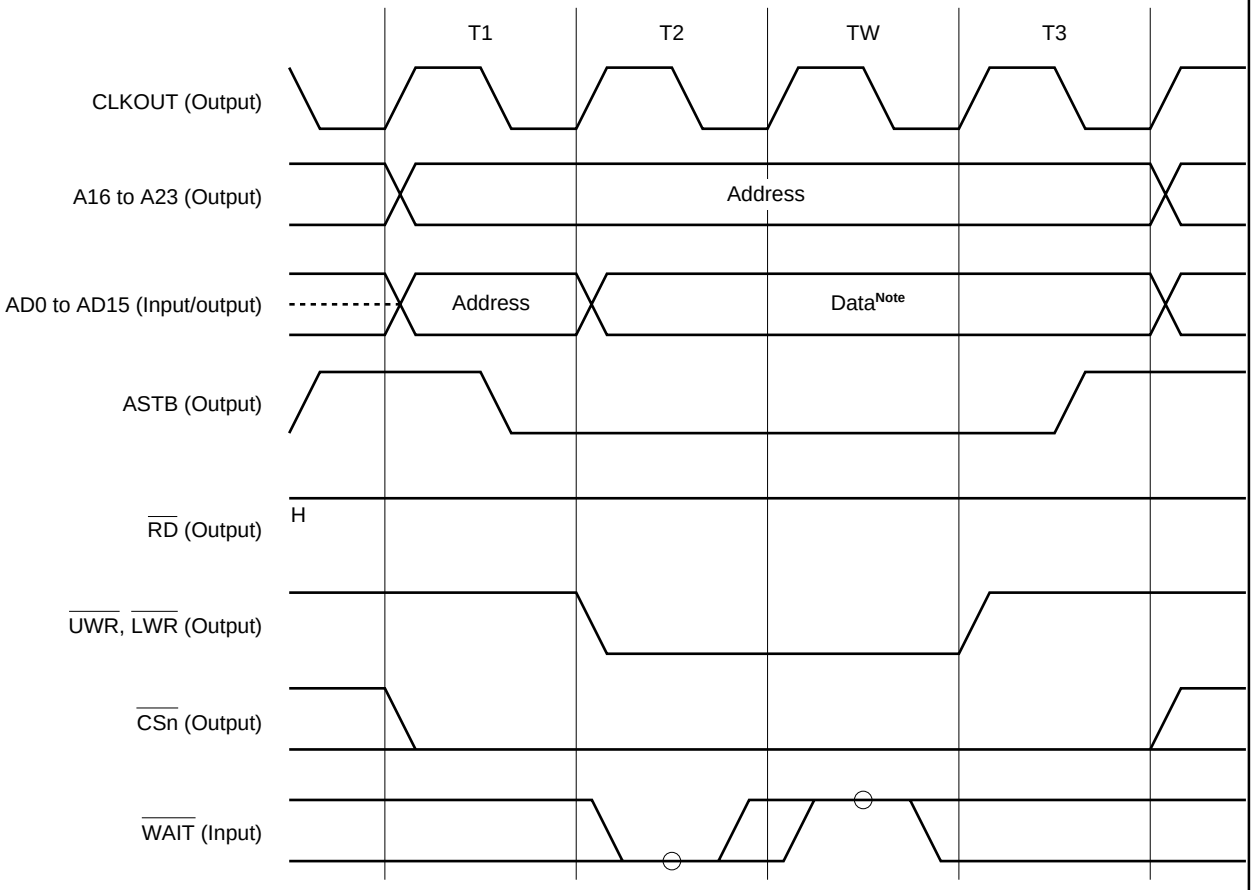
Remarks 1. The circles indicate the sampling timing.

2. Broken lines indicate high impedance.

3. n = 0 to 7

Figure 5-1. SRAM, External ROM, External I/O Access Timing (3/5)

(c) On a write (1 wait insertion)

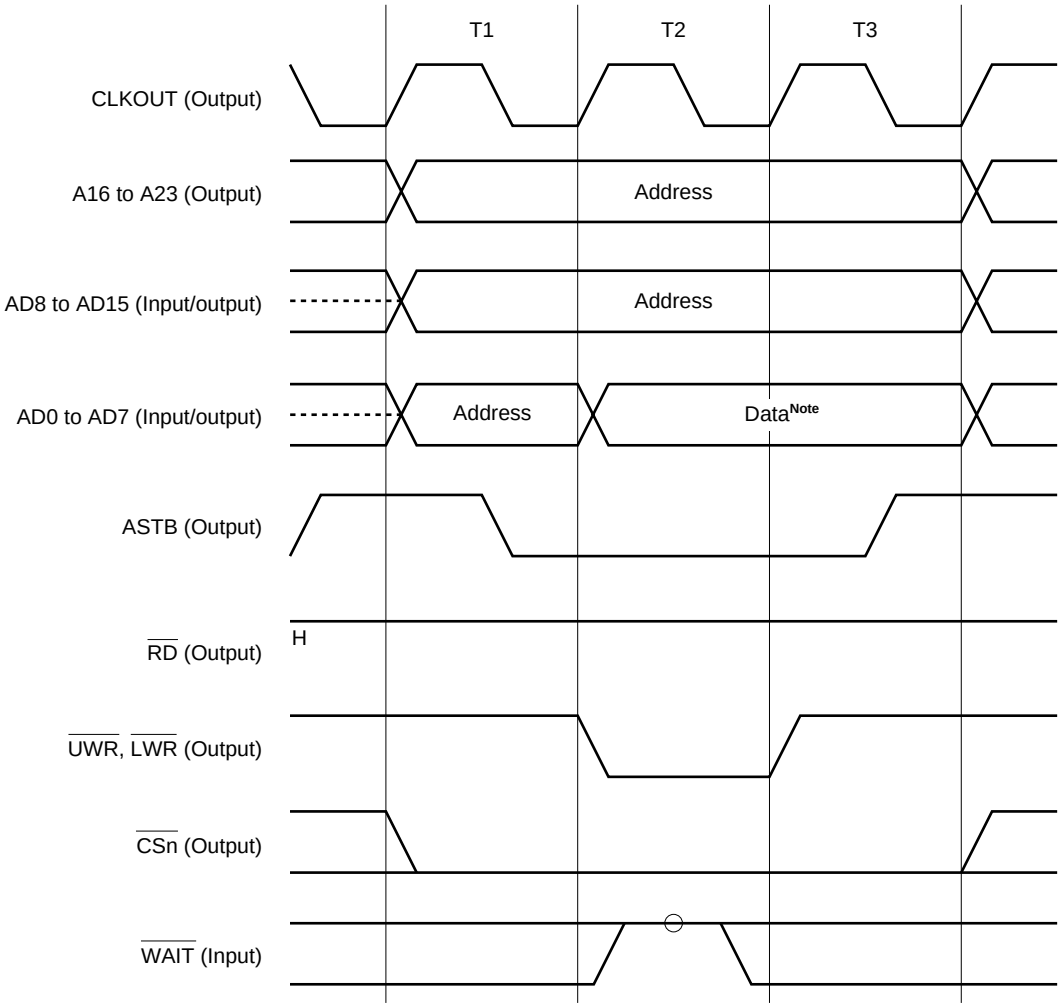


Note AD0 to AD7 output invalid data when accessed to odd-numbered address byte data.
AD8 to AD15 output invalid data when accessed to even-numbered address byte data.

Remarks 1. The circles indicate the sampling timing.
2. Broken lines indicate high impedance.
3. n = 0 to 7

Figure 5-1. SRAM, External ROM, External I/O Access Timing (4/5)

(d) On a write (0 wait insertion, for 8-bit data bus)

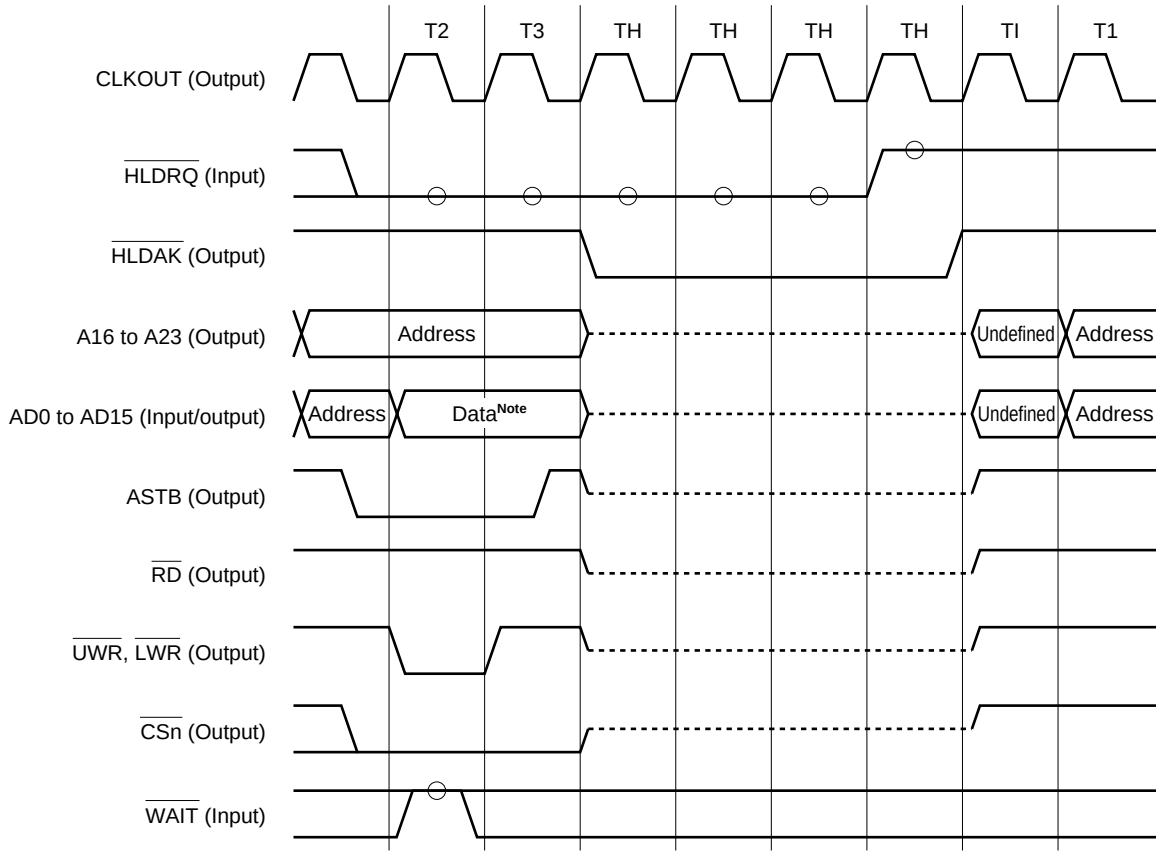


Note AD0 to AD7 output invalid data when accessed to odd-numbered address byte data.
AD8 to AD15 output invalid data when accessed to even-numbered address byte data.

Remarks 1. The circles indicate the sampling timing.
2. Broken lines indicate high impedance.
3. n = 0 to 7

Figure 5-1. SRAM, External ROM, External I/O Access Timing (5/5)

(e) Bus hold timing



Note AD0 to AD7 output invalid data when accessed to odd-numbered address byte data.
AD8 to AD15 output invalid data when accessed to even-numbered address byte data.

Remarks 1. The circles indicate the sampling timing.
2. Broken lines indicate high impedance.
3. n = 0 to 7

CHAPTER 6 DMA FUNCTIONS (DMA CONTROLLER)

The V850E/IA1 includes a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer.

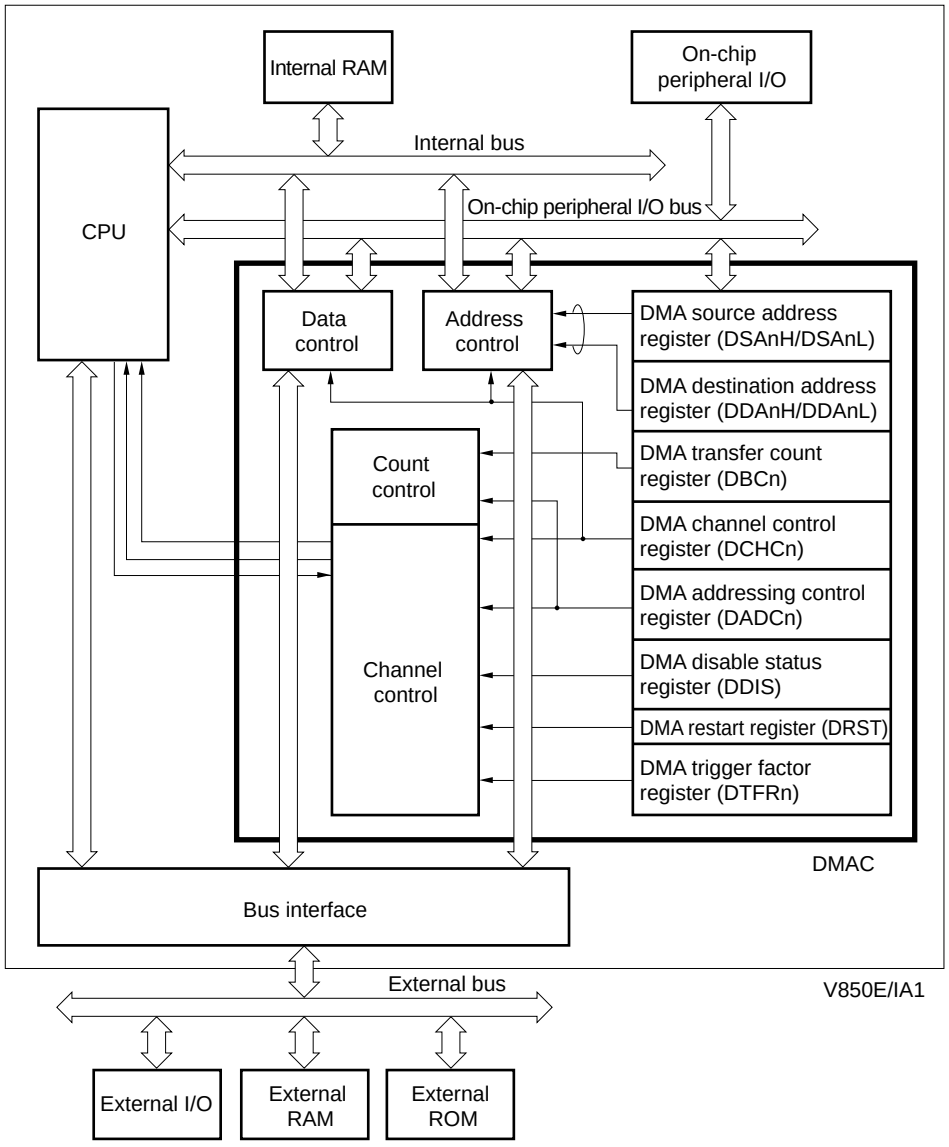
The DMAC controls data transfer between memory and I/O, among memories or among I/Os, based on DMA requests issued by the on-chip peripheral I/O (serial interface, real-time pulse unit, and A/D converter), or software triggers (memory refers to internal RAM or external memory).

6.1 Features

- 4 independent DMA channels
- Transfer units: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})

- Two-cycle transfer
- Three transfer modes
  - Single transfer mode
  - Single-step transfer mode
  - Block transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/O (serial interface, real-time pulse unit, A/D converter)
  - Requests by software trigger
- Transfer objects
  - Memory ↔ I/O
  - Memory ↔ memory
  - I/O ↔ I/O
- Next address setting function

6.2 Configuration



Remark n = 0 to 3

6.3 Control Registers

6.3.1 DMA source address registers 0 to 3 (DSA0 to DSA3)

These registers are used to set the DMA source addresses (28 bits each) for DMA channel n (n = 0 to 3). They are divided into two 16-bit registers, DSAnH and DSAnL.

Since these registers are configured as 2-stage FIFO buffer registers, a new source address for DMA transfer can be specified during DMA transfer. (Refer to **6.9 Next Address Setting Function**.)

(1) DMA source address registers 0H to 3H (DSA0H to DSA3H)

These registers can be read/written in 16-bit units.

Caution When setting an address of a peripheral I/O register for the source address, be sure to specify an address between FFFF000H and FFFFFFFH. An address of the peripheral I/O register image (3FFF000H to 3FFFFFFH) must not be specified.

Figure 6-1. DMA Source Address Registers 0H to 3H (DSA0H to DSA3H)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DSA0H	IR	0	0	0	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	FFFFF082H	Undefined
DSA1H	IR	0	0	0	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	FFFFF08AH	Undefined
DSA2H	IR	0	0	0	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	FFFFF092H	Undefined
DSA3H	IR	0	0	0	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	FFFFF09AH	Undefined

Bit Position	Bit Name	Function
15	IR	Specifies the DMA source address. 0: External memory, on-chip peripheral I/O 1: Internal RAM
11 to 0	SA27 to SA16	Sets the DMA source addresses (A27 to A16). During DMA transfer, it stores the next DMA transfer source address.

(2) DMA source address registers 0L to 3L (DSA0L to DSA3L)

These registers can be read/written in 16-bit units.

Figure 6-2. DMA Source Address Registers 0L to 3L (DSA0L to DSA3L)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DSA0L	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	FFFFF080H	Undefined
DSA1L	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	FFFFF088H	Undefined
DSA2L	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	FFFFF090H	Undefined
DSA3L	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	FFFFF098H	Undefined

Bit Position	Bit Name	Function
15 to 0	SA15 to SA0	Sets the DMA source address (A15 to A0). During DMA transfer, it stores the next DMA transfer source address.

6.3.2 DMA destination address registers 0 to 3 (DDA0 to DDA3)

These registers are used to set the DMA destination address (28 bits each) for DMA channel n (n = 0 to 3). They are divided into two 16-bit registers, DDAnH and DDAnL.

Since these registers are configured as 2-stage FIFO buffer registers, a new destination address for DMA transfer can be specified during DMA transfer. (Refer to **6.9 Next Address Setting Function**.)

(1) DMA destination address registers 0H to 3H (DDA0H to DDA3H)

These registers can be read/written in 16-bit units.

Caution When setting an address of a peripheral I/O register for the destination address, be sure to specify an address between FFFF000H and FFFFFFFH. An address of the peripheral I/O register image (3FFF000H to 3FFFFFFH) must not be specified.

Figure 6-3. DMA Destination Address Registers 0H to 3H (DDA0H to DDA3H)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DDA0H	IR	0	0	0	DA27	DA26	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16	FFFFF086H	Undefined
DDA1H	IR	0	0	0	DA27	DA26	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16	FFFFF08EH	Undefined
DDA2H	IR	0	0	0	DA27	DA26	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16	FFFFF096H	Undefined
DDA3H	IR	0	0	0	DA27	DA26	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16	FFFFF09EH	Undefined

Bit Position	Bit Name	Function
15	IR	Specifies the DMA destination address. 0: External memory, on-chip peripheral I/O 1: Internal RAM
11 to 0	DA27 to DA16	Sets the DMA destination addresses (A27 to A16). During DMA transfer, it stores the next DMA transfer destination address.

(2) DMA destination address registers 0L to 3L (DDA0L to DDA3L)

These registers can be read/written in 16-bit units.

Figure 6-4. DMA Destination Address Registers 0L to 3L (DDA0L to DDA3L)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DDA0L	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	FFFFF084H	Undefined
DDA1L	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	FFFFF08CH	Undefined
DDA2L	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	FFFFF094H	Undefined
DDA3L	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	FFFFF09CH	Undefined

Bit Position	Bit Name	Function
15 to 0	DA15 to DA0	Sets the DMA destination address (A15 to A0). During DMA transfer, it stores the next DMA transfer destination address.

6.3.3 DMA byte count registers 0 to 3 (DBC0 to DBC3)

These 16-bit registers are used to set the byte transfer counts for DMA channels n (n = 0 to 3). They store the remaining transfer counts during DMA transfer.

Since these registers are configured as 2-stage FIFO buffer registers, a new DMA byte transfer count for DMA transfer can be specified during DMA transfer. (Refer to **6.9 Next Address Setting Function**.)

These registers can be read/written in 16-bit units.

Figure 6-5. DMA Transfer Count Registers 0 to 3 (DBC0 to DBC3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DBC0	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFFFF0C0H	Undefined
DBC1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFFFF0C2H	Undefined
DBC2	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFFFF0C4H	Undefined
DBC3	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFFFF0C6H	Undefined

Bit Position	Bit Name	Function
15 to 0	BC15 to BC0	Sets the byte transfer count. It stores the remaining byte transfer count during DMA transfer.

DBCn (n = 0 to 3)	States
0000H	Byte transfer count 1 or remaining byte transfer count
0001H	Byte transfer count 2 or remaining byte transfer count
:	:
FFFFH	Byte transfer count 65,536 (2^{16}) or remaining byte transfer count

6.3.4 DMA addressing control registers 0 to 3 (DADC0 to DADC3)

These 16-bit registers are used to control the DMA transfer modes for DMA channel n (n = 0 to 3). These registers cannot be accessed during DMA operation.

They can be read/written in 16-bit units.

Figure 6-6. DMA Addressing Control Registers 0 to 3 (DADC0 to DADC3) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
DADC0	DS1	DS0	0	0	0	0	0	0	SAD1	SAD0	DAD1	DAD0	TM1	TM0	0	0	FFFFF0D0H	0000H
DADC1	DS1	DS0	0	0	0	0	0	0	SAD1	SAD0	DAD1	DAD0	TM1	TM0	0	0	FFFFF0D2H	0000H
DADC2	DS1	DS0	0	0	0	0	0	0	SAD1	SAD0	DAD1	DAD0	TM1	TM0	0	0	FFFFF0D4H	0000H
DADC3	DS1	DS0	0	0	0	0	0	0	SAD1	SAD0	DAD1	DAD0	TM1	TM0	0	0	FFFFF0D6H	0000H

Bit Position	Bit Name	Function
15, 14	DS1, DS0	Sets the transfer data size for DMA transfer. DS1 / DS0 / Transfer Data Size: 0 / 0 / 8 bits 0 / 1 / 16 bits 1 / 0 / 32 bits 1 / 1 / Setting prohibited For the peripheral I/O and programmable peripheral I/O registers, ensure the transfer size matches the access size.
7, 6	SAD1, SAD0	Sets the count direction of the source address for DMA channel n (n = 0 to 3). SAD1 / SAD0 / Count Direction: 0 / 0 / Increment 0 / 1 / Decrement 1 / 0 / Fixed 1 / 1 / Setting prohibited
5, 4	DAD1, DAD0	Sets the count direction of the destination address for DMA channel n (n = 0 to 3). DAD1 / DAD0 / Count Direction: 0 / 0 / Increment 0 / 1 / Decrement 1 / 0 / Fixed 1 / 1 / Setting prohibited

Figure 6-6. DMA Addressing Control Registers 0 to 3 (DADC0 to DADC3) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>3, 2</td><td>TM1, TM0</td><td>Sets the transfer mode during DMA transfer.
<table>
<tr><th>TM1</th><th>TM0</th><th>Transfer Mode</th></tr>
<tr><td>0</td><td>0</td><td>Single transfer mode</td></tr>
<tr><td>0</td><td>1</td><td>Single-step transfer mode</td></tr>
<tr><td>1</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>1</td><td>1</td><td>Block transfer mode</td></tr>
</table></td></tr>
</table>

6.3.5 DMA channel control registers 0 to 3 (DCHC0 to DCHC3)

These 8-bit registers are used to control the DMA transfer operating mode for DMA channel n (n = 0 to 3).

These registers can be read/written in 8-bit or 1-bit units. (However, bit 7 is read only and bits 2 and 1 are write only. If bits 2 and 1 are read, the read value is always 0.)

Figure 6-7. DMA Channel Control Registers 0 to 3 (DCHC0 to DCHC3)

	7	6	5	4	3	2	1	0	Address	Initial value
DCHC0	TC0	0	0	0	MLE0	INIT0	STG0	E00	FFFFF0E0H	00H
DCHC1	TC1	0	0	0	MLE1	INIT1	STG1	E11	FFFFF0E2H	00H
DCHC2	TC2	0	0	0	MLE2	INIT2	STG2	E22	FFFFF0E4H	00H
DCHC3	TC3	0	0	0	MLE3	INIT3	STG3	E33	FFFFF0E6H	00H

Bit Position	Bit Name	Function
7	TCn (n = 0 to 3)	This status bit indicates whether DMA transfer through DMA channel n has ended or not. This bit is read-only. It is set to 1 when DMA transfer ends and cleared (to 0) when it is read. 0: DMA transfer had not ended. 1: DMA transfer had ended.
3	MLEn (n = 0 to 3)	When this bit is set to 1 at terminal count output, the Enn bit is not cleared to 0 and the DMA transfer enable state is retained. Moreover, the next DMA transfer request can be accepted even when the TCn bit is not read. When this bit is cleared to 0 at terminal count output, the Enn bit is cleared to 0 and the DMA transfer disable state is entered. At the next DMA request, the setting of the Enn bit to 1 and the reading of the TCn bit are required.
2	INITn (n = 0 to 3)	When this bit is set to 1, DMA transfer is forcibly terminated.
1	STGn (n = 0 to 3)	If this bit is set to 1 in the DMA transfer enable state (TCn bit = 0, Enn bit = 1), DMA transfer is started.
0	Enn (n = 0 to 3)	Specifies whether DMA transfer through DMA channel n is to be enabled or disabled. This bit is cleared to 0 when DMA transfer ends. It is also cleared to 0 when DMA transfer is forcibly terminated by means of setting the INITn bit to 1 or by NMI input. 0: DMA transfer disabled 1: DMA transfer enabled

6.3.6 DMA disable status register (DDIS)

This register holds the contents of the Enn bit of the DCHCn register during NMI input (n = 0 to 3).

This register is read-only in 8-bit or 1-bit units.

Figure 6-8. DMA Disable Status Register (DDIS)

	7	6	5	4	3	2	1	0	Address	Initial value
DDIS	0	0	0	0	CH3	CH2	CH1	CH0	FFFFF0F0H	00H

Bit Position	Bit Name	Function
3 to 0	CH3 to CH0	Reflects the contents of the Enn bit of the DCHCn register during NMI input. The contents of this register are held until the next NMI input or until the system is reset.

6.3.7 DMA restart register (DRST)

This register is used to restart DMA transfer that has been forcibly interrupted by NMI input. The ENn bit of this register and the Enn bit of the DCHCn register are linked to each other (n = 0 to 3). Following forcible interrupt by NMI input, the DMA channel that was interrupted is confirmed from the contents of the DDIS register, and DMA transfer is restarted by setting the ENn bit of the corresponding channel to 1.

This register can be read/written in 8-bit or 1-bit units.

Figure 6-9. DMA Restart Register (DRST)

	7	6	5	4	3	2	1	0	Address	Initial value
DRST	0	0	0	0	EN3	EN2	EN1	EN0	FFFFF0F2H	00H

Bit Position	Bit Name	Function
3 to 0	EN3 to EN0	Specifies whether DMA transfer through DMA channel n is to be enabled or disabled. This bit is cleared to 0 when DMA transfer is completed in accordance with the terminal count output. It is also cleared to 0 when DMA transfer is forcibly terminated by setting the INITn bit to 1 or by NMI input. 0: DMA transfer disabled 1: DMA transfer enabled

6.3.8 DMA trigger factor registers 0 to 3 (DTFR0 to DTFR3)

These 8-bit registers are used to control the DMA transfer start trigger through interrupt requests from on-chip peripheral I/O.

The interrupt requests set with these registers serve as DMA transfer start factors.

These registers can be read/written in 8-bit/1-bit units.

Figure 6-10. DMA Trigger Factor Registers 0 to 3 (DTFR0 to DTFR3) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
DTFR0	0	0	IFC05	IFC04	IFC03	IFC02	IFC01	IFC00	FFFFF810H	00H
DTFR1	0	0	IFC15	IFC14	IFC13	IFC12	IFC11	IFC10	FFFFF812H	00H
DTFR2	0	0	IFC25	IFC24	IFC23	IFC22	IFC21	IFC20	FFFFF814H	00H
DTFR3	0	0	IFC35	IFC34	IFC33	IFC32	IFC31	IFC30	FFFFF816H	00H

Bit Position	Bit Name	Function
5 to 0	IFCn5 to IFCn0	Sets the interrupt source that serves as the DMA start factor.

IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0	Interrupt Source
0	0	0	0	0	0	DMA request from on-chip peripheral I/O disabled
0	0	0	0	0	1	INTP0
0	0	0	0	1	0	INTP1
0	0	0	0	1	1	INTP2
0	0	0	1	0	0	INTP3
0	0	0	1	0	1	INTP4
0	0	0	1	1	0	INTP5
0	0	0	1	1	1	INTP6
0	0	1	0	0	0	INTDET0
0	0	1	0	0	1	INTDET1
0	0	1	0	1	0	INTTM00
0	0	1	0	1	1	INTCM003
0	0	1	1	0	0	INTTM01
0	0	1	1	0	1	INTCM013
0	0	1	1	1	0	INTP100/INTCC100
0	0	1	1	1	1	INTP101/INTCC101
0	1	0	0	0	0	INTCM100
0	1	0	0	0	1	INTCM101
0	1	0	0	1	0	INTP110/INTCC110
0	1	0	0	1	1	INTP111/INTCC111
0	1	0	1	0	0	INTCM110
0	1	0	1	0	1	INTCM111
0	1	0	1	1	0	INTTM20

Cautions 1. Be sure to stop DMA operation before making changes to DTFRn register settings.

2. An interrupt request input in a standby mode (IDLE or software STOP mode) cannot be used as a DMA transfer start factor.

Remark n = 0 to 3

Figure 6-10. DMA Trigger Factor Registers 0 to 3 (DTFR0 to DTFR3) (2/2)

Bit Position	Bit Name	Function
5 to 0	IFCn5 to IFCn0	

IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0	Interrupt Source
0	1	0	1	1	1	INTTM21
0	1	1	0	0	0	INTP20/INTCC20
0	1	1	0	0	1	INTP21/INTCC21
0	1	1	0	1	0	INTP22/INTCC22
0	1	1	0	1	1	INTP23/INTCC23
0	1	1	1	0	0	INTP24/INTCC24
0	1	1	1	0	1	INTP25/INTCC25
0	1	1	1	1	0	INTTM3
0	1	1	1	1	1	INTP30/INTCC30
1	0	0	0	0	0	INTP31/INTCC31
1	0	0	0	0	1	INTCM4
1	0	0	0	1	0	INTDMA0
1	0	0	0	1	1	INTDMA1
1	0	0	1	0	0	INTDMA2
1	0	0	1	0	1	INTDMA3
1	0	0	1	1	0	INTCREC
1	0	0	1	1	1	INTCTRX
1	0	1	0	0	0	INTCERR
1	0	1	0	0	1	INTCMAC
1	0	1	0	1	0	INTCSI0
1	0	1	0	1	1	INTCSI1
1	0	1	1	0	0	INTSR0
1	0	1	1	0	1	INTST0
1	0	1	1	1	0	INTSER0
1	0	1	1	1	1	INTSR1
1	1	0	0	0	0	INTST1
1	1	0	0	0	1	INTSR2
1	1	0	0	1	0	INTST2
1	1	0	0	1	1	INTAD0
1	1	0	1	0	0	INTAD1
1	1	0	1	0	1	NBDAD
1	1	0	1	1	0	NBDREW
Other than above						Setting prohibited

Cautions 1. Be sure to stop DMA operation before making changes to DTFRn register settings.

2. An interrupt request input in a standby mode (IDLE or software STOP mode) cannot be used as a DMA transfer start factor.

Remark n = 0 to 3

6.4 DMA Bus States

6.4.1 Types of bus states

The DMAC bus states consist of the following 10 states.

(1) TI state

The TI state is an idle state, during which no access request is issued.
The DMA request signals are sampled at the rising edge of the CLKOUT signal.

(2) T0 state

DMA transfer ready state (state in which a DMA transfer request has been issued and the bus mastership is acquired for the first DMA transfer).

(3) T1R state

The bus enters the T1R state at the beginning of a read operation in the two-cycle transfer mode.
Address driving starts. After entering the T1R state, the bus invariably enters the T2R state.

(4) T1RI state

The T1RI state is a state in which the bus waits for the acknowledge signal corresponding to an external memory read request.
After entering the last T1RI state, the bus invariably enters the T2R state.

(5) T2R state

The T2R state corresponds to the last state of a read operation in the two-cycle transfer mode, or to a wait state.
In the last T2R state, read data is sampled. After entering the last T2R state, the bus invariably enters the T1W state.

(6) T2RI state

State in which the bus is ready for DMA transfer to on-chip peripheral I/O or internal RAM (state in which the bus mastership is acquired for DMA transfer to on-chip peripheral I/O or internal RAM).
After entering the last T2RI state, the bus invariably enters the T1W state.

(7) T1W state

The bus enters the T1W state at the beginning of a write operation in the two-cycle transfer mode.
Address driving starts. After entering the T1W state, the bus invariably enters the T2W state.

(8) T1WI state

State in which the bus waits for the acknowledge signal corresponding to an external memory write request.
After entering the last T1WI state, the bus invariably enters the T2W state.

(9) T2W state

The T2W state corresponds to the last state of a write operation in the two-cycle transfer mode, or to a wait state.
In the last T2W state, the write strobe signal is made inactive.

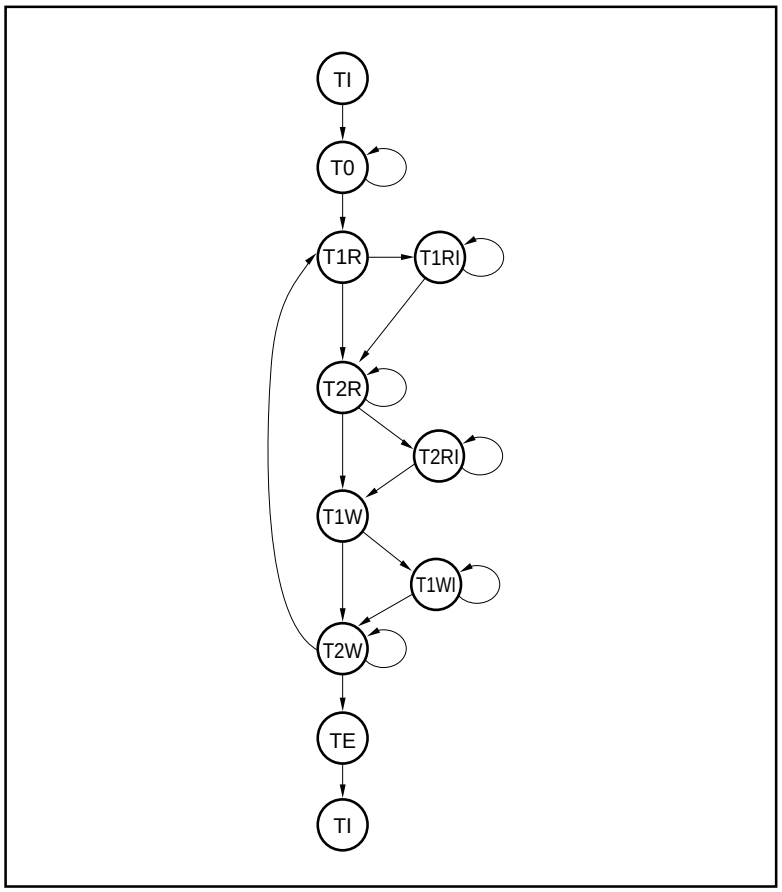
(10) TE state

The TE state corresponds to DMA transfer completion. The DMAC generates the internal DMA transfer completion signal and various internal signals are initialized (n = 0 to 3). After entering the TE state, the bus invariably enters the TI state.

6.4.2 DMAC bus cycle state transition

Except for the block transfer mode, each time the processing for a DMA transfer is completed, the bus mastership is released.

Figure 6-11. DMAC Bus Cycle (Two-Cycle Transfer) State Transition



6.5 Transfer Mode

6.5.1 Single transfer mode

In single transfer mode, the DMAC releases the bus at each byte/halfword transfer. If there is a subsequent DMA transfer request, transfer is performed again once. This operation continues until a terminal count occurs.

When the DMAC has released the bus, if another higher priority DMA transfer request is issued, the higher priority DMA request always takes precedence.

6.5.2 Single-step transfer mode

In single-step transfer mode, the DMAC releases the bus at each byte/halfword transfer. Once a DMA transfer request signal is received, transfer is performed again. This operation continues until a terminal count occurs.

When the DMAC has released the bus, if another higher priority DMA transfer request is issued, the higher priority DMA request always takes precedence.

6.5.3 Block transfer mode

In the block transfer mode, once transfer starts, the DMAC continues the transfer operation without releasing the bus until a terminal count occurs. No other DMA requests are acknowledged during block transfer.

After the block transfer ends and the DMAC releases the bus, another DMA transfer can be acknowledged.

6.6 Transfer Types

6.6.1 Two-cycle transfer

In two-cycle transfer, data transfer is performed in two cycles, a read cycle (source to DMAC) and a write cycle (DMAC to destination).

In the first cycle, the source address is output and reading is performed from the source to the DMAC. In the second cycle, the destination address is output and writing is performed from the DMAC to the destination.

6.7 Transfer Object

6.7.1 Transfer type and transfer object

Table 6-1 lists the relationships between transfer type and transfer object (√: transfer enabled, ×: transfer disabled).

Table 6-1. Relationship Between Transfer Type and Transfer Object

		Destination				
		Two-Cycle Transfer				
		Internal ROM	On-Chip Peripheral I/O	External I/O	Internal RAM	External Memory
Source	On-chip peripheral I/O	×	√	√	√	√
	External I/O	×	√	√	√	√
	Internal RAM	×	√	√	×	√
	External memory	×	√	√	√	√
	Internal ROM	×	×	×	×	×

Cautions 1. The operation is not guaranteed for combinations of transfer destination and source marked with "×" in Table 6-1.

2. Addresses between 3FFF000H and 3FFFFFFH cannot be specified for the source and destination address of DMA transfer. Be sure to specify an address between FFFF000H and FFFFFFFH.

Remark During two-cycle 16-bit transfer, if the data bus width of the transfer source and that of the transfer destination are different, the operation becomes as follows.

In the case of transfer from a 16-bit bus to an 8-bit bus

A 16-bit read cycle is generated and then an 8-bit write cycle is generated twice.

In the case of transfer from an 8-bit bus to a 16-bit bus

An 8-bit read cycle is generated twice and then a 16-bit write cycle is generated.

6.7.2 External bus cycles during DMA transfer (two-cycle transfer)

The external bus cycles during DMA transfer (two-cycle transfer) are shown below.

Table 6-2. External Bus Cycles During DMA Transfer (Two-Cycle Transfer)

Transfer Object	External Bus Cycle	
On-chip peripheral I/O, internal RAM	None[Note]	–
External I/O	Yes	SRAM cycle
External memory	Yes	Memory access cycle set by the BCT register

Note Other external cycles, such as a CPU-based bus cycle can be started.

6.8 DMA Channel Priorities

The DMA channel priorities are fixed as follows.

DMA channel 0 > DMA channel 1 > DMA channel 2 > DMA channel 3

These priorities are valid in the TI state only. In the block transfer mode, the channel used for transfer is never switched.

In the single-step transfer mode, if a higher priority DMA transfer request is issued while the bus is released (in the TI state), the higher priority DMA transfer request is acknowledged.

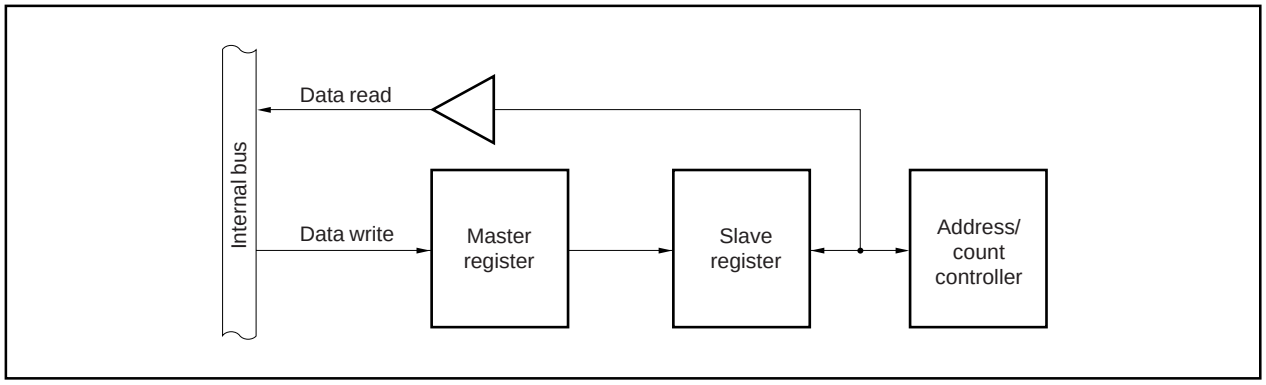
6.9 Next Address Setting Function

The DMA source address registers (DSAnH, DSAnL), DMA destination address registers (DDAnH, DDAnL), and DMA transfer count register (DBCn) are buffer registers with a 2-stage FIFO configuration (n = 0 to 3).
When the terminal count is issued, these registers are automatically rewritten with the value that was set immediately before.

Therefore, during DMA transfer, transfer is automatically started when a new DMA transfer setting is made for these registers and the MLEn bit of the DCHCn register is set to 1 (however, the DMA transfer end interrupt may be issued even if DMA transfer is automatically started).

Figure 6-12 shows the configuration of the buffer register.

Figure 6-12. Buffer Register Configuration



6.10 DMA Transfer Start Factors

There are two types of DMA transfer start factors, as shown below.

(1) Request from software

If the STGn, Enn, and TCn bits of the DCHCn register are set as follows, DMA transfer starts (n = 0 to 3).

- STGn bit = 1
- Enn bit = 1
- TCn bit = 0

(2) Request from on-chip peripheral I/O

If, when the Enn and TCn bits of the DCHCn register are set as shown below, an interrupt request is issued from the on-chip peripheral I/O that is set in the DTFRn register, DMA transfer starts (n = 0 to 3).

- Enn bit = 1
- TCn bit = 0

6.11 Forcible Interruption

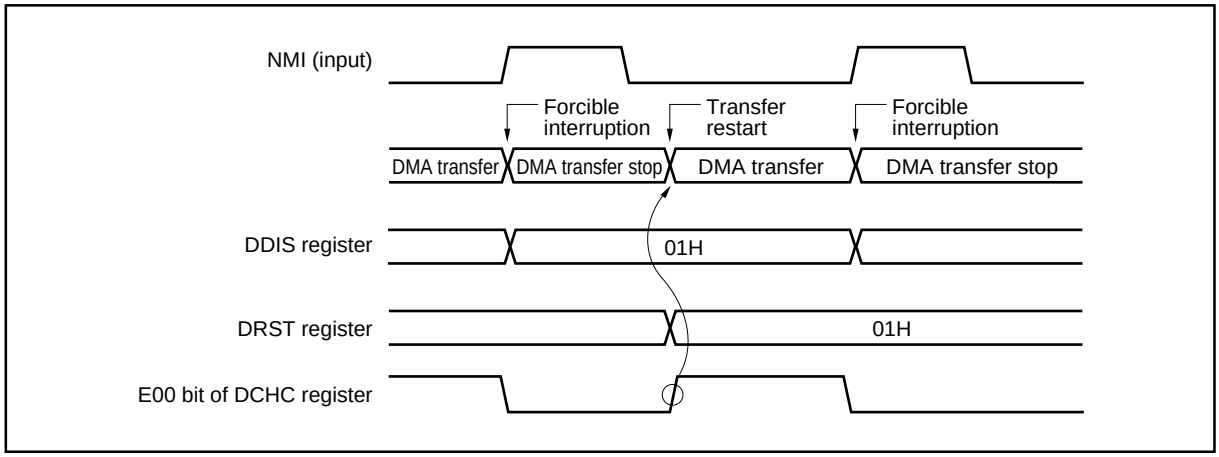
DMA transfer can be forcibly interrupted by NMI input during DMA transfer.

At such a time, the DMAC resets the Enn bit of the DCHCn register of all channels to 0 and the DMA transfer disabled state is entered. An NMI request can then be acknowledged after the DMA transfer executed during NMI input is terminated (n = 0 to 3).

In the single-step transfer mode or block transfer mode, the DMA transfer request is held in the DMAC. If the Enn bit is set to 1, DMA transfer restarts from the point where it was interrupted.

In the single transfer mode, if the Enn bit is set to 1, the next DMA transfer request is acknowledged and DMA transfer starts.

Figure 6-13. Example of Forcible Interruption of DMA Transfer



6.12 DMA Transfer End

6.12.1 DMA transfer end interrupt

When DMA transfer ends and the TCn bit of the DCHCn register is set to 1, a DMA transfer end interrupt (INTDMAn) is issued to the interrupt controller (INTC) (n = 0 to 3).

6.12.2 Terminal count output upon DMA transfer end

The terminal count signal becomes active for one clock during the last DMA transfer cycle.

6.13 Forcible Termination

In addition to the forcible interruption operation by means of NMI input, DMA transfer can be forcibly terminated by the INITn bit of the DCHCn register (n = 0 to 3).

Remark The next condition can be set even during DMA transfer because the DSAn, DDAn, and DBCn registers are buffered registers. However, the setting to the DADCn register is invalid (refer to **6.9 Next Address Setting Function** and **6.3.4 DMA addressing control registers 0 to 3 (DADC to DADC3)**).

6.14 Precautions

(1) Memory boundary

The transfer operation is not guaranteed if the source or the destination address exceeds the area of DMA objects (external memory, internal RAM, or peripheral I/O) during DMA transfer.

(2) Transfer of misaligned data

DMA transfer of 16-bit bus width misaligned data is not supported.

(3) Times related to DMA transfer

The overhead before and after DMA transfer and the minimum execution clock for DMA transfer are shown below.

- Internal RAM access: 2 clocks

Note that for external memory access, the time depends on the type of external memory connected.

(4) Bus arbitration for CPU

The CPU can access external memory, on-chip peripheral I/O, and internal RAM not undergoing DMA transfer.

While data transfer among external memories or to and from I/O is being performed, the CPU can access internal RAM.

While data transfer is being executed between internal RAMs, the CPU can access external memory and peripheral I/O.

6.14.1 Interrupt factors

DMA transfer is interrupted if a bus hold is issued.

If the factor (bus hold) interrupting DMA transfer disappears, DMA transfer promptly restarts.

[MEMO]

CHAPTER 7 INTERRUPT/EXCEPTION PROCESSING FUNCTION

The V850E/IA1 is provided with a dedicated interrupt controller (INTC) for interrupt servicing and can process a total of 53 interrupt requests.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution. Generally, an exception takes precedence over an interrupt.

The V850E/IA1 can process interrupt requests from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (i.e. fetching of an illegal opcode) (exception trap).

Eight levels of software-programmable priorities can be specified for each interrupt request. Interrupt servicing starts after no fewer than 5 system clocks (100 ns (@ 50 MHz)) following the generation of an interrupt request.

7.1 Features

○ Interrupts
- Non-maskable interrupts: 1 source
- Maskable interrupts: 52 sources
- 8 levels of programmable priorities (maskable interrupts)
- Multiple interrupt control according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination[Note], edge detection, and valid edge specification for external interrupt request signals.

Note For details of the noise eliminator, refer to **14.4 Noise Eliminator.**

○ Exceptions
- Software exceptions: 32 sources
- Exception traps: 2 sources (illegal opcode exception and debug trap)

Interrupt/exception sources are listed in Table 7-1.

Table 7-1. Interrupt/Exception Source List (1/2)

Type	Classification	Interrupt/Exception Source				Default Priority	Exception Code	Handler Address	Restored PC
		Name	Controlling Register	Generating Source	Generating Unit				
Reset	Interrupt	RESET	–	$\overline{\text{RESET}}$ input	Pin	–	0000H	00000000H	Undefined
Non-maskable	Interrupt	NMI	–	NMI input	Pin	–	0010H	00000010H	nextPC
Software exception	Exception	TRAP0n[Note]	–	TRAP instruction	–	–	004nH[Note]	00000040H	nextPC
	Exception	TRAP1n[Note]	–	TRAP instruction	–	–	005nH[Note]	00000050H	nextPC
Exception trap	Exception	ILGOP/ DBTRAP	–	Illegal opcode/ DBTRAP instruction	–	–	0060H	00000060H	nextPC
Maskable	Interrupt	INTP0	P0IC0	INTP0 pin	Pin	0	0080H	00000080H	nextPC
	Interrupt	INTP1	P0IC1	INTP1 pin	Pin	1	0090H	00000090H	nextPC
	Interrupt	INTP2	P0IC2	INTP2 pin	Pin	2	00A0H	000000A0H	nextPC
	Interrupt	INTP3	P0IC3	INTP3 pin	Pin	3	00B0H	000000B0H	nextPC
	Interrupt	INTP4	P0IC4	INTP4 pin	Pin	4	00C0H	000000C0H	nextPC
	Interrupt	INTP5	P0IC5	INTP5 pin	Pin	5	00D0H	000000D0H	nextPC
	Interrupt	INTP6	P0IC6	INTP6 pin	Pin	6	00E0H	000000E0H	nextPC
	Interrupt	INTDET0	DETIC0	AD0 voltage detection	ADC	7	00F0H	000000F0H	nextPC
	Interrupt	INTDET1	DETIC1	AD1 voltage detection	ADC	8	0100H	00000100H	nextPC
	Interrupt	INTTM00	TM0IC0	TM00 underflow	RPU	9	0110H	00000110H	nextPC
	Interrupt	INTCM003	CM03IC0	CM003 match	RPU	10	0120H	00000120H	nextPC
	Interrupt	INTTM01	TM0IC1	TM01 underflow	RPU	11	0130H	00000130H	nextPC
	Interrupt	INTCM013	CM03IC1	CM013 match	RPU	12	0140H	00000140H	nextPC
	Interrupt	INTP100/ INTCC100	CC10IC0	INTP100 pin/ CC100 match	Pin/RPU	13	0150H	00000150H	nextPC
	Interrupt	INTP101/ INTCC101	CC10IC1	INTP101 pin/ CC101 match	Pin/RPU	14	0160H	00000160H	nextPC
	Interrupt	INTCM100	CM10IC0	CM100 match	RPU	15	0170H	00000170H	nextPC
	Interrupt	INTCM101	CM10IC1	CM101 match	RPU	16	0180H	00000180H	nextPC
	Interrupt	INTP110/ INTCC110	CC11IC0	INTP110 pin/ CC110 match	Pin/RPU	17	0190H	00000190H	nextPC
	Interrupt	INTP111/ INTCC111	CC11IC1	INTP111 pin/ CC111 match	Pin/RPU	18	01A0H	000001A0H	nextPC
	Interrupt	INTCM110	CM11IC0	CM110 match	RPU	19	01B0H	000001B0H	nextPC
	Interrupt	INTCM111	CM11IC1	CM111 match	RPU	20	01C0H	000001C0H	nextPC
	Interrupt	INTTM20	TM2IC0	TM20 overflow	RPU	21	01D0H	000001D0H	nextPC
	Interrupt	INTTM21	TM2IC1	TM20 overflow	RPU	22	01E0H	000001E0H	nextPC
	Interrupt	INTP20/ INTCC20	CC2IC0	INTP20 pin/CC20 match	Pin/RPU	23	01F0H	000001F0H	nextPC
	Interrupt	INTP21/ INTCC21	CC2IC1	INTP21 pin/CC21 match	Pin/RPU	24	0200H	00000200H	nextPC
	Interrupt	INTP22/ INTCC22	CC2IC2	INTP22 pin/CC22 match	Pin/RPU	25	0210H	00000210H	nextPC
	Interrupt	INTP23/ INTCC23	CC2IC3	INTP23 pin/ CC23 match	Pin/RPU	26	0220H	00000220H	nextPC
	Interrupt	INTP24/ INTCC24	CC2IC4	INTP24 pin/ CC24 match	Pin/RPU	27	0230H	00000230H	nextPC
	Interrupt	INTP25/ INTCC25	CC2IC5	INTP25 pin CC25 match	Pin/RPU	28	0240H	00000240H	nextPC
	Interrupt	INTTM3	TM3IC0	TM3 overflow	RPU	29	0250H	00000250H	nextPC

Note n = 0 to FH

Table 7-1. Interrupt/Exception Source List (2/2)

Type	Classification	Interrupt/Exception Source				Default Priority	Exception Code	Handler Address	Restored PC
		Name	Controlling Register	Generating Source	Generating Unit				
Maskable	Interrupt	INTP30/ INTCC30	CC3IC0	INTP30 pin/CC30 match	Pin/RPU	30	0260H	00000260H	nextPC
	Interrupt	INTP31/ INTCC31	CC3IC1	INTP31 pin/CC31 match	Pin/RPU	31	0270H	00000270H	nextPC
	Interrupt	INTCM4	CM4IC0	CM4 match signal	RPU	32	0280H	00000280H	nextPC
	Interrupt	INTDMA0	DMAIC0	End of DMA0 transfer	DMA	33	0290H	00000290H	nextPC
	Interrupt	INTDMA1	DMAIC1	End of DMA1 transfer	DMA	34	02A0H	000002A0H	nextPC
	Interrupt	INTDMA2	DMAIC2	End of DMA2 transfer	DMA	35	02B0H	000002B0H	nextPC
	Interrupt	INTDMA3	DMAIC3	End of DMA3 transfer	DMA	36	02C0H	000002C0H	nextPC
	Interrupt	INTCREC	CANIC0	CAN1 reception complete	FCAN	37	02D0H	000002D0H	nextPC
	Interrupt	INTCTRX	CANIC1	CAN1 transmission complete	FCAN	38	02E0H	000002E0H	nextPC
	Interrupt	INTCERR	CANIC2	CAN1 communication error	FCAN	39	02F0H	000002F0H	nextPC
	Interrupt	INTCMAC	CANIC3	CAN illegal write	FCAN	40	0300H	00000300H	nextPC
	Interrupt	INTCSI0	CSIIC0	CSI0 transmission complete	SIO	41	0310H	00000310H	nextPC
	Interrupt	INTCSI1	CSIIC1	CSI1 reception complete	SIO	42	0320H	00000320H	nextPC
	Interrupt	INTSR0	SRIC0	UART0 reception complete	SIO	43	0330H	00000330H	nextPC
	Interrupt	INTST0	STIC0	UART0 transmission complete	SIO	44	0340H	00000340H	nextPC
	Interrupt	INTSER0	SEIC0	UART0 receiver error	SIO	45	0350H	00000350H	nextPC
	Interrupt	INTSR1	SRIC1	UART1 reception complete	SIO	46	0360H	00000360H	nextPC
	Interrupt	INTST1	STIC1	UART1 transmission complete	SIO	47	0370H	00000370H	nextPC
	Interrupt	INTSR2	SRIC2	UART2 reception complete	SIO	48	0380H	00000380H	nextPC
	Interrupt	INTST2	STIC2	UART2 transmission complete	SIO	49	0390H	00000390H	nextPC
	Interrupt	INTAD0	ADIC0	End of AD0 conversion	ADC	50	03A0H	000003A0H	nextPC
	Interrupt	INTAD1	ADIC1	End of AD0 conversion	ADC	51	03B0H	000003B0H	nextPC

Remarks 1. Default priority: The priority order when two or more maskable interrupt requests are generated at the same time. The highest priority is 0.

Restored PC: The value of the PC saved to EIPC or FEPC when interrupt/exception processing is started. However, the value of the PC saved when an interrupt is acknowledged during division (DIV, DIVH, DIVU, DIVHU) instruction execution is the value of the PC of the current instruction (DIV, DIVH, DIVU, DIVHU).

nextPC: The PC value that starts the processing following interrupt/exception processing.

2. The execution address of the illegal instruction when an illegal opcode exception occurs is calculated by (Restored PC – 4).

7.2 Non-Maskable Interrupt

A non-maskable interrupt request is acknowledged unconditionally, even when interrupts are in the interrupt disabled (DI) status. An NMI is not subject to priority control and takes precedence over all the other interrupts.

A non-maskable interrupt request is input from the NMI pin. When the valid edge specified by bit 0 (ESN0) of the external interrupt mode register 0 (INTM0) is detected on the NMI pin, the interrupt occurs.

While the service program of the non-maskable interrupt is being executed (PSW.NP = 1), the acknowledgement of another non-maskable interrupt request is held pending. The pending NMI is acknowledged after the original service program of the non-maskable interrupt under execution has been terminated (by the RETI instruction), or when PSW.NP is cleared to 0 by the LDSR instruction. Note that if two or more NMI requests are input during the execution of the service program for an NMI, the number of NMIs that will be acknowledged after PSW.NP is cleared to 0 is only one.

Remark PSW.NP: The NP bit of the PSW register.

7.2.1 Operation

If a non-maskable interrupt is generated, the CPU performs the following processing, and transfers control to the handler routine:

(1) Saves the restored PC to FEPC.
(2) Saves the current PSW to FEPSW.
(3) Writes exception code 0010H to the higher halfword (FECC) of ECR.
(4) Sets the NP and ID bits of the PSW and clears the EP bit.
(5) Sets the handler address (00000010H) corresponding to the non-maskable interrupt to the PC, and transfers control.

The processing configuration of a non-maskable interrupt is shown in Figure 7-1.

Figure 7-1. Processing Configuration of Non-Maskable Interrupt

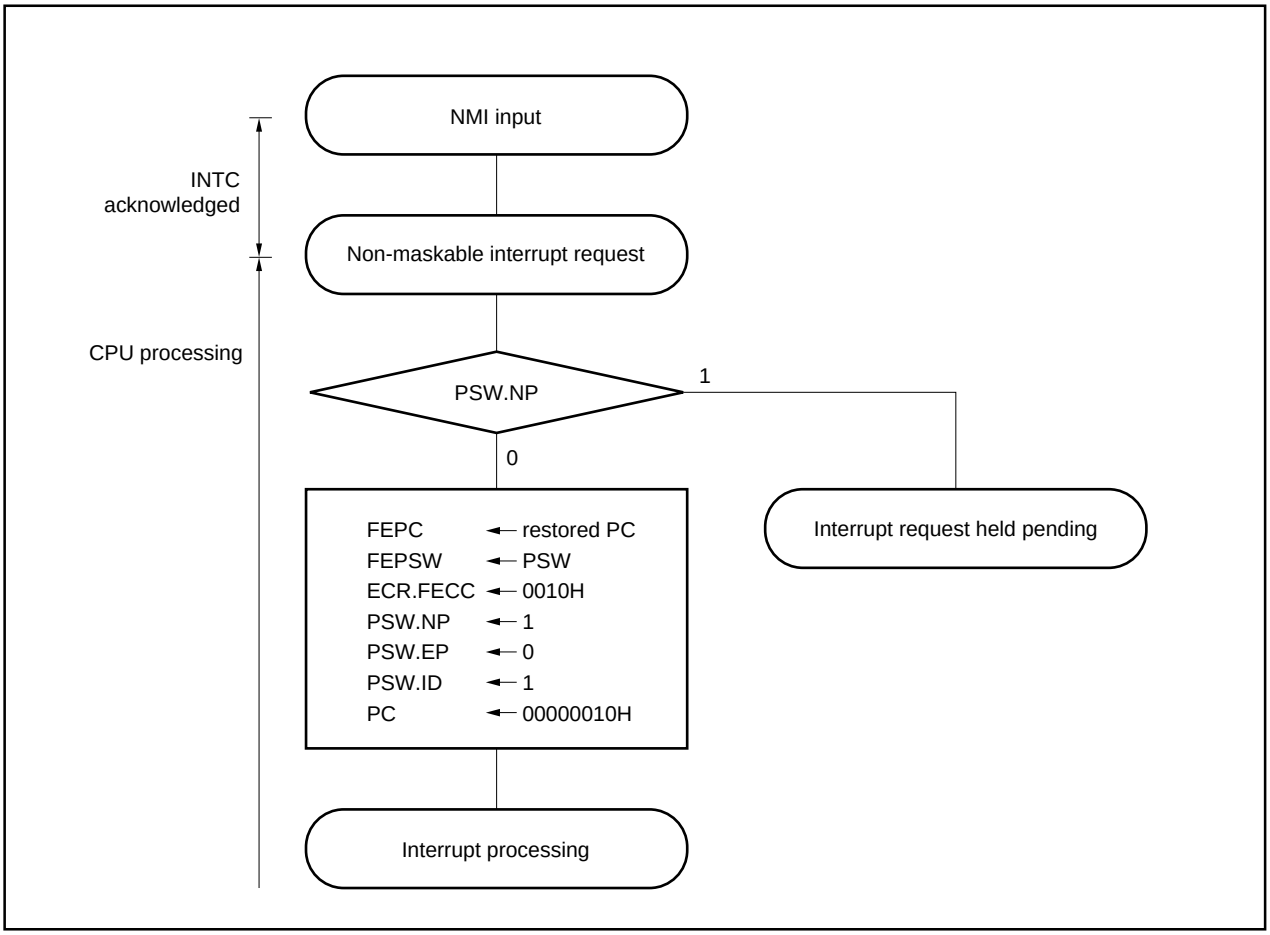
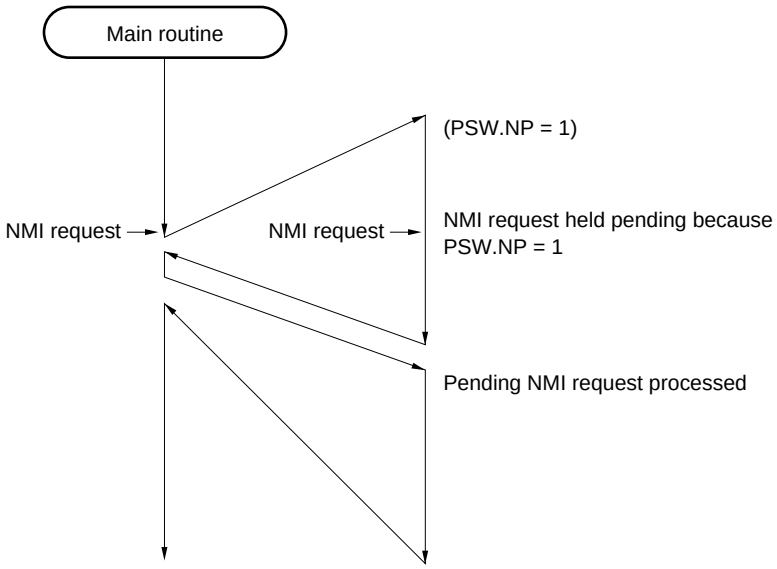
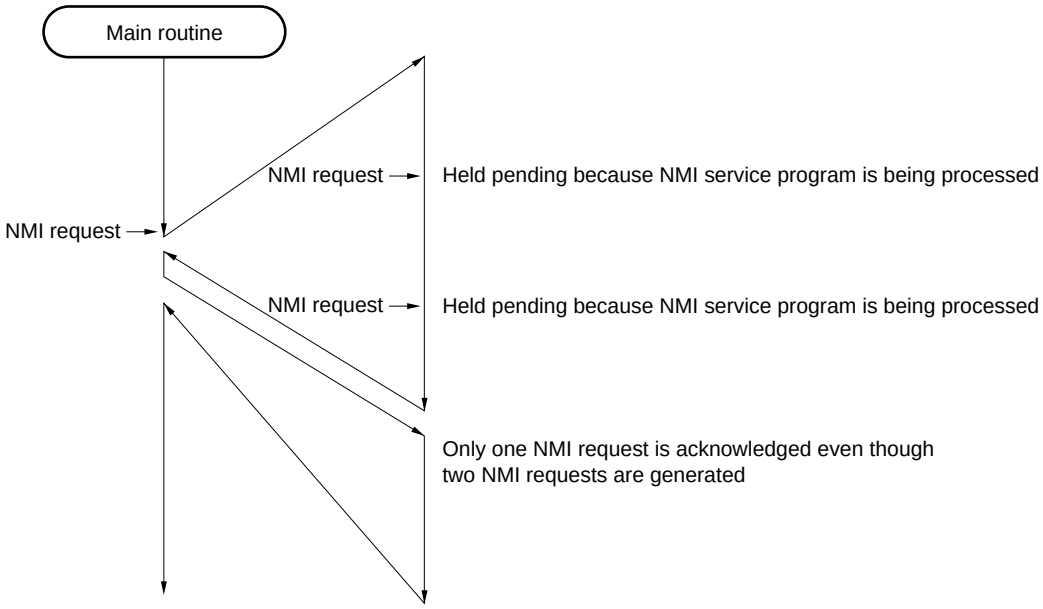


Figure 7-2. Acknowledging Non-Maskable Interrupt Request

(a) If a new NMI request is generated while an NMI service program is being executed



(b) If a new NMI request is generated twice while an NMI service program is being executed



7.2.2 Restore

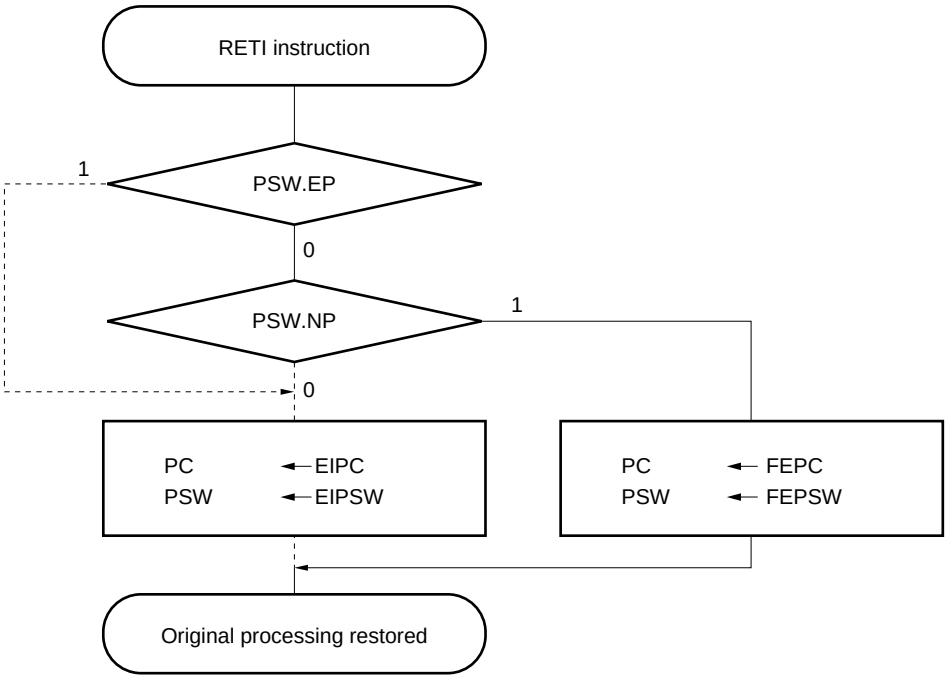
Execution is restored from the non-maskable interrupt processing by the RETI instruction.

When the RETI instruction is executed, the CPU performs the following processing, and transfers control to the address of the restored PC.

(1) Restores the values of the PC and the PSW from FEPC and FEPSW, respectively, because the EP bit of the PSW is 0 and the NP bit of the PSW is 1.
(2) Transfers control back to the address of the restored PC and PSW.

Figure 7-3 illustrates how the RETI instruction is processed.

Figure 7-3. RETI Instruction Processing



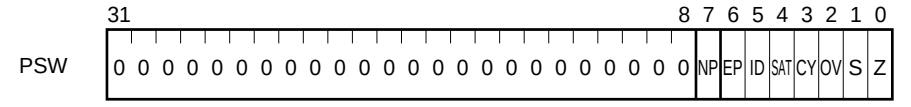
Caution When the PSW.EP bit and PSW.NP bit are changed by the LDSR instruction during non-maskable interrupt processing, in order to restore the PC and PSW correctly during recovery by the RETI instruction, it is necessary to set PSW.EP back to 0 and PSW.NP back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The broken lines show the CPU processing flow.

7.2.3 Non-maskable interrupt status flag (NP)

The NP flag is a status flag that indicates that non-maskable interrupt (NMI) processing is under execution.

This flag is set when an NMI interrupt has been acknowledged, and masks all interrupt requests and exceptions to prohibit multiple interrupts from being acknowledged.



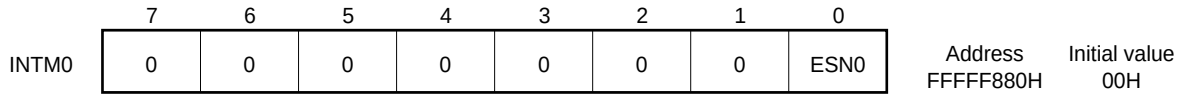
Bit Position	Bit Name	Function
7	NP	Indicates whether NMI interrupt processing is in progress. 0: No NMI interrupt processing 1: NMI interrupt currently being processed

7.2.4 Edge detection function

External interrupt mode register 0 (INTM0) is a register that specifies the valid edge of a non-maskable interrupt (NMI). The NMI valid edge can be specified to be either the rising edge or the falling edge by the ESN0 bit.

This register can be read/written in 8-bit or 1-bit units.

Figure 7-4. External Interrupt Mode Register 0 (INTM0)



Bit Position	Bit Name	Function
0	ESN0	Specifies the NMI pin's valid edge. 0: Falling edge 1: Rising edge

7.3 Maskable Interrupts

Maskable interrupt requests can be masked by interrupt control registers. The V850E/IA1 has 52 maskable interrupt sources.

If two or more maskable interrupt requests are generated at the same time, they are acknowledged according to the default priority. In addition to the default priority, eight levels of priorities can be specified by using the interrupt control registers (programmable priority control).

When an interrupt request has been acknowledged, the acknowledgement of other maskable interrupt requests is disabled and the interrupt disabled (DI) status is set.

When the EI instruction is executed in an interrupt processing routine, the interrupt enabled (EI) status is set, which enables servicing of interrupts having a higher priority than the interrupt request in progress (specified by the interrupt control register). Note that only interrupts with a higher priority will have this capability; interrupts with the same priority level cannot be nested.

However, if multiple interrupts are executed, the following processing is necessary.

<1> Save EIPC and EIPSW in memory or a general-purpose register before executing the EI instruction.
<2> Execute the DI instruction before executing the RETI instruction, then reset EIPC and EIPSW with the values saved in <1>.

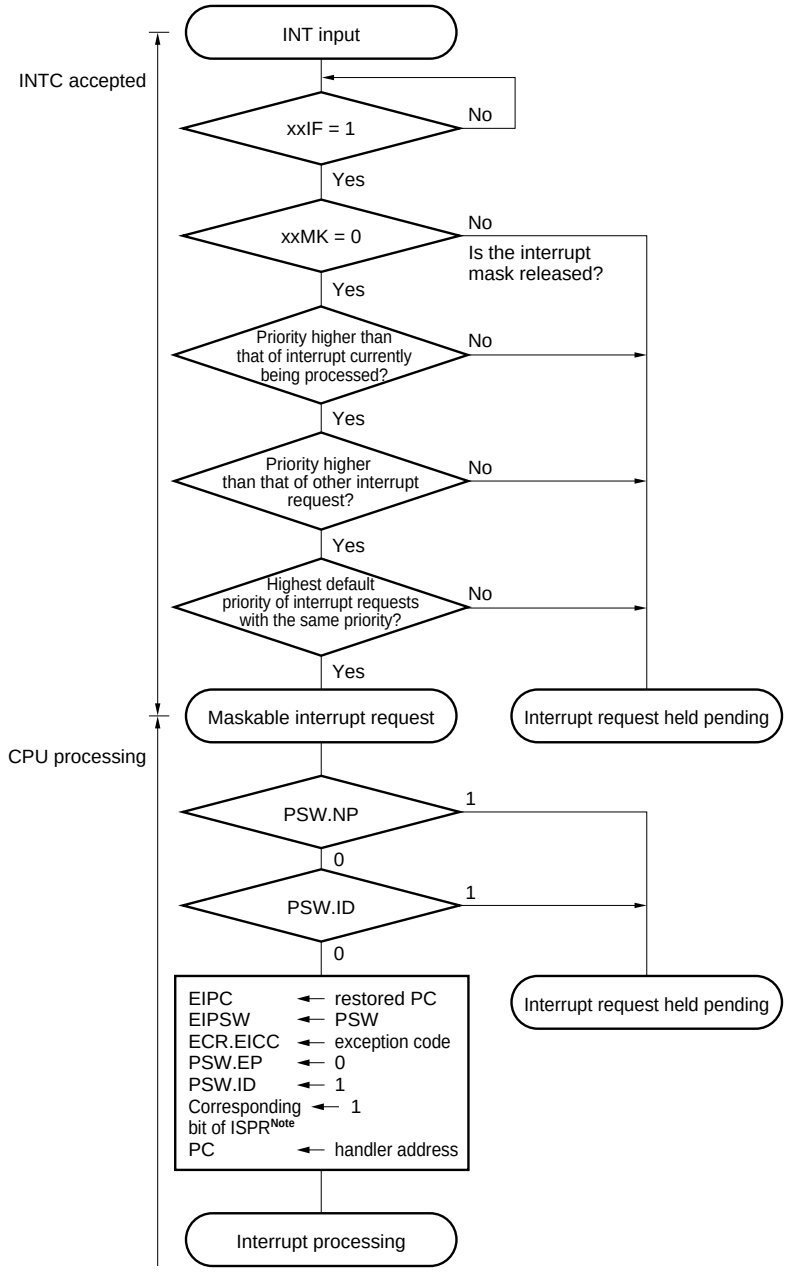
7.3.1 Operation

If a maskable interrupt occurs by INT input, the CPU performs the following processing, and transfers control to a handler routine:

(1) Saves the restored PC to EIPC.
(2) Saves the current PSW to EIPSW.
(3) Writes an exception code to the lower halfword of ECR (EICC).
(4) Sets the ID bit of the PSW and clears the EP bit.
(5) Sets the handler address corresponding to each interrupt to the PC, and transfers control.

The processing configuration of a maskable interrupt is shown in Figure 7-5.

Figure 7-5. Maskable Interrupt Processing



Note For the ISPR register, see **7.3.6 In-service priority register (ISPR)**.

The INT input masked by the interrupt controllers and the INT input that occurs while another interrupt is being processed (when PSW.NP = 1 or PSW.ID = 1) are held pending internally by the interrupt controller. In such case, if the interrupts are unmasked, or when PSW.NP = 0 and PSW.ID = 0 as set by the RETI and LDSR instructions, input of the pending INT starts the new maskable interrupt processing.

7.3.2 Restore

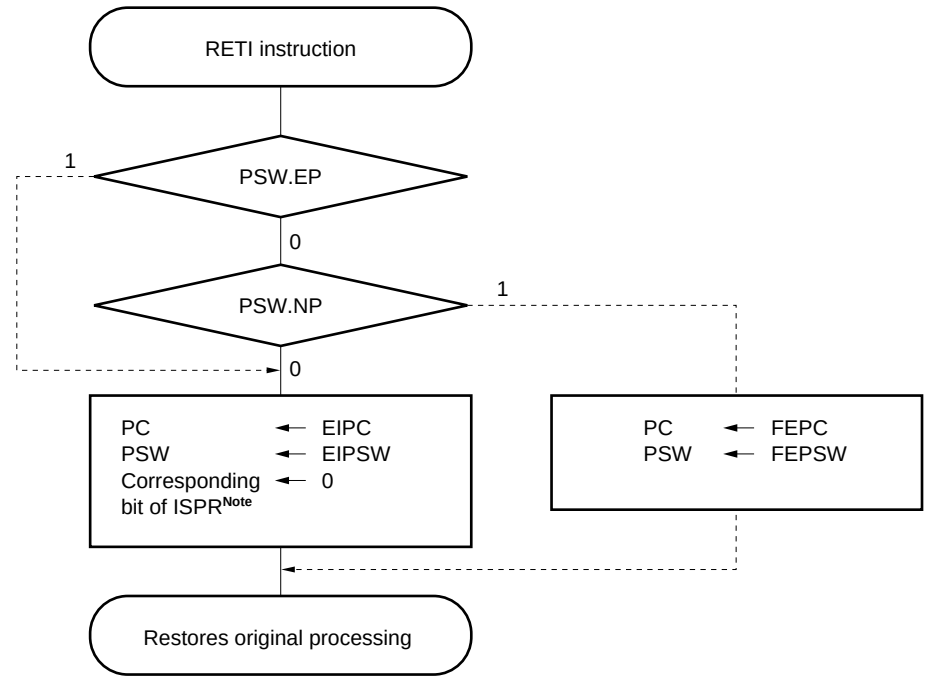
Recovery from maskable interrupt processing is carried out by the RETI instruction.

When the RETI instruction is executed, the CPU performs the following steps, and transfers control to the address of the restored PC.

(1) Restores the values of the PC and the PSW from EIPC and EIPSW because the EP bit of the PSW is 0 and the NP bit of the PSW is 0.
(2) Transfers control to the address of the restored PC and PSW.

Figure 7-6 illustrates the processing of the RETI instruction.

Figure 7-6. RETI Instruction Processing



Note For the ISPR register, see **7.3.6 In-service priority register (ISPR)**.

Caution When the PSW.EP bit and the PSW.NP bit are changed by the LDSR instruction during maskable interrupt processing, in order to restore the PC and PSW correctly during recovery by the RETI instruction, it is necessary to set PSW.EP back to 0 and PSW.NP back to 0 using the LDSR instruction immediately before the RETI instruction.

Remark The broken lines show the CPU processing flow.

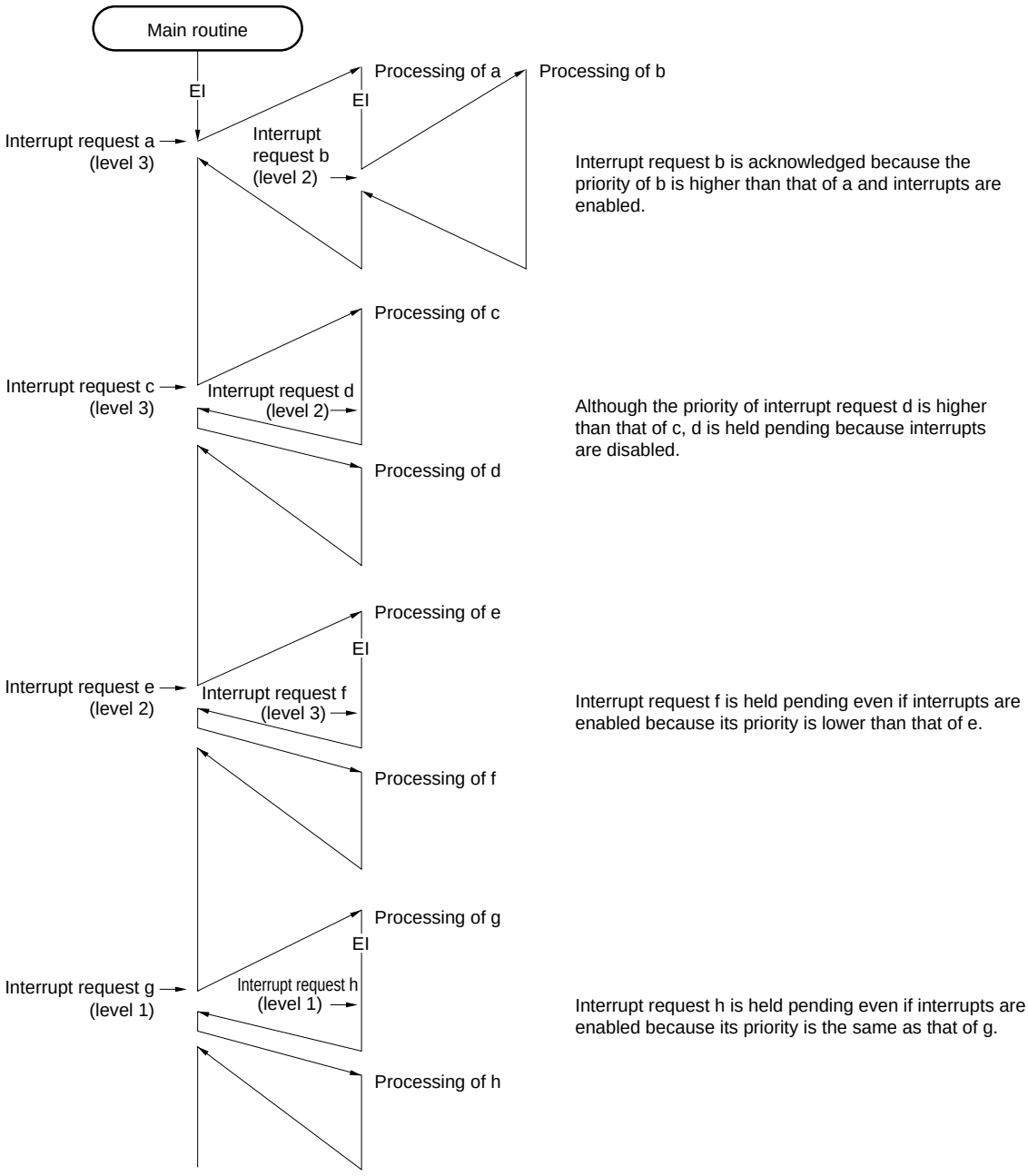
7.3.3 Priorities of maskable interrupts

The V850E/IA1 provides multiple interrupt servicing in which an interrupt is acknowledged while another interrupt is being serviced. Multiple interrupts can be controlled by priority levels.

There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels that are specified by the interrupt priority level specification bit (xxPRn) of the interrupt control register (xxICn). When two or more interrupts having the same priority level specified by the xxPRn bit are generated at the same time, interrupts are serviced in order depending on the priority level allocated to each interrupt request type (default priority level) beforehand. For more information, refer to **Table 7-1 Interrupt/Exception Source List**. The programmable priority control customizes interrupt requests into eight levels by setting the priority level specification flag.

Note that when an interrupt request is acknowledged, the ID flag of PSW is automatically set to 1. Therefore, when multiple interrupts are to be used, clear the ID flag to 0 beforehand (for example, by placing the EI instruction in the interrupt service program) to set the interrupt enable mode.

Figure 7-7. Example of Processing in Which Another Interrupt Request Is Issued While an Interrupt Is Being Processed (1/2)



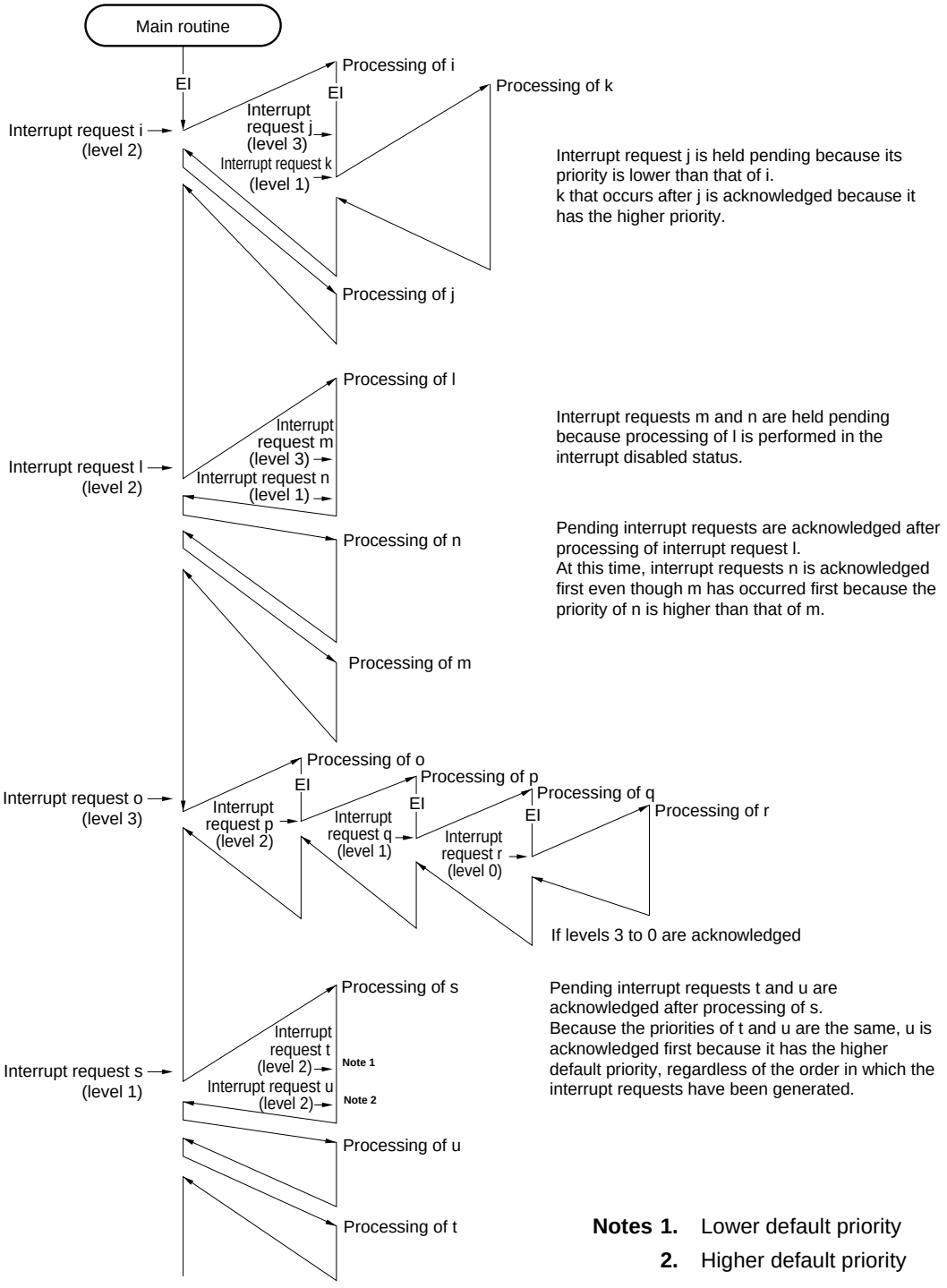
Caution The values of the EIPC and EIPSW registers must be saved before executing multiple interrupts.

When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

Remarks 1. a to u in the figure are the temporary names of interrupt requests shown for the sake of explanation.

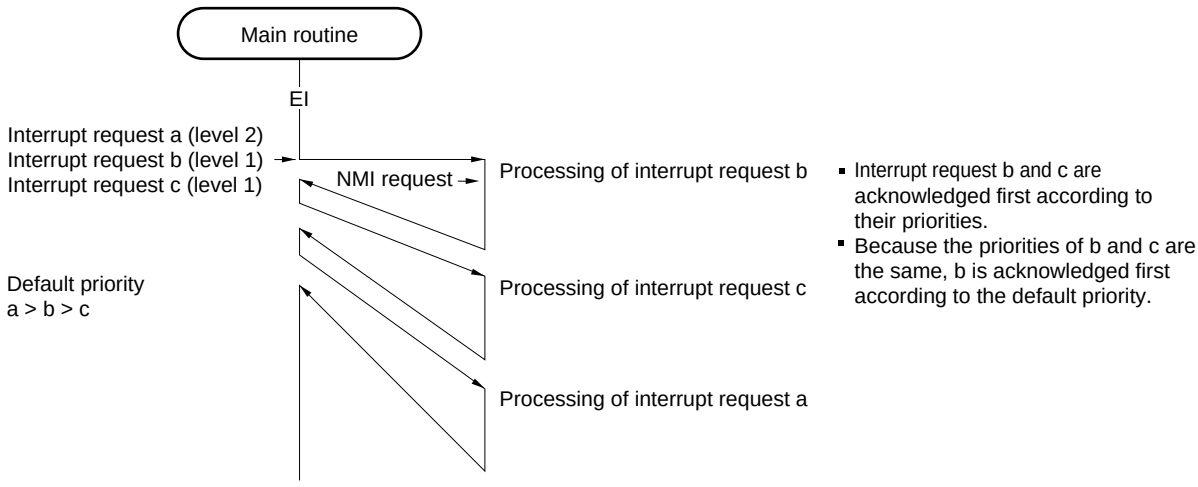
2. The default priority in the figure indicates the relative priority between two interrupt requests.

Figure 7-7. Example of Processing in Which Another Interrupt Request Is Issued While an Interrupt Is Being Processed (2/2)



Caution The values of the EIPC and EIPSW registers must be saved before executing multiple interrupts. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

Figure 7-8. Example of Processing Interrupt Requests Simultaneously Generated



Caution The values of the EIPC and EIPSW registers must be saved before executing multiple interrupts. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

7.3.4 Interrupt control register (xxICn)

An interrupt control register is assigned to each interrupt request (maskable interrupt) and sets the control conditions for each maskable interrupt request.

This register can be read/written in 8-bit or 1-bit units.

Figure 7-9. Interrupt Control Register (xxICn)

	7	6	5	4	3	2	1	0	Address	Initial value
xxICn	xxIFn	xxMKn	0	0	0	xxPRn2	xxPRn1	xxPRn0	FFFFF110H to FFFF176H	47H

Bit Position	Bit Name	Function
7	xxIFn	This is an interrupt request flag. 0: Interrupt request not issued 1: Interrupt request issued The flag xxIFn is reset automatically by the hardware if an interrupt request is acknowledged.
6	xxMKn	This is an interrupt mask flag. 0: Enables interrupt processing 1: Disables interrupt processing (pending)
2 to 0	xxPRn2 to xxPRn0	8 levels of priority order are specified for each interrupt.

xxPRn2	xxPRn1	xxPRn0	Interrupt Priority Specification Bit
0	0	0	Specifies level 0 (highest).
0	0	1	Specifies level 1.
0	1	0	Specifies level 2.
0	1	1	Specifies level 3.
1	0	0	Specifies level 4.
1	0	1	Specifies level 5.
1	1	0	Specifies level 6.
1	1	1	Specifies level 7 (lowest).

Remark xx: Identification name of each peripheral unit (P0, DET, TM0, TM2, TM3, CM03, CM10, CM11, CM4, CC10, CC11, CC2, CC3, DMA, CAN, CSI, SR, ST, SE, AD)

n: Peripheral unit number (Refer to **Table 7-2**).

The address and bit of each interrupt control register are as follows:

Table 7-2. Addresses and Bits of Interrupt Control Registers (1/2)

Address	Register	Bit							
		7	6	5	4	3	2	1	0
FFFFF110H	P0IC0	P0IF0	P0MK0	0	0	0	P0PR02	P0PR01	P0PR00
FFFFF112H	P0IC1	P0IF1	P0MK1	0	0	0	P0PR12	P0PR11	P0PR10
FFFFF114H	P0IC2	P0IF2	P0MK2	0	0	0	P0PR22	P0PR21	P0PR20
FFFFF116H	P0IC3	P0IF3	P0MK3	0	0	0	P0PR32	P0PR31	P0PR30
FFFFF118H	P0IC4	P0IF4	P0MK4	0	0	0	P0PR42	P0PR41	P0PR40
FFFFF11AH	P0IC5	P0IF5	P0MK5	0	0	0	P0PR52	P0PR51	P0PR50
FFFFF11CH	P0IC6	P0IF6	P0MK6	0	0	0	P0PR62	P0PR61	P0PR60
FFFFF11EH	DETIC0	DETIF0	DETMK0	0	0	0	DETPR02	DETPR01	DETPR00
FFFFF120H	DETIC1	DETIF1	DETMK1	0	0	0	DETPR12	DETPR11	DETPR10
FFFFF122H	TM0IC0	TM0IF0	TM0MK0	0	0	0	TM0PR02	TM0PR01	TM0PR00
FFFFF124H	CM3IC0	CM03IF0	CM03MK0	0	0	0	CM03PR02	CM03PR01	CM03PRC0
FFFFF126H	TM0IC1	TM0IF1	TM0MK1	0	0	0	TM0PR12	TM0PR11	TM0PR10
FFFFF128H	CM03IC1	CM03IF1	CM03MK1	0	0	0	CM03PR12	CM03PR11	CM03PR10
FFFFF12AH	CC10IC0	CC10IF0	CC10MK0	0	0	0	CC10PR02	CC10PR01	CC10PR00
FFFFF12CH	CC1ClC1	CC10IF1	CC10MK1	0	0	0	CC10PR12	CC10PR11	CC10PR10
FFFFF12EH	CM10IC0	CM10IF0	CM10MK0	0	0	0	CM10PR02	CM10PR01	CM10PR00
FFFFF130H	CM10IC1	CM10IF1	CM10MK1	0	0	0	CM10PR12	CM10PR11	CM10PR10
FFFFF132H	CC11IC0	CC11IF0	CC11MK0	0	0	0	CC11PR02	CC11PR01	CC11PR00
FFFFF134H	CC11IC1	CC11IF1	CC11MK1	0	0	0	CC11PR12	CC11PR11	CC11PR10
FFFFF136H	CM11IC0	CM11IF0	CM11MK0	0	0	0	CM11PR02	CM11PR01	CM11PR00
FFFFF138H	CM11IC1	CM11IF1	CM11MK1	0	0	0	CM11PR12	CM11PR11	CM11PR10
FFFFF13AH	TM2IC0	TM2IF0	TM2MK0	0	0	0	TM2PR02	TM2PR01	TM2PR00
FFFFF13CH	TM2IC1	TM2IF1	TM2MK1	0	0	0	TM2PR12	TM2PR11	TM2PR10
FFFFF13EH	CC2IC0	CC2IF0	CC2MK0	0	0	0	CC2PR02	CC2PR01	CC2PR00
FFFFF140H	CC2IC1	CC2IF1	CC2MK1	0	0	0	CC2PR12	CC2PR11	CC2PR10
FFFFF142H	CC2IC2	CC2IF2	CC2MK2	0	0	0	CC2PR22	CC2PR21	CC2PR20
FFFFF144H	CC2IC3	CC2IF3	CC2MK3	0	0	0	CC2PR32	CC2PR31	CC2PR30
FFFFF146H	CC2IC4	CC2IF4	CC2MK4	0	0	0	CC2PR42	CC2PR41	CC2PR40
FFFFF148H	CC2IC5	CC2IF5	CC2MK5	0	0	0	CC2PR52	CC2PR51	CC2PR50
FFFFF14AH	TM3IC0	TM3IF0	TM3MK0	0	0	0	TM3PR02	TM3PR01	TM3PR00
FFFFF14CH	CC3IC0	CC3IF0	CC3MK0	0	0	0	CC3PR02	CC3PR01	CC3PR00
FFFFF14EH	CC3IC1	CC3IF1	CC3MK1	0	0	0	CC3PR12	CC3PR11	CC3PR10
FFFFF150H	CM4IC0	CM4IF0	CM4MK0	0	0	0	CM4PR02	CM4PR01	CM4PR00
FFFFF152H	DMAIC0	DMAIF0	DMAMK0	0	0	0	DMAPR02	DMAPR01	DMAPR00
FFFFF154H	DMAIC1	DMAIF1	DMAMK1	0	0	0	DMAPR12	DMAPR11	DMAPR10
FFFFF156H	DMAIC2	DMAIF2	DMAMK2	0	0	0	DMAPR22	DMAPR21	DMAPR20
FFFFF158H	DMAIC3	DMAIF3	DMAMK3	0	0	0	DMAPR32	DMAPR31	DMAPR30
FFFFF15AH	CANIC0	CANIF0	CANMK0	0	0	0	CANPR02	CANPR01	CANPR00
FFFFF15CH	CANIC1	CANIF1	CANMK1	0	0	0	CANPR12	CANPR11	CANPR10
FFFFF15EH	CANIC2	CANIF2	CANIF2	0	0	0	CANPR22	CANPR21	CANPR20
FFFFF160H	CANIC3	CANIF3	CANMK3	0	0	0	CANPR32	CANPR31	CANPR30
FFFFF162H	CSIIC0	CSIIF0	CSIMK0	0	0	0	CSIPR02	CSIPR01	CSIPR00

Table 7-2. Addresses and Bits of Interrupt Control Registers (2/2)

Address	Register	Bit							
		7	6	5	4	3	2	1	0
FFFFF164H	CSIIC1	CSIIF1	CSIMK1	0	0	0	CSIPR12	CSIPR11	CSIPR10
FFFFF166H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF168H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF16AH	SEIC0	SEIF0	SEMK0	0	0	0	SEPR02	SEPR01	SEPR00
FFFFF16CH	SRIC1	SRIF1	SRMK1	0	0	0	SRPR12	SRPR11	SRPR10
FFFFF16EH	STIC1	STIF1	STMK1	0	0	0	STPR12	STPR11	STPR10
FFFFF170H	SRIC2	SRIF2	SRMK2	0	0	0	SRPR22	SRPR21	SRPR20
FFFFF172H	STIC2	STIF2	STMK2	0	0	0	STPR22	STPR21	STPR20
FFFFF174H	ADIC0	ADIF0	ADMK0	0	0	0	ADPR02	ADPR01	ADPR00
FFFFF176H	ADIC1	ADIF1	ADMK1	0	0	0	ADPR12	ADPR11	ADPR10

7.3.5 Interrupt mask registers 0 to 3 (IMR0 to IMR3)

These registers set the interrupt mask state for the maskable interrupts.

The xxMKn bit of the IMR0 to IMR3 registers is equivalent to the xxMKn bit of the xxICn register.

IMRm can be read/written in 16-bit units (m = 0 to 3).

When the IMRm register is divided into two registers: higher 8 bits (IMRmH register) and lower 8 bits (IMRmL register), these registers can be read/written in 8-bit or 1-bit units (m = 0 to 3).

Figure 7-10. Interrupt Mask Registers 0 to 3 (IMR0 to IMR3)

	15	14	13	12	11	10	9	8	Address	Initial value
IMR0	CM10MK0	CC10MK1	CC10MK0	CM03MK1	TM0MK1	CM03MK0	TM0MK0	DETMK1	FFFFF100H	FFFFH
	7	6	5	4	3	2	1	0		
	DETMK0	P0MK6	P0MK5	P0MK4	P0MK3	P0MK2	P0MK1	P0MK0		

	15	14	13	12	11	10	9	8	Address	Initial value
IMR1	CC3MK1	CC3MK0	TM3MK0	CC2MK5	CC2MK4	CC2MK3	CC2MK2	CC2MK1	FFFFF102H	FFFFH
	7	6	5	4	3	2	1	0		
	CC2MK0	TM2MK1	TM2MK0	CM11MK1	CM11MK0	CC11MK1	CC11MK0	CM10MK1		

	15	14	13	12	11	10	9	8	Address	Initial value
IMR2	STMK1	SRMK1	SEMK0	STMK0	SRMK0	CSIMK1	CSIMK0	CANMK3	FFFFF104H	FFFFH
	7	6	5	4	3	2	1	1		
	CANMK2	CANMK1	CANMK0	DMAMK3	DMAMK2	DMAMK1	DMAMK0	CM4MK0		

	15	14	13	12	11	10	9	8	Address	Initial value
IMR3	1	1	1	1	1	1	1	1	FFFFF106H	FFFFH
	7	6	5	4	3	2	1	0		
	1	1	1	1	ADMK1	ADMK0	STMK2	SRMK2		

Bit Position	Bit Name	Function
15 to 0 (IMR0 to 2), 0 to 3 (IMR3)	xxMKn	Interrupt mask flag 0: Interrupt servicing enabled 1: Interrupt servicing disabled (pending)

Remark xx: Identification name of each peripheral unit (P0, DET, TM0, TM2, TM3, CM03, CM10, CM11, CM4, CC10, CC11, CC2, CC3, DMA, CAN, CSI, SR, ST, SE, and AD).

n: Peripheral unit number (See **Table 7-2**)

7.3.6 In-service priority register (ISPR)

This register holds the priority level of the maskable interrupt currently acknowledged. When an interrupt request is acknowledged, the bit of this register corresponding to the priority level of that interrupt request is set to 1 and remains set while the interrupt is serviced.

When the RETI instruction is executed, the bit corresponding to the interrupt request having the highest priority is automatically reset to 0 by hardware. However, it is not reset to 0 when execution is returned from non-maskable interrupt servicing or exception processing.

This register is read-only in 8-bit or 1-bit units.

Figure 7-11. In-Service Priority Register (ISPR)

	7	6	5	4	3	2	1	0	Address	Initial value
ISPR	ISPR7	ISPR6	ISPR5	ISPR4	ISPR3	ISPR2	ISPR1	ISPR0	FFFFF1FAH	00H

Bit Position	Bit Name	Function
7 to 0	ISPR7 to ISPR0	Indicates priority of interrupt currently acknowledged 0: Interrupt request with priority n not acknowledged 1: Interrupt request with priority n acknowledged

Remark n = 0 to 7 (priority level)

7.3.7 Maskable interrupt status flag (ID)

The ID flag is bit 5 of the PSW and this controls the maskable interrupt's operating state, and stores control information regarding enabling or disabling of interrupt requests.

Figure 7-12. Maskable Interrupt Status Flag (ID)

	31	8	7	6	5	4	3	2	1	0	Initial value
PSW	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		NP	EP	ID	SAT	CY	OV	S	Z	00000020H

Bit Position	Bit Name	Function
5	ID	Indicates whether maskable interrupt processing is enabled or disabled. 0: Maskable interrupt request acknowledgement enabled 1: Maskable interrupt request acknowledgement disabled (pending) This bit is set to 1 by the DI instruction and reset to 0 by the EI instruction. Its value is also modified by the RETI instruction or LDSR instruction when referencing the PSW. Non-maskable interrupt requests and exceptions are acknowledged regardless of this flag. When a maskable interrupt is acknowledged, the ID flag is automatically set to 1 by hardware. The interrupt request generated during the acknowledgement disabled period (ID = 1) is acknowledged when the xxIFn bit of xxICn register is set to 1, and the ID flag is reset to 0.

7.3.8 Interrupt trigger mode selection

The valid edge of the INTPn, ADTRG0, ADTRG1, TIUD10, TIUD11, TCUD10, TCUD11, TCLR10, TCLR11, TCLR3, and TI3 pins can be selected by program. The edge that can be selected as the valid edge is one of the following (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111).

- Rising edge
- Falling edge
- Both the rising and falling edges

When the INTPn, ADTRG0, ADTRG1, TIUD10, TIUD11, TCUD10, TCUD11, TCLR10, TCLR11, TCLR3, and TI3 signals are edge-detected, they become an interrupt source or capture trigger.

The valid edge is specified by external interrupt mode registers 1 and 2 (INTM1 and INTM2), signal edge selection registers 10 and 11 (SESA10 and SESA11), the valid edge selection register (SESC), and TM2 input filter mode registers 0 to 5 (FEM0 to FEM5).

(1) External interrupt mode registers 1, 2 (INTM1, INTM2)

These registers specify the valid edge for external interrupt requests (INTP0 to INTP6), input via external pins.

The correspondence between each register and the external interrupt requests that register controls is shown below.

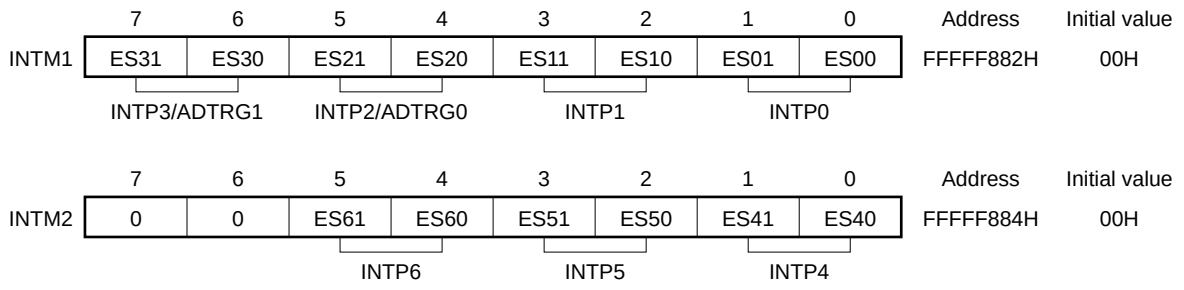
- INTM1: INTP0, INTP1, INTP2/ADTRG0, INTP3/ADTRG1
- INTM2: INTP4 to INTP6

INTP2 and INTP3 function alternately as ADTRG0 and ADTRG1 (A/D converter external trigger input). Therefore, if the external trigger mode has been set by the TRG0 to TRG2 bits of A/D converter mode register n0 (ADSCMn0), setting the ES20 and ES21, and ES30 and ES31 bits of INTM1 also specifies the valid edge of the external trigger input (ADTRG0 and ADTRG1).

The valid edge can be specified independently for each pin (rising edge, falling edge, or both rising and falling edges).

These registers can be read/written in 8-bit or 1-bit units.

Figure 7-13. External Interrupt Mode Registers 1, 2 (INTM1, INTM2)



Bit Position	Bit Name	Function
7 to 0 (INTM1), 5 to 0 (INTM2)	ESn1, ESn2 (n = 0 to 6)	Specifies the valid edge of the INTPn, ADTRG0 and ADTRG1 pins.

ESn1	ESn0	Operation
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

(2) Signal edge selection registers 10, 11 (SESA10, SESA11)

These registers specify the valid edge of external interrupt requests (INTP100, INTP101, INTP110, INTP111, TIUD10, TIUD11, TCUD10, TCUD11, TCLR10, and TCLR11), input via external pins. The correspondence between each register and the external interrupt requests that register controls is shown below.

- SESA10: TIUD10, TCUD10, TCLR10, INTP100, INTP101
- SESA11: TIUD11, TCUD11, TCLR11, INTP110, INTP111

The valid edge can be specified independently for each pin (rising edge, falling edge, or both rising and falling edges).

These registers can be read/written in 8-bit or 1-bit units.

Cautions 1. The bits of the SESA1n register cannot be changed during TM1n operation (CE1 bit = 1).

2. Timer control registers 10 and 11 (TMC10, TMC11) must be set (1) before using the TCUD10/INTP100, TCLR10/INTP101, TCUD11/INTP110, and TCLR11/INTP111 pins as INTP100, INTP101, and INTP111, even if not using timer 1.

Figure 7-14. Signal Edge Selection Registers 10, 11 (SESA10, SESA11) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
SESA10	TESUD01	TESUD00	CESUD01	CESUD00	IES1011	IES1010	IES1001	IES1000	FFFFF5EDH	00H
	TIUD10, TCUD10		TCLR10		INTP101		INTP100			

	7	6	5	4	3	2	1	0	Address	Initial value
SESA11	TESUD11	TESUD10	CESUD11	CESUD10	IES1111	IES1110	IES1101	IES1100	FFFFF60DH	00H
	TIUD11, TCUD11		TCLR11		INTP111		INTP110			

Bit Position	Bit Name	Function
7, 6	TESUDn1, TESUDn0	Specifies the valid edge of the TIUD10, TIUD11, TCUD10, TCUD11 pins.

TESUDn1	TESUDn0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Remark n = 0, 1

Figure 7-14. Signal Edge Selection Registers 10, 11 (SESA10, SESA11) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>7, 6</td><td>TESUDn1,
TESUDn0</td><td>Cautions 1. The values set to the TESUDn1 and TESUDn0 bits are valid only in UDC mode A[Note 1] and UDC mode B[Note 1].
2. If TM1n operation has been specified in mode 4[Note 2], the valid edge specification for the TIUD1n and TCUD1n pins is invalid.</td></tr>
<tr><td>5, 4</td><td>CESUDn1,
CESUDn0</td><td>Specifies the valid edge of the TLCR10, TLCR11 pins
<table><tr><th>CESUDn1</th><th>CESUDn0</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Low level</td></tr><tr><td>1</td><td>1</td><td>High level</td></tr></table>The setting values of the CESUDn1 and CESUDn0 bits and the operation of TM1n are as follows.
00: TM1n cleared after detection of TCLR1n rising edge
01: TM1n cleared after detection of TCLR1n falling edge
10: TM1n holds cleared status while TCLR1n input is low level
11: TM1n holds cleared status while TCLR1n input is high level

Caution The values set to the CESUDn1 and CESUDn0 bits are valid only in UDC mode A[Note 1].</td></tr>
<tr><td>3, 2</td><td>IES1n11,
IES1n10</td><td>Specifies the valid edge of the INTP101, INTP111 pins
<table><tr><th>IES1n11</th><th>IES1n10</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>1</td><td>1</td><td>Both rising and falling edges</td></tr></table></td></tr>
<tr><td>1, 0</td><td>IES1n01,
IES1n00</td><td>Specifies the valid edge of the INTP100, INTP110 pins
<table><tr><th>IES1n01</th><th>IES1n00</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>1</td><td>1</td><td>Both rising and falling edges</td></tr></table></td></tr>
</table>

Remark n = 0, 1

Notes 1. See Figure 9-54. Timer Unit Mode Registers 0, 1 (TUM0, TUM1)

2. See Figure 9-58. Prescaler Mode Registers 10, 11 (PRM10, PRM11)

(3) Valid edge selection register (SESC)

This register specifies the valid edge for external interrupt requests (INTP30, INTP31, TCLR3, TI3), input via external pins.

The valid edge can be specified independently for each pin (rising edge, falling edge, or both rising and falling edges).

This register can be read/written in 8-bit or 1-bit units.

Caution Timer control register 30 (TMC30) must be set (1) before using the TI3/TCLR3/INTP30 and TO3/INTP31 pins as INTP30 and INTP3, even if not using timer 3.

Figure 7-15. Valid Edge Selection Register (SESC)

	7	6	5	4	3	2	1	0	Address	Initial value
SESC	TES31	TES30	CES31	CES30	IES311	IES310	IES301	IES300	FFFFF689H	00H
	TI3		TCLR3		INTP31		INTP30			

Bit Position	Bit Name	Function
7, 6	TES31, TES30	Specifies the valid edge of the INTP30, INTP31, TLCR3, TI3 pins.
5, 4	CES31, CES30	
3, 2	IES311, IES310	
1, 0	TES301, TES300	

xESn1	xESn0	Operation
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Remark n = 3, 30, 31

(4) Timer 2 input filter mode registers 0 to 5 (FEM0 to FEM5)

These registers specify the valid edge for external interrupts input to timer 2 (INTP20 to INTP25). The correspondence between each register and the external interrupt request that register controls is shown below.

- FEM0: INTP20
- FEM1: INTP21
- FEM2: INTP22
- FEM3: INTP23
- FEM4: INTP24
- FEM5: INTP25

The valid edge can be specified independently for each pin (rising edge, falling edge, or both rising and falling edges).

These registers can be read/written in 8-bit or 1-bit units.

Figure 7-16. Timer 2 Input Filter Mode Registers 0 to 5 (FEM0 to FEM5) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
FEM0	DFEN00	0	FSMP010	FSMP000	EDGE010	EDGE000	TMS010	TMS000	FFFFF630H	00H
					INTP20					
FEM1	DFEN01	0	FSMP011	FSMP001	EDGE011	EDGE001	TMS011	TMS001	FFFFF631H	00H
					INTP21					
FEM2	DFEN02	0	FSMP012	FSMP002	EDGE012	EDGE002	TMS012	TMS002	FFFFF632H	00H
					INTP22					
FEM3	DFEN03	0	FSMP013	FSMP003	EDGE013	EDGE003	TMS013	TMS003	FFFFF633H	00H
					INTP23					
FEM4	DFEN04	0	FSMP014	FSMP004	EDGE014	EDGE004	TMS014	TMS004	FFFFF634H	00H
					INTP24					
FEM5	DFEN05	0	FSMP015	FSMP005	EDGE015	EDGE005	TMS015	TMS005	FFFFF635H	00H
					INTP25					

Bit Position	Bit Name	Function
7	DFEN0n	Specifies the filter of the INTP2n pin. 0: Analog filter 1: Digital filter
5, 4	FSMP01n, FSMP00n	Selects the sampling clock of the digital filter.

FSMP01n	FSMP00n	Operation
0	0	ϕ_{TM2}
Other than above		Setting prohibited

Remark ϕTM2: Clock selected by PRM02 register

Bit Position	Bit Name	Function
3, 2	EDGE01n, EDGE00n	Specifies the valid edge of the INTP2n pin.

EDGE01n	EDGE00n	Operation
0	0	Interrupt by INTCC2n[Note]
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

Note Set when INTCC2n is selected by a match between TM20, TM21 and the subchannel compare register (specified by the TMS01n, TMS00n bits) (n = 0 to 5).

Remark n = 0 to 5

Figure 7-16. Timer 2 Input Filter Mode Registers 0 to 5 (FEM0 to FEM5) (2/2)

Bit Position	Bit Name	Function
1, 0	TMS01n, TMS00n	Selects the capture input[Note].

TMS01n	TMS00n	Operation
0	0	Used as a pin
0	1	Digital filter (noise eliminator specification)
1	0	Timer-based capture to subchannel 1
1	1	Timer-based capture to subchannel 2

Note Selection of capture input based on INTCM100 and INTCM101 is valid only for the FEM1 and FEM2 registers. Set the TMS01m and TMS00m bits of the FEMm register to 00B or 01B. All other settings are prohibited (m = 1, 3 to 5).

Subchannels 1 and 2 of timer 2 can be captured by INTP21, INTP22, and INTCM100, INTCM101. An example is given below.

(a) When subchannel 1 is captured by INTCM101

FEM1 register = xxxxxx10B

TMIC0 register = 00000010B

(b) When subchannel 2 is captured by INTCM101

FEM2 register = xxxxxx11B

TMIC0 register = 00001000B

Remark n = 0 to 5

7.4 Software Exception

A software exception is generated when the CPU executes the TRAP instruction, and can be always acknowledged.

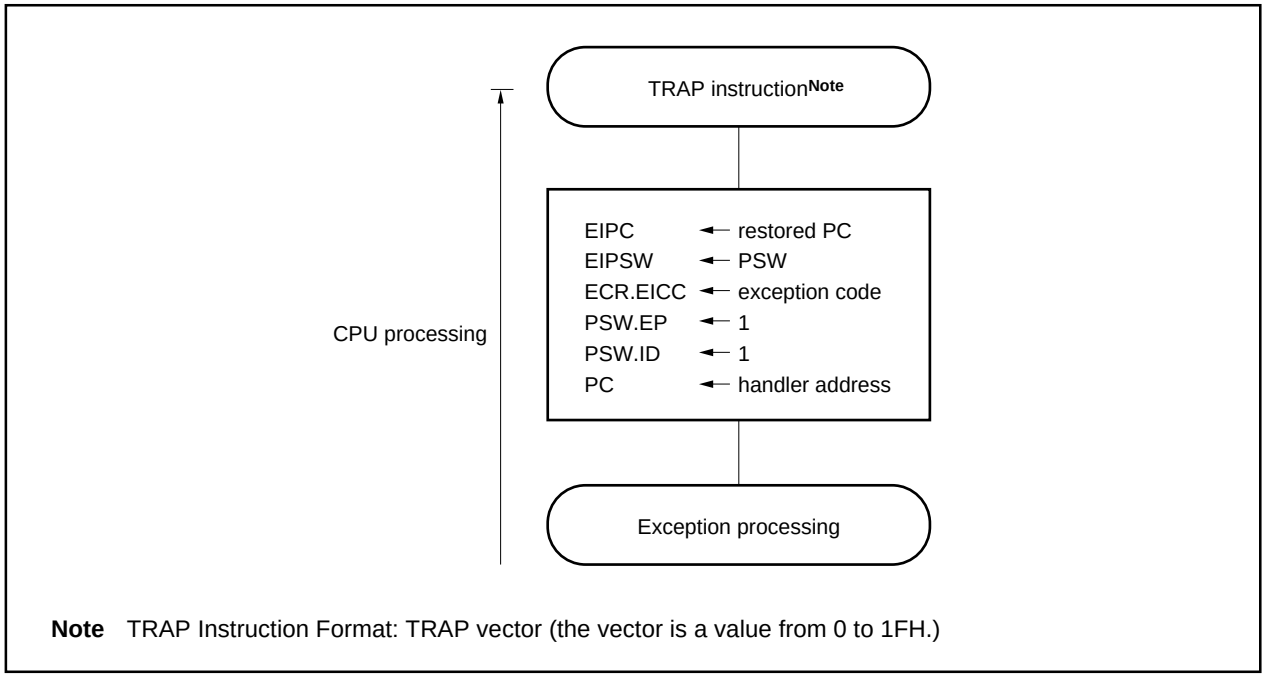
7.4.1 Operation

If a software exception occurs, the CPU performs the following processing, and transfers control to the handler routine:

(1) Saves the restored PC to EIPC.
(2) Saves the current PSW to EIPSW.
(3) Writes an exception code to the lower 16 bits (EICC) of ECR (interrupt source).
(4) Sets the EP and ID bits of the PSW.
(5) Sets the handler address (00000040H or 00000050H) corresponding to the software exception to the PC, and transfers control.

Figure 7-17 illustrates the processing of a software exception.

Figure 7-17. Software Exception Processing



Note TRAP Instruction Format: TRAP vector (the vector is a value from 0 to 1FH.)

The handler address is determined by the TRAP instruction's operand (vector). If the vector is 0 to 0FH, it becomes 00000040H, and if the vector is 10H to 1FH, it becomes 00000050H.

7.4.2 Restore

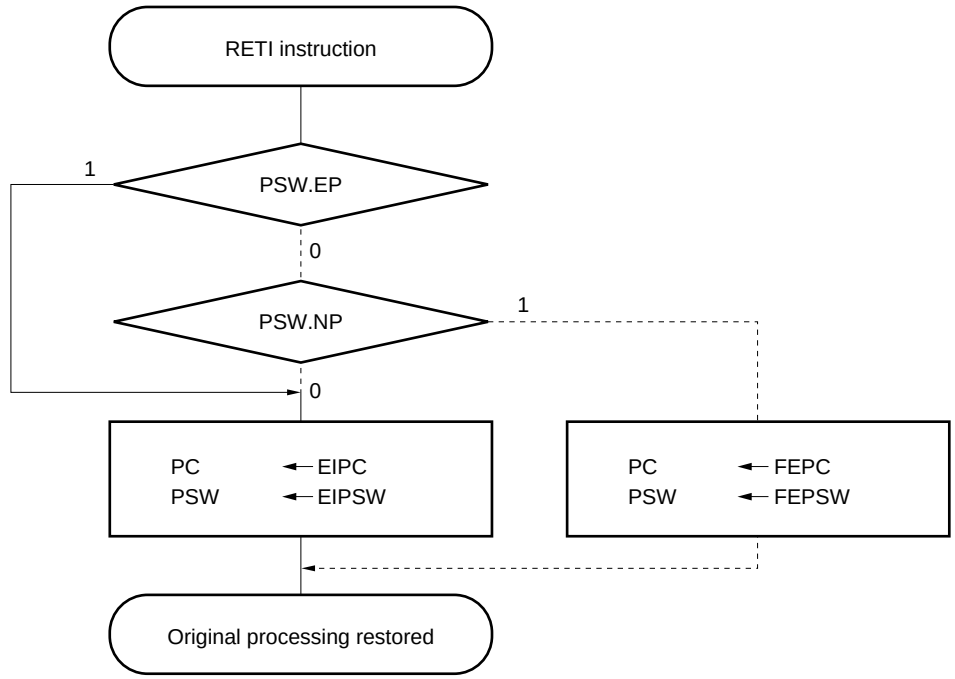
Recovery from software exception processing is carried out by the RETI instruction.

By executing the RETI instruction, the CPU carries out the following processing and shifts control to the restored PC's address.

(1) Loads the restored PC and PSW from EIPC and EIPSW because the EP bit of the PSW is 1.
(2) Transfers control to the address of the restored PC and PSW.

Figure 7-18 illustrates the processing of the RETI instruction.

Figure 7-18. RETI Instruction Processing



Caution When the PSW.EP bit and the PSW.NP bit are changed by the LDSR instruction during the software exception processing, in order to restore the PC and PSW correctly during recovery by the RETI instruction, it is necessary to set PSW.EP back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The broken lines show the CPU processing flow.

7.4.3 Exception status flag (EP)

The EP flag is bit 6 of PSW, and is a status flag used to indicate that exception processing is in progress. It is set when an exception occurs.

PSW

31																							8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NP	EP	ID	SAT	CY	OV	S	Z

Initial value
00000020H

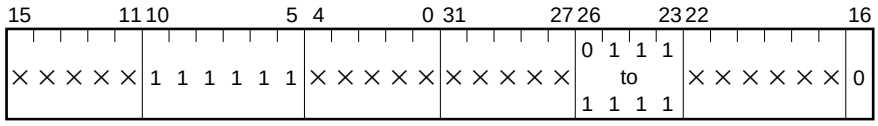
Bit Position	Bit Name	Function
6	EP	Shows that exception processing is in progress. 0: Exception processing not in progress. 1: Exception processing in progress.

7.5 Exception Trap

An exception trap is an interrupt that is requested when an illegal execution of an instruction takes place. In the V850E/IA1, an illegal opcode exception (ILGOP: Illegal Opcode Trap) is considered as an exception trap.

7.5.1 Illegal opcode definition

The illegal instruction has an opcode (bits 10 to 5) of 111111B, a sub-opcode (bits 26 to 23) of 0111B to 1111B, and a sub-opcode (bit 16) of 0B. An exception trap is generated when an instruction applicable to this illegal instruction is executed.



×: Arbitrary

Caution Since it is possible to assign this instruction to an illegal opcode in the future, it is recommended that it not be used.

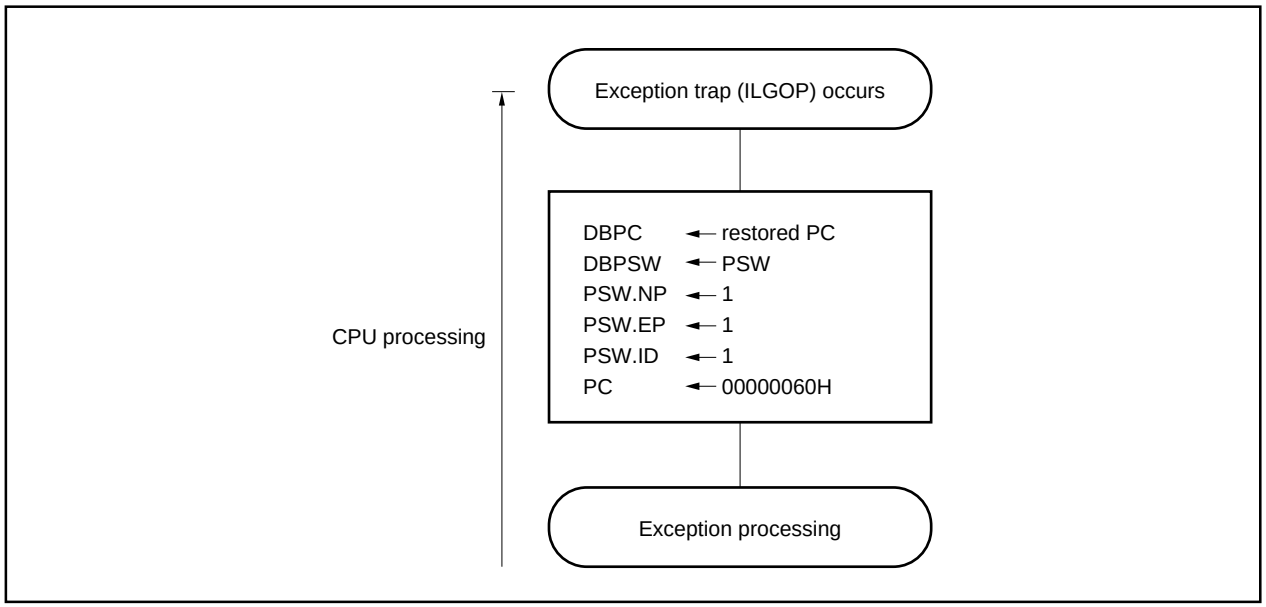
(1) Operation

If an exception trap occurs, the CPU performs the following processing, and transfers control to the handler routine:

(1) Saves the restored PC to DBPC.
(2) Saves the current PSW to DBPSW.
(3) Sets the NP, EP, and ID bits of the PSW.
(4) Sets the handler address (00000060H) corresponding to the exception trap to the PC, and transfers control.

Figure 7-19 illustrates the processing of the exception trap.

Figure 7-19. Exception Trap Processing



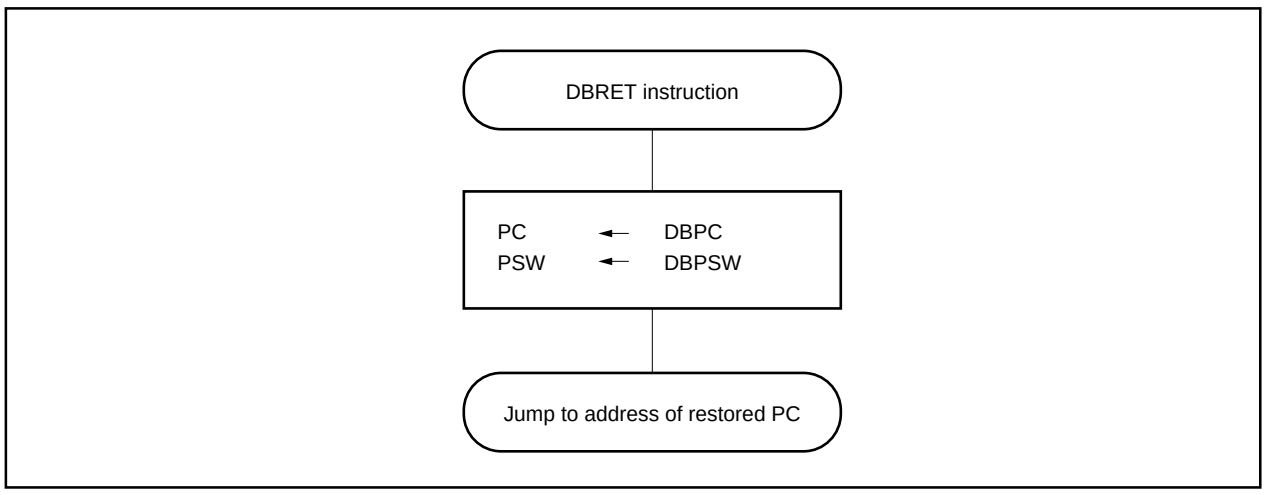
(2) Restore

Recovery from an exception trap is carried out by the DBRET instruction. By executing the DBRET instruction, the CPU carries out the following processing and controls the address of the restored PC.

(1) Loads the restored PC and PSW from DBPC and DBPSW.
(2) Transfers control to the address indicated by the restored PC and PSW.

Figure 7-20 illustrates the restore processing from an exception trap.

Figure 7-20. Restore Processing from Exception Trap



7.5.2 Debug trap

The debug trap is an exception that can be acknowledged every time and is generated by execution of the DBTRAP instruction.

When the debug trap is generated, the CPU performs the following processing.

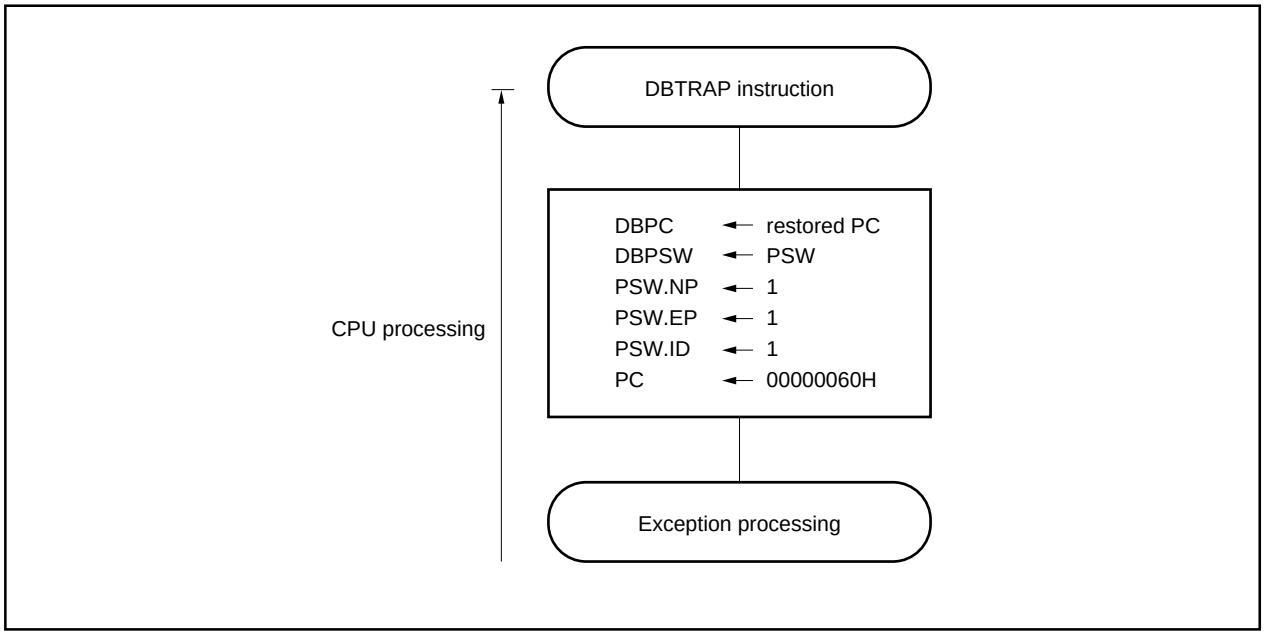
(1) Operation

When the debug trap is generated, the CPU performs the following processing, transfers control to the debug monitor routine, and shifts to debug mode.

(1) Saves the restored PC to DBPC.
(2) Saves the current PSW to DBPSW.
(3) Sets the NP, EP and ID bits of the PSW.
(4) Sets the handler address (00000060H) corresponding to the debug trap to the PC and transfers control.

Figure 7-21 illustrates the processing of the debug trap.

Figure 7-21. Debug Trap Processing



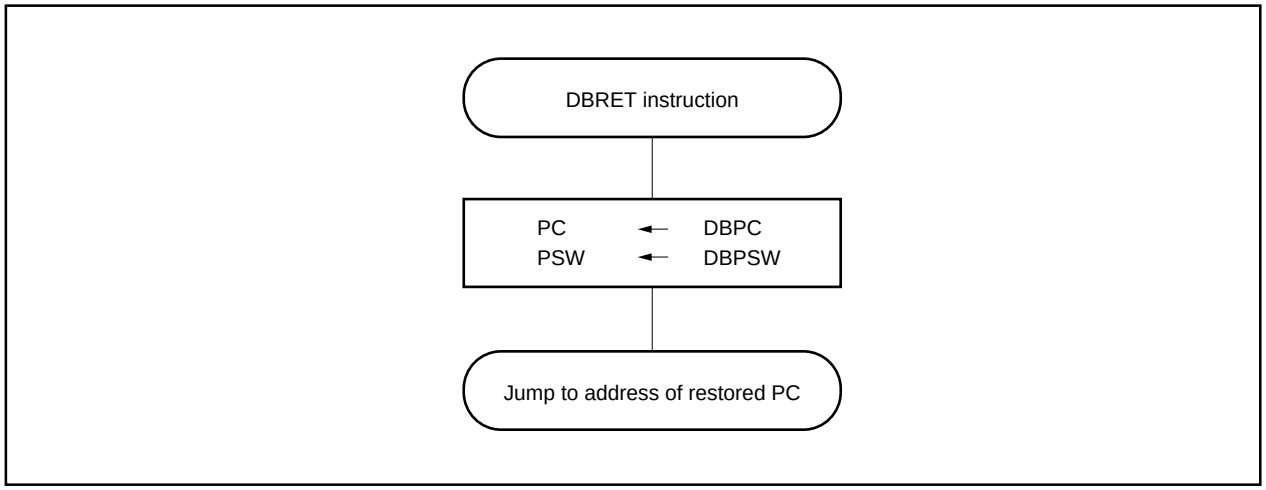
(2) Restore

Recovery from a debug trap is carried out by the DBRET instruction. By executing the DBRET instruction, the CPU carries out the following processing and controls the address of the restored PC.

(1) Loads the restored PC and PSW from DBPC and DBPSW.
(2) Transfers control to the address indicated by the restored PC and PSW.

Figure 7-22 illustrates the restore processing from a debug trap.

Figure 7-22. Restore Processing from Debug Trap



7.6 Multiple Interrupt Processing Control

Multiple interrupt processing control is a process by which an interrupt request that is currently being processed can be interrupted during processing if there is an interrupt request with a higher priority level, and the higher priority interrupt request is received and processed first.

If there is an interrupt request with a lower priority level than the interrupt request currently being processed, that interrupt request is held pending.

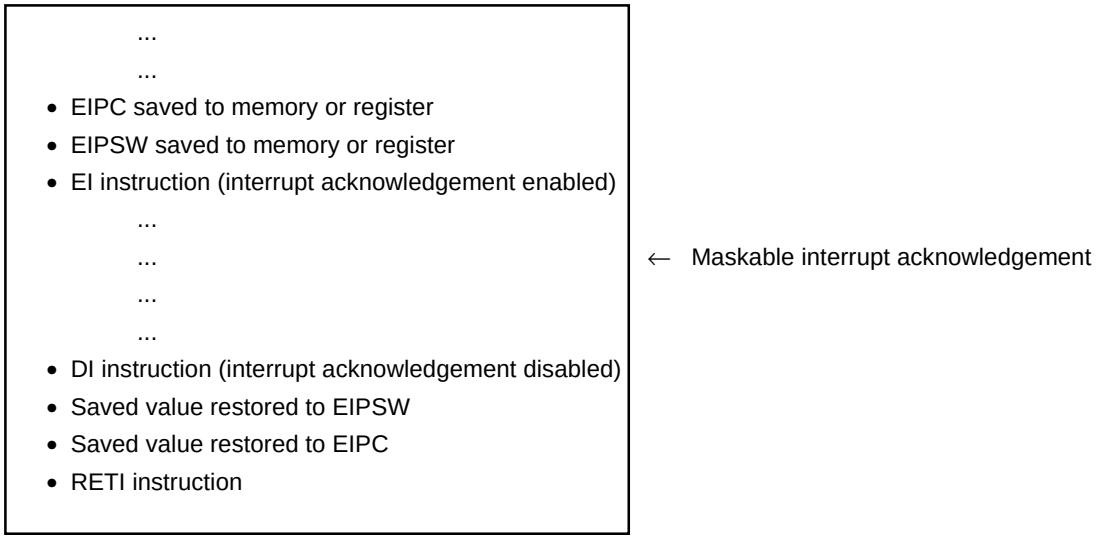
Maskable interrupt multiple processing control is executed when an interrupt has an enable status (ID = 0). Thus, if multiple interrupts are executed, it is necessary to have an interrupt enable status (ID = 0) even for an interrupt processing routine.

If a maskable interrupt enable or a software exception is generated in a maskable interrupt or software exception service program, it is necessary to save EIPC and EIPSW.

This is accomplished by the following procedure.

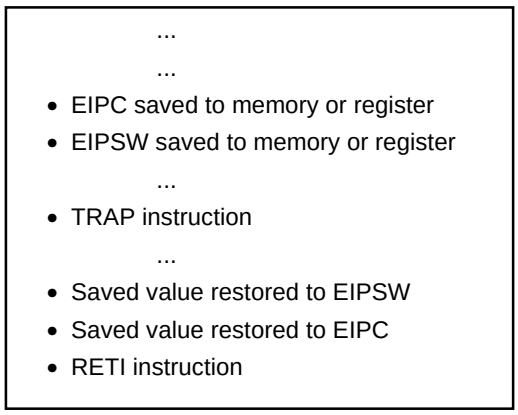
(1) Acknowledgement of maskable interrupts in service program

Service program of maskable interrupt or exception



(2) Generation of exception in service program

Service program of maskable interrupt or exception



← Exception such as TRAP instruction acknowledged.

The priority order for multiple interrupt processing control has 8 levels, from 0 to 7 for each maskable interrupt request (0 is the highest priority), but it can be set as desired via software. Setting of the priority order level is done using the xxPRn0 to xxPRn2 bits of the interrupt control request register (xxlCn), which is provided for each maskable interrupt request. After system reset, an interrupt request is masked by the xxMKn bit and the priority order is set to level 7 by the xxPRn0 to xxPRn2 bits.

The priority order of maskable interrupts is as follows.

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

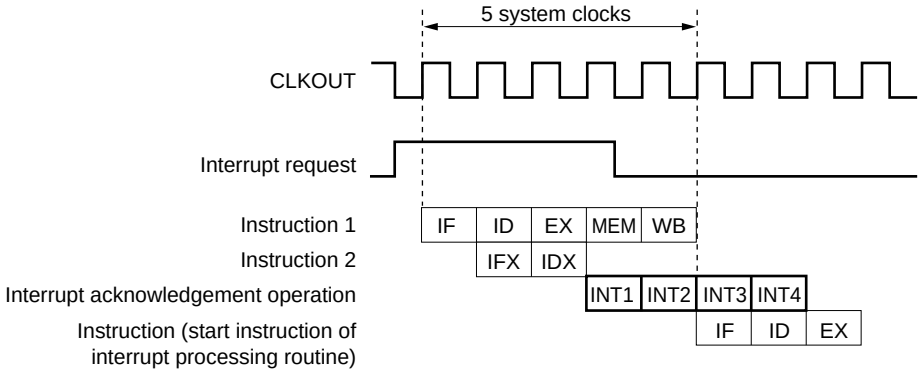
Interrupt processing that has been suspended as a result of multiple processing control is resumed after the processing of the higher priority interrupt has been completed and the RETI instruction has been executed.
A pending interrupt request is acknowledged after the current interrupt processing has been completed and the RETI instruction has been executed.

Caution In a non-maskable interrupt processing routine (time until the RETI instruction is executed), maskable interrupts are suspended and not acknowledged.

7.7 Interrupt Response Time

The following table describes the V850E/IA1 interrupt response time (from interrupt generation to start of interrupt processing).

Figure 7-23. Pipeline Operation at Interrupt Request Acknowledgement (Outline)



INT1 to INT4: Interrupt acknowledgement processing
IFX: Invalid instruction fetch
IDX: Invalid instruction decode

Interrupt Response Time (Internal System Clock)					Condition
	Internal Interrupt	External Interrupt			
		INTP0 to INTP6, INTP20 to INTP25	INTP20 to INTP25	INTP100, INTP101 INTP110, INTP111 INTP30, INTP31	
Minimum	5	5+ analog delay time	5+ digital noise filter	5 + **Note** + digital noise filter	The following cases are exceptions. • In IDLE/software STOP mode • External bus access • Two or more interrupt request non-sample instructions are executed in succession • Access to interrupt control register
Maximum	11	11+ analog delay time	11+ digital noise filter	11 + **Note** + digital noise filter	

Note The number of internal system clocks are as follows.

- For timers 10, 11 (TM10, TM11) using INTP100, INTP101, INTP110, and INTP111 as external interrupt inputs (see **9.2.4 (1) Timer 1n/timer 2n clock selection register (PRM02)**):
  $t_{CLK} = \phi/2$ (PRM2 bit = 1): 2
  $t_{CLK} = \phi/4$ (PRM2 bit = 0): 4

- For timer 3 (TM3) using INTP30 and INTP31 as external interrupt inputs (see **9.4.4 (1) Timer 3 clock selection register (PRM03)**):
  $t_{CLK} = \phi$ (PRM3 bit = 1): 2
  $t_{CLK} = \phi/2$ (PRM3 bit = 0): 4

7.8 Periods in Which Interrupts Are Not Acknowledged

An interrupt is acknowledged while an instruction is being executed. However, no interrupt will be acknowledged between an interrupt non-sample instruction and the next instruction.

The interrupt request non-sampling instructions are as follows.

- EI instruction
- DI instruction
- LDSR reg2, 0x5 instruction (for PSW)
- The store instruction for the interrupt control register (xxlCn), in-service priority register (ISPR), and command register (PRCMD).

[MEMO]

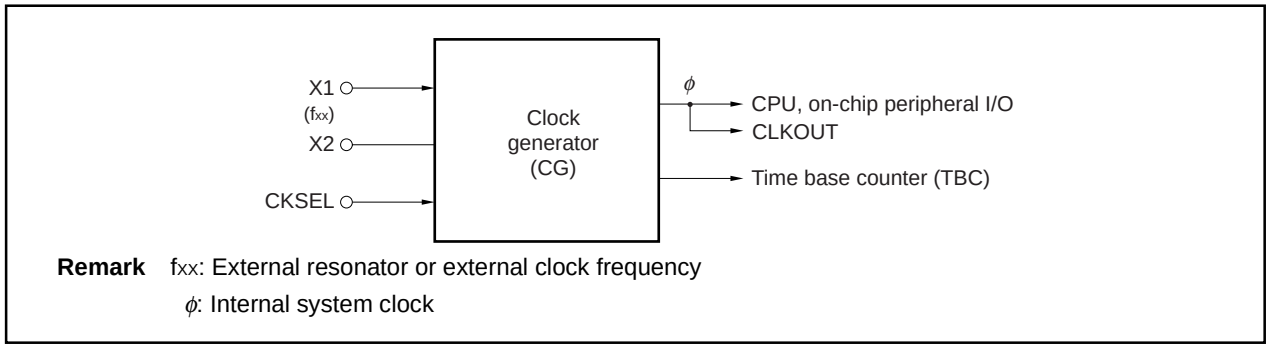
CHAPTER 8 CLOCK GENERATOR FUNCTION

The clock generator (CG) generates and controls the internal system clock (ϕ) that is supplied to each internal unit, such as the CPU.

8.1 Features

- Multiplier function using a phase locked loop (PLL) synthesizer
- Clock sources
  - Oscillation by connecting a resonator
  - External clock
- Power saving modes
  - HALT mode
  - IDLE mode
  - Software STOP mode
- Internal system clock output function

8.2 Configuration



Remark fxx: External resonator or external clock frequency
ϕ: Internal system clock

8.3 Input Clock Selection

The clock generator consists of an oscillator and a PLL synthesizer. For example, connecting a 5.0 MHz crystal resonator or ceramic resonator to pins X1 and X2 enables a 50 MHz internal system clock (ϕ) to be generated when the multiplier is 10. Also, an external clock can be input directly to the oscillator. In this case, the clock signal should be input only to pin X1 (pin X2 should be left open). Two basic operation modes are provided for the clock generator. These are PLL mode and direct mode. The operation mode is selected by the CKSEL pin. The input to this pin is latched on reset.

CKSEL	Operating Mode
0	PLL mode
1	Direct mode

Caution The input level for the CKSEL pin must be fixed. If it is switched during operation, a malfunction may occur.

8.3.1 Direct mode

In direct mode, an external clock having twice the frequency of the internal system clock is input. Since the oscillator and PLL synthesizer are not operating, a greater degree of power saving is achieved. The maximum frequency that can be input in direct mode is 50 MHz. The V850E/IA1 is mainly used in application systems in which operates at relatively low frequencies. Taking EMI prevention into consideration, if the external clock frequency (f_{XX}) is 32 MHz (internal system clock (ϕ) = 16 MHz) or greater, PLL mode is recommended.

Caution In direct mode, an external clock must be input (an external resonator should not be connected).

8.3.2 PLL mode

In PLL mode, an external resonator is connected or external clock is input and multiplied by the PLL synthesizer. The multiplied PLL output is divided by the division ratio specified by the clock control register (CKC) to generate a system clock that is 10, 5, 2.5, or 1 times the frequency (f_{XX}) of the external resonator or external clock.

After reset, an internal system clock (ϕ) that is 1 time the frequency ($1 \times f_{XX}$) of the internal clock frequency (f_{XX}) is generated.

When a frequency ($10 \times f_{XX}$) that is 10 times the clock frequency (f_{XX}) is generated, a system with low noise and low power consumption can be realized because a frequency of up to 50 MHz is obtained based on a 4 to 5 MHz external resonator or external clock.

In PLL mode, if the clock supply from an external resonator or external clock source stops, operation of the internal system clock (ϕ) based on the self-propelled frequency of the clock generator's internal voltage controlled oscillator (VCO) continues. In this case, ϕ is undefined. However, do not devise an application method expecting to use this self-propelled frequency.

Example: Clocks when PLL mode ($\phi = 10 \times f_{XX}$) is used

System Clock Frequency (ϕ)	External Resonator or External Clock Frequency (f_{XX})
50.000 MHz	5.0000 MHz
40.000 MHz	4.0000 MHz

Caution Only an f_{XX} (4 to 5 MHz) value for which $10 \times f_{XX}$ does not exceed the system clock maximum frequency (50 MHz) can be used for the oscillation frequency or external clock frequency.

Remark Note the following when PLL mode is selected ($\phi = 5 \times f_{XX}$, $\phi = 2.5 \times f_{XX}$, or $\phi = 1 \times f_{XX}$)
If the V850E/IA1 need not be operated at high frequency, use $\phi = 5 x f_{XX}$, $\phi = 2.5 \times f_{XX}$, or $\phi = 1 \times f_{XX}$ to reduce the power consumption by lowering the system clock frequency using software.

8.3.3 Peripheral command register (PHCMD)

This is an 8-bit register that is used to set protection for writing to registers that can significantly affect the system so that the application system is not halted unexpectedly due to erroneous program execution. This register can be written only in 8-bit units (when it is read, undefined data is read out).

Writing to the first specific register (CKC or FLPMC register) is only valid after first writing to the PHCMD register. Because of this, the register value can be overwritten only with the specified sequence, preventing an illegal write operation from being performed.

Figure 8-1. Peripheral Command Register (PHCMD)

	7	6	5	4	3	2	1	0	Address	Initial value
PHCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0	FFFFF800H	Undefined

Bit Position	Bit Name	Function
7 to 0	REG7 to REG0	The specific registers targeted are as follows. • Clock control register (CKC) • Flash programming mode control register (FLPMC)

The generation of an illegal store operation can be checked with the PRERR bit of the peripheral status register (PHS).

8.3.4 Clock control register (CKC)

The clock control register is an 8-bit register that controls the internal system clock (ϕ) in PLL mode. It can be written to only by a specific sequence combination so that it cannot easily be overwritten by mistake due to erroneous program execution.

This register can be read or written in 8-bit or 1-bit units.

Caution Do not change bits CKDIV2 to CKDIV0 in direct mode.

Figure 8-2. Clock Control Register (CKC)

	7	6	5	4	3	2	1	0	Address	Initial value
CKC	0	0	TBCS	CESEL	0	CKDIV2	CKDIV1	CKDIV0	FFFFF822H	00H

Bit Position	Bit Name	Function
5	TBCS	Selects the time base counter clock. 0: $f_{XX}/2^8$ 1: $f_{XX}/2^9$ For details, see **8.6.2 Time base counter (TBC)**.
4	CESEL	Specifies the functions of the X1 and X2 pins. 0: A resonator is connected to the X1 and X2 pins 1: An external clock is connected to the X1 pin When CESEL = 1, the oscillator feedback loop is disconnected to prevent current leak in software STOP mode.
2 to 0	CKDIV2 to CKDIV0	Sets the internal system clock frequency (ϕ) when PLL mode is used.

CKDIV2	CKDIV1	CKDIV0	Internal System Clock (ϕ)
0	0	0	f_{XX}
0	0	1	$2.5 \times f_{XX}$
0	1	1	$5 \times f_{XX}$
1	1	1	$10 \times f_{XX}$
Other than above			Setting prohibited

Caution When changing the internal system clock during operation, be sure to set the clock to be changed after setting the CKDIV2 to CKDIV0 bits to 000 (f_{XX}).

Example Clock generator settings

Operation Mode	CKSEL Pin	CKC Register			Input Clock (f_{XX})	Internal System Clock (ϕ)
		CKDIV2	CKDIV0	CKDIV0		
Direct mode	High-level input	0	0	0	16 MHz	8 MHz
PLL mode	Low-level input	0	0	0	5 MHz	5 MHz
		0	0	1	5 MHz	12.5 MHz
		0	1	1	5 MHz	25 MHz
		1	1	1	5 MHz	50 MHz
Other than above					Setting prohibited	Setting prohibited

Data is set in the clock control register (CKC) according to the following sequence.

<1> Disable interrupts (set the NP bit of PSW to 1)
<2> Prepare data in any one of the general registers to set in the specific register.
<3> Write arbitrary data to the peripheral command register (PHCMD)
<4> Set the clock control register (CKC) (with the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<5> Assert the NOP instructions (5 instructions (<5> to <9>))
<10> Release the interrupt disabled state (set the NP bit of PSW to 0).

[Sample coding]

```
<1> LDSR    rX, 5
<2> MOV     0X04, r10
<3> ST.B    r10, PHCMD [r0]
<4> ST.B    r10, CKC [r0]
<5> NOP
<6> NOP
<7> NOP
<8> NOP
<9> NOP
<10> LDSR   rY, 5
```

Remark rX: Value written to PSW
rY: Value returned to PSW

No special sequence is required to read the specific register.

Cautions 1. If an interrupt is acknowledged between the issuing of data to the PHCMD <3> and writing to the specific register immediately after <4>, the write operation to the specific register is not performed and a protection error (the PRERR bit of the PHS register = 1) may occur. Therefore, set the NP bit of the PSW to 1 <1> to disable interrupt acknowledgement. Also disable interrupt acknowledgement as well when selecting a bit manipulation instruction for the specific register setting.

2. Although the data written to the PHCMD register is dummy data however, use the same register as the general register used in specific register setting <4> for writing to the PHCMD register (<3>). The same method should be applied when using a general register for addressing.

3. Do not perform a write operation to the PRCMD register and specific register using DMA transfer.

8.3.5 Peripheral status register (PHS)

If a write operation is not performed in the correct sequence including access to the command register for the protection-targeted internal registers, writing is not performed and a protection error is generated, setting the status flag (PRERR) to 1. This flag is a cumulative flag. After checking the PRERR flag, it is cleared to 0 by an instruction.

This register can be read or written in 8-bit or 1-bit units

Figure 8-3. Peripheral Status Register (PHS)

	7	6	5	4	3	2	1	0	Address	Initial value
PHS	0	0	0	0	0	0	0	PRERR	FFFFF802H	00H

Bit Position	Bit Name	Function
0	PRERR	0: Protection error does not occur 1: Protection error occurs

The operation conditions of the PRERR flag are as follows.

Set conditions: <1> If the operation of the relevant store instruction for the peripheral I/O is not a write operation for the PHCMD register, but the peripheral specific register is written to.

<2> If the first store instruction operation after the write operation to the PHCMD register is for memory other than the specific registers and peripheral I/O.

Reset conditions: <1> If the PRERR flag of the PHS register is set to 0.

<2> If the system is reset

8.4 PLL Lockup

The lockup time (frequency stabilization time) is the time from when the power is turned on or the software STOP mode is released until the phase locks at the prescribed frequency. The state until this stabilization occurs is called a lockup state, and the stabilized state is called a lock state.

The lock register (LOCK) has a LOCK flag that reflects the stabilized state of the PLL frequency.

This register is read-only in 8-bit or 1-bit units.

Figure 8-4. Lock Register (LOCK)

	7	6	5	4	3	2	1	0	Address	Initial value
LOCK	0	0	0	0	0	0	0	LOCK	FFFFF824H	Undefined

Bit position	Bit name	Function
0	LOCK	This is a read-only flag that indicates the PLL state. This flag holds the value 0 as long as a lockup state is maintained and is not initialized by a system reset. 0: Indicates that the PLL is locked. 1: Indicates that the PLL is not locked (UNLOCK state).

Caution When the PLL is locked, the LOCK flag is 0. If the system then enters an unlocked state due to a standby, the LOCK flag becomes 1. If anything other than a standby causes the system to enter an unlocked state, the LOCK flag remains 0 (i.e. does not become 1).

If the clock stops, the power fails, or some other factor operates to cause an unlock state to occur, for control processing that depends on software execution speed, such as real-time processing, be sure to judge the LOCK flag according to software immediately after operation begins so that processing does not begin until after the clock stabilizes.

On the other hand, static processing such as the setting of internal hardware or the initialization of register data or memory data can be executed without waiting for the LOCK flag to be reset.

The relationship between the oscillation stabilization time (the time from when the resonator starts to oscillate until the input waveform stabilizes) when a resonator is used, and the PLL lockup time (the time until frequency stabilizes) is shown below.

Oscillation stabilization time < PLL lockup time.

8.5 Power Save Control

8.5.1 Overview

The power save function has the following three modes.

(1) HALT mode

In this mode, the clock generator (oscillator and PLL synthesizer) continues to operate, but the CPU's operation clock stops. Since the supply of clocks to on-chip peripheral functions other than the CPU continues, operation continues. The power consumption of the overall system can be reduced by intermittent operation that is achieved due to a combination of HALT mode and normal operation mode.

The system is switched to HALT mode by a specific instruction (the HALT instruction).

(2) IDLE mode

In this mode, the clock generator (oscillator and PLL synthesizer) continues to operate, but the supply of internal system clocks is stopped, which causes the overall system to stop.

When the system is released from IDLE mode, it can be switched to normal operation mode quickly because the oscillator's oscillation stabilization time need not be secured.

The system is switched to IDLE mode according to the PSMR register setting.

IDLE mode is located midway between software STOP mode and HALT mode in relation to the clock stabilization time and current consumption. It is used for situations in which a low current consumption mode is to be used and the clock stabilization time is to be eliminated after the mode is released.

(3) Software STOP mode

In this mode, the overall system is stopped by stopping the clock generator (oscillator and PLL synthesizer). The system enters an ultra-low power consumption state in which only leak current is lost.

The system is switched to software STOP mode according to a PSMR register setting.

(a) PLL mode

The system is switched to software STOP mode by setting the register according to software. The PLL synthesizer's clock output is stopped at the same time that the oscillator is stopped. After software STOP mode is released, the oscillator's oscillation stabilization time must be secured until the system clock stabilizes. Also, PLL lockup time may be required depending on the program. When a resonator or external clock is connected, following the release of the software STOP mode, execution of the program is started after the count time of the time base counter has elapsed.

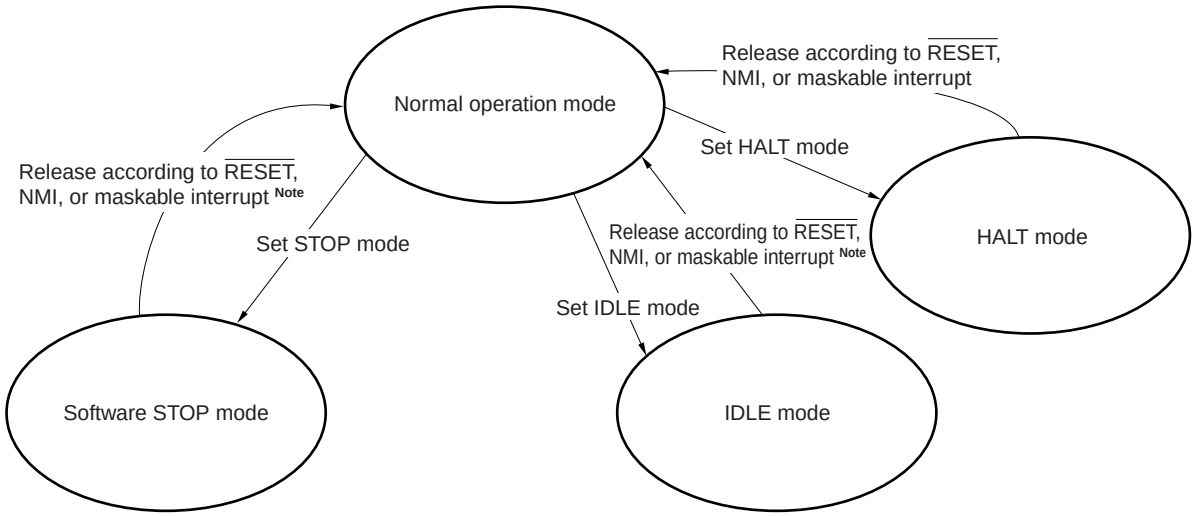
(b) Direct Mode

To stop the clock, set the X1 pin to low level. After the release of software STOP mode, execution of the program is started after the count-time of the time base counter has elapsed.

Figure 8-1 shows the operation of the clock generator in normal operation mode, HALT mode, IDLE mode, and software STOP mode.

An effective low power consumption system can be realized by combining these modes and switching modes according to the required use.

Figure 8-5. Power Save Mode State Transition Diagram



Note INTPn (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111)
When level detection is specified for INTPn, the internal system clock is not supplied in the software STOP or IDLE mode. Consequently, in cases such as when INTPn is specified for input via digital sampling, the software STOP or IDLE cannot be released.

Table 8-1. Clock Generator Operation Using Power Save Control

Clock Source		Power Save Mode	Oscillator	PLL Synthesizer	Clock Supply to Peripheral I/O	Clock Supply to the CPU
PLL mode	Oscillation with resonator	Normal Operation	√	√	√	√
		HALT mode	√	√	√	–
		IDLE mode	√	√	–	–
		Software STOP mode	–	–	–	–
	External clock	Normal Operation	–	√	√	√
		HALT mode	–	√	√	–
		IDLE mode	–	√	–	–
		Software STOP mode	–	–	–	–
Direct mode	External clock	Normal Operation	–	–	√	√
		HALT mode	–	–	√	–
		IDLE mode	–	–	–	–
		Software STOP mode	–	–	–	–

Remark √: Operating
–: Stopped

8.5.2 Control registers

(1) Power save mode register (PSMR)

This is an 8-bit register that controls power save mode. It is effective only when the STB bit of the PSC register is set to 1.

Writing to the PSMR register is executed by the store instruction (ST/SST instruction) and a bit manipulation instruction (SET1/CLR1/NOT1 instruction).

This register can be read or written in 8-bit or 1-bit units.

Figure 8-6. Power Save Mode Register (PSMR)

	7	6	5	4	3	2	1	0	Address	Initial value
PSMR	0	0	0	0	0	0	0	PSM	FFFFF820H	00H

Bit Position	Bit Name	Function
0	PSM	Specifies IDLE mode or software STOP mode. 0: Switches the system to IDLE mode 1: Switches the system to software STOP mode

(2) Command register (PRCMD)

This is an 8-bit register that is used to set protection for write operations to registers that can significantly affect the system so that the application system is not halted unexpectedly due to erroneous program execution.

Writing to the first specific register (power save control register (PSC)) is only valid after first writing to the PRCMD register. Because of this, the register value can be overwritten only by the specified sequence, preventing an illegal write operation from being performed.

This register can only be written in 8-bit units. The undefined data is read out if read.

Figure 8-7. Command Register (PRCMD)

	7	6	5	4	3	2	1	0	Address	Initial value
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0	FFFFF1FCH	Undefined

Bit Position	Bit Name	Function
7 to 0	REG7 to REG0	Registration Code (arbitrary 8-bit data) The specific register targeted is the power save control register (PSC).

(3) Power save control register (PSC)

This is an 8-bit register that controls the power save function. This register, which is one of the specific registers, is effective only when accessed by a specific sequence during a write operation (see **3.4.9 Specific registers**).

This register can be read or written in 8-bit or 1-bit units.

Figure 8-8. Power Save Control Register (PSC)

	7	6	5	4	3	2	1	0	Address	Initial value
PSC	0	0	NMIM	INTM	0	0	STB	0	FFFFF1FEH	00H

Bit Position	Bit Name	Function
5	NMIM	This is the enable/disable setting bit for standby mode release using valid edge input of NMI. 0: Enables NMI cancellation 1: Disables NMI cancellation
4	INTM	This is the enable/disable setting for standby mode release using an unmasked maskable interrupt (INTPn) (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111). 0: Enables maskable interrupt cancellation 1: Disables maskable interrupt cancellation
1	STB	Indicates the stand-by mode status. If 1 is written to this bit, the system enters stand-by mode (when it is in IDLE or software STOP mode). When stand-by mode is released, this bit is automatically reset to 0. 0: Stand-by mode is released 1: Stand-by mode is in effect

Caution It is impossible to set STB bit and NMIM or INTM bit at the same time. Be sure to set STB bit after setting NMIM or INTM bit.

Data is set in the power save control register (PSC) according to the following sequence.

<1> Set the power save mode register (PSMR) (with the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<2> Prepare data in any one of the general-purpose registers to set to the specific register.

<3> Write arbitrary data to the command register (PRCMD).

<4> Set the power save control register (PSC) (with the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<5> Assert the NOP instructions (5 instructions (<5> to <9>).

Sample coding

```
<1> ST.B    r11, PSMR [r0]     ; Set PSMR register
<2> MOV     0×04, r10
<3> ST.B    r10, PRCMD [r0]    ; Write PRCMD register
<4> ST.B    r10, PSC [r0]      ; Set PSC register
<5> NOP                        ; Dummy instruction
<6> NOP                        ; Dummy instruction
<7> NOP                        ; Dummy instruction
<8> NOP                        ; Dummy instruction
<9> NOP                        ; Dummy instruction
(next instruction)             ; Execution routine after software STOP mode and IDLE mode release
```

No special sequence is required to read the specific register.

Cautions 1. A store instruction for the command register does not accept interrupts. This coding is made on assumption that <3> and <4> above are executed by the program with consecutive store instructions. If another instruction is set between <3> and <4>, the above sequence may become in effective when the interrupt is accepted by that instruction, and a malfunction of the program may result.

2. Although the data written to the PHCMD register is dummy data, use the same register as the general register used in specific register setting <4> for writing to the PHCMD register (<3>). The same method should be applied when using a general register for addressing.

3. At least 5 NOP instructions must be inserted after executing a store instruction to the PSC register to set software STOP or IDLE mode.

4. Do not perform a write operation to the PRCMD and specific registers using DMA transfer.

8.5.3 HALT mode

(1) Setting and operation status

In HALT mode, the clock generator (oscillator and PLL synthesizer) continues to operate, but the operation clock of the CPU is stopped. Since the supply of clocks to on-chip peripheral I/O units other than the CPU continues, operation continues. The power consumption of the overall system can be reduced by setting the system to HALT mode while the CPU is idle.

The system is switched to HALT mode by the HALT instruction.

Although program execution stops in HALT mode, the contents of all registers, internal RAM, and ports are maintained in the state they were in immediately before HALT mode began. Also, operation continues for all on-chip peripheral I/O units (other than ports) that do not depend on CPU instruction processing. Table 8-2 shows the status of each hardware unit in HALT mode.

Table 8-2. Operation Status in HALT Mode

Function	Operation Status
Clock generator	Operating
Internal system clock	Operating
CPU	Stopped
Ports	Maintained
On-chip peripheral I/O (excluding ports)	Operating
Internal data	All internal data such as CPU registers, statuses, data, and the contents of internal RAM are maintained in the state they were in immediately before HALT mode began.
AD0 to AD15	Operating
A16 to A23	
$\overline{RD}$, ASTB	
$\overline{UWR}$, $\overline{LWR}$	
$\overline{CS0}$ to $\overline{CS7}$	
$\overline{HLDRQ}$	
$\overline{HLDAK}$	
$\overline{WAIT}$	
CLKOUT	Clock output

(2) Release of HALT mode

HALT mode is released by a non-maskable interrupt request, an unmasked maskable interrupt request, or $\overline{\text{RESET}}$ pin input.

(a) Release according to a non-maskable interrupt request or an unmasked maskable interrupt request

HALT mode is released by a non-maskable interrupt request or by an unmasked maskable interrupt request regardless of the priority. However, if the system is set to HALT mode during an interrupt servicing routine, operation will differ as follows.

(i) If an interrupt request is generated with a lower priority than that of the interrupt request that is currently being serviced, HALT mode is released, but the newly generated interrupt request is not acknowledged. The new interrupt request is held pending.

(ii) If an interrupt request (including non-maskable interrupt requests) is generated with a higher priority than that of the interrupt request that is currently being serviced, HALT mode is released and the newly generated interrupt request is acknowledged.

Table 8-3. Operation After HALT Mode Is Released by Interrupt Request

Release Source	Enable Interrupt (EI) Status	Disable Interrupt (DI) Status
Non-maskable interrupt request	Branch to handler address	
Maskable interrupt request	Branch to handler address or execute next instruction	Execute next instruction

(b) Release according to $\overline{\text{RESET}}$ pin input

This is the same as a normal reset operation.

8.5.4 IDLE mode

(1) Setting and operation status

In IDLE mode, the clock generator (oscillator and PLL synthesizer) continues to operate, but the supply of internal system clocks is stopped which causes the overall system to stop.

When IDLE mode is released, the system can be switched to normal operation mode quickly because the oscillator's oscillation stabilization time or the PLL lockup time need not be secured.

The system is switched to IDLE mode by setting the PSC or PSMR register using a store instruction (ST or SST instruction) or a bit manipulation instruction (SET1, CLR1, or NOT1 instruction) (see **8.5.2 Control registers**).

In IDLE mode, program execution is stopped, and the contents of all registers, internal RAM, and ports are maintained in the state they were in immediately before execution stopped. The operation of on-chip peripheral I/O units (excluding ports) also is stopped.

Table 8-4 shows the status of each hardware unit in IDLE mode.

Table 8-4. Operation Status in IDLE Mode

Function	Operation Status
Clock generator	Operating
Internal system clock	Stopped
CPU	Stopped
Ports	Maintained
On-chip peripheral I/O (excluding ports)	Stopped[Note]
Internal data	All internal data such as CPU registers, statuses, data, and the contents of internal RAM are maintained in the state they were in immediately before IDLE mode began.
AD0 to AD15	High impedance
A16 to A23	
$\overline{RD}$	High level output
$\overline{UWR}$, $\overline{LWR}$	
$\overline{CS0}$ to $\overline{CS7}$	
$\overline{HLDAK}$	High impedance
$\overline{HLDRQ}$	Input (no sampling)
$\overline{WAIT}$	
ASTB	Low-level output
CLKOUT	

Note NBD cannot be used in IDLE mode.

(2) Release of IDLE mode

IDLE mode is released by a non-maskable interrupt request, an unmasked maskable interrupt request (INTPn), or $\overline{\text{RESET}}$ pin input (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111).

(a) Release according to a non-maskable interrupt request or an unmasked maskable interrupt request

IDLE mode is released by a non-maskable interrupt request or by an unmasked maskable interrupt request (INTPn) regardless of the priority. However, if the system is set to IDLE mode during a maskable interrupt servicing routine, operation will differ as follows (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111).

(i) If an interrupt request is generated with a lower priority than that of the interrupt request that is currently being serviced, IDLE mode is released, but the newly generated interrupt request is not acknowledged. The new interrupt request is held pending.

(ii) If an interrupt request (including non-maskable interrupt requests) is generated with a higher priority than that of the interrupt request that is currently being serviced, IDLE mode is released and the newly generated interrupt request is acknowledged.

Table 8-5. Operation After IDLE Mode Is Released by Interrupt Request

Release Source	Enable Interrupt (EI) Status	Disable Interrupt (DI) Status
Non-maskable interrupt request	Branch to handler address	
Maskable interrupt request	Branch to handler address or execute next instruction	Execute next instruction

If the system is set to IDLE mode during an NMI servicing routine, IDLE mode is released, but the interrupt is not acknowledged (interrupt is held pending).

Interrupt servicing that is started when IDLE mode is released by NMI pin input is handled in the same way as normal NMI interrupt servicing that occurs during an emergency (because the NMI interrupt handler address is unique). Therefore, when a program must be able to distinguish between these two situations, a software status must be prepared in advance and that status must be set before setting the PSMR register using a store instruction or a bit manipulation instruction. By checking for this status during NMI interrupt servicing, an ordinary NMI can be distinguished from the processing that is started when IDLE mode is released by NMI pin input.

(b) Release according to $\overline{\text{RESET}}$ pin input

This is the same as a normal reset operation.

8.5.5 Software STOP mode

(1) Setting and operation status

In software STOP mode, the clock generator (oscillator and PLL synthesizer) is stopped. The overall system is stopped, and ultra-low power consumption is achieved in which only leak current is lost.

The system is switched to software STOP mode by using a store instruction (ST or SST instruction) or bit manipulation instruction (SET1, CLR1, or NOT1 instruction) to set the PSC and PSMR registers (see **8.5.2 Control registers**).

When PLL mode and resonator connection mode (CESEL bit of CKC register = 1) are used, the oscillator's oscillation stabilization time must be secured after software STOP mode is released.

In both PLL and direct mode, following the release of software STOP mode, execution of the program is started after the count time of the time base counter has elapsed.

Although program execution stops in software STOP mode, the contents of all registers, internal RAM, and ports are maintained in the state they were in immediately before software STOP mode began. The operation of all on-chip peripheral I/O units (excluding ports) is also stopped.

Table 8-6 shows the status of each hardware unit in software STOP mode.

Table 8-6. Operation Status in Software STOP Mode

Function	Operation Status
Clock generator	Stopped
Internal system clock	Stopped
CPU	Stopped
Ports	Retained[Note1]
On-chip peripheral I/O (excluding ports)	Stopped[Note2]
Internal data	All internal data such as CPU registers, statuses, data, and the contents of internal RAM are retained in the state before STOP mode has been set[Note1].
AD0 to AD15	High impedance
A16 to A23	
$\overline{RD}$	High-level output
$\overline{UWR}$, $\overline{LWR}$	
$\overline{CS0}$ to $\overline{CS7}$	
$\overline{HLDAK}$	High impedance
$\overline{HLDRQ}$	Input (no sampling)
$\overline{WAIT}$	
ASTB	Low-level output
CLKOUT	

Notes 1. When the V_{DDS} value is within the operable range. However, even if it drops below the minimum operable voltage, as long as the data retention voltage V_{DDDR} is maintained, the contents of only the internal RAM will be maintained.

2. NBD cannot be used in software STOP mode.

(2) Release of software STOP mode

Software STOP mode is released by a non-maskable interrupt request, an unmasked maskable interrupt request (INTPn), or $\overline{\text{RESET}}$ pin input. Also, to release software STOP mode when PLL mode (CKSEL pin = low level) and resonator connection mode (CESEL bit of CKC register = 0) are used, the oscillator's oscillation stabilization time must be secured (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111)

Moreover, the oscillation stabilization time must be secured even when an external clock is connected (CESEL bit = 1). See **8.4 LL Lockup** for details.

(a) Release according to a non-maskable interrupt request or an unmasked maskable interrupt request

Software STOP mode is released by a non-maskable interrupt request or by an unmasked maskable interrupt request (INTPn) regardless of the priority. However, if the system is set to software STOP mode during an interrupt servicing routine, operation will differ as follows (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111).

(i) If an interrupt request is generated with a lower priority than that of the interrupt request that is currently being servicing, software STOP mode is released, but the newly generated interrupt request is not acknowledged. The new interrupt request is held pending.

(ii) If an interrupt request (including non-maskable interrupt requests) is generated with a higher priority than that of the interrupt request that is currently being serviced, software STOP mode is released and the newly generated interrupt request is acknowledged.

Table 8-7. Operation After Software STOP Mode Is Released by Interrupt Request

Cancellation Source	Enable Interrupt (EI) Status	Disable Interrupt (DI) Status
Non-maskable interrupt request	Branch to handler address	
Maskable interrupt request	Branch to handler address or execute next instruction	Execute next instruction

If the system is set to software STOP mode during an NMI servicing routine, software STOP mode is released, but the interrupt is not acknowledged (interrupt is held pending).

Interrupt servicing that is started when software STOP mode is released by NMI pin input is handled in the same way as normal NMI interrupt servicing that occurs during an emergency (because the NMI interrupt handler address is unique). Therefore, when a program must be able to distinguish between these two situations, a software status must be prepared in advance and that status must be set before setting the PSMR register using a store instruction or a bit manipulation instruction.

By checking for this status during NMI interrupt servicing, an ordinary NMI can be distinguished from the servicing that is started when software STOP mode is released by NMI pin input.

(b) Release according to $\overline{\text{RESET}}$ pin input

This is the same as a normal reset operation.

8.6 Securing Oscillation Stabilization Time

8.6.1 Oscillation stabilization time security specification

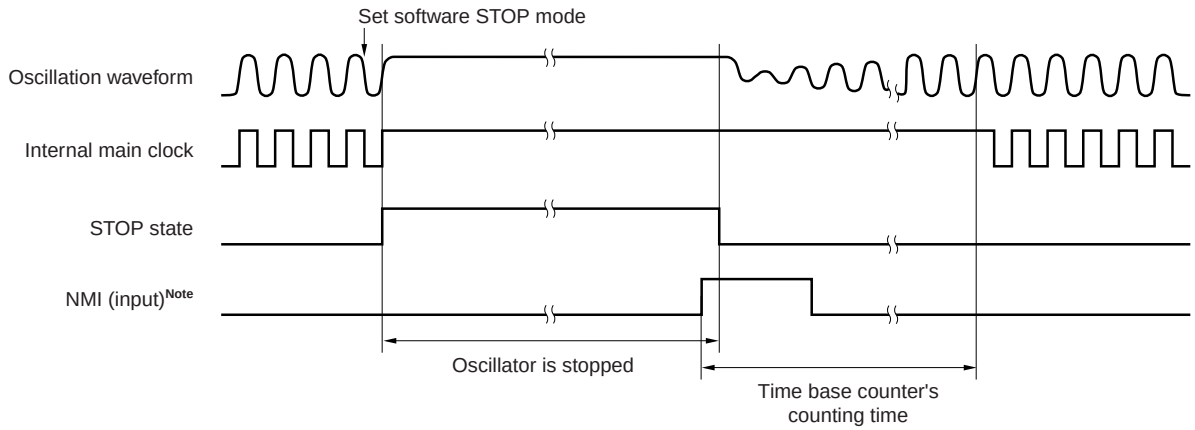
Two specification methods can be used to secure the time from when software STOP mode is released until the stopped oscillator stabilizes.

(1) Securing the time using an on-chip time base counter

Software STOP mode is released when a valid edge is input to the NMI pin or a maskable interrupt request is input (INTPn). Valid edge input to the pin causes the time base counter (TBC) to start counting, and the time until the clock output from the oscillator stabilizes is secured during that counting time (n = 0 to 6, 20 to 25, 30, 31, 100, 101, 110, 111).

Oscillation stabilization time = TBC counting time

After a fixed time, internal system clock output begins, and processing branches to the NMI interrupt or maskable interrupt (INTPn) handler address.



Note Valid edge: When specified as the rising edge.

The NMI pin should usually be set to an inactive level (for example, high level when the valid edge is specified as the falling edge) in advance.

Software STOP mode is immediately released if an operation is performed according to NMI valid edge input or maskable interrupt request input (INTPn) timing in which STOP mode is set until the CPU acknowledges the interrupt.

If direct mode or external clock connection mode (CESEL bit of CKC register = 1) is used, program execution begins after the count time of the time base counter has elapsed.

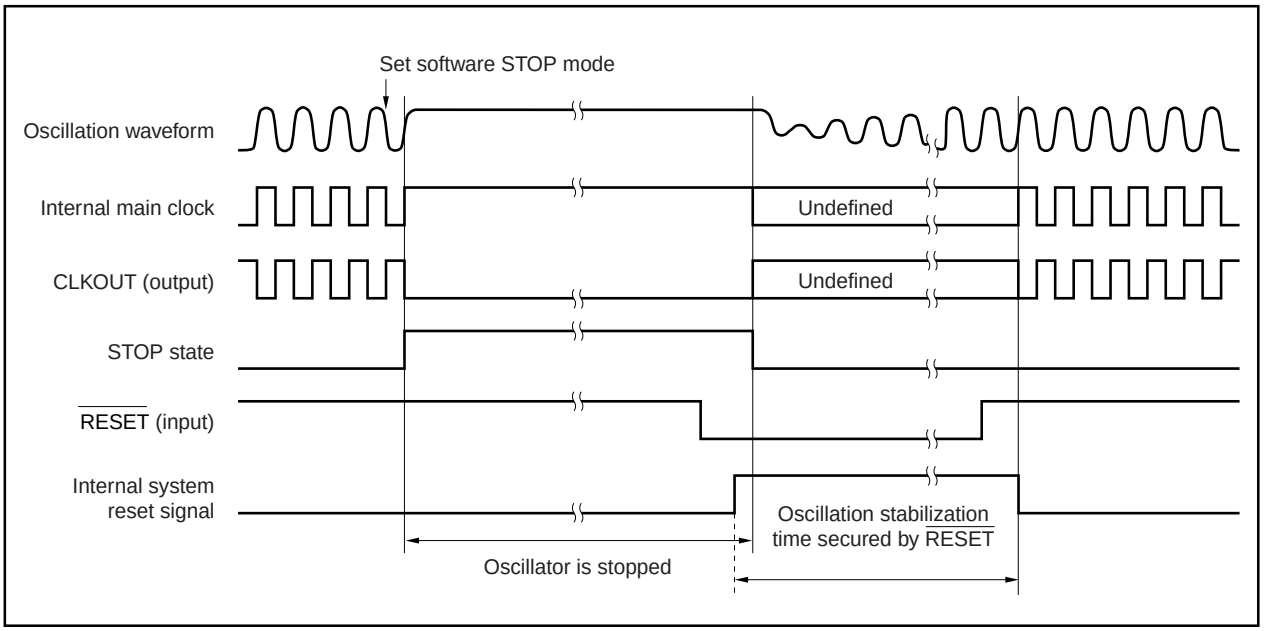
Also, even if PLL mode and resonator connection mode (CESEL bit of CKC register = 0) are used, program execution begins after the oscillation stabilization time is secured according to the time base counter, which begins counting due to NMI pin valid edge input.

(2) Securing the time according to the signal level width ($\overline{\text{RESET}}$ pin input)

Software STOP mode is released due to falling edge input to the $\overline{\text{RESET}}$ pin.

The time until the clock output from the oscillator stabilizes is secured according to the low level width of the signal that is input to the pin.

The supply of internal system clocks begins after a rising edge is input to the $\overline{\text{RESET}}$ pin, and processing branches to the handler address used for a system reset.



8.6.2 Time base counter (TBC)

The time base counter (TBC) is used to secure the oscillator's oscillation stabilization time when software STOP mode is released.

When an external clock is connected (CESEL bit of CKC register = 1) or a resonator is connected (PLL mode and CESEL bit of CKC register = 0), the TBC counts the oscillation stabilization time after software STOP mode is released, and program execution begins after the count is completed.

The TBC count clock is selected according to the TBCS bit of the CKC register, and the next counting time can be set (reference).

Table 8-8. Counting Time Examples ($\phi = 10 \times f_{XX}$)

TBCS Bit	Count Clock	Counting Time	
		f_{XX} = 4.0000 MHz	f_{XX} = 5.0000 MHz
0	$f_{XX}/2^8$	16.3ms	13.1ms
1	$f_{XX}/2^9$	32.6ms	26.2ms

f_{XX}: External oscillation frequency

[MEMO]

CHAPTER 9 TIMER/COUNTER FUNCTION (REAL-TIME PULSE UNIT)

9.1 TIMER 0

9.1.1 Features (timer 0)

Timers 00, 01 (TM00, TM01) are 16-bit timer/counters with a 3-phase PWM output function that have the following functions.

- 3-phase PWM output function
  PWM mode 0 (symmetric triangular wave)
  PWM mode 1 (asymmetric triangular wave)
  PWM mode 2 (sawtooth wave)
- Interrupt culling function
  Culling ratios (1/1, 1/2, 1/3, 1/4, 1/8, 1/16)
- Forcible 3-phase PWM output stop function
  3-phase PWM output can be forcibly stopped by inputting a signal from external signal input pin ESOn during anomalies.
  This function can also be used when the clock is stopped.
- Real-time output function
  3-phase PWM output or rectangular wave output can be changed with the desired timing.

9.1.2 Function overview (timer 0)

- 16-bit timer (TM0n) for 3-phase PWM inverter control: 2 channels
- Compare registers: 4 registers × 2 channels
- 12-bit dead-time timers (DTMn0 to DTMn2): 3 timers × 2 channels
- Count clock division selectable by prescaler (maximum frequency of count clock: 40 MHz)
- Base clock (f_{CLK}): 2 types (maximum frequency of f_{CLK}: 40 MHz)
  ϕ and ϕ/2 can be selected
- Prescaler divide ratio
  The following divide ratios can be selected according to the base clock (f_{CLK}).

Divide Ratio	Base Clock (f_{CLK})	
	ϕ Selected	ϕ/2 Selected
1/1	ϕ	ϕ/2
1/2	ϕ/2	ϕ/4
1/4	ϕ/4	ϕ/8
1/8	ϕ/8	ϕ/16
1/16	ϕ/16	ϕ/32
1/32	ϕ/32	ϕ/64

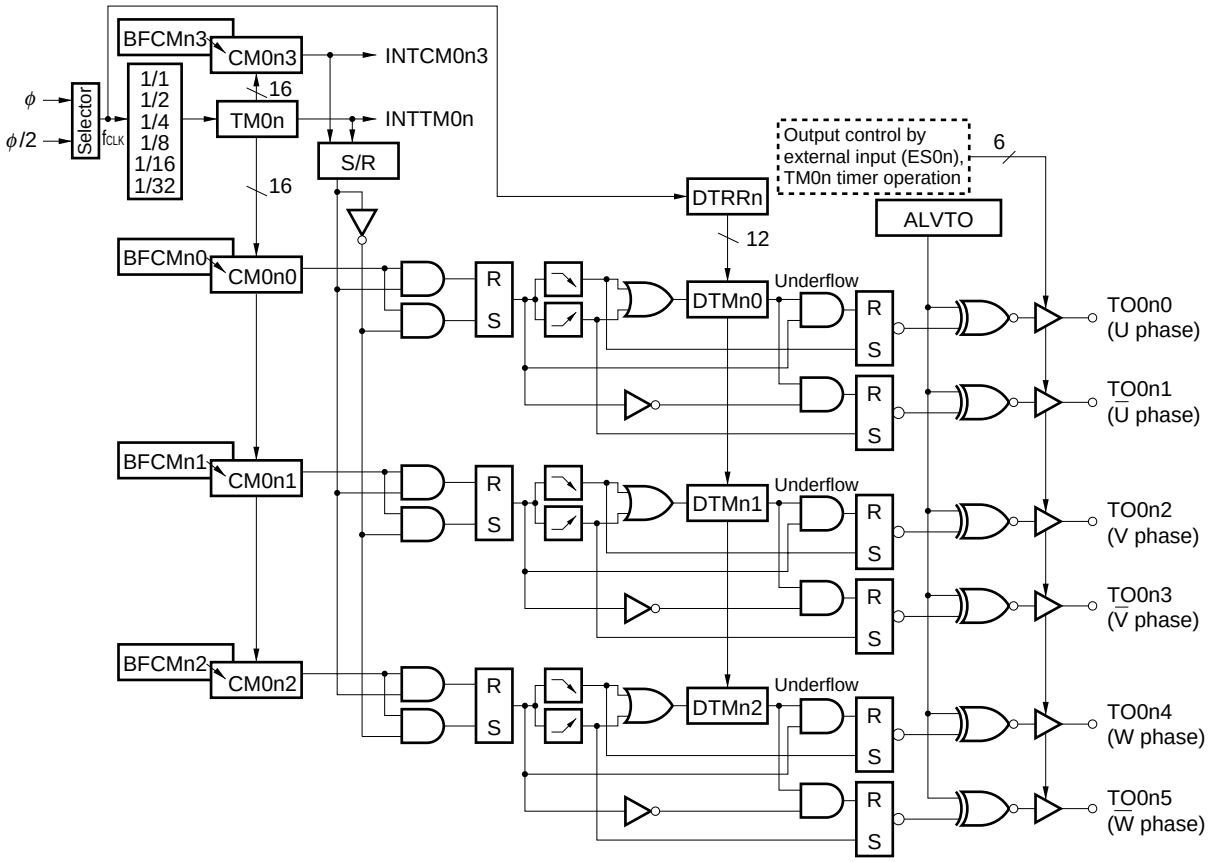
- Interrupt request sources
  - Compare-match interrupt request: 2 types
    INTCM0n3 generated with CM0n3 matching signal
  - Underflow interrupt request: 2 types
    INTTM0n generated by underflow
- External pulse output (TO0n0 to TO0n5): 6 × 2 channels

Remark ϕ : Internal system clock
n = 0, 1

9.1.3 Basic configuration

The basic configuration is shown below.

Figure 9-1. Block Diagram of Timer 0 (Mode 0: Symmetric Triangular Wave, Mode 1: Asymmetric Triangular Wave)



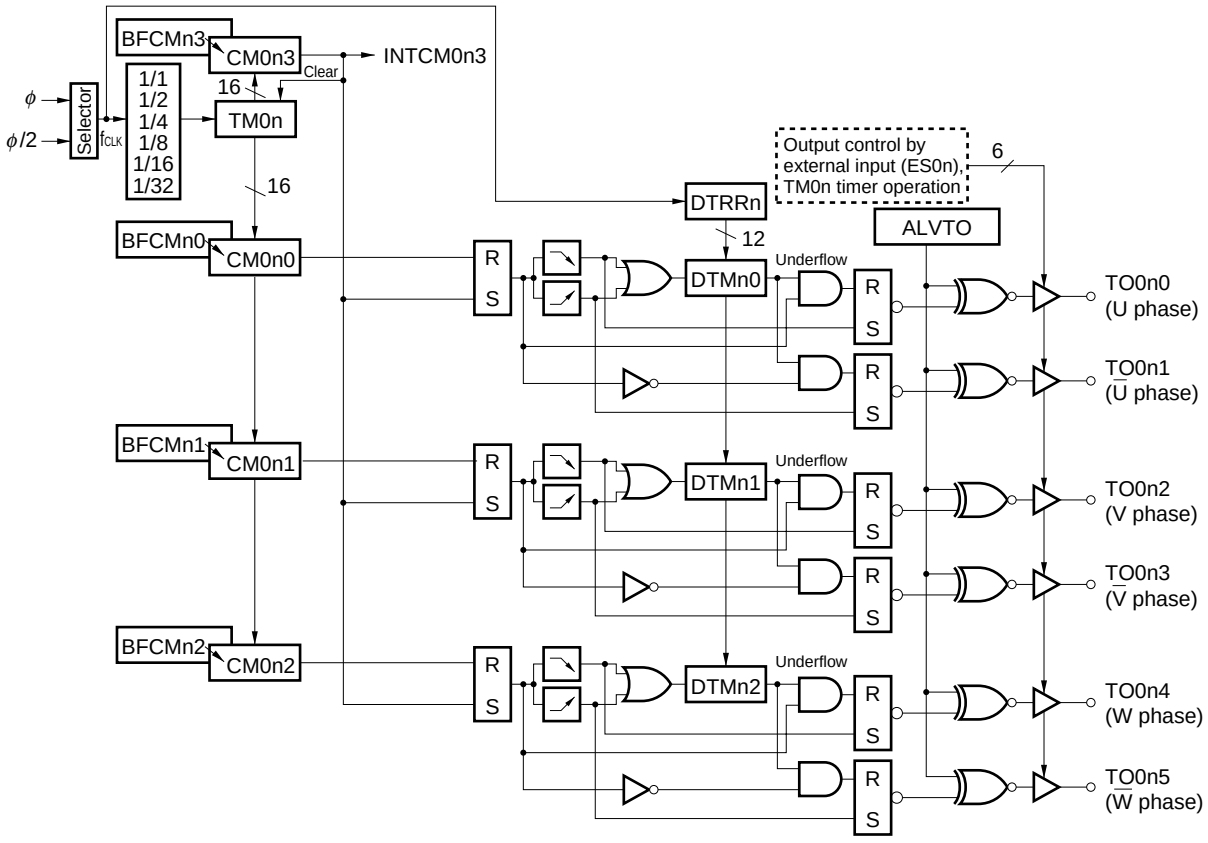
Remarks 1. TM0n: Timer register
CM0n0 to CM0n3: Compare registers
BFCMn0 to BFCMn3: Buffer registers
DTRRn: Reload register
DTMn0 to DTMn2: Dead time timers
ALVTO: Bit 7 of TOMRn register
S/R: Set/Reset

2. n = 0, 1

3. ϕ : Internal system clock

4. f_{CLK}: Base clock (40 MHz (MAX.))

Figure 9-2. Block Diagram of Timer 0 (Mode 2: Sawtooth Wave)



Remarks 1. TM0n: Timer register
CM0n0 to CM0n3: Compare registers
BFCMn0 to BFCMn3: Buffer registers
DTRRn: Reload register
DTMn0 to DTMn2: Dead time timers
ALVTO: Bit 7 of TOMRn register

2. n = 0, 1

3. ϕ : Internal system clock

4. f_{CLK}: Base clock (40 MHz (MAX.))

(1) Timers 00, 01 (TM00, TM01)

TM0n operates as a 16-bit up/down timer or up timer. The cycle is controlled by compare register 0n3 (CM0n3) (n = 0, 1).

TM0n start/stop is controlled by the CE0 bit of timer control register 0n (TMC0n).

Division by the prescaler can be selected for the count clock from among f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$ with the PRM02 to PRM00 bits of the TMC0n registers (f_{CLK}: base clock, see **9.1.4 (1) Timer 0n clock selection register (PRM01)**).

The conditions when TM0n becomes 0000H are as follows.

- Reset input
- CE0 bit = 0
- TM0n register and compare register 0n3 (CM0n3) match (PWM mode 2 (sawtooth wave) only)
- Immediately after overflow or underflow

The TM0n timer has 3 operation modes, shown in Table 9-1. The operation mode is selected with timer control register 0n (TMC0n).

Table 9-1. Timer 0 Operation Modes

Operation Mode	Count Operation	Timer Clear Cause	Interrupt Source	BFCMn3 → CM0n3 Transfer Timing	BFCMn0 to BFCMn2→ CM0n0 to CM0n2 Transfer Timing
PWM mode 0 (symmetric triangular wave)	Up/down	–	INTTM0n INTCM0n3	INTTM0n	INTTM0n
PWM mode 1 (asymmetric triangular wave)	Up/down	–	INTTM0n INTCM0n3	INTTM0n	INTTM0n INTCM0n3
PWM mode 2 (sawtooth wave)	Up	INTCM0n3	INTCM0n3	INTCM0n3	INTCM0n3

Remark n = 0, 1

(2) Dead time timers 00 to 02, 10 to 12 (DTM00 to DTM02, DTM10 to DTM12)

DTMn0 to DTMn2 are dedicated 12-bit down timers that generate dead time suitable for inverter control application. DTMn0 to DTMn2 operate as one-shot timer.

Counting by a dead time timer is enabled or disabled by the CED bit of timer control register 0n (TMC0n) and cannot be controlled through software. Dead time timer count start and stop is controlled through hardware.

A dead time timer starts counting down when the value of the dead time timer reload register n (DTRRn) is transferred in synchronization with the compare match timing of CM0n0 to CM0n2.

When the value of a dead time timer changes from 0000H to FFFFH, the dead time timer generates an underflow signal, and the timer stops at the value FFFFH.

If the value of a dead time timer coincides with the value of the corresponding compare register before underflow of the dead time timer takes place, the value of DTRRn is transferred to the dead time timer again, and the timer starts down counting.

The count clock of the dead time timer is fixed to the base clock (f_{CLK}), and the dead time width is (Set value of DTRRn + 1)/base clock (f_{CLK}).

If TM0n operates in PWM mode 0, PWM mode 1 with the dead time timer count operation disabled, an opposite signal without dead time is output to TO0n0 and TO0n1, TO0n2 and TO0n3, and TO0n4 and TO0n5.

(3) Dead time timer reload registers 0, 1 (DTRR0, DTRR1)

DTRRn register is a 12-bit register used to set the values of the three dead time timers (DTMn0 to DTMn2 registers) (n = 0, 1). However, a value is transferred from the DTRRn register to each dead time register independently.

DTRRn can be read/written in 16-bit units. All 0s are read for the high-order 4 bits when 16-bit read access is performed to the DTRRn register.

Figure 9-3. Dead Time Timer Reload Registers 0, 1 (DTRR0, DTRR1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DTRR0																	FFFFF570H	FFFH
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DTRR1																	FFFFF5B0H	FFFH

Caution Changing the value of the DTRRn register during TM0n operation (CE0 bit of TMC0n register = 1) is prohibited.

(4) Compare registers 000 to 002, 010 to 012 (CM000 to CM002, CM010 to CM012)

CM0n0 to CM0n2 are 16-bit registers that always compare their own values with the value of TM0n. If the value of a compare register matches the value of TM0n, the compare register outputs a trigger signal, and changes the contents of the flip-flop (F/F) connected to the compare register. Each of CM0n0 to CM0n2 is provided with a buffer register (BFCMn0 to BFCMn2), so that the contents of the buffer are transferred to CM0n0 to CM0n2 at the following base clock (f_{CLK}). Transfer is enabled or disabled by the BFTEN bit of the TMC0n register.

(5) Compare registers 003, 013 (CM003, CM013)

CM0n3 is a 16-bit register that always compare its value with the value of TM0n. If the values match, CM0n3 outputs an interrupt signal (INTCM0n3). CM0n3 controls the maximum count value of TM0n, and if the values match, it performs the following operations at the next timer count clock.

- In triangular wave setting mode (PWM modes 0, 1): Switches TM0n operation from up count to down count
- Sawtooth wave setting mode (PWM mode 2): Clears the count value of TM0n

CM0n3 also has a buffer register (BFCMn3) and transfers the buffer contents in the next base clock (f_{CLK}) cycle to CM0n3. Transfer enable or disable is controlled with the BFTE3 bit of the TMC0n register.

(6) Buffer registers CM00 to CM02, CM10 to CM12 (BFCM00 to BFCM02, BFCM10 to BFCM12)

BFCMn0 to BFCMn2 are 16-bit registers that transfer data to the compare register (CM0n0 to CM0n2) corresponding to each buffer register when an interrupt signal (INTCM0n3/INTTM0n) is generated.

BFCMn0 to BFCMn2 can be read/written in 16-bit units.

Caution The set values of the BFCMn0 to BFCMn2 registers are transferred to the CM0n0 to CM0n2 registers in the following timing (n = 0, 1).

- **When CE0 bit of TMC0n register = 0: Transfer at next operation timing after write to BFCMn0 to BFCMn2 register**
- **When CE0 bit of TMC0n register = 1: Value of BFCMn0 to BFCMn2 registers is transferred to CM0n0 to CM0n2 registers upon occurrence of INTTM0n or INTCM0n3. At this time, transfer enable or disable is controlled by the BFTEN bit of the timer control register (TMC0n).**

Figure 9-4. Buffer Registers CM00 to CM02, CM10 to CM12 (BFCM00 to BFCM02, BFCM10 to BFCM12)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
BFCM00																	FFFFF572H	FFFFH
BFCM10																	FFFFF5B2H	FFFFH
BFCM01																	FFFFF574H	FFFFH
BFCM11																	FFFFF5B4H	FFFFH
BFCM02																	FFFFF576H	FFFFH
BFCM12																	FFFFF5B6H	FFFFH

(7) Buffer registers CM03, CM13 (BFCM03, BFCM13)

BFCMn3 is a 16-bit register that transfers data to the compare register at any timing. Transfer enable or disable is controlled by the BFTE3 bit of the TMC0n register.

BFCMn3 can be read/written in 16-bit units.

Cautions 1. The set value of the BFCMn3 register is transferred to the CM0n3 register in the following timing (n = 0, 1).

- **When CE0 bit of TMC0n register = 0: Transfer at next operation timing after write to BFCMn3 register**
- **When CE0 bit of TMC0n register = 1: Value of BFCMn3 register is transferred to CM0n3 register upon occurrence of INTTM0n. At this time, transfer enable or disable is controlled by the BFTE3 bit of the timer control register (TMC0n).**

2. Setting the BFCMn3 register to 0000H is prohibited.

Figure 9-5. Buffer Registers CM03, CM13 (BFCM03, BFCM13)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
BFCM03																	FFFFF578H	FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
BFCM13																	FFFFF5B8H	FFFFH

9.1.4 Control registers

(1) Timer 0n clock selection register (PRM01)

The PRM01 register is used to select the base clock (f_{CLK}) of timer 0 (TM0n).

It can be read/written in 8- or 1-bit units.

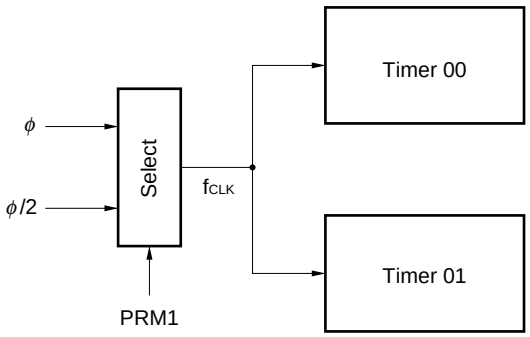
Caution Always set this register before using the timer.

Figure 9-6. Timer 0n Clock Selection Register (PRM01)

	7	6	5	4	3	2	1	0	Address	Initial Value
PRM01	0	0	0	0	0	0	0	PRM1	FFFFF5D0H	00H

Bit Position	Bit Name	Function
0	PRM1	Specifies the base clock (f_{CLK}) of timer 0 (TM0n) (See **Figure 9-7**). 0: ϕ/2 (When 0 > 40 MHz) 1: ϕ (When 0 ≤ 40 MHz) **Remark** ϕ: Internal system clock

Figure 9-7. Timer 00 and Timer 01 Clock



Remarks 1. ϕ: Internal system clock

2. f_{CLK}: Base clock

(2) Timer control registers 00, 01 (TMC00, TMC01)

TMC0n register is a 16-bit register that sets the operation of timer 0 (TM0n).

The TMC0n register can be read/written in 16-bit units.

If the high-order 8 bits of the TMC0n register are used as the TMC0nH register and the low-order 8 bits as the TMC0nL register, the register can be read/written in 8- or 1-bit units.

Caution To operate timer 0, first set CE0 = 0 and then set CE0 = 1.

Figure 9-8. Timer Control Registers 00, 01 (TMC00, TMC01) (1/4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TMC00	CE0	STINT	CUL02	CUL01	CUL00	PRM02	PRM01	PRM00	0	0	CED	BFTE3	BFTEN	MBFTE	MOD01	MOD00	FFFFF57AH	0508H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TMC01	CE0	STINT	CUL02	CUL01	CUL00	PRM02	PRM01	PRM00	0	0	CED	BFTE3	BFTEN	MBFTE	MOD01	MOD00	FFFFF5BAH	0508H

Bit Position	Bit Name	Function
15	CE0	Specifies the operation of TM0n. 0: Count disabled (stops after all count values are cleared) 1: Count enabled **Caution When CE0 = 0, TO0n0 to TO0n5 output becomes high impedance.**
14	STINT	Specifies interrupt during TM0n timer start. 0: Don't generate interrupt at operation start 1: Generate interrupt at operation start When STINT bit = 1, an interrupt is generated immediately after the rising edge of the CE0 signal. When the MOD01 bit = 0 (triangular wave mode), the INTTM0n interrupt (see **Figure 9-9**) is generated, and when the MOD01 bit = 1 (sawtooth wave mode), the INTCM0n3 interrupt is generated. **Caution Changing the STINT bit during TM0n operation (CE0 bit = 1) is prohibited.**
13 to 11	CUL02 to CUL00	Specifies the interrupt culling ratio.

CUL02	CUL01	CUL00	Interrupt Culling Ratio
0	0	0	1/1
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	1/16
Other than above			Don't perform culling

Remark n = 0, 1

Figure 9-8. Timer Control Registers 00, 01 (TMC00, TMC01) (2/4)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>13 to 11</td><td>CUL02 to CUL00</td><td>Cautions 1. INTTM0n interrupts and INTCM0n3 interrupts can be culled with the same culling ratio (1/1, 1/2, 1/4, 1/8, 1/16).
2. Even when BFTE3 bit = 1, BFTEN bit = 1 (settings to transfer data from BFCMn0 to BFCMn3 registers to CM0n0 to CM0n3 registers), transfer is not performed with the generation timing of culled INTTM0n and INTCM0n3 interrupts if the MBFTE bit = 0.
3. If the culling ratio is changed during counter operation, the new culling ratio is applied after an interrupt has occurred with the culling ratio prior to the change (See Figure 9-10).</td></tr>
<tr><td>10 to 8</td><td>PRM02 to PRM00</td><td>Specifies the count clock for TM0n.

<table>
<tr><th>PRM02</th><th>PRM01</th><th>PRM00</th><th>Count Clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>f_{CLK}</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>$f_{CLK}/2$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>$f_{CLK}/4$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>$f_{CLK}/8$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>$f_{CLK}/16$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>$f_{CLK}/32$</td></tr>
<tr><td colspan="3">Other than above</td><td>Setting prohibited</td></tr>
</table>
Cautions 1. The divide ratio switch timing is from when the TM0n value has become 0000H and an INTTM0n interrupt has occurred. Therefore, in the timing that corresponds to interrupt culling, the divide ratio is not switched.
2. Set the count clock of timer 0 to 40 MHz as the upper limit.
Remark For the base clock (f_{CLK}), see 9.1.4 (1) Timer 0n clock selection register (PRM01).</td></tr>
<tr><td>5</td><td>CED</td><td>Specifies the operation of DTMn0 to DTMn2 timers..
0: DTMn0 to DTMn2 perform count operation
1: DTMn0 to DTMn2 stopped

Cautions 1. Changing the CED bit during TM0n operation (CE0 = 1) is prohibited.
2. If TM0n is operated when the CED bit = 1, a signal without dead time is output to the TO0n0 to TO0n5 pins.</td></tr>
</table>

Remark n = 0, 1

Figure 9-8. Timer Control Registers 00, 01 (TMC00, TMC01) (3/4)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>4</td><td>BFTE3</td><td>Specifies transfer of data from BFCMn3 register to CM0n3 register.
0: Transfer disabled
1: Transfer enabled
The transfer timing from the BFCMn3 register to the CM0n3 register is as follows.
<table>
<tr><th>BFTE3</th><th>TM0n Operation Mode</th><th>BFCMn3 → CM0n3 Transfer Timing</th></tr>
<tr><td>0</td><td>All modes</td><td>Don’t transfer</td></tr>
<tr><td>1</td><td>PWM mode 0 (symmetric triangular wave)</td><td>INTTM0n</td></tr>
<tr><td>1</td><td>PWM mode 1 (asymmetric triangular wave)</td><td>INTTM0n</td></tr>
<tr><td>1</td><td>PWM mode 2 (sawtooth wave)</td><td>INTCM0n3</td></tr>
</table>
When the BFTE3 bit = 1, the value of the BFCMn3 register is transferred to the CM0n3 register upon occurrence of an INTTM0n or INTCM0n3 interrupt.</td></tr>
<tr><td>3</td><td>BFTEN</td><td>Specifies transfer of data from BFCMn0 to BFCMn2 registers to CM0n0 to CM0n2 registers.
0: Transfer disabled
1: Transfer enabled
<table>
<tr><th>BFTEN</th><th>TM0n Operation Mode</th><th>BFCMn0 to BFCMn2 → CM0n0 to CM0n2 Transfer Timing</th></tr>
<tr><td>0</td><td>All modes</td><td>Don’t transfer</td></tr>
<tr><td>1</td><td>PWM mode 0 (symmetric triangular wave)</td><td>INTTM0n</td></tr>
<tr><td>1</td><td>PWM mode 1 (asymmetric triangular wave)</td><td>INTTM0n, INTCM0n3</td></tr>
<tr><td>1</td><td>PWM mode 2 (sawtooth wave)</td><td>INTCM0n3</td></tr>
</table>
When the BFTEN bit = 1, the values of the BFCMn0 to BFCMn2 registers are transferred to the CM0n0 to CM0n2 registers upon occurrence of an INTTM0n or INTCM0n3 interrupt.</td></tr>
<tr><td>2</td><td>MBFTE</td><td>When culling of INTTM0n and INTCM0n3 interrupts is set with the CUL02 to CUL00 bits, specifies whether enable or disable the BFTE3 and BFTEN bit settings upon occurrence of an interrupt for culling.
0: Disable the set values of BFTE3, BFTEN bits upon occurrence of a culling interrupt
1: Enable the set values of BFTE3, BFTEN bits upon occurrence of a culling interrupt
The various combinations are as follows.
<table>
<tr><th colspan="2" rowspan="2">MBFTE</th><th colspan="2">Operation upon Occurrence of Interrupt for Culling</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">BFTEN</td><td>0</td><td>BFCMn0 to BFCMn2 → CM0n0 to CM0n2 transfer disabled</td><td>BFCMn0 to BFCMn2 → CM0n0 to CM0n2 transfer disabled</td></tr>
<tr><td>1</td><td>BFCMn0 to BFCMn2 → CM0n0 to CM0n2 transfer disabled</td><td>BFCMn0 to BFCMn2 → CM0n0 to CM0n2 transfer enabled</td></tr>
<tr><td rowspan="2">BFTE3</td><td>0</td><td>BFCMn3 → CM0n3 transfer disabled</td><td>BFCMn3 → CM0n3 transfer disabled</td></tr>
<tr><td>1</td><td>BFCMn3 → CM0n3 transfer disabled</td><td>BFCMn3 → CM0n3 transfer enabled</td></tr>
</table>
.</td></tr>
</table>

Remark n = 0, 1

Figure 9-8. Timer Control Registers 00, 01 (TMC00, TMC01) (4/4)

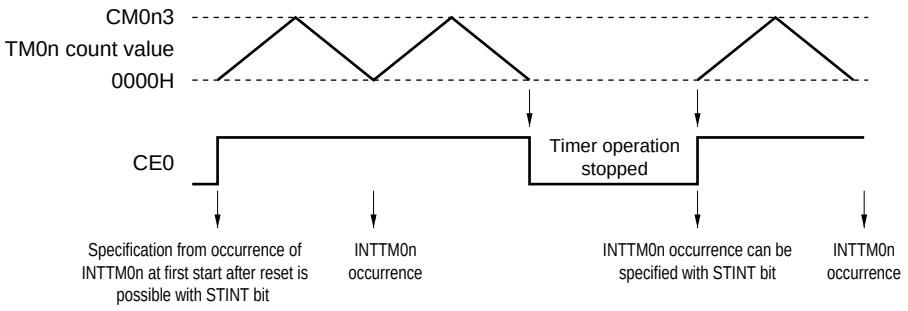
Bit Position	Bit Name	Function
1, 0	MOD01, MOD00	Specifies the operation mode of TM0n.

MOD 01	MOD 00	Operation Mode	TM0n Operation	Timer Clear Cause	BFCMn3 → CM0n3 Timing	BFCM0 to BFCM2 → CM0n0 to CM0n2 Timing
0	0	PWM mode 0 (symmetric triangular wave)	Up/down	–	INTTM0n	INTTM0n
0	1	PWM mode 1 (asymmetric triangular wave)	Up/down	–	INTTM0n	INTTM0n, INTCM0n3
1	0	PWM mode 2 (sawtooth wave)	Up	INTCM0n3	INTCM0n3	INTCM0n3
1	1	Setting prohibited				

Caution Changing the value of the MOD01, MOD00 bits during TM0n operation (CE0 bit = 1) is prohibited.

Remark n = 0, 1

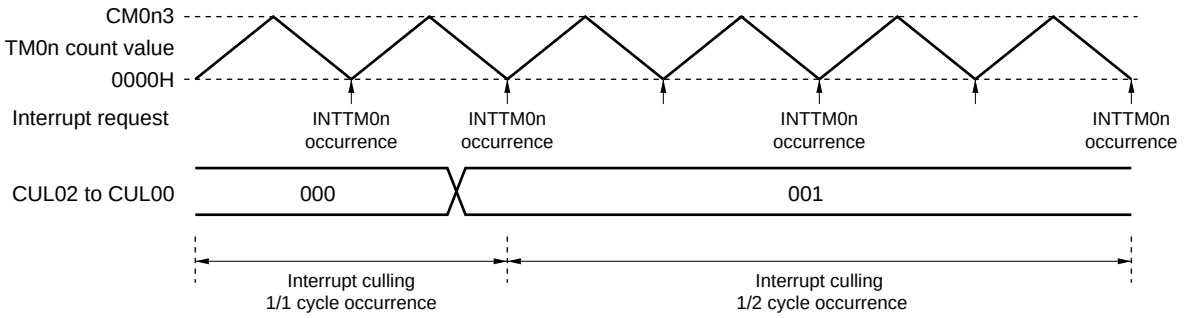
Figure 9-9. Specification of INTTM0n Interrupt During PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave) (MOD01, MOD00 Bits of TMC0n Register = 0n)



Remark n = 0, 1

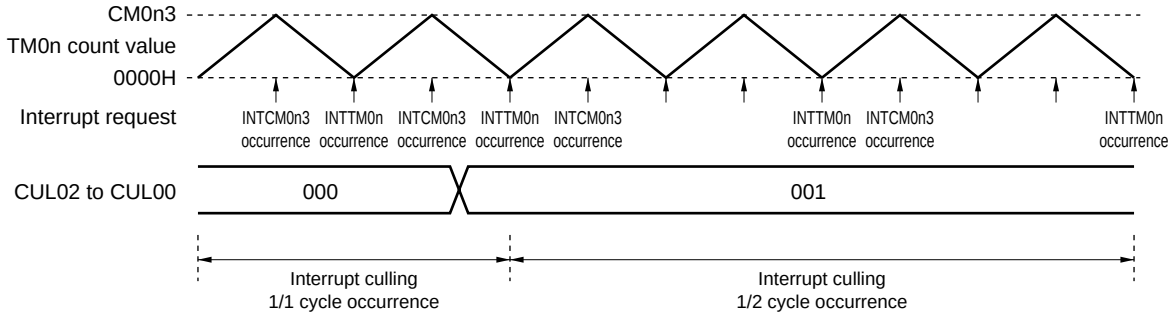
Figure 9-10. Interrupt Culling Processing

(a) PWM mode 0 (symmetric triangular wave)



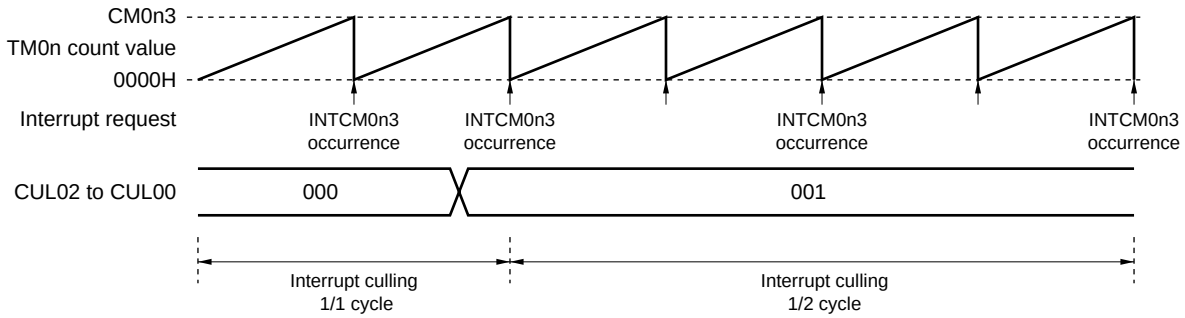
Remark n = 0, 1

(b) PWM mode 1 (asymmetric triangular wave)



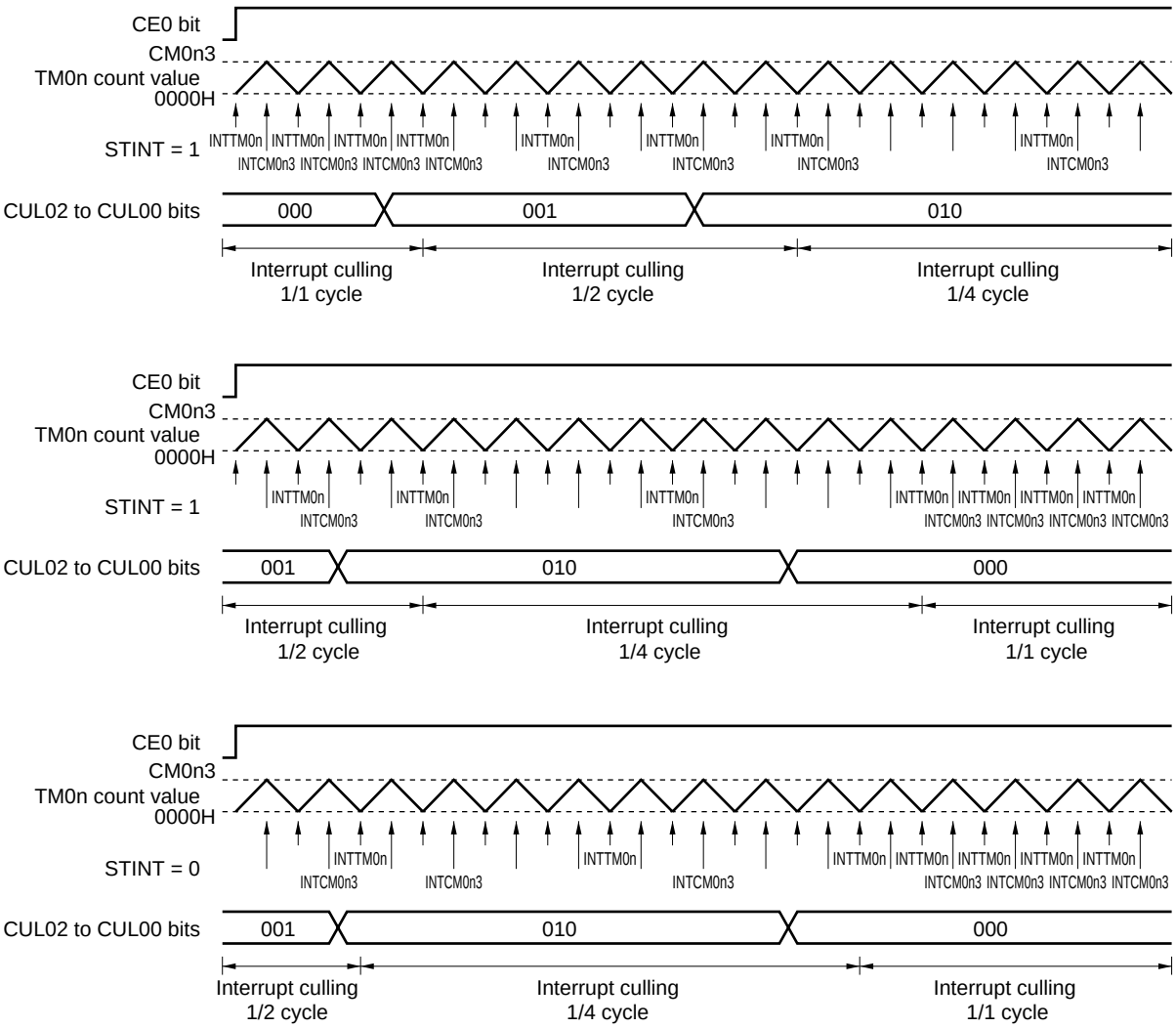
Remark n = 0, 1

(c) PWM mode 2 (sawtooth wave)



Remark n = 0, 1

Figure 9-11. Interrupt Culling Ratio Change Timing
(Relationship Between STINT Bit Setting and CUL Bit Change): PWM Mode 1 (Asymmetric Triangular Wave)



Caution If, in TM0n, to realize the INTTM0n and INTCM0n3 culling function, the culling ratio is set to a value other than 1/1 with bits CUL02 to CUL00 and counting is started, the subsequent interrupt output sequence will differ due to the set value of the STINT bit at count start.

Remark n = 0, 1

(3) Timer unit control registers 00, 01 (TUC00, TUC01)

TUC0n register is an 8-bit register that controls TO0n0 to TO0n5 outputs.

TUC0n can be read/written in 8- or 1-bit units.

Figure 9-12. Timer Unit Control Registers 00, 01 (TUC00, TUC01)

	7	6	5	4	3	2	1	0	Address	Initial Value
TUC00	0	0	0	0	0	0	TORS	TOSTA	FFFFF57CH	01H

	7	6	5	4	3	2	1	0	Address	Initial Value
TUC01	0	0	0	0	0	0	TORS	TOSTA	FFFFF5BCH	01H

Bit Position	Bit Name	Function
1	TORS	Flag that restarts TO0n0 to TO0n5 pin outputs that was forcibly stopped through ESOn pin input. Causes output to resume by writing “1” to TORS bit. **Cautions 1. If the level is the ESOn pin input level (TOMR register TOEDG1 bit = 1, TOEDG0 bit = 0 or 1), the output disabled state is not released even if “1” is written to the TORS bit while the level is the output disable level.** **2. After reset, be sure to write “1” to the TORS bit prior to operating TM0n. A “0” is read when the TORS bit is read.**
0	TOSTA	TO0n0 to TO0n5 pin output status flag through ES0n pin input 0: Output enabled status 1: Output disabled status

Remark n = 0, 1

(4) Timer output mode registers 0, 1 (TOMR0, TOMR1)

The TOMRn register controls timer output from the TO0n0 to TO0n5 pins.

To prevent abnormal output from pins TO0n0 to TO0n5 due to illegal access, data write to the TOMRn register consists of the following two sequences.

(a) Write access to the TOMR write enable register (SPECn), followed by

(b) Write access to the TOMRn register

Write is not enabled hardware-wise unless the these two sequences are implemented.

TOMRn can be read/written in 8-bit units.

Caution When interrupt requests are generated during write access to the TOMRn register (after write access to the SPECn register and prior to write to the TOMRn register), write processing to the TOMRn register may not be performed normally if access to other addresses is performed using the internal bus during servicing of these interrupts. Add one of the following processing items during the TOMRn register write routine.

- **Prior to write access to the TOMRn register, disable acknowledge of all interrupts of CPU.**
- **Following write access to the TOMRn register, check that write was performed normally.**

Figure 9-13. Timer Output Mode Registers 0, 1 (TOMR0, TOMR1) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial Value
TOMR0	ALVTO	0	0	0	TOSP	0	TOEDG1	TOEDG0	FFFFF57DH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
TOMR1	ALVTO	0	0	0	TOSP	0	TOEDG1	TOEDG0	FFFFF5BDH	00H

Bit Position	Bit Name	Function
7	ALVTO	Specifies the active level of TO0n0 to TO0n5 pins. 0: Active level is low level 1: Active level is high level **Caution Changing the ALVTO bit during TM0n operation (CE0 = 1) is prohibited.**

Remark n = 0, 1

Figure 9-13. Timer Output Mode Registers 0, 1 (TOMR0, TOMR1) (2/2)

Bit Position	Bit Name	Function
3	TOSP	Controls TO0n0 to TO0n5 pin output stop through ESOn pin input. 0: Enables ESOn pin input 1: Disables ESOn pin input **Cautions 1. The output stop status can be released by writing "1" to the TORS bit of the TUC0n register. The operation continues even if output is prohibited for all timers and counters.** **2. Before changing the ESOn pin input status from disable to enable (changing TOSP bit from 1 to 0), write "1" to the TORS bit of the TUCn register to reset the ESOn pin input status.**
1, 0	TOEDG1, TOEDG0	These bits select the valid edge or level when setting forcible stop of TO0n0 to TO0n5 output through ESOn pin input with the TOSP bit. TOEDG1 / TOEDG0 / Operation 0 / 0 / Rising edge 0 / 1 / Falling edge 1 / 0 / Low level 1 / 1 / High level **Cautions 1. Changing the TOEDG1, TOEDG0 bits during TM0n operation (CE0 = 1) is prohibited.** **2. Before changing the settings of bits TOEDG1 and TOEDG0, write "1" to the TORS bit of the TUC0n register to reset the ESOn pin input status.**

Remark n = 0, 1

Data setting to timer output mode registers 0, 1 (TOMR0, TOMR1) is done in the following sequence.

<1> Prepare the data to be set to timer output mode registers 0, 1 (TOMR0, TOMR1) in a general-purpose register.
<2> Write data to the TOMR write enable registers 0, 1 (SEPC0, SPEC1).
<3> Set timer output mode registers 0, 1 (TOMR0, TOMR1) (performed with the following instructions).
- Store instruction (ST/SST instructions)
- Bit manipulation instruction (SET1/CLR1/NOT1 instructions)

[Description Example]
```
<1>  MOV    0x04, r10
<2>  ST.B   r10, SPECn [r0]
<3>  ST.B   r10, TOMRn [r0]
```

Remark n = 0, 1

To read the TOMRn register, no special sequence is required.

Cautions 1. Prohibit interrupts between SPECn issue (<2>) and TOMRn register write that immediately follows (<3>).

2. The data written to the SPECn register is dummy data; use the same register as the general-purpose register used to set the TOMRn register (<3> in the above example) for SPECn register write (<2> in the above example). The same applies when using a general-purpose register for addressing.

3. Do not write to the SPECn register or TOMRn register via DMA transfer.

(5) PWM output enable registers 0, 1 (POER0, POER1)

The POERn register is used to make the external pulse output (TO0n0 to TO0n5) status inactive by software. POERn can be read/written in 8- or 1-bit units.

Figure 9-14. PWM Output Enable Registers 0, 1 (POER0, POER1)

	7	6	5	4	3	2	1	0	Address	Initial Value
POER0	0	0	OE21	OE20	OE11	OE10	OE01	OE00	FFFFF57FH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
POER1	0	0	OE21	OE20	OE11	OE10	OE01	OE00	FFFFF5BFH	00H

Bit Position	Bit Name	Function
5	OE21	Specifies output status of TO0n5 pin. 0: TO0n5 output status is high impedance. 1: TO0n5 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.
4	OE20	Specifies output status of TO0n4 pin. 0: TO0n4 output status is high impedance. 1: TO0n4 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.
3	OE11	Specifies output status of TO0n3 pin. 0: TO0n3 output status is high impedance. 1: TO0n3 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.
2	OE10	Specifies output status of TO0n2 pin. 0: TO0n2 output status is high impedance. 1: TO0n2 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.
1	OE01	Specifies output status of TO0n1 pin. 0: TO0n1 output status is high impedance. 1: TO0n1 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.
0	OE00	Specifies output status of TO0n0 pin. 0: TO0n0 output status is high impedance. 1: TO0n0 output status is controlled by CE0 bit of TMC0n register and TORTO bit of PSTOn register and ESOn pin.

Remark n = 0, 1

(6) PWM software timing output registers 0, 1 (PSTO0, PSTO1)

The PSTOn register is used to perform settings to output the desired waveforms to the external pulse output pins (TO0n0 to TO0n5) by software.

PSTOn can be read/written in 8- or 1-bit units.

Figure 9-15. PWM Software Timing Output Registers 0, 1 (PSTO0, PSTO1)

	7	6	5	4	3	2	1	0	Address	Initial Value
PSTO0	TORTO	0	0	0	0	UPORT	VPORT	WPORT	FFFFF57EH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
PSTO1	TORTO	0	0	0	0	UPORT	VPORT	WPORT	FFFFF5BEH	00H

Bit Position	Bit Name	Function
7	TORTO	Specifies TO0n0 to TO0n5 output control. 0: Timer output 1: Software output The TO0n0 to TO0n5 signals changes during software output are implemented when the TORTO bit is set (to “1”) and a value is written to the UPORT, VPORT, and WPORT bits. A dead time timer can be used. **Caution When the value of the TORTO bit has been changed from “0” to “1” during timer output (setting changed to software output), the timing is delayed by the dead time portion when the output level differs from the timer output signal during output due to the settings of the UPORT, VPORT, and WPORT bits.** **When the output level is the same as the timer output signal during output due to the settings of the UPORT, VPORT, and WPORT bits, output is performed maintaining the same output level.**
2	UPORT	Specifies the U-phase output value. 0: Output opposite level of level specified with ALVTO bit of TOMRn register to TO0n0 1: Output level specified with ALVTO bit of TOMRn register to TO0n0 For the $\overline{U}$ phase (TO0n1), the opposite level of the U phase (TO0n0) is output.
1	VPORT	Specifies the V-phase output value. 0: Output opposite level of level specified with ALVTO bit to TO0n2 1: Output level specified with ALVTO bit to TO0n2 For the $\overline{V}$ phase (TO0n3), the opposite level of the V phase (TO0n2) is output.
0	WPORT	Specifies the W-phase output value. 0: Output opposite level of level specified with ALVTO bit to TO0n4 1: Output level specified with ALVTO bit of TO0n4 For the $\overline{W}$ phase (TO0n5), the opposite level of the W phase (TO0n4) is output.

Remark n = 0, 1

The following table shows the output status of external pulse output (in the case of TO0n0).

Table 9-2. Output Status of External Pulse Output (In Case of TO0n0)

OE00 Bit	TORTO, UPORT Bits	CE0 Bit	TO0n0
0	0/1	0/1	High impedance
1	0	0	High impedance
		1	PWM output
	1	0/1	Output by UPORT bit

Remarks 1. OE00 bit: Bit 0 of POERn register
TORTO bit: Bit 7 of PSTOn register
UPORT bit: Bit 2 of PSTOn register
CE0 bit: Bit 15 of TMC0n register

2. n = 0, 1

(7) TOMR write enable registers 0, 1 (SPEC0, SPEC1)

The SPECn register enables write to the TOMRn register. Unless write to the TOMRn register is performed following immediately after write to the SPECn register (any data can be written), write processing to the TOMRn register is not performed normally. Normally, 0000H is read.

The SPECn register can be read/written in 16-bit units.

Figure 9-16. TOMR Write Enable Registers 0, 1 (SPEC0, SPEC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SPEC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FFFFF580H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SPEC1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FFFFF5C0H	0000H

9.1.5 Operation

(1) Basic operation

Timer 0 (TM0n) is a 16-bit interval timer that operates as an up/down timer or as an up timer. The cycle is controlled with compare register 0n3 (CM0n3) (n = 0, 1).

All TM0n bits are cleared (0) by $\overline{\text{RESET}}$ input and count operation is stopped.

Count operation enable/disable is controlled by the CE0 bit of timer control register 0n (TMC0n). The count operation is started by setting the CE0 bit to 1 by software. Resetting the CE0 bit to 0 clears TM0n and stops the count operation.

When the value of compare register 0n3 (CM0n3) set beforehand and the value of the TM0n counter match, a match interrupt (INTCM0n3) is generated.

The count clock to TM0n can be selected from among 6 internal clocks with the TMC0n register. If the TM0n has been set as an up/down timer, an underflow interrupt (INTTM0n) is generated when TM0n becomes 0000H during down counting.

The TM0n has the following three operation modes, which are selected with timer control register 0n (TMC0n).

- PWM mode 0: Triangular wave modulation (Right-left symmetric waveform control)
- PWM mode 1: Triangular wave modulation (Right-left asymmetric waveform control)
- PWM mode 2: Sawtooth wave modulation control

Table 9-3. Timer 0 (TM0n) Operation Modes

TMC0n Register		Operation Mode	TM0n Operation	Timer Clear Cause	Interrupt Source	BFCMn3 → CM0n3 Timing	BFCM0 to BFCM2→ CM0n0 to CM0n2 Timing
MOD01	MOD00						
0	0	PWM mode 0 (Symmetric triangular wave)	Up/down	–	INTTM0n INTCM0n3	INTTM0n	INTTM0n
0	1	PWM mode 1 (Asymmetric triangular wave)	Up/down	–	INTTM0n INTCM0n3	INTTM0n	INTTM0n INTCM0n3
1	0	PWM mode 2 (Sawtooth wave)	Up	INTCM0n3	INTCM0n3	INTCM0n3	INTCM0n3
1	1	Setting prohibited					

Caution Changing bits MOD01, MOD00 during TM0n operation (CE0 = 1) is prohibited.

Remark n = 0, 1

The various operation modes are described below.

(2) PWM mode 0: Triangular wave modulation (right-left symmetric waveform control)

[Setting procedure]

(a) Set PWM mode 0 (symmetric triangular wave) with bits MOD01 and MOD00 of the TMC0n register. Also set the active level of pins TO0n0 to TO0n5 with the ALVTO bit of the TOMRn register (n = 0, 1).

(b) Set the count clock of TM0n with bits PRM02 to PRM00 of the TMC0n register. The transfer operation from BFCMn3 to CM0n3 is set with bit BFTE3, and the transfer operation from BFCMn0 to BFCMn2 to CM0n0 to CM0n2 is set with bit BFTEN.

(c) Set the initial values.

(i) Specify the interrupt culling ratio with bits CUL02 to CUL00 of the TMC0n register.

(ii) Set the half-cycle width of the PWM cycle in BFCMn3.
- PWM cycle = BFCMn3 value $\times$ 2 $\times$ TM0n count clock
  (The TM0n count clock is set with the TMC0n register.)

(iii) Set the dead time width in DTRRn.
- Dead time width = (DTRRn + 1)/f_{CLK}
  f_{CLK}: Base clock

(iv) Set the set/reset timing of the F/F used in the PWM cycle in BFCMn0 to BFCMn2.

(d) Clear (0) the CED bit of the TMC0n register to enable dead time timer operation. Set CED = 1 if you wish not to use dead time.

(e) Setting (1) the CE0 bit of the TMC0n register starts TM0n counting, and a 6-channel PWM signal is output from pins TO0n0 to TO0n5.

Caution Setting CM0n3 to 0000H is prohibited.

Remark The CE0 bit of the TMC0n register indicates transfer operation under the following conditions.
- When CE0 bit of TMC0n register is 0
  Transfer to the CM0n0 to CM0n2 registers is performed at the next base clock after write to registers BFCMn0 to BFCMn2.
- When CE0 bit of TMC0n register is 1
  The value of the BFCMn0 to BFCMn2 registers is transferred to the CM0n0 to CM0n2 registers upon occurrence of the INTTM0n or INTCM0n3 interrupt. Transfer enable/disable at this time is controlled by bit BFTEN of the TMC0n register.

[Operation]

In PWM mode 0, TM0n performs up/down count operation. When TM0n = 0000H during down counting, an underflow interrupt (INTTM0n) is generated, and when TM0n = CM0n3 during up counting, a match interrupt (INTCM0n3) is generated (n = 0, 1).

Switching from up counting to down counting is performed when TM0n and CM0n3 match (INTCM0n3), and switching from down counting to up counting is performed when TM0n underflow occurs after TM0n becomes 0000H.

The PWM cycle in this mode is (BFCMn3 value $\times$ 2 $\times$ TM0n count clock). Concerning setting of data to BFCMn3, the next PWM cycle width is set to BFCMn3.

The data of BFCMn3 is automatically transferred by hardware to CM0n3 upon generation of the INTTM0n interrupt. Furthermore, calculation is performed by software processing started by INTTM0n, and the data for the next cycle is set to BFCMn3.

Data setting to CM0n0 to CM0n2, which control the PWM duty, is explained next.

Setting of data to CM0n0 to CM0n2 consists in setting the duty output from BFCMn0 to BFCMn2.

The values of BFCMn0 to BFCMn2 are automatically transferred by hardware to CM0n0 to CM0n2 upon generation of the INTTM0n interrupt. Furthermore, software processing is started up and calculation performed, and set/reset timing of the F/F for the next cycle is set to BFCMn0 to BFCMn2.

The PWM cycle and the PWM duty are set in the above procedure.

The F/F set/reset conditions upon match of CM0n0 to CM0n2 are as follows.

- Set: CM0n0 to CM0n2 match detection during TM0n up count operation
- Reset: CM0n0 to CM0n2 match detection during TM0n down count operation

In this mode, the F/F set/reset timing is performed in the same timing (right-left symmetric control). The values of DTRRn are transferred to the corresponding dead time timers (DTMn0 to DTMn2) in synchronization with the set/reset timing of the F/F, and down counting is started. DTMn0 to DTMn2 count down to 000H, and stop when they count down further to FFFH.

DTMn0 to DTMn2 can automatically generate a width (dead time) at which the active levels of the positive phase (TO0n0, TO0n2, TO0n4) and negative phase (TO0n1, TO0n3, TO0n5) do not overlap.

In this way, software processing is started by an interrupt (INTTM0n) that occurs once during every PWM cycle after initial setting has been performed, and by setting the PWM cycle and PWM duty to be used in the next cycle, it is possible to automatically output a PWM waveform to TO0n0 to TO0n5 pins taking into consideration the dead time width (in case of interrupt culling ratio of 1/1).

[Output waveform width in respect to set value]

- PWM cycle = BFCMn3 × 2 × T_{TM0n}
- Dead time width T_{Dnm} = (DTRRn + 1)/f_{CLK}
- Active width of positive phase (TO0n0, TO0n2, TO0n4 pins)
  = { (CM0n3 – $CM0nX_{up}$) + (CM0n3 – $CM0nX_{down}$) } × T_{TM0n} – T_{Dnm}
- Active width of negative phase (TO0n1, TO0n3, TO0n5 pins)
  = ($CM0nX_{down}$ + $CM0nX_{up}$) × T_{TM0n} – T_{Dnm}
- In this mode, $CM0nX_{up}$ = $CM0nX_{down}$ (However, within the same PWM cycle).
  Since $CM0nX_{up}$ and $CM0nX_{down}$ in the negative phase formula are prepared in a separate PWM cycle, $CM0nX_{up} \neq CM0nX_{down}$.

f_{CLK}: Base clock
T_{TM0n}: TM0n count clock
$CM0nX_{up}$: Set value of CM0n0 to CM0n2 while TM0n is counting up
$CM0nX_{down}$: Set value of CM0n0 to CM0n2 while TM0n is counting down

The pin level when the TO0n0 to TO0n5 pins are reset is the high impedance state. When the control mode is selected thereafter, the following levels are output until the TM0n is started.

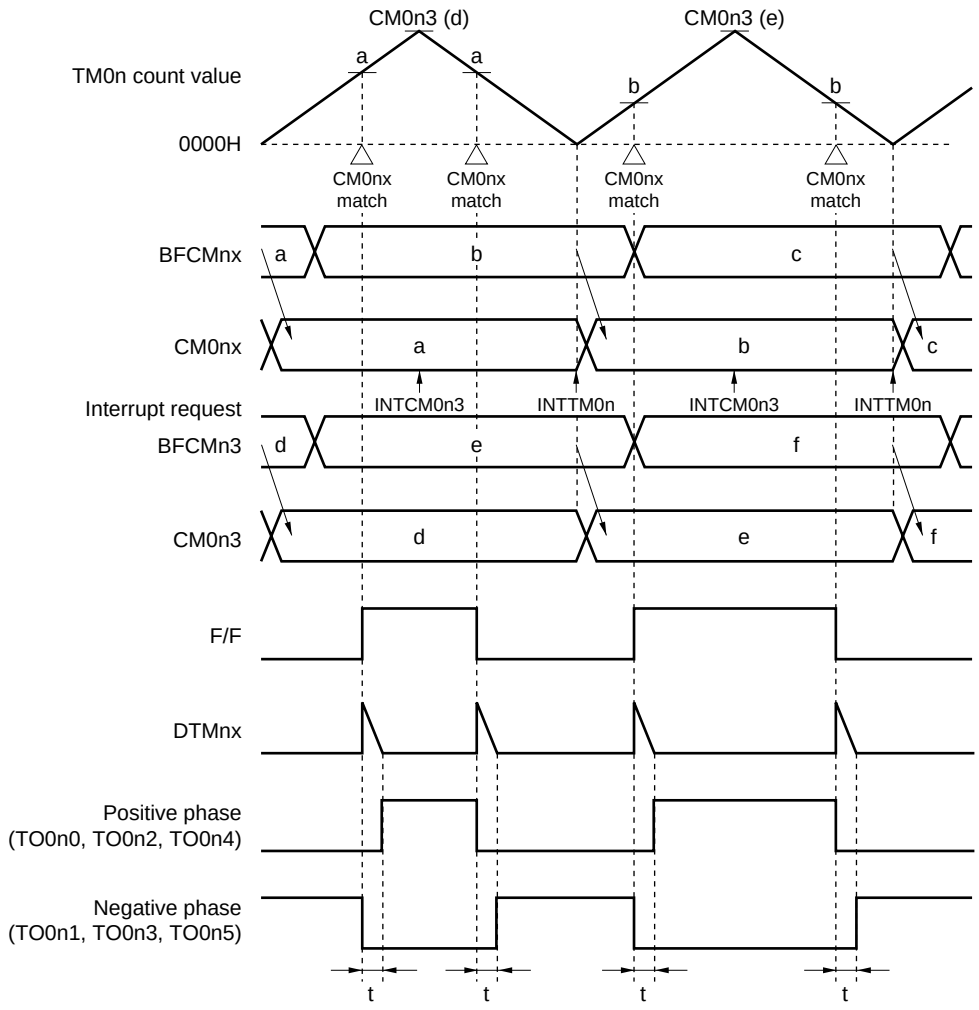
- TO0n0, TO0n2, TO0n4… When low active → High level
  When high active → Low level
- TO0n1, TO0n3, TO0n5… When low active → Low level
  When high active → High level

The active level is set with the ALVTO bit of the TOMRn register. The default is low active.

Caution If a value such that the positive phase or negative phase active width is "0" or a negative value in the above formula, the TO0n0 to TO0n5 pins output a waveform fixed to the inactive level waveform with active width "0".

Remark m = 0 to 2
n = 0, 1

Figure 9-17. Operation Timing in PWM Mode 0 (Symmetric Triangular Wave)



Remarks 1. The above figure shows the timing chart when BFTE3 of the TMC0n register is 1, and transfer from BFCMn3 to CM0n3 is enabled. Transfer is not performed when BFTE3 = 0.

2. n = 0, 1

3. x = 0 to 2

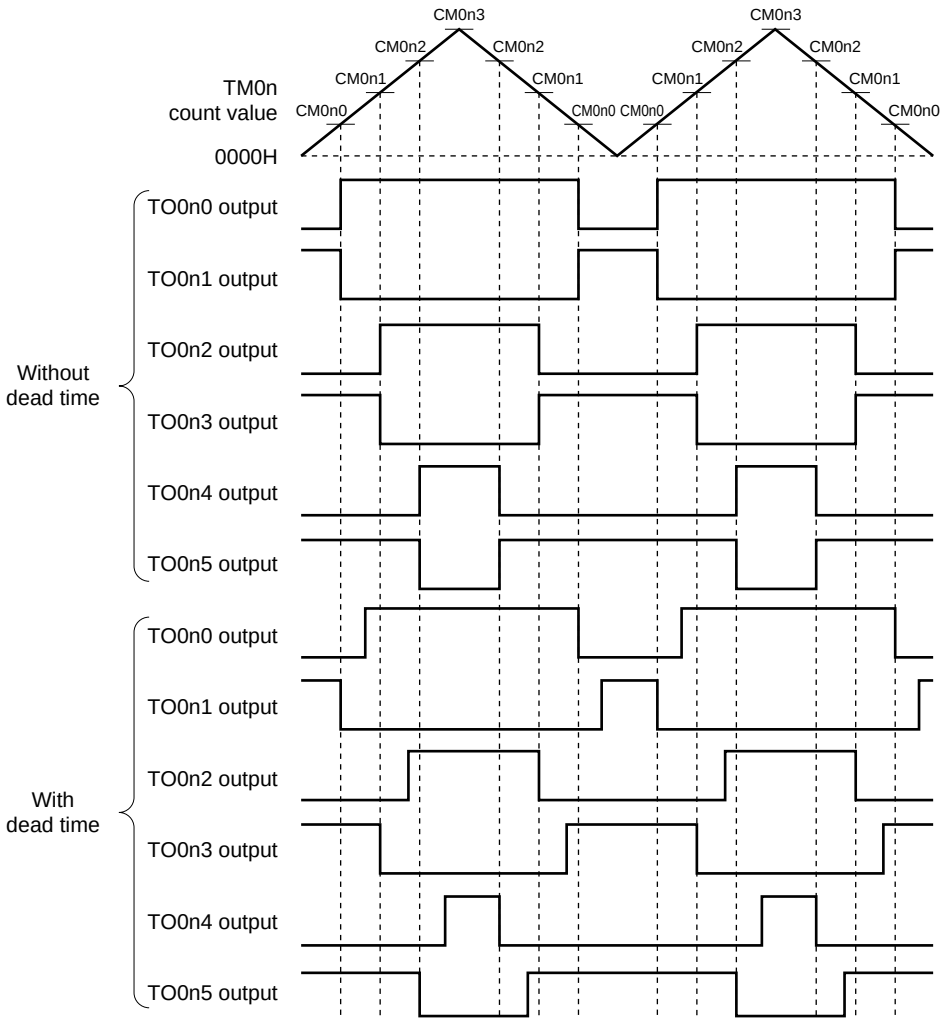
4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

5. To not use dead time, set the CED bit of the TMC0n register to 1.

6. The above figure shows an active high case.

Figure 9-18 shows the overall operation image.

Figure 9-18. Overall Operation Image of PWM Mode 0 (Symmetric Triangular Wave)

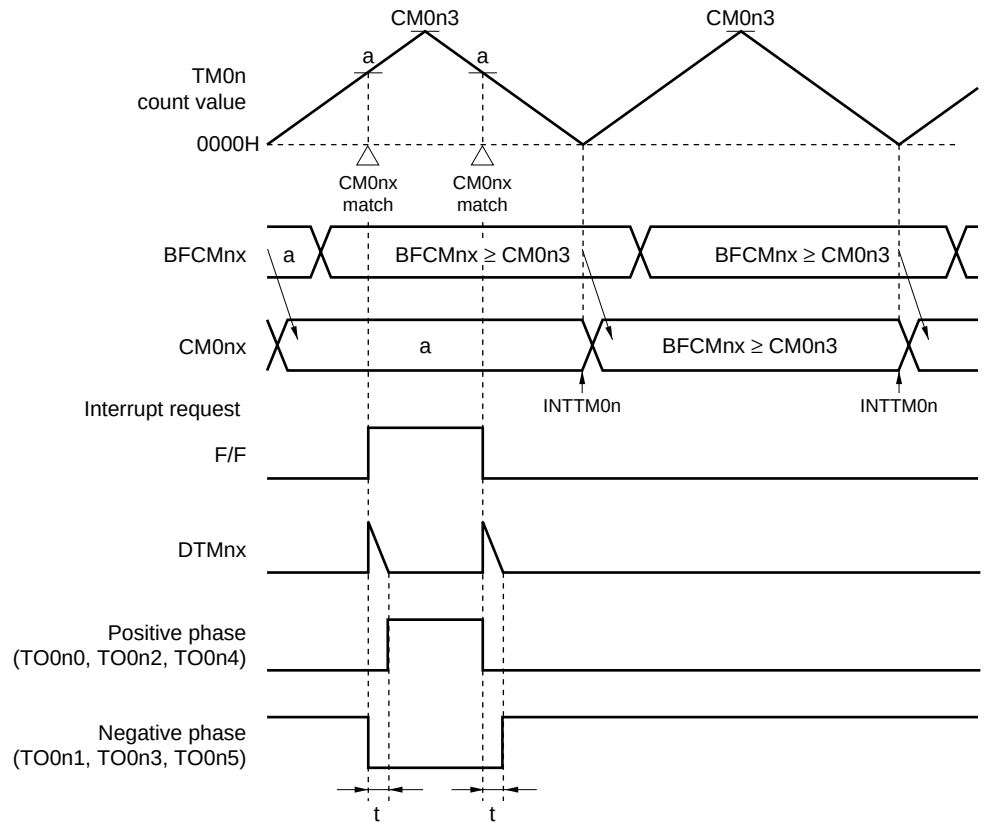


Remark n = 0, 1

Next, an example of the operation timing, which depends on the values set to CM0n0 to CM0n2 (BFCMn0 to BFCMn2) is shown.

(a) When CM0nx (BFCMnx) ≥ CM0n3 is set

Figure 9-19. Operation Timing in PWM Mode 0 (Symmetric Triangular Wave, BFCMnx ≥ CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

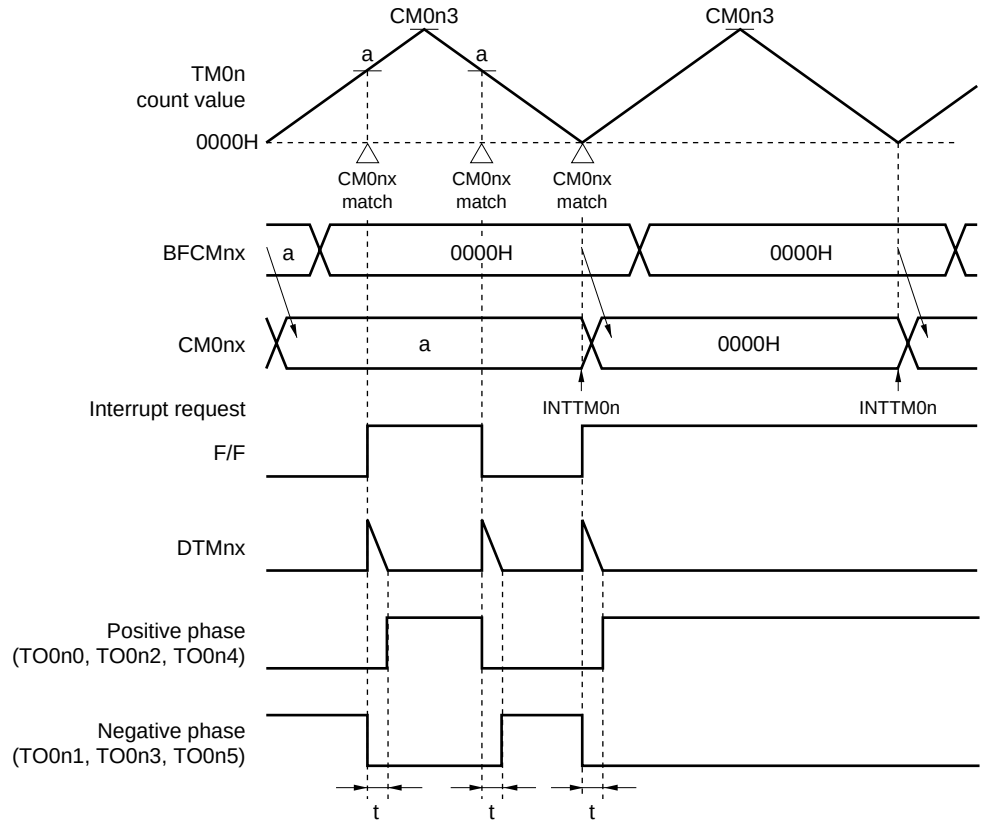
4. The above figure shows an active high case.

When a value greater than CM0n3 is set to BFCMnx, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a low level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a high level. This feature is effective for outputting a low-level or high-level width exceeding the PWM cycle in an application such as inverter control. Furthermore, if CM0nx = CM0n3 is set, matching of TM0n and CM0nx is detected during down counting by TM0n, so that the F/F remains reset as is, and does not get set.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

(b) When CM0nx (BFCMnx) = 0000H is set

Figure 9-20. Operation Timing in PWM Mode 0 (Symmetric Triangular Wave, BFCMnx = 0000H)



Remarks 1. n = 0, 1

2. x = 0 to 2

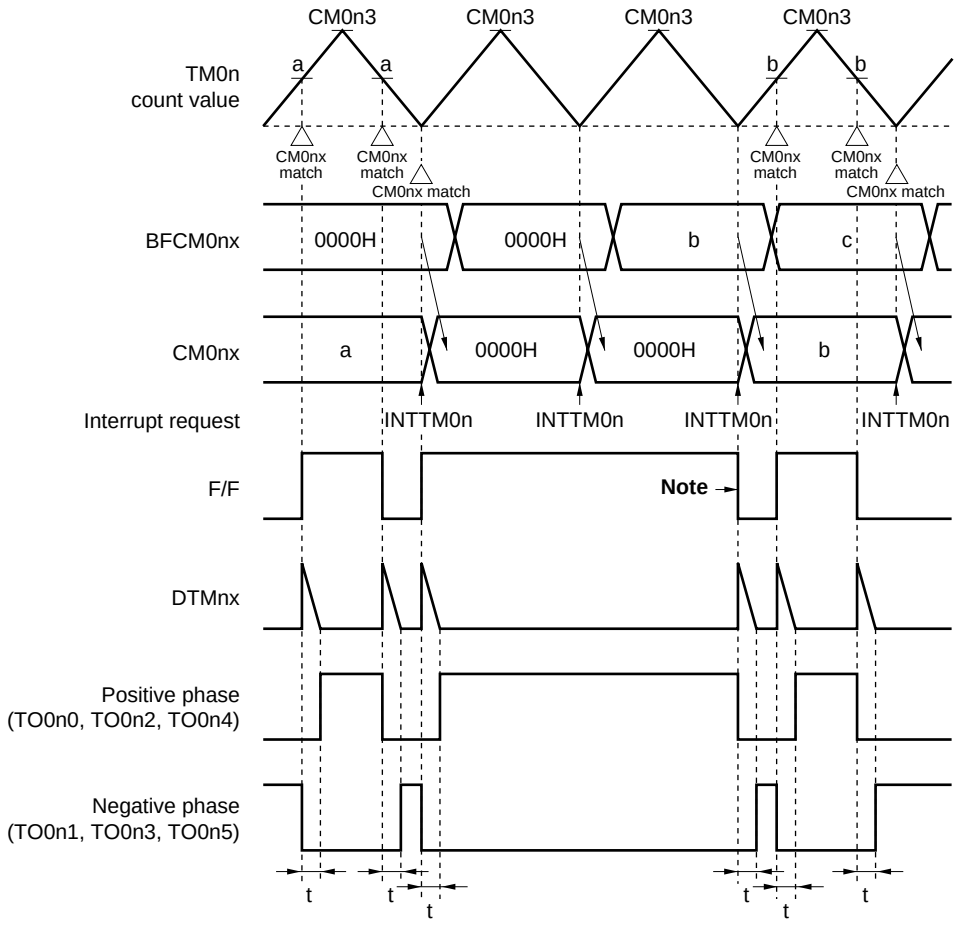
3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

4. The above figure shows an active high case.

Since TM0n = CM0nx = 0000H match is detected during up counting by TM0n, the F/F is just set and does not get reset. Even when the setting value is 0000H, F/F is changed in the cycle during which transfer is performed from BFCMnx to CM0nx similarly to when the setting value is other than 0000H.

Figure 9-21 shows the change timing from the 100% duty state.

Figure 9-21. Change Timing from 100% Duty State (PWM Mode 0)



Note F/F is reset upon INTTM0n occurrence.

Remarks 1. n = 0, 1

2. x = 0 to 2

3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

4. The above figure shows an active high case.

(3) PWM mode 1: Triangular wave modulation (right-left asymmetric waveform control)

[Setting procedure]

(a) Set PWM mode 1 (asymmetric triangular wave) with bits MOD01 and MOD00 of the TMC0n register. Also set the active level of pins TO0n0 to TO0n5 with the ALVTO bit of the TOMRn register (n = 0, 1).

(b) Set the count clock of TM0n with bits PRM02 to PRM00 of the TMC0n register. The transfer operation from BFCMn3 to CM0n3 is set with bit BFTE3, and the transfer operation from BFCMn0 to BFCMn2 to CM0n0 to CM0n2 is set with bit BFTEN.

(c) Set the initial values.

(i) Specify the interrupt culling ratio with bits CUL02 to CUL00 of the TMC0n register.

(ii) Set the half-cycle width of the first PWM cycle in BFCMn3.
- PWM cycle = BFCMn3 value $\times$ 2 $\times$ TM0n count clock
  (The TM0n count clock is set with the TMC0n register.)

(iii) Set the dead time width in DTRRn.
- Dead time width = (DTRRn + 1)/f_{CLK}
  f_{CLK}: Base clock

(iv) Set the set timing of the F/F used in the PWM cycle in BFCMn0 to BFCMn2.

(d) Clear (0) the CED bit of the TMC0n register to enable dead time timer operation. Set CED = 1 if you wish not to use dead time.

(e) Setting (1) the CE0 bit of the TMC0n register starts TM0n counting, and a 6-channel PWM signal is output from pins TO0n0 to TO0n5.

Caution Setting CM0n3 to 0000H is prohibited.

Remark The CE0 bit of the TMC0n register indicates transfer operation under the following conditions.
- When CE0 bit of TMC0n register is 0
  Transfer to the CM0n0 to CM0n2 registers is performed at the next base clock after write to registers BFCMn0 to BFCMn2.
- When CE0 bit of TMC0n register is 1
  The value of the BFCMn0 to BFCMn2 registers is transferred to the CM0n0 to CM0n2 registers upon occurrence of the INTTM0n or INTCM0n3 interrupt. Transfer enable/disable at this time is controlled by bit BFTEN of the TMC0n register.

[Operation]

In PWM mode 1, TM0n performs up/down count operation. When TM0n = 0000H during down counting, an underflow interrupt (INTTM0n) is generated, and when TM0n = CM0n3 during up counting, a match interrupt (INTCM0n3) is generated (n = 0, 1).

Switching from up counting to down counting is performed when TM0n and CM0n3 match (INTCM0n3), and switching from down counting to up counting is performed by INTTM0n.

The PWM cycle in this mode is (BFCMn3 value $\times$ 2 $\times$ TM0n count clock). Concerning setting of data to BFCMn3, the next PWM cycle width is set to BFCMn3.

The data of BFCMn3 is automatically transferred by hardware to CM0n3 upon generation of the INTTM0n interrupt. Furthermore, calculation is performed by software processing started by INTTM0n, and the data for the next cycle is set to BFCMn3.

Data setting to CM0n0 to CM0n2, which control the PWM duty, is explained next.

Setting of data to CM0n0 to CM0n2 consists in setting the duty output from BFCMn0 to BFCMn2.

The values of BFCMn0 to BFCMn2 are automatically transferred by hardware to CM0n0 to CM0n2 upon generation of the INTTM0n and INTCM0n3 (TM0n and CM0n3 match interrupts). Furthermore, software processing is started up and calculation performed, and the set/reset timing of the F/F after a half cycle is set in BFCMn0 to BFCMn2.

The PWM cycle and the PWM duty are set in the above procedure.

The F/F set/reset conditions upon match of CM0n0 to CM0n2 are as follows.

- Set: CM0n0 to CM0n2 match detection during TM0n up count operation
- Reset: CM0n0 to CM0n2 match detection during TM0n down count operation

The values of DTRRn are transferred to the corresponding dead time timers (DTMn0 to DTMn2) in synchronization with the set/reset timing of the F/F, and down counting is started. DTMn0 to DTMn2 count down to 000H, and stop when they count down further to FFFH.

DTMn0 to DTMn2 can automatically generate a width (dead time) at which the active levels of the positive phase (TO0n0, TO0n2, TO0n4) and negative phase (TO0n1, TO0n3, TO0n5) do not overlap.

In this way, software processing is started by two interrupts (INTTM0n and INTCM0n3) that occur during every PWM cycle after initial setting has been performed, and by setting the PWM cycle and PWM duty to be used after a half cycle, it is possible to automatically output a PWM waveform to TO0n0 to TO0n5 pins taking into consideration the dead time width (in case of interrupt culling ratio of 1/1).

The difference between right-left symmetric waveform control and control in this mode (right-left asymmetric waveform control) is that BFCMn0 to BFCMn2 are transferred to CM0n0 to CM0n2, and that the interrupt signals that start software processing consist just of INTTM0n (generated once per PWM cycle) in the case of right-left symmetric waveform control, and INTTM0n and INTCM0n3 (generated twice per PWM cycle, or once per half cycle) in the case of right-left asymmetric waveform control.

[Output waveform width in respect to set value]

- PWM cycle = $BFCMn3 \times 2 \times T_{TM0n}$
- Dead time width $T_{Dnm} = (DTRRn + 1)/f_{CLK}$
- Active width of positive phase (TO0n0, TO0n2, TO0n4 pins)
  $= \{ (CM0n3 - CM0nX_{up}) + (CM0n3 - CM0nX_{down}) \} \times T_{TM0n} - T_{Dnm}$
- Active width of negative phase (TO0n1, TO0n3, TO0n5 pins)
  $= (CM0nX_{down} + CM0nX_{up}) \times T_{TM0n} - T_{Dnm}$

f_{CLK}: Base clock
T_{TM0n}: TM0n count clock
$CM0nX_{up}$: Set value of CM0n0 to CM0n2 while TM0n is counting up
$CM0nX_{down}$: Set value of CM0n0 to CM0n2 while TM0n is counting down

The pin level when the TO0n0 to TO0n5 pins are reset is the high impedance state. When the control mode is selected thereafter, the following levels are output until the TM0n is started.

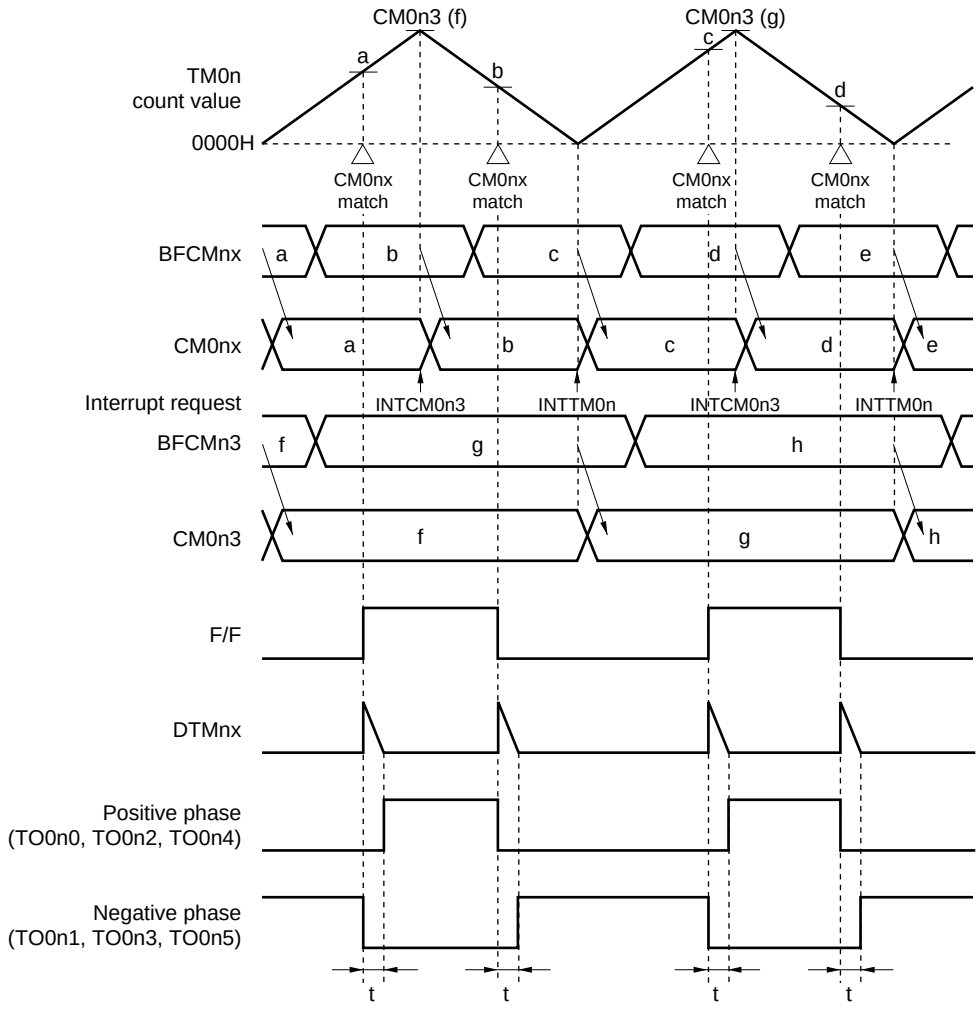
- TO0n0, TO0n2, TO0n4… When low active → High level
  When high active → Low level
- TO0n1, TO0n3, TO0n5… When low active → Low level
  When high active → High level

The active level is set with the ALVTO bit of the TOMRn register. The default is low active.

Caution If a value such that the positive phase or negative phase active width is "0" or a negative value in the above formula, the TO0n0 to TO0n5 pins output a waveform fixed to the inactive level waveform with active width "0".

Remark m = 0 to 2
n = 0, 1

Figure 9-22. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave)



Remarks 1. The above figure shows the timing chart when BFTE3 of the TMC0n register is 1, and transfer from BFCMn3 to CM0n3 is enabled. Transfer is not performed when BFTE3 = 0.

2. n = 0, 1

3. x = 0 to 2

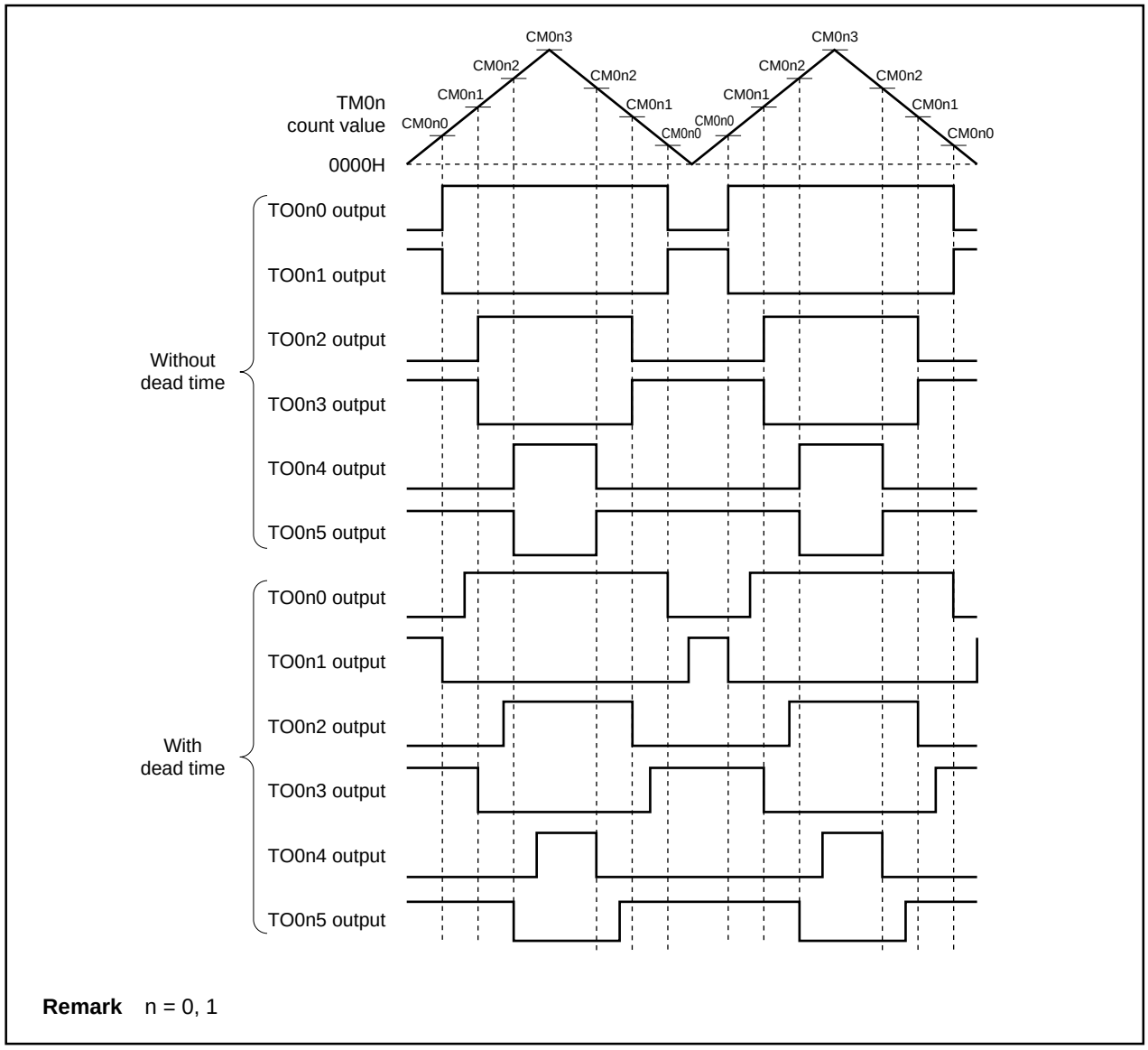
4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

5. To not use dead time, set the CED bit of the TMC0n register to 1.

6. The above figure shows an active high case.

Figure 9-23 shows the overall operation image.

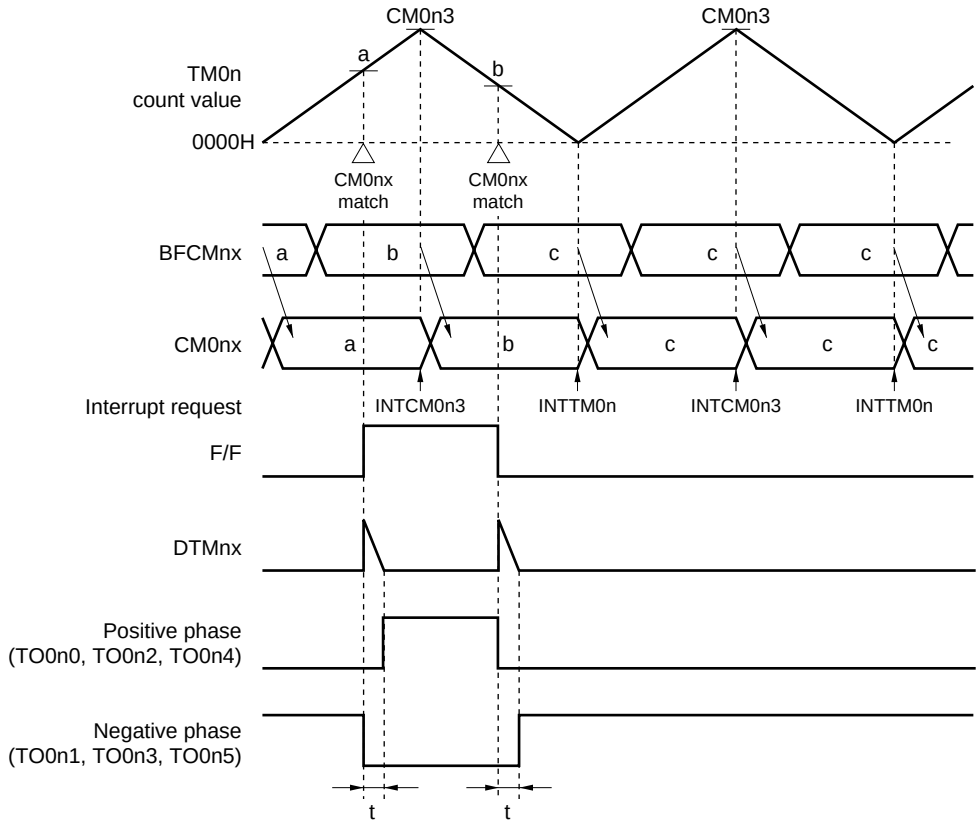
Figure 9-23. Overall Operation Image of PWM Mode 1 (Asymmetric Triangular Wave)



Remark n = 0, 1

(a) When BFCMnx ≥ CM0n3 is set in software processing started by INTCM0n3

Figure 9-24. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave, BFCMnx ≥ CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. c ≥ CM0n3

4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

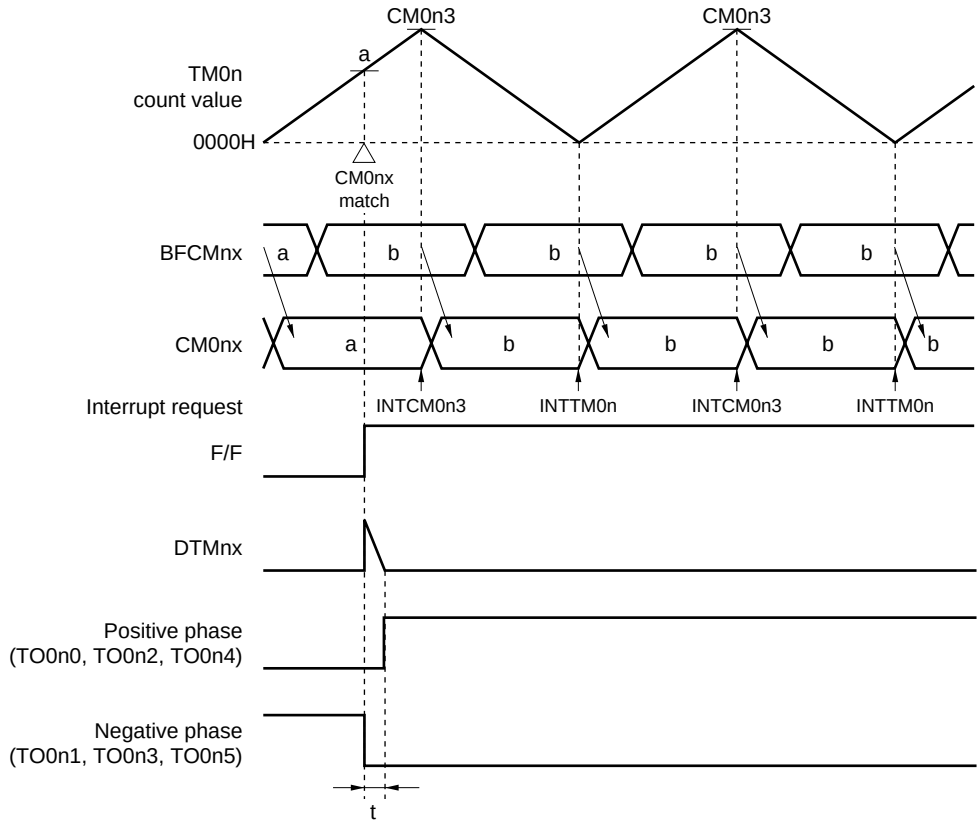
5. The above figure shows an active high case.

When a value greater than CM0n3 is set to BFCMnx, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a low level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a high level. This feature is effective for outputting a low-level or high-level width exceeding the PWM cycle in an application such as inverter control. Furthermore, if CM0nx = CM0n3 is set, matching of TM0n and CM0nx is detected during down counting by TM0n, so that the F/F remains reset as is, and does not get set.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

(b) When BFCMnx > CM0n3 is set in software processing started by INTTM0n

Figure 9-25. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave, BFCMnx > CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. b > CM0n3

4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

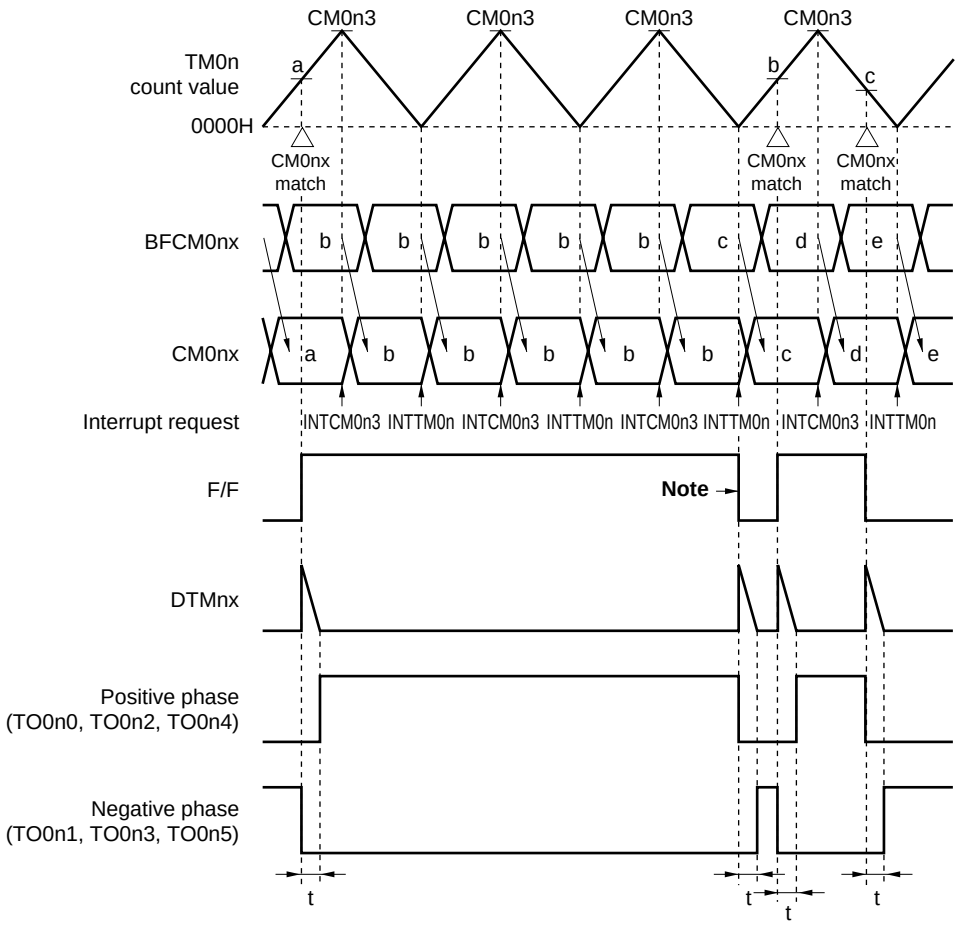
5. The above figure shows an active high case.

When a value greater than CM0n3 is set to BFCMnx, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a high level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a low level. This feature is effective for outputting a low-level or high-level width exceeding the PWM cycle in an application such as inverter control.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

Figure 9-26 shows the change timing from the 100% duty state.

Figure 9-26. Change Timing from 100% Duty State (PWM Mode 1)



Note F/F is reset upon INTTM0n occurrence.

Remarks 1. n = 0, 1

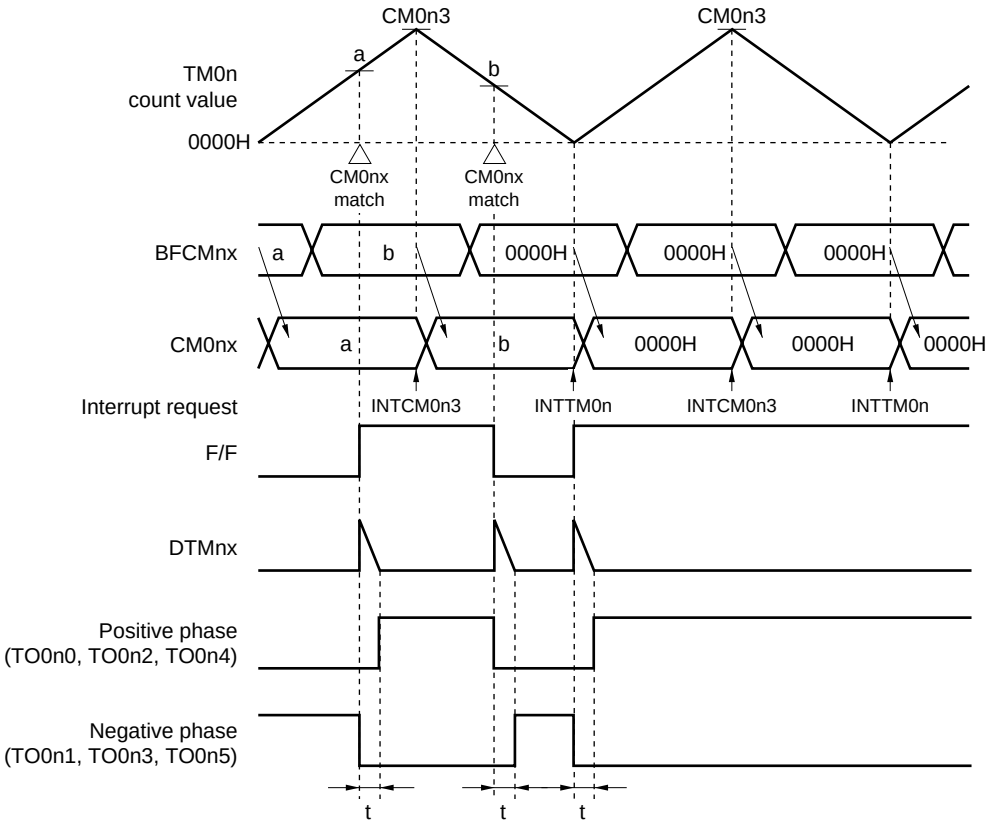
2. x = 0 to 2

3. b > CM0n3

4. The above figure shows an active high case.

(c) When BFCMnx = 0000H is set in software processing started by INTCM0n3

Figure 9-27. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave, BFCMnx = 0000H) (1)



Remarks 1. n = 0, 1

2. x = 0 to 2

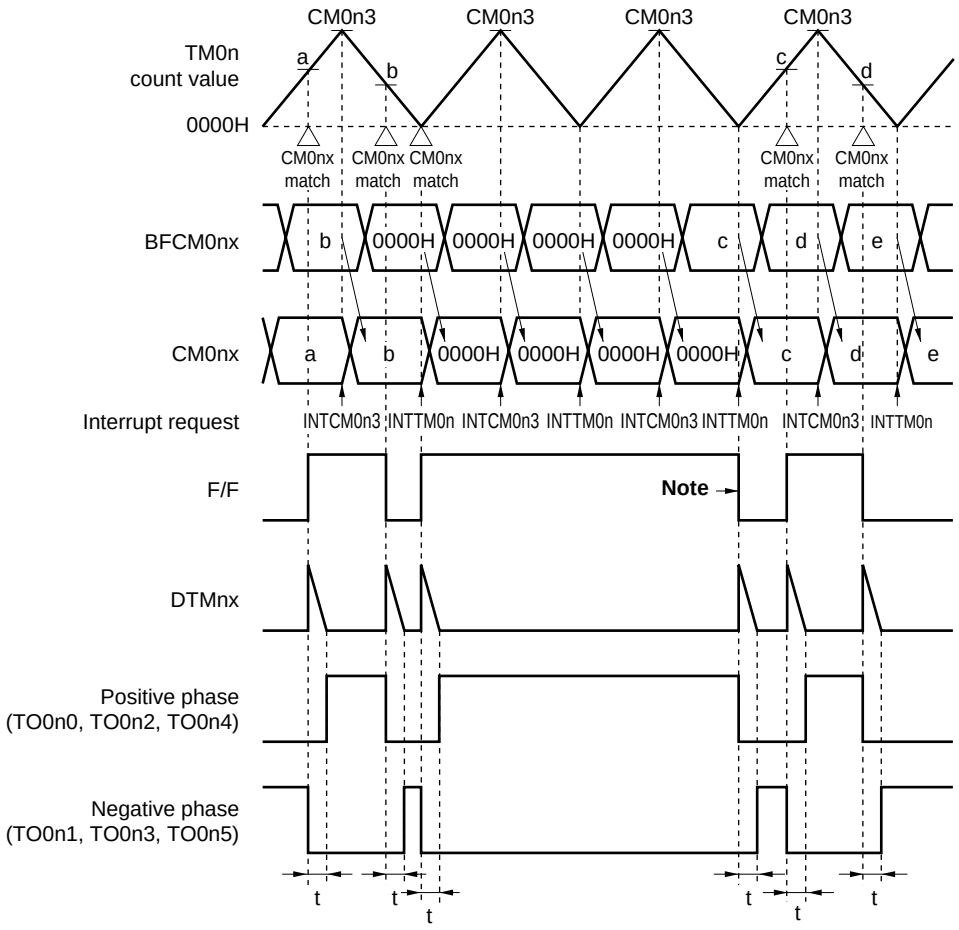
3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

4. The above figure shows an active high case.

Since TM0n = CM0nx = 0000H match is detected during up counting by TM0n, the F/F is just set and does not get reset. Moreover, the F/F gets set upon match detection in the cycle when 0000H is transferred to CM0nx by INTTM0n interrupt.

Figure 9-28 shows the change timing from the 100% duty state.

Figure 9-28. Change Timing from 100% Duty State (1) (PWM Mode 1)



Note F/F is reset upon INTTM0n occurrence.

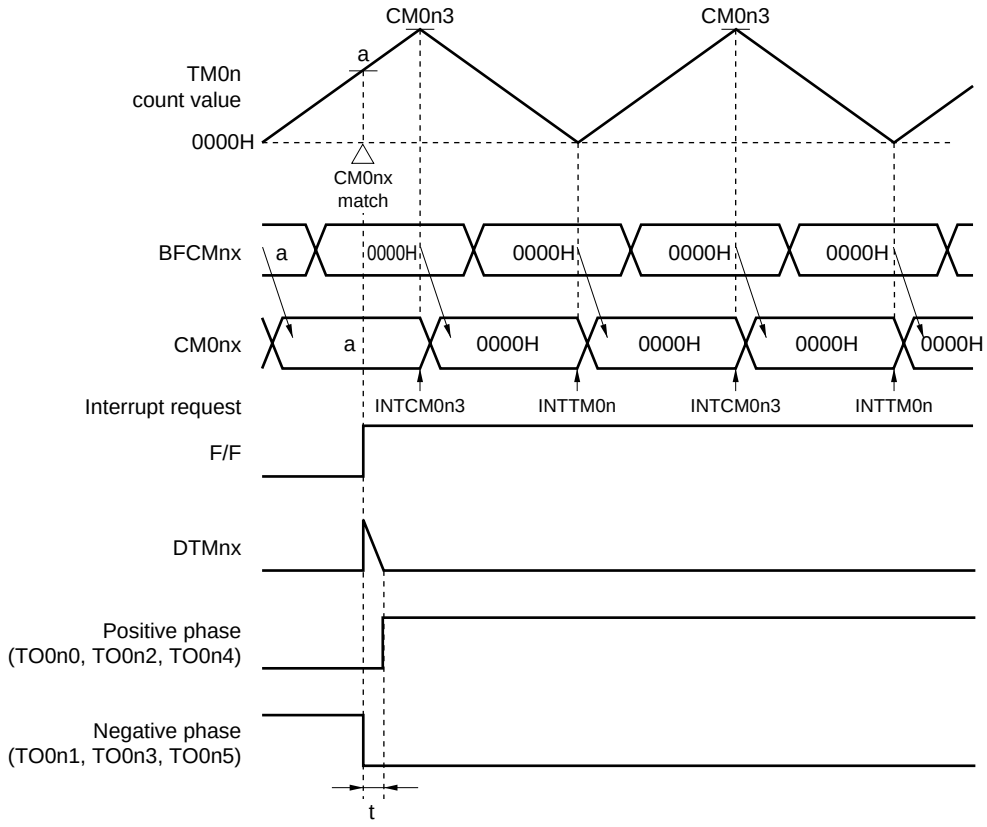
Remarks 1. n = 0, 1

2. x = 0 to 2

3. The above figure shows an active high case.

(d) When BFCMnx = 0000H is set in software processing started by INTTM0n

Figure 9-29. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave, BFCMnx = 0000H) (2)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

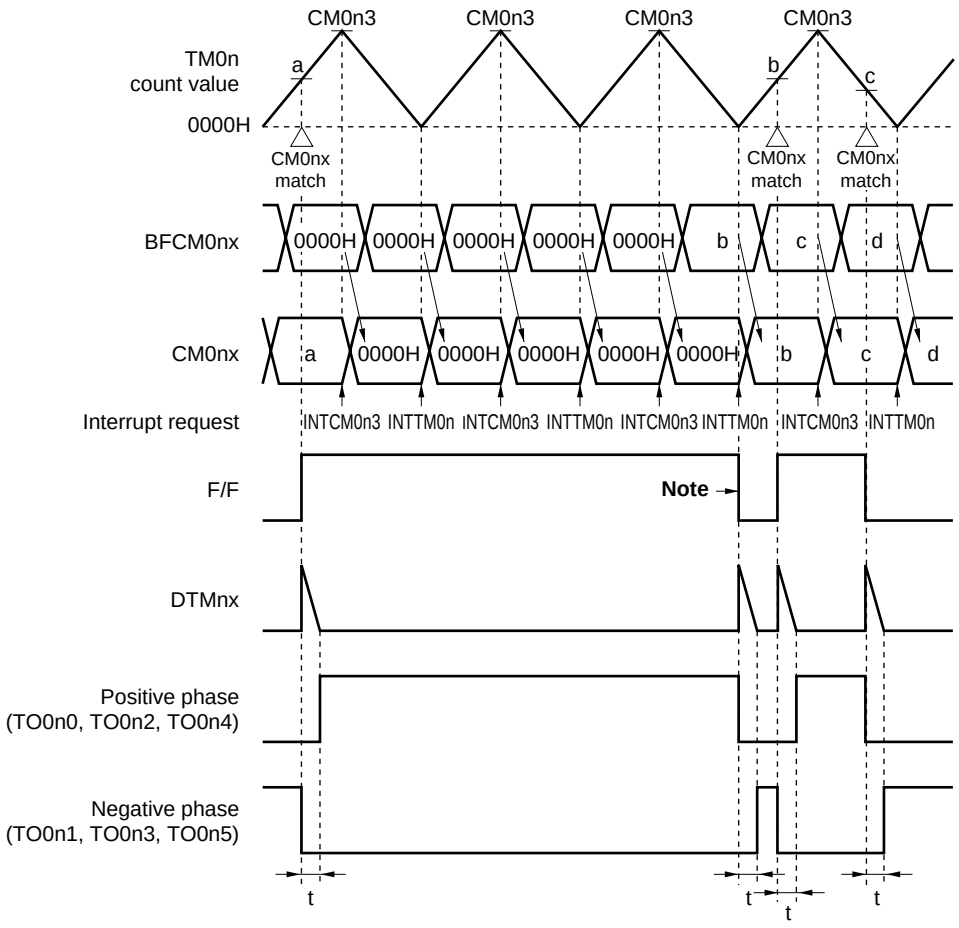
4. The above figure shows an active high case.

Since TM0n = CM0nx = 0000H match is detected during up counting by TM0n, the F/F is just set and does not get reset. Therefore, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a high level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a low level.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

Figure 9-30 shows the change timing from the 100% duty state.

Figure 9-30. Change Timing from 100% Duty State (2) (PWM Mode 1)



Note F/F is reset upon INTTM0n occurrence.

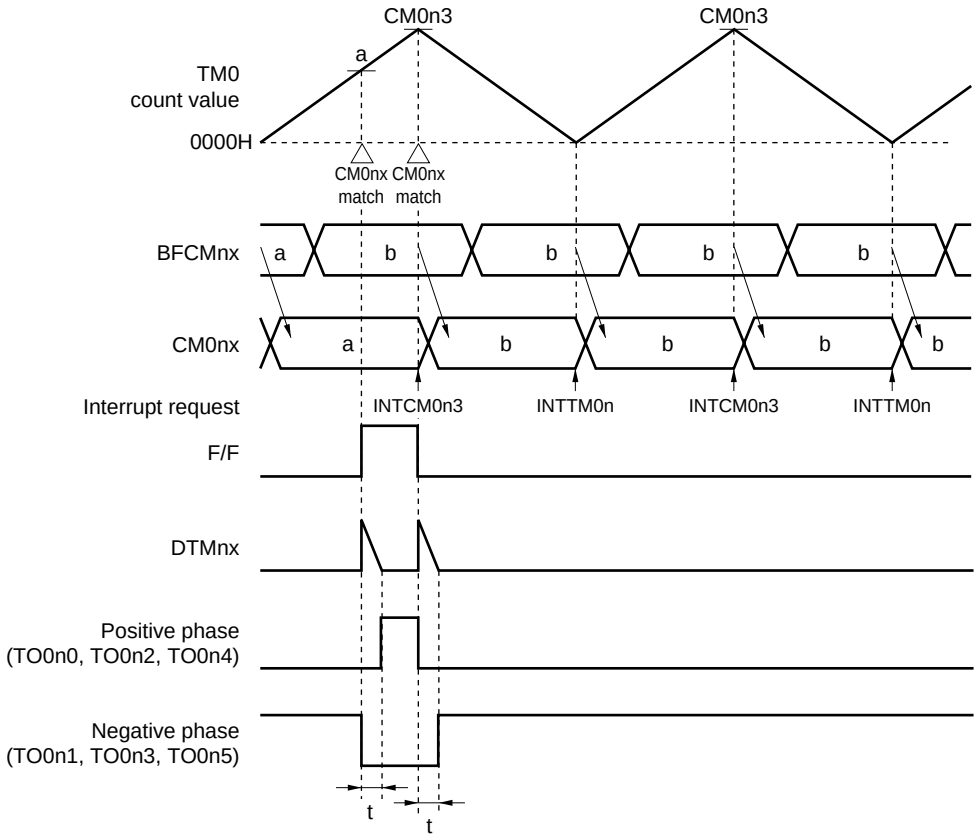
Remarks 1. n = 0, 1

2. x = 0 to 2

3. The above figure shows an active high case.

(e) When BFCMnx = CM0n3 is set in software processing started by INTTM0n

Figure 9-31. Operation Timing in PWM Mode 1 (Asymmetric Triangular Wave, BFCMnx = CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. b = CM0n3

4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

5. The above figure shows an active high case.

Since TM0n and CM0nx match is detected during count down of TM0n when BFCMnx = CM0n3 has been set, the F/F remains reset as is and does not get set. Therefore, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a high level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a low level. Moreover, the timing of matching with TM0n with CM0nx = CM0n3 is the cycle when transfer is performed from BFCMnx to CM0nx by INTCM0n3.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

(4) PWM mode 2: Sawtooth wave modulation

[Setting procedure]

(a) Set PWM mode 2 (sawtooth wave) with bits MOD01 and MOD00 of the TMC0n register. Also set the active level of pins TO0n0 to TO0n5 with the ALVTO bit of the TOMRn register.

(b) Set the count clock of TM0n with bits PRM02 to PRM00 of the TMC0n register. The transfer operation from BFCMn3 to CM0n3 is set with bit BFTE3, and the transfer operation from BFCMn0 to BFCMn2 to CM0n0 to CM0n2 is set with bit BFTEN.

(c) Set the initial values.

(i) Specify the interrupt culling ratio with bits CUL02 to CUL00 of the TMC0n register.

(ii) Set the half-cycle width of the PWM cycle in BFCMn3.
- PWM cycle = BFCMn3 value $\times$ 2 $\times$ TM0n count clock
  (The TM0n count clock is set with the TMC0n register.)

(iii) Set the dead time width in DTRRn.
- Dead time width = (DTRRn + 1)/f_{CLK}
  f_{CLK}: Base clock

(iv) Set the set/reset timing of the F/F used in the second cycle in BFCM0n0 to BFCM0n2.

(d) Clear (0) the CED bit of the TMC0n register to enable dead time timer operation. Set CED = 1 if you wish not to use dead time.

(e) Setting (1) the CE0 bit of the TMC0n register starts TM0n counting, and a 6-channel PWM signal is output from pins TO0n0 to TO0n5.

Caution Setting CM0n3 to 0000H is prohibited.

[Operation]

In PWM mode 2, TM0n performs up count operation, and when it matches the value of CM0n3, match interrupt INTCM0n3 is generated and TM0n is cleared (n = 0, 1).

The PWM cycle in this mode is ((BFCMn3 value + 1) × TM0n count clock). Concerning setting of data to CM0n3, the next PWM cycle width is set to BFCMn3.

The data of BFCMn3 is automatically transferred by hardware to CM0n3 upon generation of the INTCM0n3 interrupt. Furthermore, calculation is performed by software processing started by INTCM0n3, and the data for the next cycle is set to BFCMn3.

Data setting to CM0n0 to CM0n2, which control the PWM duty, is explained next.

Setting of data to CM0n0 to CM0n2 consists in setting the duty output from BFCMn0 to BFCMn2.

The values of BFCMn0 to BFCMn2 are automatically transferred by hardware to CM0n0 to CM0n2 upon generation of the INTCM0n3 interrupt. Furthermore, software processing is started up and calculation performed, and reset timing of the F/F for the next cycle is set to BFCMn0 to BFCMn2.

The PWM cycle and the PWM duty are set in the above procedure.

The F/F set/reset conditions upon match of CM0n0 to CM0n2 are as follows.

- Set: TM0n and CM0n3 match detection and rising edge of CE0 bit of TMC0n register
- Reset: TM0n and CM0n0 to CM0n2 match detection

The values of DTRRn are transferred to the corresponding dead time timers (DTMn0 to DTMn2) in synchronization with the set/reset timing of the F/F, and down counting is started. DTMn0 to DTMn2 count down to 000H, and stop when they count down further to FFFH.

DTMn0 to DTMn2 can automatically generate a width (dead time) at which the active levels of the positive phase (TO0n0, TO0n2, TO0n4) and negative phase (TO0n1, TO0n3, TO0n5) do not overlap.

In this way, software processing is started by an interrupt (INTCM0n3) that occurs once during every PWM cycle after initial setting has been performed, and by setting the PWM cycle and PWM duty to be used in the next cycle, it is possible to automatically output a PWM waveform to TO0n0 to TO0n5 pins taking into consideration the dead time width (in case of interrupt culling ratio of 1/1).

[Output waveform width in respect to set value]

- PWM cycle = (BFCMn3 + 1) × T_{TM0n}
- Dead time width T_{Dnm} = (DTRRn + 1)/f_{CLK}
- Active width of positive phase (TO0n0, TO0n2, TO0n4 pins)
  = (CM0nX + 1) × T_{TM0n} – T_{Dnm}
- Active width of negative phase (TO0n1, TO0n3, TO0n5 pins)
  = (CM0n3 – CM0nX) × T_{TM0n} – T_{Dnm}

f_{CLK}: Base clock
T_{TM0n}: TM0n count clock
CM0nX: Set value of CM0n0 to CM0n2

The pin level when the TO0n0 to TO0n5 pins are reset is the high impedance state. When the control mode is selected thereafter, the following levels are output until the TM0n is started.

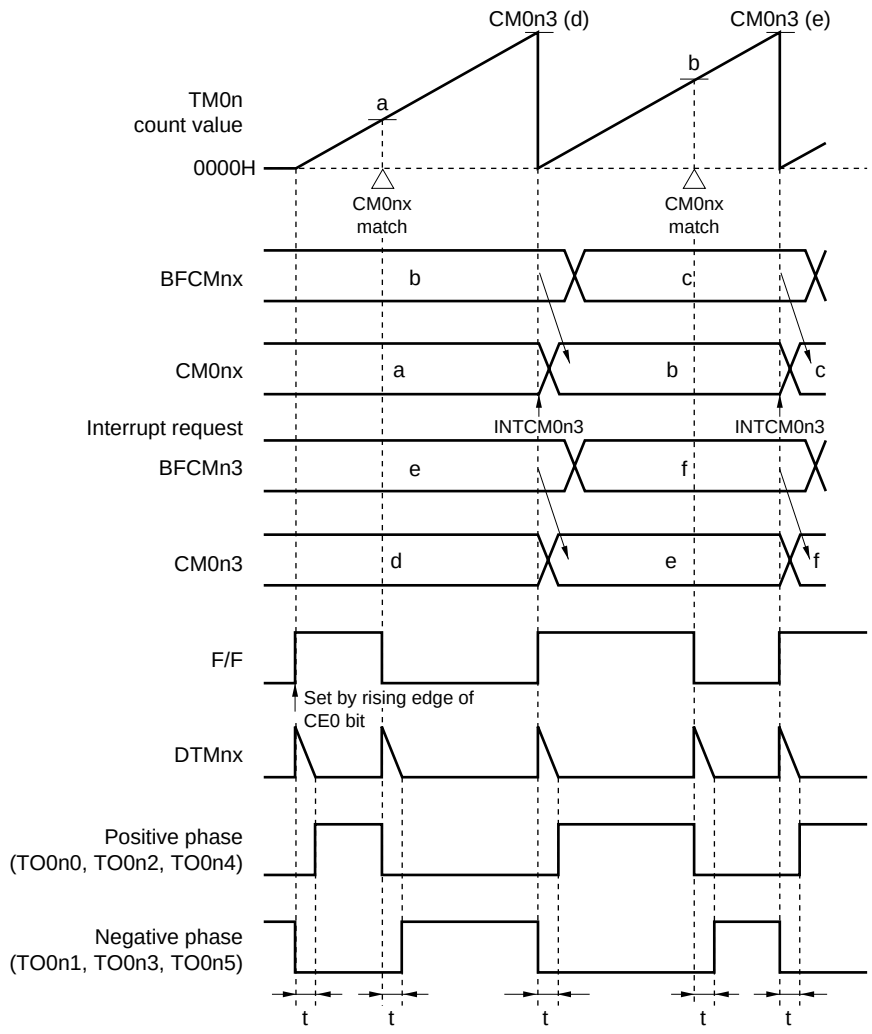
- TO0n0, TO0n2, TO0n4… When low active → High level
  When high active → Low level
- TO0n1, TO0n3, TO0n5… When low active → Low level
  When high active → High level

The active level is set with the ALVTO bit of the TOMRn register. The default is low active.

Caution If a value such that the positive phase or negative phase active width is "0" or a negative value in the above formula, the TO0n0 to TO0n5 pins output a waveform fixed to the inactive level waveform with active width "0".

Remark m = 0 to 2
n = 0, 1

Figure 9-32. Operation Timing in PWM Mode 2 (Sawtooth Wave)



Remarks 1. n = 0, 1

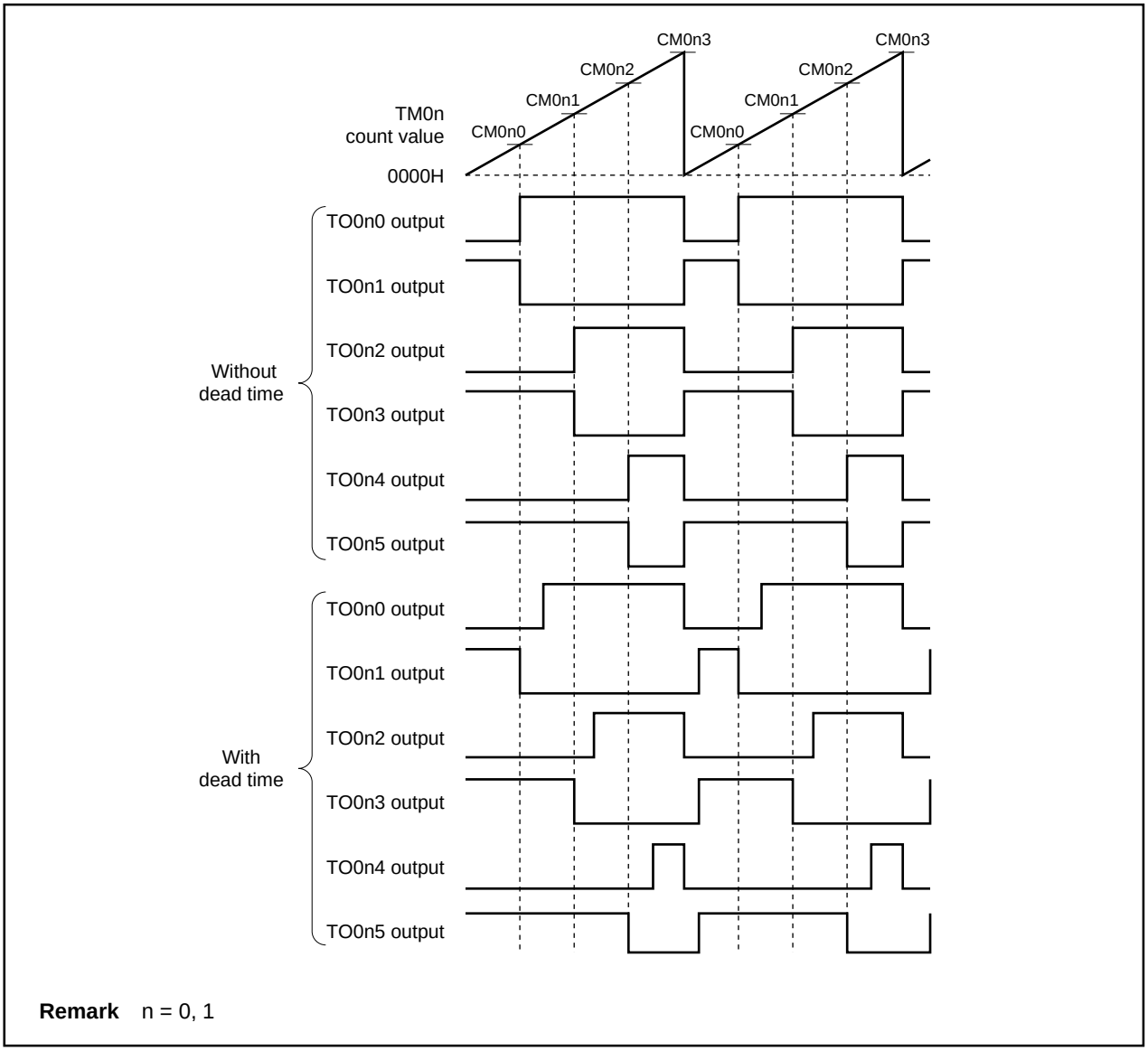
2. x = 0 to 2

3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

4. The above figure shows an active high case.

Figure 9-33 shows the overall operation image.

Figure 9-33. Overall Operation Image of PWM Mode 2 (Sawtooth Wave)

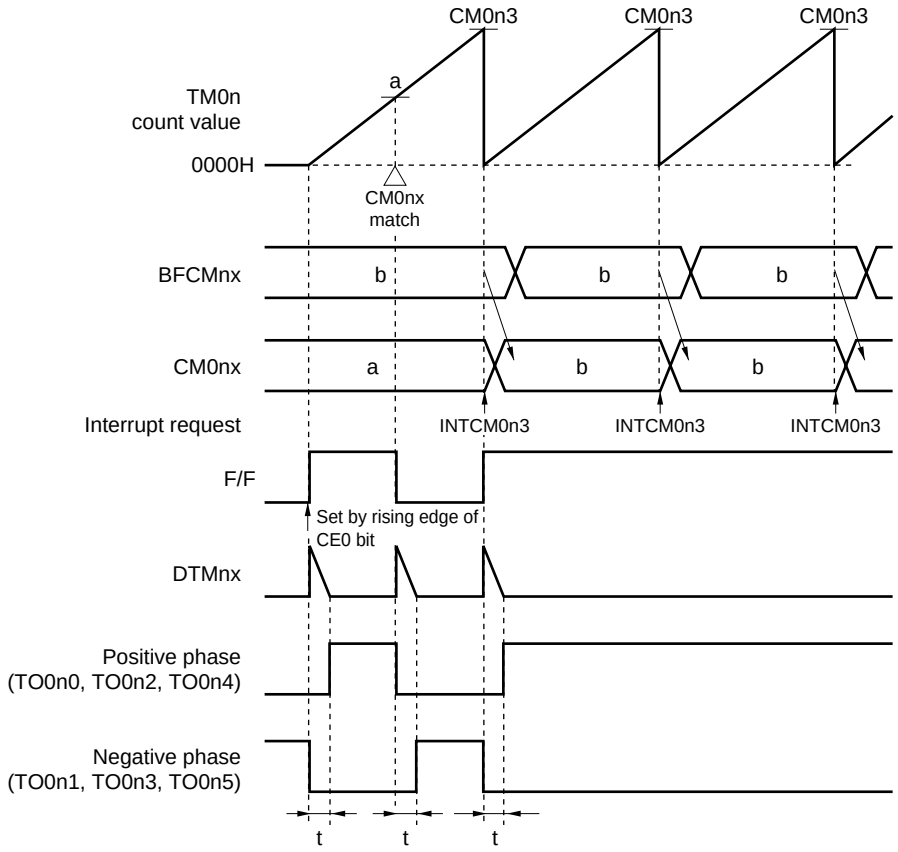


Remark n = 0, 1

Since the F/F is set at the rising edge of the CE0 bit of the TMC0n register in the first cycle, the PWM signal can be output.

(a) When BFCMnx > CM0n3 is set

Figure 9-34. Operation Timing in PWM Mode 2 (Sawtooth Wave, BFCMnx > CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. b > CM0n3

4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

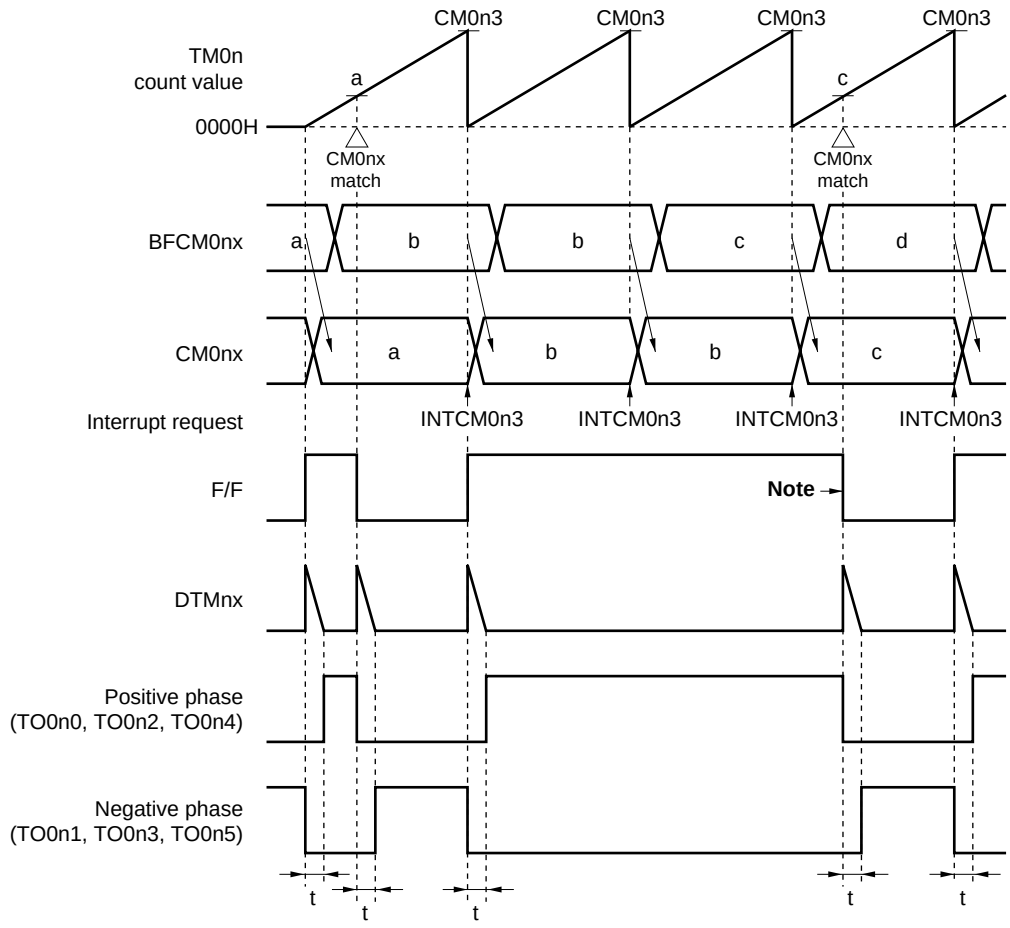
5. The above figure shows an active high case.

When a value greater than CM0n3 is set to BFCMnx, the positive phase side (TO0n0, TO0n2, TO0n4 pins) outputs a high level, and the negative phase side (TO0n1, TO0n3, TO0n5 pins) continues to output a low level. Since TM0n and CM0nx match does not occur, the F/F does not get reset. This feature is effective for outputting a low-level or high-level width exceeding the PWM cycle in an application such as inverter control.

The above explanation applies to an active high case. In an active low case, the levels of positive and negative phases are merely inverted and other operations remain the same.

Figure 9-35 shows the change timing from the 100% duty state.

Figure 9-35. Change Timing from 100% Duty State (PWM Mode 2)



Note F/F is reset upon occurrence match with CM0nx.

Remarks 1. n = 0, 1

2. x = 0 to 2

3. b > CM0n3

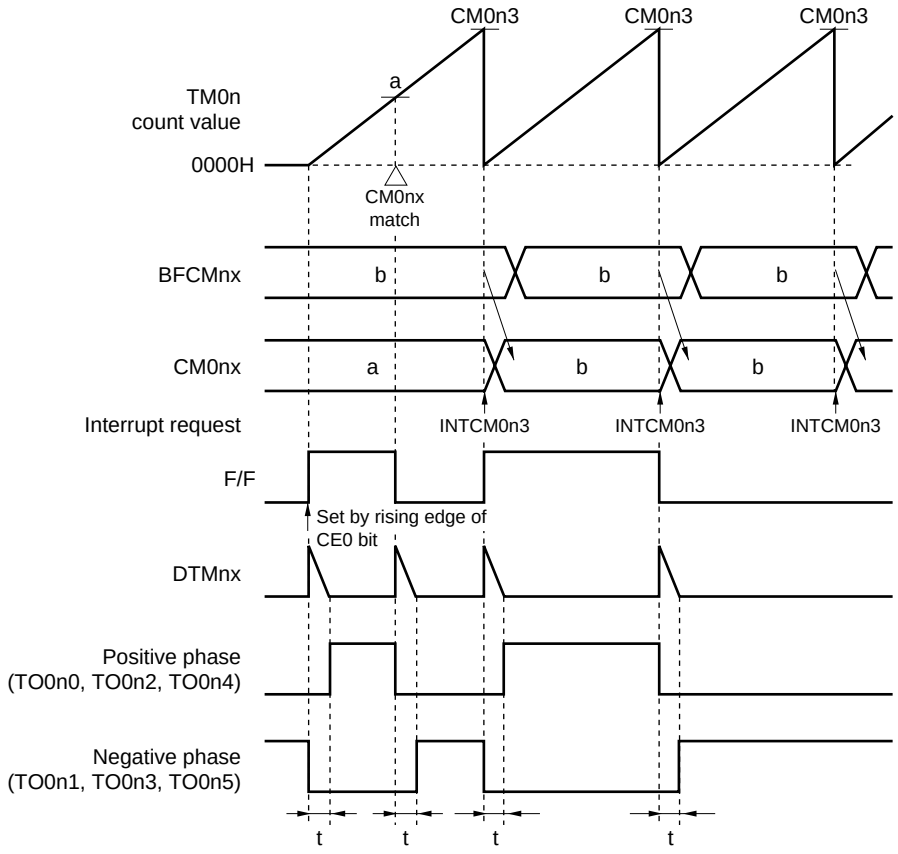
4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

5. The above figure shows an active high case.

The timing at which the F/F is reset is upon occurrence of match with CM0nx as normal.

(b) When BFCMnx = CM0n3 is set

Figure 9-36. Operation Timing in PWM Mode 2 (Sawtooth Wave, BFCMnx = CM0n3)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. b = CM0n3

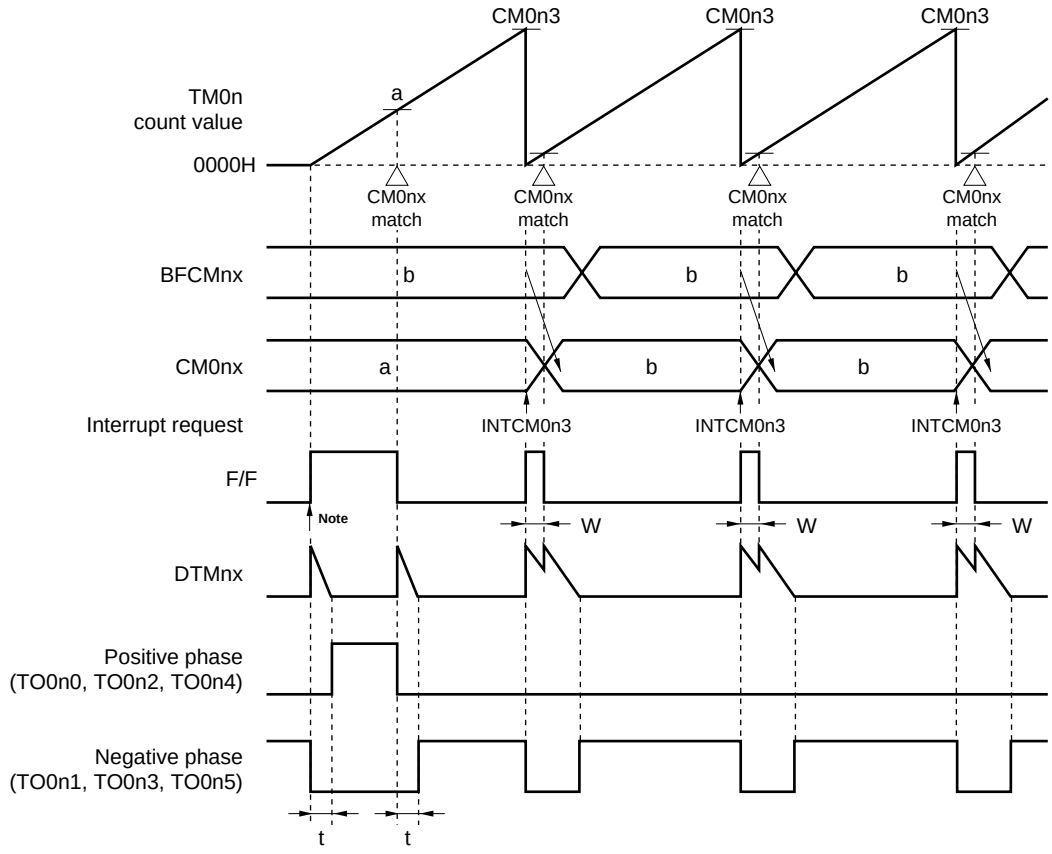
4. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

5. The above figure shows an active high case.

If match signal INTCM0n3 for TM0n and CM0n3 and the match signal for TM0n and CM0nx conflict, reset of the F/F takes precedence, so that the F/F does not get set following match of CM0nx (= CM0n3) with TM0n.

(c) When BFCMnx = 0000H is set

Figure 9-37. Operation Timing in PWM Mode 2 (Sawtooth Wave, BFCMnx = 0000H)



Remarks 1. n = 0, 1

2. x = 0 to 2

3. t: Dead time = (DTRRn + 1)/f_{CLK} (f_{CLK}: Base clock)

4. The above figure shows an active high case.

5. W: Width between CM0n3 match and CM0nx match (timer count clock)

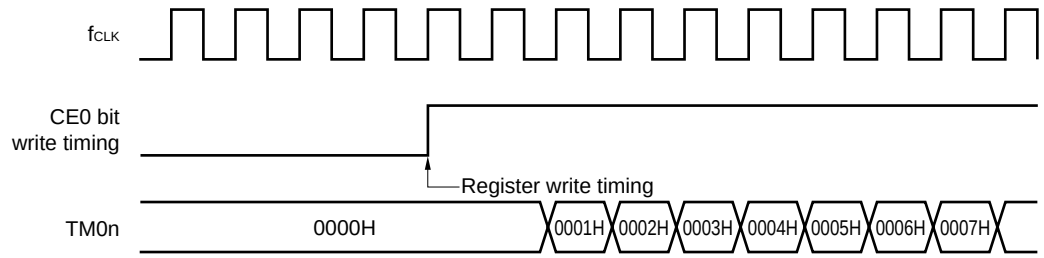
If CM0nx = 0000H has been set, the output waveform resulting from the TM0n count clock rate and the DTRRn set value differ.

9.1.6 Operation timing

(1) CE0 bit write and TM0n timer operation timing

Figure 9-38 shows the timing from write of the CE0 bit of the TMC0n register until the TM0n timer starts operating.

Figure 9-38. CE0 Bit Write and TM0n Timer Operation Timing



Caution The operation of TM0n starts $2f_{CLK}$ after the register write timing.

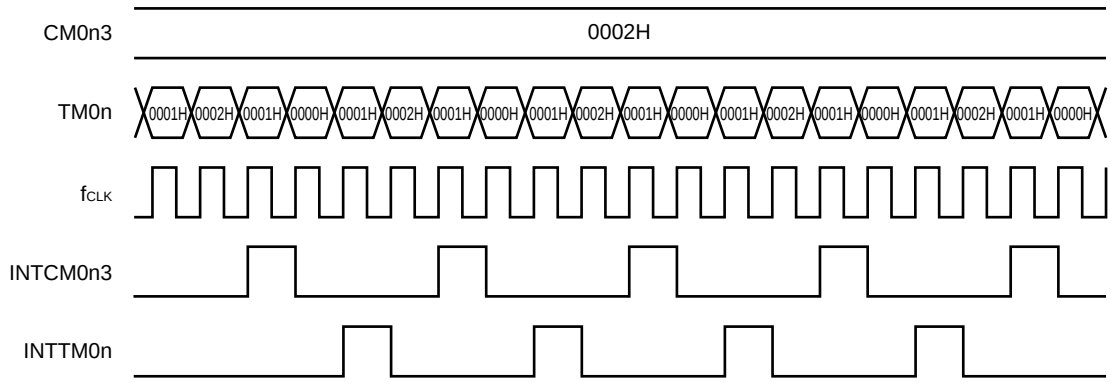
Remark f_{CLK}: Base clock

(2) Interrupt generation timing

The interrupt generation timing with the count clock setting (PRM02 to PRM00 bits of the TMC0n register) to TM0n in the various modes is described below.

Figure 9-39. Interrupt Generation Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave) (1/2)

(a) Count clock = f_{CLK}



Cautions 1. INTCM0n3 is generated at the next count clock of TM0n after detection of TM0n and CM0n3 match.

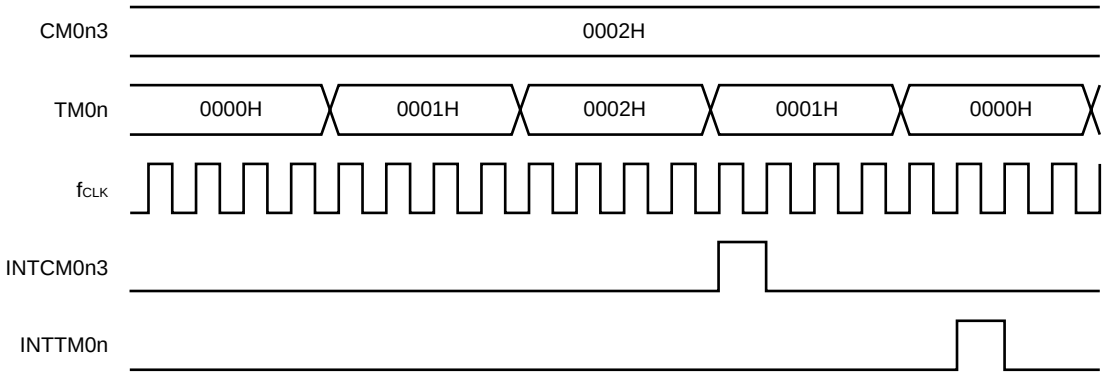
2. INTTM0n is generated at the next f_{CLK} after detection of TM0n and 0000H match.

Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-39. Interrupt Generation Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave) (2/2)

(b) Count clock = $f_{CLK}/4$



Cautions 1. INTCM0n3 is generated at the next count clock of TM0n after detection of TM0n and CM0n3 match.

2. INTTM0n is generated at the next f_{CLK} after detection of TM0n and 0000H match.

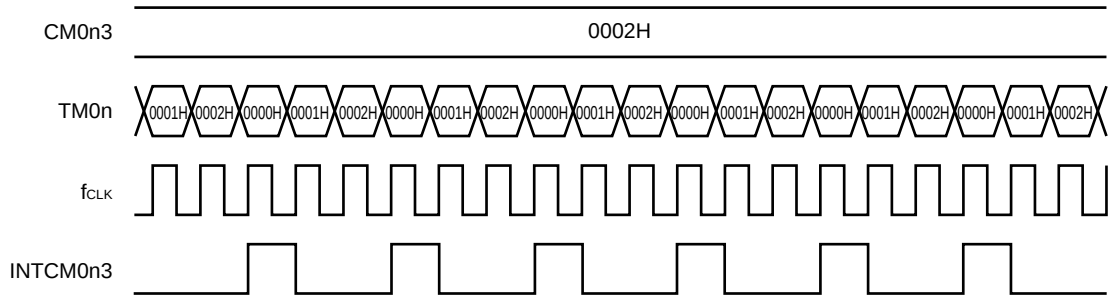
3. INTTM0n is generated at the next f_{CLK} after detection of TM0n and 0000H match, even if the count clock is 1/2, 1/8, 1/16, or 1/32.

Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-40. Interrupt Generation Timing in PWM Mode 2 (Sawtooth Wave)

(a) Count clock = f_{CLK}

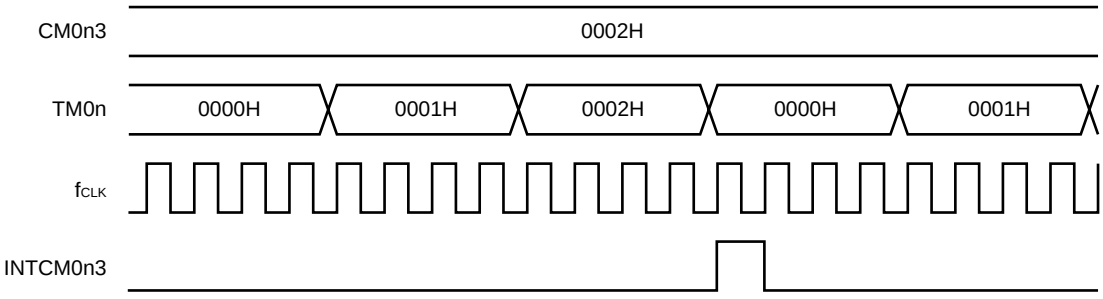


Caution INTCM0n3 is generated at the next count clock of TM0n after detection of TM0n and CM0n3 match.

Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

(b) Count clock = $f_{CLK}/4$



Cautions 1. INTCM0n3 is generated at the next count clock of TM0n after detection of TM0n and CM0n3 match.

2. INTCM0n3 is generated at the next count clock of TM0n after detection of TM0n and CM0n3 match even if the count clock is 1/2, 1/8, 1/16, or 1/32.

Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

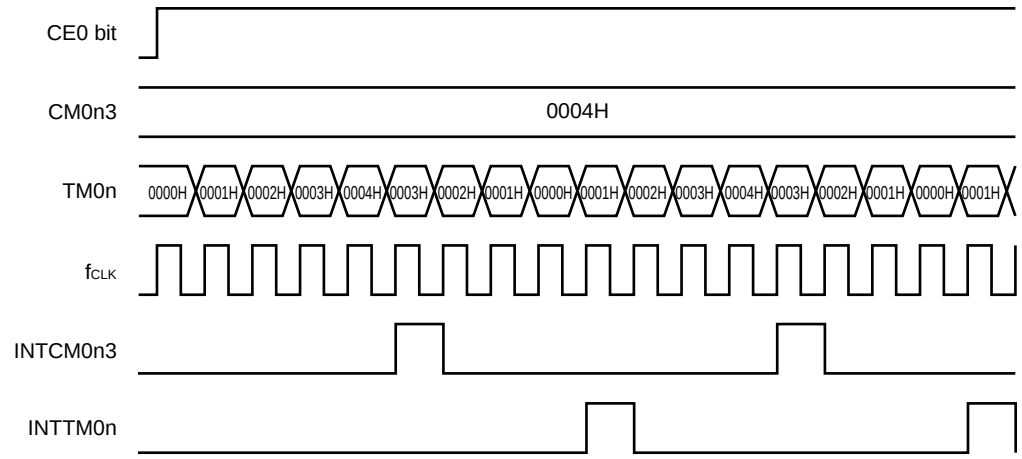
(3) Relationship between interrupt generation and STINT bit of TMC0n register

The interrupt generation timing for the setting of the STINT bit of the TMC0n register and the interrupt culling ratio setting (bits CUL02 to CUL00) in the various modes is described below.

If, to realize the INTTM0n and INTCM0n3 interrupt culling function for TM0n, bits CUL02 to CUL00 of the TMC0n register are set for a culling ratio other than 1/1, and count operation is started, the interrupt output order differs according to the setting of the STINT bit when counting starts.

Figure 9-41. Interrupt Generation Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave): In case of Interrupt Culling Ratio of 1/1 (1/2)

(a) When STINT bit = 0

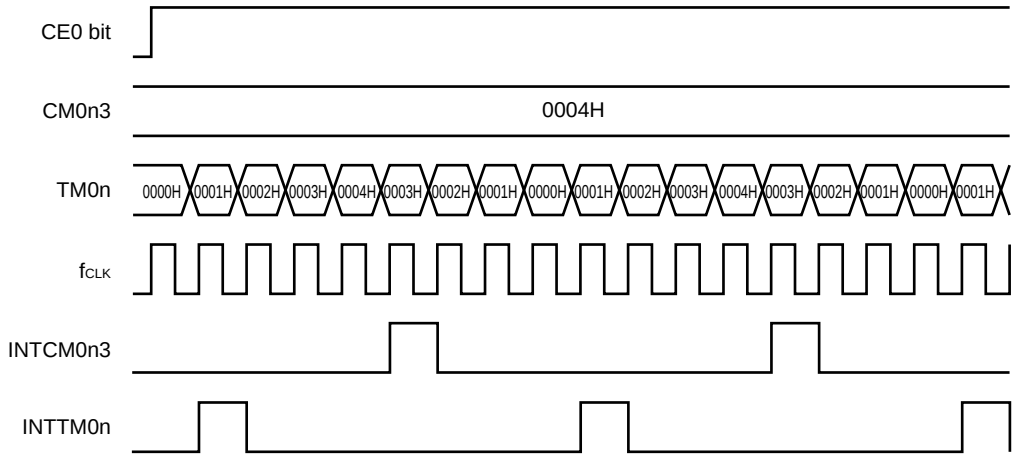


Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-41. Interrupt Generation Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave): In case of Interrupt Culling Ratio of 1/1 (2/2)

(b) When STINT bit = 1

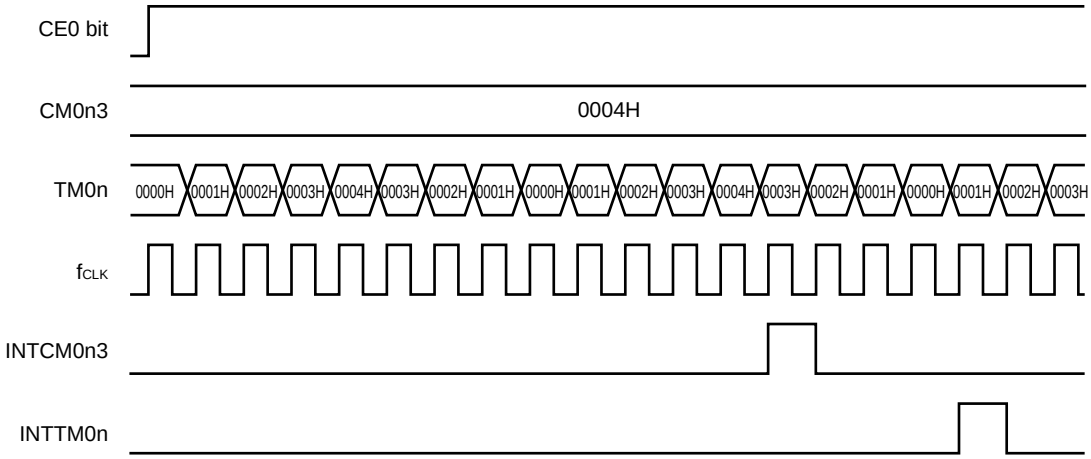


Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-42. Interrupt Generation Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave): In case of Interrupt Culling Ratio of 1/2

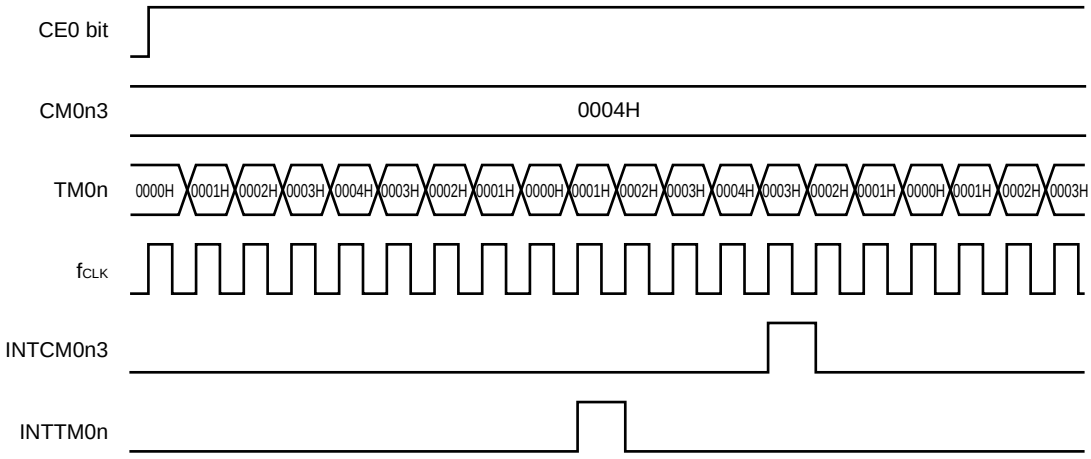
(a) When STINT bit = 0



Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

(b) When STINT bit = 1

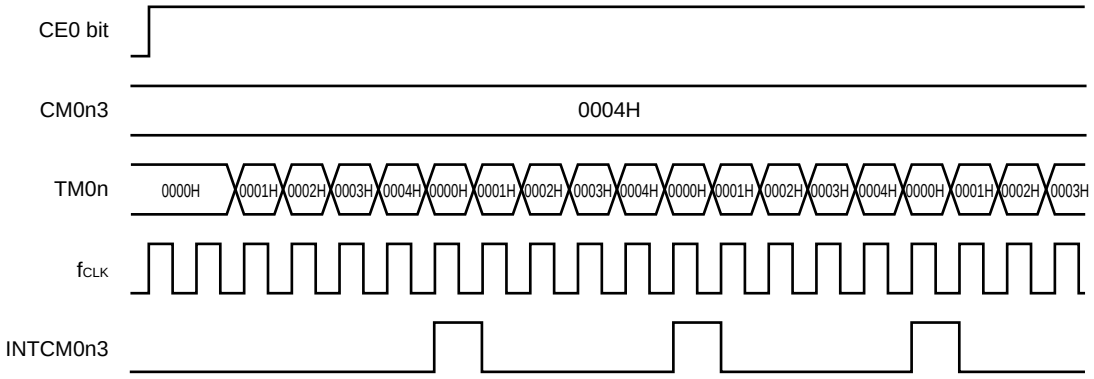


Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-43. Interrupt Generation Timing in PWM Mode 2 (Sawtooth Wave): In Case of Interrupt Culling Ratio of 1/1

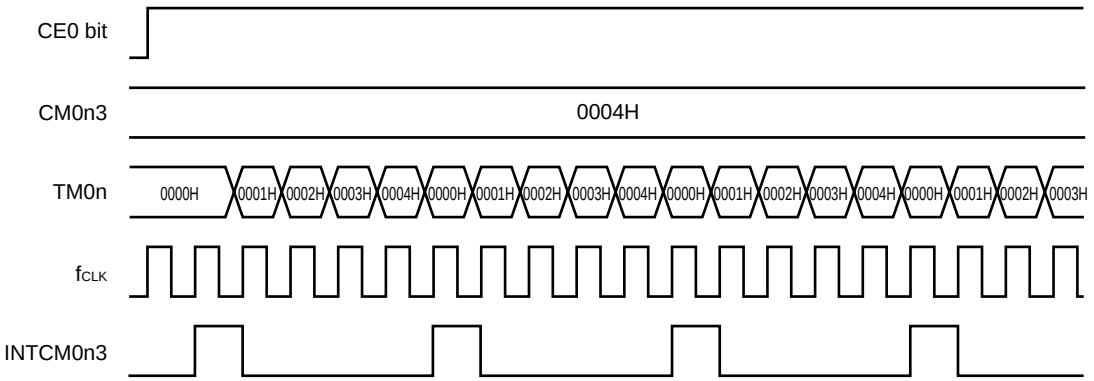
(a) When STINT bit = 0



Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

(b) When STINT bit = 1

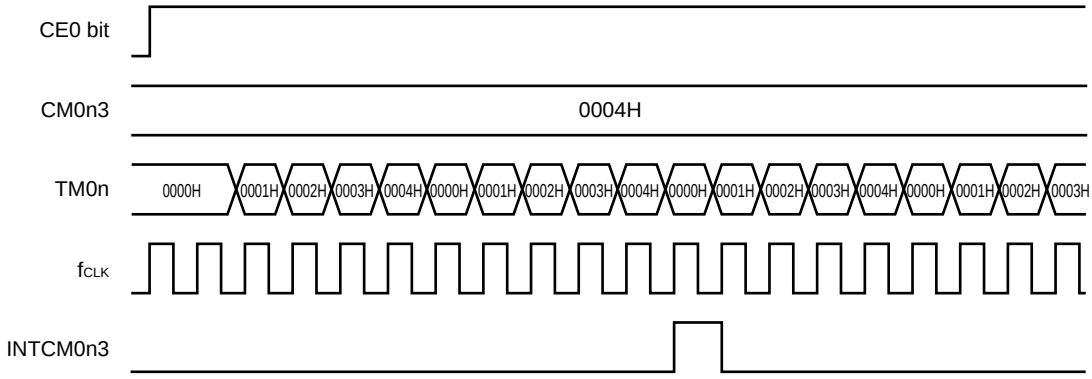


Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

Figure 9-44. Interrupt Generation Timing in PWM Mode 2 (Sawtooth Wave): In Case of Interrupt Culling Ratio of 1/2

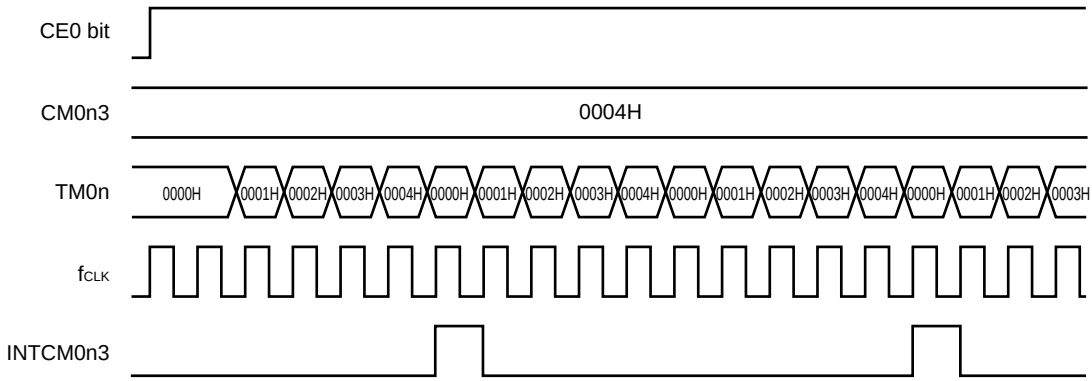
(a) When STINT bit = 0



Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

(b) When STINT bit = 1

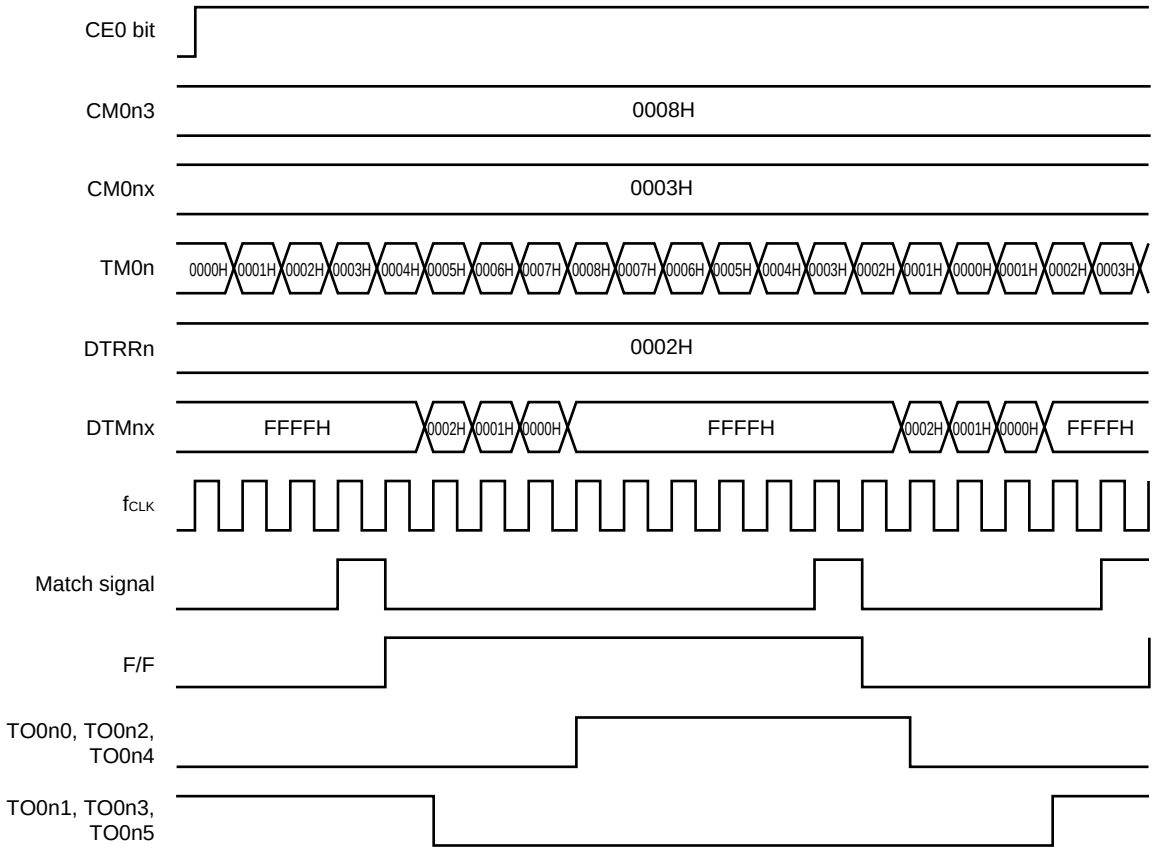


Remarks 1. n = 0, 1

2. f_{CLK}: Base clock

(4) TO0n0 to TO0n5 output timing

Figure 9-45. TO0n0 to TO0n5 Output Timing in PWM Mode 0 (Symmetric Triangular Wave), PWM Mode 1 (Asymmetric Triangular Wave)



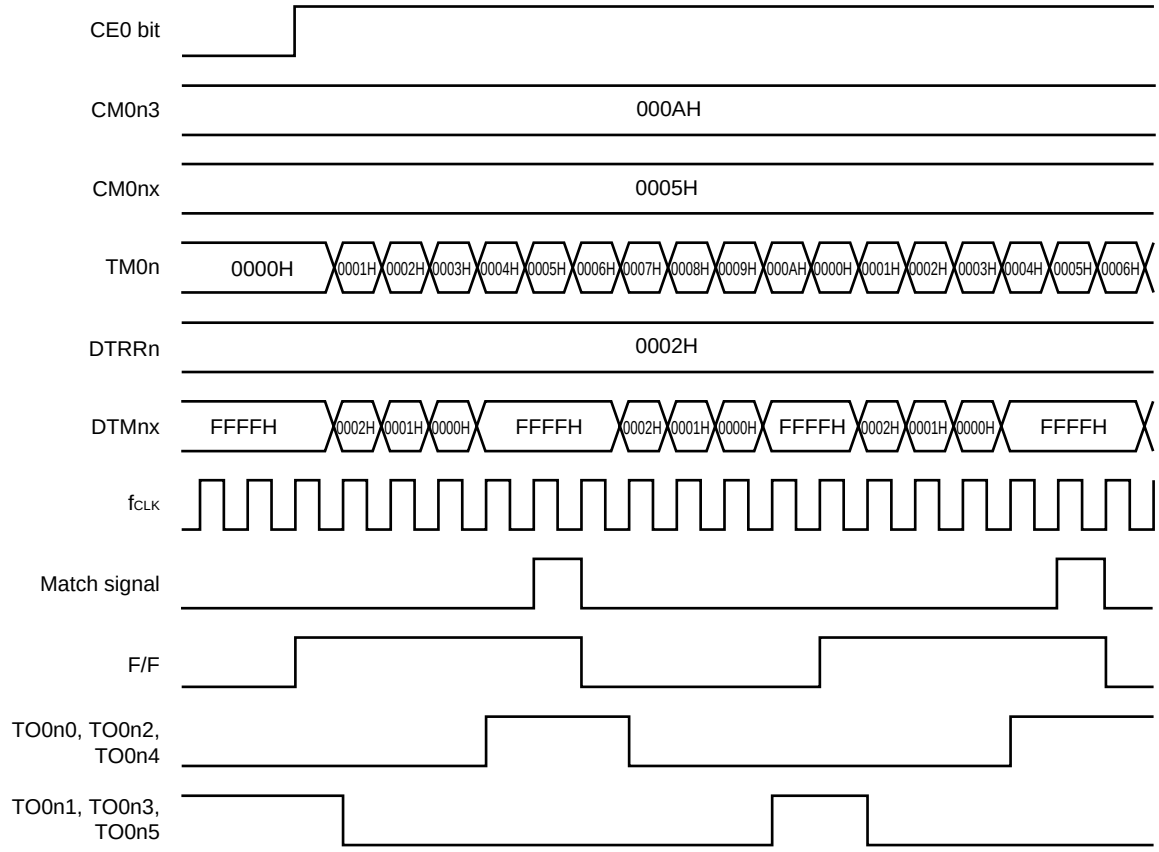
Remarks 1. The above figure shows the timing until the compare register and the TM0n timer match and the TO0n0 to TO0n5 outputs change.

2. x = 0 to 2

3. n = 0, 1

4. f_{CLK}: Base clock

Figure 9-46. TO0n0 to TO0n5 Output Timing in PWM Mode 2 (Sawtooth Wave)



Remarks 1. The above figure shows the timing until the compare register and the TM0n timer match and the TO0n0 to TO0n5 outputs change.

2. x = 0 to 2

3. n = 0, 1

4. f_{CLK}: Base clock

9.2 Timer 1

9.2.1 Features (timer 1)

Timers 10, 11 (TM10, TM11) are 16-bit up/down counters that perform the following operations.

- General-purpose timer mode
  Free-running timer
  PWM output
- Up/down counter mode
  UDC mode A
  UDC mode B

9.2.2 Function overview (timer 1)

- 16-bit 2-phase encoder input up/down counter & general-purpose timer (TM1n): 2 channels
- Compare register: 2 × 2 channels
- Capture/compare register: 2 × 2 channels
- Interrupt request source
  - Capture/compare match interrupt: 2 types × 2 channels
  - Compare match interrupt request: 2 types × 2 channels
- Capture request signal: 2 types × 2 channels
  - The TM1n value can be latched using the valid edge of the INTP1n0, INTP1n1 pins corresponding to the capture/compare register as the capture trigger.
- Count clocks selectable through division by prescaler (maximum frequency of count clock: 8 MHz)
- Base clock (f_{CLK}): 2 types (maximum frequency of f_{CLK}: 16 MHz)
  ϕ/2 and ϕ/4 can be selected
- Prescaler divide ratio
  The following divide ratios can be selected according to the base clock (f_{CLK}).

Divide Ratio	Base Clock (f_{CLK})	
	ϕ/2 Selected	ϕ/4 Selected
1/2	ϕ/4	ϕ/8
1/4	ϕ/8	ϕ/16
1/8	ϕ/16	ϕ/32
1/16	ϕ/32	ϕ/64
1/32	ϕ/64	ϕ/128
1/64	ϕ/128	ϕ/256
1/128	ϕ/256	ϕ/512

- 2-phase encoder input

  The 2-phase encoder signal from external is used as the count clock of the timer counter with the external clock input pins (TIUD1n, TCUD1n). The counter mode can be selected from among the four following modes.

  - Mode 1: Counts the input pulses of the count pulse input pin.
    Up/down is specified by the level of one more input pin.
  - Mode 2: Counts up/down using the respective input pulses of the up count pulse input pin and down count pulse input pin.
  - Mode 3: Counts up/down using the phase relationship of the pulses input to 2 pins.
  - Mode 4: Counts up/down using the phase relationship of the pulses input to 2 pins. Counting is done using the respective rising edges and the falling edges of the pulses.

- PWM output function

  In the general-purpose timer mode, 16-bit resolution PWM output can be output from the TO1n pin.

- Timer clear

  The following timer clear operations are performed according to the mode that is used.

  (a) General-purpose timer mode: Timer clear operation is possible upon occurrence of match with CM1n0 set value.

  (b) Up/down counter mode: The timer clear operation can be selected from among the following four conditions.

  (i) Timer clear performed upon occurrence of match with CM1n0 set value during TM1n up count operation, and timer clear performed upon occurrence of match with CM1n1 set value during TM1n down count operation.

  (ii) Timer clear performed only by external input.

  (iii) Timer clear performed upon occurrence of match between TM1n count value and CM1n0 set value.

  (iv) Timer clear performed upon occurrence of external input and match between TM1n count value and CM1n0 set value.

- External pulse output (TO1n): 1 × 2 channels

Remark ϕ : Internal system clock
n = 0, 1

9.2.3 Basic configuration

The basic configuration is shown below.

Table 9-4. Timer 1 Configuration List

Timer	Count Clock		Register	Read/Write	Generated Interrupt Signal	Capture Trigger
	Note 1	**Note 2**				
Timer 1	ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256	ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256, ϕ/512	TM10	Read/write	–	–
			CM100	Read/write	INTCM100	–
			CM101	Read/write	INTCM101	–
			CC100	Read/write	INTCC100	INTP100
			CC101	Read/write	INTCC101	INTP100 or INTP101
			TM11	Read/write	–	–
			CM110	Read/write	INTCM110	–
			CM111	Read/write	INTCM111	–
			CC110	Read/write	INTCC110	INTP110
			CC111	Read/write	INTCC111	INTP110 or INTP111

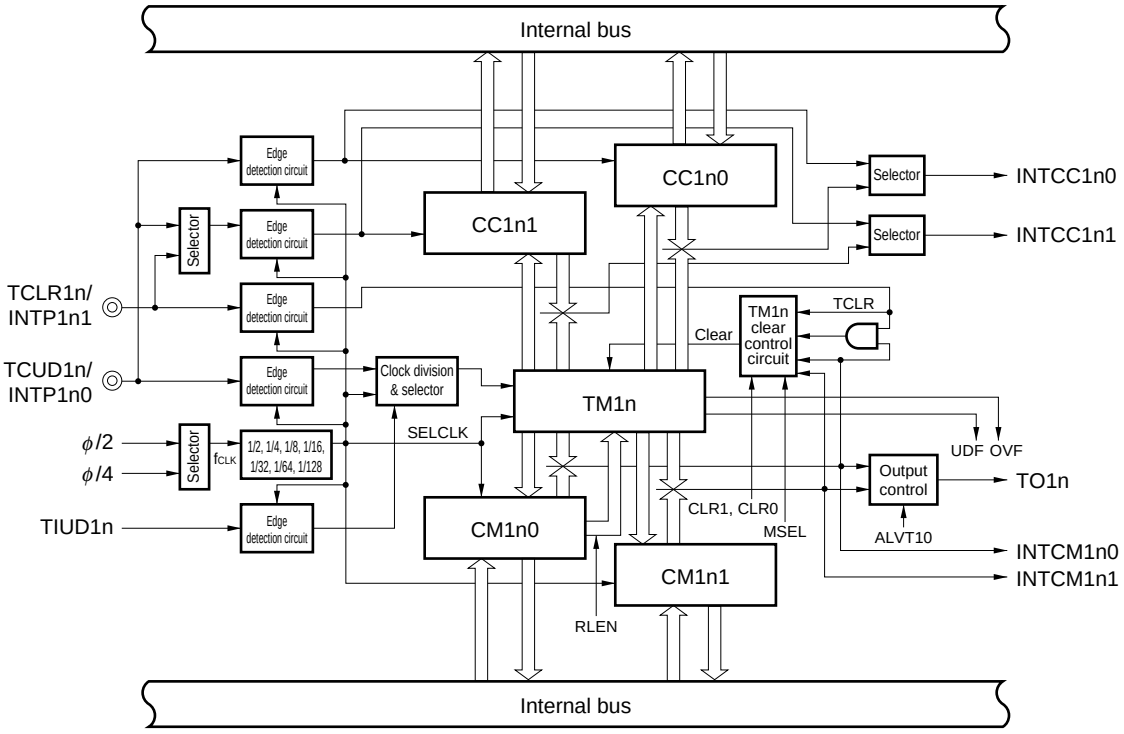
Notes 1. When ϕ/2 is selected as the base clock to TM1n.

2. When ϕ/4 is selected as the base clock to TM1n.

Remark ϕ: Internal system clock
S/R: Set/Reset

Figure 9-47 shows the block diagram of timer 1.

Figure 9-47. Block Diagram of Timer 1



Remarks 1. n = 0, 1

2. ϕ : Internal system clock

3. f_{CLK}: Base clock (16 MHz (MAX.))

(1) Timers 10, 11 (TM10, TM11)

TM1n is a 2-phase encoder input up/down counter and general-purpose timer.
It can be read/written in 16-bit units.

Cautions 1. Write to TM1n is enabled only when the CE1 bit of the TMC1n register is "0" (count operation disabled).

2. It is prohibited to set the CMD bit (general-purpose timer mode) and the MSEL bit (UDC mode B) of the TUMn register to "0" and "1", respectively.

3. Continuous reading of TM1n is prohibited. If TM1n is continuously read, the second read value may differ from the actual value. If TM1n must be read twice, be sure to read another register between the first and the second read operation.

Correct usage example	**Incorrect usage example**
TM10 read	TM10 read
TM11 read	TM10 read
TM10 read	TM11 read
TM11 read	TM11 read

Figure 9-48. Timers 10, 11 (TM10, TM11)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TM10																	FFFFF5E0H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TM11																	FFFFF600H	0000H

TM1n start and stop is controlled by the CE1 bit of timer control register 1n (TMC1n).
The TM1n operation consists of the following two modes.

(a) General-purpose timer mode

In the general-purpose timer mode, TM1n operates as a 16-bit interval timer, free-running timer, or for PWM output.

Counting is performed based on the clock selected by software.

Division by the prescaler can be selected for the count clock from among $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$, or $f_{CLK}/128$ with bits PRM12 to PRM10 of prescaler mode register 1n (PRM1n). (f_{CLK}: base clock, refer to **9.2.4 (1) Timer 1n/timer 2n clock selection register (PRM02)**).

(b) Up/down counter mode (UDC mode)

In the UDC mode, TM1n functions as a 16-bit up/down counter, counting based on the TCUD1n and TIUD1n input signals.

Two operation modes can be set with the MSEL bit of the TUMn register for this mode.

(i) UDC mode A (when CMD bit = 1, MSEL bit = 0)

TM1n can be cleared by setting the CLR1 and CLR0 bits of the TMC1n register.

(ii) UDC mode B (when CMD bit = 1, MSEL bit = 1)

TM1n is cleared upon match with CM1n0 during TM1n up count operation.

TM1n is cleared upon match with CM1n1 during TM1n down count operation.

When the CE1 bit of the TMC1n register is “1”, TM1n counts up when the operation mode is the general-purpose mode, and it counts up/down when the operation mode is the UDC mode.

The conditions for clearing the TM1n are classified as follows depending on the operation mode.

Table 9-5. Timer 1 (TM1n) Clear Conditions

Operation Mode	TUMn Register		TMC1n Register			TM1n Clear
	CMD Bit	MSEL Bit	ENMD Bit	CLR1 Bit	CLR0 Bit	
General-purpose timer mode	0	0	0	×	×	Clearing not performed
			1	×	×	Cleared upon match with CM1n0 set value
UDC mode A	1	0	×	0	0	Cleared only by TCLR1n input
			×	0	1	Cleared upon match with CM1n0 set value during up count operation
			×	1	0	Cleared by TCLR1n input or upon match with CM1n0 set value during up count operation
			×	1	1	Clearing not performed
UDC mode B	1	1	×	×	×	Cleared upon match with CM1n0 set value during up count operation or upon match with CM1n1 set value during down count operation
Settings other than the above						Setting prohibited

Remarks 1. n = 0, 1

2. ×: Indicates that the set value of that bit is ignored.

(2) Compare registers 100, 110 (CM100, CM110)

CM1n0 is a 16-bit register that always compares its value with the value of TM1n. When the value of a compare register matches the value of TM1n, an interrupt signal is generated. The interrupt generation timing in the various modes is described below.

- In the general-purpose timer mode (CMD bit of TUMn register = 0) and UDC mode A (MSEL bit of TUMn register = 0), an interrupt signal (INTCM1n0) is always generated upon occurrence of a match.
- In UDC mode B (MSEL bit of TUMn register = 1), an interrupt signal (INTCM1n0) is generated only upon occurrence of a match during down count operation.

CM1n0 can be read/written in 16-bit units.

Caution When the CE1 bit of the TMC1n register is "1", it is prohibited to overwrite the value of the CM1n0 register.

Figure 9-49. Compare Registers 100, 110 (CM100, CM110)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CM100																	FFFFF5E2H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CM110																	FFFFF602H	0000H

(3) Compare registers 101, 111 (CM101, CM111)

CM1n1 is a 16-bit register that always compares its value with the value of TM1n. When the value of a compare register matches the value of TM1n, an interrupt signal is generated. The interrupt generation timing in the various modes is described below.

- In the general-purpose timer mode (CMD bit of TUMn register = 0) and UDC mode A (MSEL bit of TUMn register = 0), an interrupt signal (INTCM1n1) is always generated upon occurrence of a match.
- In UDC mode B (MSEL bit of TUMn register = 1), an interrupt signal (INTCM1n1) is generated only upon occurrence of a match during down count operation.

CM1n1 can be read/written in 16-bit units.

Caution When the CE1 bit of the TMC1n register is "1", it is prohibited to overwrite the value of the CM1n1 register.

Figure 9-50. Compare Registers 101, 111 (CM101, CM111)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CM101																	FFFFF5E4H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CM111																	FFFFF604H	0000H

(4) Capture/compare registers 100, 110 (CC100, CC110)

CC1n0 is a 16-bit register. It can be used as a capture register or as a compare register through specification with capture/compare control register n (CCRn). CC1n0 can be read/written in 16-bit units.

Cautions 1. When used as a capture register (CMS0 bit of CCRn register = 0), write access from the CPU is prohibited.

2. When used as a compare register (CMS0 bit of CCRn register = 1) and the CE1 bit of the TMC1n register is "1", overwriting the CC1n0 register values is prohibited.

3. When the CE1 bit of the TMC1n register is "0", the capture trigger is disabled.

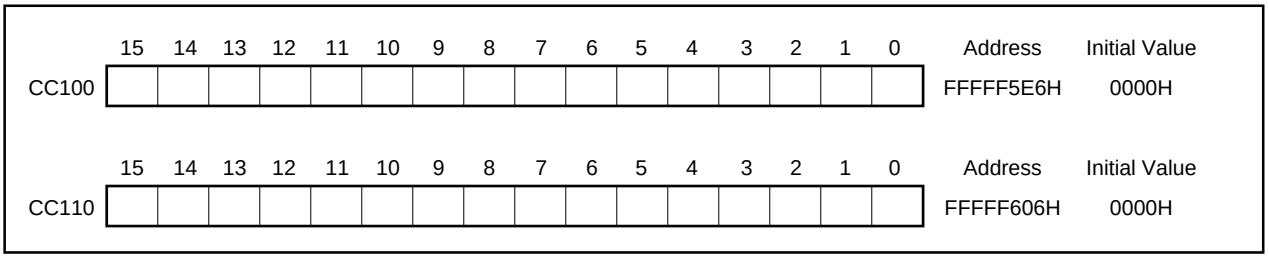
4. When the operation mode is changed from capture register to compare register, newly set a compare value.

5. Continuous reading of CC1n0 is prohibited. If CC1n0 is continuously read, the second read value may differ from the actual value. If CC1n0 must be read twice, be sure to read another register between the first and the second read operation.

Correct usage example	**Incorrect usage example**
CC100 read	CC100 read
CC110 read	CC100 read
CC100 read	CC110 read
CC110 read	CC110 read

Remark n = 0, 1

Figure 9-51. Capture/Compare Registers 100, 110 (CC100, CC110)



(a) When set as a capture register

When CC1n0 is set as a capture register, the valid edge of the corresponding external interrupt INTP1n0 signal is detected as the capture trigger. TM1n latches the count value in synchronization with the capture trigger (capture operation). The latched value is held in the capture register until the next capture operation.

The valid edge of external interrupts (rising edge, falling edge, both edges) is selected with signal edge selection register 1n (SESA1n).

When the CC1n0 register is specified as a capture register, interrupts are generated upon detection of the valid edge of the INTP1n0 signal.

(b) When set as a compare register

When CC1n0 is set as a compare register, it always compares its own value with the value of TM1n. If the value of CC1n0 matches the value of the TM1n, CC1n0 generates an interrupt signal (INTCC1n0).

(5) Capture/compare registers 101, 111 (CC101, CC111)

CC1n1 is a 16-bit register. It can be used as a capture register or as a compare register through specification with capture/compare control register n (CCRn). CC1n1 can be read/written in 16-bit units.

Cautions 1. When used as a capture register (CMS1 bit of CCRn register = 0), write access from the CPU is prohibited.

2. When used as a compare register (CMS1 bit of CCRn register = 1) and the CE1 bit of the TMC1n register is "1", overwriting the CC1n1 register values is prohibited.

3. When the CE1 bit of the TMC1n register is "0", the capture trigger is disabled.

4. When the operation mode is changed from capture register to compare register, newly set a compare value.

5. Continuous reading of CC1n1 is prohibited. If CC1n1 is continuously read, the second read value may differ from the actual value. If CC1n1 must be read twice, be sure to read another register between the first and the second read operation.

Correct usage example	**Incorrect usage example**
CC101 read	CC101 read
CC111 read	CC101 read
CC101 read	CC111 read
CC111 read	CC111 read

Remark n = 0, 1

Figure 9-52. Capture/Compare Registers 101, 111 (CC101, CC111)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CC101																	FFFFF5E8H	0000H
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CC111																	FFFFF608H	0000H

(a) When set as a capture register

When CC1n1 is set as a capture register, the valid edge of either corresponding external interrupt signal INTP1n0 or INTP1n1 is selected with the selector, and the valid edge of the selected external interrupt signal is detected as the capture trigger. TM1n latches the count value in synchronization with the capture trigger (capture operation). The latched value is held in the capture register until the next capture operation.

The valid edge of external interrupts (rising edge, falling edge, both edges) is selected with signal edge selection register 1n (SESA1n).

When the CC1n1 register is specified as a capture register, interrupts are generated upon detection of the valid edge of either the INTP1n0 or INTP1n1 signal.

(b) When set as a compare register

When CC1n1 is set as a compare register, it always compares its own value with the value of TM1n. If the value of CC1n1 matches the value of the TM1n, CC1n1 generates an interrupt signal (INTCC1n1).

9.2.4 Control registers

(1) Timer 1n/timer 2n clock selection register (PRM02)

The PRM02 register is used to select the base clock (f_{CLK}) of timer 1 (TM1n) and timer 2 (TM2n).

This register can be read/written in 8- or 1-bit units.

Caution Always set this register before using the timers.

Figure 9-53. Timer 1n/Timer 2n Clock Selection Register (PRM02)

	7	6	5	4	3	2	1	0	Address	Initial Value
PRM02	0	0	0	0	0	0	0	PRM2	FFFFF5D8H	00H

Bit Position	Bit Name	Function
0	PRM2	Specifies the base clock of timer 1 (TM1n) and timer 2 (TM2n). 0: ϕ/4 (when ϕ > 32 MHz) 1: ϕ/2 (when $\phi \leq$ 32 MHz)

Remark ϕ: Internal system clock

n = 0, 1

(2) Timer unit mode registers 0, 1 (TUM0, TUM1)

The TUMn register is an 8-bit register used to specify the TM1n operation mode or to control the operation of the PWM output pin.

TUMn can be read/written in 8- or 1-bit units.

Cautions 1. Changing the value of the TUMn register during TM1n operation (CE1 bit of TMCn register = 1) is prohibited.

2. When the CMD bit = 0 (general-purpose timer mode), setting MSEL bit = 1 (UDC mode B) is prohibited.

Figure 9-54. Timer Unit Mode Registers 0, 1 (TUM0, TUM1) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial Value
TUM0	CMD	0	0	0	TOE10	ALVT10	0	MSEL	FFFFF5EBH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
TUM1	CMD	0	0	0	TOE10	ALVT10	0	MSEL	FFFFF60BH	00H

Bit Position	Bit Name	Function
7	CMD	Specifies TM1n operation mode. 0: General-purpose timer mode (up count) 1: UDC mode (up/down count)
3	TOE10	Specifies timer output (TO1n) enable. 0: Timer output disabled 1: Timer output enabled **Caution When CMD bit = 1 (UDC mode), timer output is not performed regardless of the setting of the TOE10 bit. At this time, timer output consists of the negative phase level of the level set by the ALVT10 bit.**
2	ALVT10	Specifies active level of timer output (TO1n). 0: Active level is high level 1: Active level is low level **Caution When CMD bit = 1 (UDC mode), timer output is not performed regardless of the setting of the TOE10 bit. At this time, timer output consists of the negative phase level of the level set by the ALVT10 bit.**

Remark n = 0, 1

Figure 9-54. Timer Unit Mode Registers 0, 1 (TUM0, TUM1) (2/2)

Bit Position	Bit Name	Function
0	MSEL	Specifies operation in UDC mode (up/down count) 0: UDC mode A TM1n can be cleared by setting the CLR1, CLR0 bits of the TMC1n register. 1: UDC mode B TM1n is cleared in the following cases. • Upon match with CM1n0 during TM1n up count operation • Upon match with CM1n1 during TM1n down count operation When UDC mode B is set, the ENMD, CLR1, and CLR0 bits of the TMC1n register becomes ineffective.

Remark n = 0, 1

(3) Timer control registers 10, 11 (TMC10, TMC11)

The TMC1n register is used to enable/disable TM1n operation and to set transfer and timer clear operations. TMC1n can be read/written in 8- or 1-bit units.

Caution Changing the value of bits of the TMC1n register other than the CE1 bit during TM1n operation (CE1 bit = 1) is prohibited.

Figure 9-55. Timer Control Registers 10, 11 (TMC10, TMC11) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial Value
TMC10	0	CE1	0	0	RLEN	ENMD	CLR1	CLR0	FFFFF5ECH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
TMC11	0	CE1	0	0	RLEN	ENMD	CLR1	CLR0	FFFFF60CH	00H

Bit Position	Bit Name	Function
6	CE1	Enables/disables TM1n operation. 0: Disable TM1n count operation 1: Enable TM1n count operation
3	RLEN	Enables/disables transfer from CM1n0 to TM1n. 0: Disable transfer 1: Enable transfer **Cautions 1. When RLEN = 1, the value set to CM1n0 is transferred to TM1n upon occurrence of TM1n underflow.** **2. When the CMD bit of the TUMn register = 0, the RLEN bit setting becomes ineffective.**
2	ENMD	Enables/disables clearing of TM1n in general-purpose timer mode (CMD bit of TUMn register = 0). 0: Clear disable (free running mode) Clearing is not performed even when TM1n and CM1n0 values match. 1: Clear enable Clearing is performed when TM1n and CM1n0 values match. **Caution When the CMD bit of the TUMn register = 1 (UDC mode), the ENMD bit setting becomes ineffective.**

Remark n = 0, 1

Figure 9-55. Timer Control Registers 10, 11 (TMC10, TMC11) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>1, 0</td><td>CLR1, CLR0</td><td>Controls TM1n clear operation in UDC mode A.

<table>
<tr><th>CLR1</th><th>CLR0</th><th>Specify TM1n Clear Source</th></tr>
<tr><td>0</td><td>0</td><td>Clear only by external input (TCLR1n)</td></tr>
<tr><td>0</td><td>1</td><td>Clear upon match of TM1n count value and CM1n0 set value</td></tr>
<tr><td>1</td><td>0</td><td>Clear by TCLR1n input or upon match of TM1n count value and CM1n0 set value</td></tr>
<tr><td>1</td><td>1</td><td>Don’t clear</td></tr>
</table>
Cautions 1. Clearing by match of the TM1n count value and CM1n0 set value is effective only during TM1n up count operation (TM1n is not cleared during TM1n down count operation).
2. When the CMD bit of the TUMn register = 0 (general-purpose timer mode), the CLR1 and CLR0 bit settings are ineffective.
3. When the MSEL bit of the TUMn register = 1 (UDC mode B), the CLR1 and CLR0 bit settings are ineffective.
4. When clearing by TCLR1n has been enabled with bits CLR1 and CLR0, clearing is performed whether the value of the CE1 bit is 1 or 0.</td></tr>
</table>

Remark n = 0, 1

(4) Capture/compare control registers 0, 1 (CCR0, CCR1)

The CCRn register specifies the operation mode of the capture/compare registers (CC1n0, CC1n1). CCRn can be read/written in 8- or 1-bit units.

Caution Overwriting the CCRn register during TM1n operation (CE1 bit = 1) is prohibited.

Figure 9-56. Capture/Compare Control Registers 0, 1 (CCR0, CCR1)

	7	6	5	4	3	2	1	0	Address	Initial Value
CCR0	0	0	0	0	0	0	CMS1	CMS0	FFFFF5EAH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
CCR1	0	0	0	0	0	0	CMS1	CMS0	FFFFF60AH	00H

Bit Position	Bit Name	Function
1	CMS1	Specifies operation mode of CC1n1. 0: Capture register 1: Compare register
0	CMS0	Specifies operation mode of CC1n0. 0: Capture register 1: Compare register

Remark n = 0, 1

(5) Signal edge selection registers 10, 11 (SESA10, SESA11)

The SESA1n register is used to specify the valid edge of external interrupt requests from external pins (INTP100, INTP101, INTP110, INTP111, TIUD10, TIUD11, TCUD10, TCUD11, TCLR10, TCLR11). The correspondences between each register and the external interrupt requests it controls are as follows.

- SESA10: TIUD10, TCUD10, TCLR10, INTP100, INTP101
- SESA11: TIUD11, TCUD11, TCLR11, INTP110, INTP111

The valid edge (rising edge, falling edge, or both edges) can be specified independently for each pin.
SESA1n can be read/written in 8- or 1-bit units.

Cautions 1. Changing the values of the SESA1n register bits during TM1n operation (CE1 bit = 1) is prohibited.

2. Be sure to set (to 1) the CE1 bit of timer control registers 10, 11 (TMC10, TMC11) even when timer 1 is not used and the TCUD10/INTP100, TCLR10/INTP101, TCUD11/INTP110, and TCLR11/INTP111 pins are used as INTP100, INTP101, INTP110, and INTP111.

Figure 9-57. Signal Edge Selection Registers 10, 11 (SESA10, SESA11) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial Value
SESA10	TESUD01	TESUD00	CESUD01	CESUD00	IES1011	IES1010	IES1001	IES1000	FFFFF5EDH	00H
	TIUD10, TCUD10		TCLR10		INTP101		INTP100			

	7	6	5	4	3	2	1	0	Address	Initial Value
SESA11	TESUD11	TESUD10	CESUD11	CESUD10	IES1111	IES1110	IES1101	IES1100	FFFFF60DH	00H
	TIUD11, TCUD11		TCLR11		INTP111		INTP110			

Bit Position	Bit Name	Function
7, 6	TESUDn1, TESUDn0	Specifies valid edge of pins TIUD10, TIUD11, TCUD10, TCUD11.

TESUDn1	TESUDn0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Remark n = 0, 1

Figure 9-57. Signal Edge Selection Registers 10, 11 (SESA10, SESA11) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>7, 6</td><td>TESUDn1,
TESUDn0</td><td>Cautions 1. The set values of the TESUDn1 and TESUDn0 bits are only effective in UDC mode A and UDC mode B.
2. If mode 4 is specified as the operation mode of TM1n (specified with PRM12 to PRM10 bits of PRM1n register), the valid edge specifications for pins TIUD1n and TCUD1n (bits TESUDn1 and TESUDn0) are not effective.</td></tr>
<tr><td>5, 4</td><td>CESUDn1,
CESUDn0</td><td>Specifies valid edge of pins TCLR10, TCLR11.
<table><tr><th>CESUDn1</th><th>CESUDn0</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Low level</td></tr><tr><td>1</td><td>1</td><td>High level</td></tr></table>The set values of bits CESUDn1 and CESUDn0 and the TM1n operation are related as follows.
00: TM1n cleared after detection of rising edge of TCLR1n
01: TM1n cleared after detection of falling edge of TCLR1n
10: TM1n cleared status held while TCLR1n input is low level
11: TM1n cleared status held while TCLR1n input is high level
Caution The set values of the CESUDn1 and CESUDn0 bits are effective only in UDC mode A.</td></tr>
<tr><td>3, 2</td><td>IES1n11,
IES1n10</td><td>Specifies valid edge of pins INTP101, INTP111.
<table><tr><th>IES1n11</th><th>IES1n10</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>1</td><td>1</td><td>Both rising and falling edges</td></tr></table></td></tr>
<tr><td>1, 0</td><td>IES1n01,
IES1n00</td><td>Specifies valid edge of pins INTP100, INTP110.
<table><tr><th>IES1n01</th><th>IES1n00</th><th>Valid Edge</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td></tr><tr><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>1</td><td>1</td><td>Both rising and falling edges</td></tr></table></td></tr>
</table>

Remark n = 0, 1

(6) Prescaler mode registers 10, 11 (PRM10, PRM11)

The PRM1n register is used to perform the following selections.

- Selection of count clock in the general-purpose timer mode (CMD bit of TUMn register = 0)
- Selection of count operation mode in the UDC mode (CMD bit = 1)

PRM1n can be read/written in 8- or 1-bit units.

Cautions 1. Overwriting the PRM1n register during TM1n operation (CE1 bit = 1) is prohibited.

2. When the CMD bit of the TUMn register = 1 (UDC mode), setting the values of bits PRM12 through PRM10 to 000, 001, 010, and 011 is prohibited.

3. When TM1n is in mode 4, specification of the valid edge for the TIUD1n and TCUD1n pins is ineffective.

Figure 9-58. Prescaler Mode Registers 10, 11 (PRM10, PRM11)

	7	6	5	4	3	2	1	0	Address	Initial Value
PRM10	0	0	0	0	0	PRM12	PRM11	PRM10	FFFFF5EEH	07H

	7	6	5	4	3	2	1	0	Address	Initial Value
PRM11	0	0	0	0	0	PRM12	PRM11	PRM10	FFFFF60EH	07H

Bit Position	Bit Name	Function
2 to 0	PRM12 to PRM10	Specifies the up/down count operation mode during input of the clock rate when the internal clock of the TM1n is used, or during external clock (TIUD1n) input.

PRM12	PRM11	PRM10	CMD = 0	CMD = 1	
			Count Clock	Count Clock	Up/Down Count
0	0	0	Setting prohibited	Setting prohibited (Mode 4) (At this time, SESA1n register is enabled.)	
0	0	1	$f_{CLK}/2$		
0	1	0	$f_{CLK}/4$		
0	1	1	$f_{CLK}/8$		
1	0	0	$f_{CLK}/16$	TIUD1n	Mode 1
1	0	1	$f_{CLK}/32$		Mode 2
1	1	0	$f_{CLK}/64$		Mode 3
1	1	1	$f_{CLK}/128$		Mode 4

Remarks 1. f_{CLK}: Base clock

2. n = 0, 1

(a) In general-purpose timer mode (CMD bit of TUMn register = 0)

The count clock is fixed to the internal clock. The clock rate of TM1n is specified with bits PRM12 through PRM10.

(b) UDC mode (CMD bit of TUMn register = 1)

The TM1n count causes in the UDC mode are as follows.

Operation Mode	TM1n Operation
Mode 1	Down count when TCUD1n = high level Up count when TCUD1n = low level
Mode 2	Up count upon detection of valid edge of TIUD1n input Down count upon detection of valid edge of TCUD1n input
Mode 3	Automatic judgment with TCUD1n input level upon detection of valid edge of TIUD1n input
Mode 4	Automatic judgment upon detection of both edges of TIUD1n input and both edges of TCUD1n input

(7) Status registers 0, 1 (STATUS0, STATUS1)

The STATUSn register indicates the operating status of TM1n.

STATUSn is read-only in 8- or 1-bit units.

Caution Overwriting the STATUSn register during TM1n operation (CE1 bit = 1) is prohibited.

Figure 9-59. Status Registers 0, 1 (STATUS0, STATUS1)

	7	6	5	4	3	2	1	0	Address	Initial Value
STATUS0	0	0	0	0	0	UDF	OVF	UB/D	FFFFF5EFH	00H

	7	6	5	4	3	2	1	0	Address	Initial Value
STATUS1	0	0	0	0	0	UDF	OVF	UB/D	FFFFF60FH	00H

Bit Position	Bit Name	Function
2	UDF	TM1n underflow flag 0: No TM1n count underflow 1: TM1n count underflow **Caution The UDF bit is cleared (to "0") upon completion of read access to the STATUSn register from the CPU.**
1	OVF	TM1n overflow flag 0: No TM1n count overflow 1: TM1n count overflow **Caution The OVF bit is cleared (to "0") upon completion of read access to the STATUSn register from the CPU.**
0	UB/D	Indicates the operating status of TM1n up/down count. 0: TM1n up count in progress 1: TM1n down count in progress **Caution The state of the UB/D bit differs according to the mode as follows.** • **The UB/D bit is fixed to "0" by hardware when the CMD bit of the TUMn register = 0 (general-purpose timer mode).** • **The UB/D bit indicates the TM1n up/down count status when the CMD bit of the TUMn register = 1 (UDC mode).**

Remark n = 0, 1

(8) CC101 capture input selection register (CSL10)

The CSL10 register specifies capture input that is input to TM10.

CSL10 can be read/written in 8- or 1-bit units.

Figure 9-60. CC101 Capture Input Selection Register (CSL10)

	7	6	5	4	3	2	1	0	Address	Initial Value
CSL10	0	0	0	0	0	0	0	CSL0	FFFFF5F6H	00H

Bit Position	Bit Name	Function
0	CSL0	Specifies capture input to CC101. 0: INTP101 1: INTP100

(9) CC111 capture input selection register (CSL11)

The CSL11 register specifies capture input that is input to TM11.

CSL11 can be read/written in 8- or 1-bit units.

Figure 9-61. CC111 Capture Input Selection Register (CSL11)

	7	6	5	4	3	2	1	0	Address	Initial Value
CSL11	0	0	0	0	0	0	0	CSL1	FFFFF616H	00H

Bit Position	Bit Name	Function
0	CSL1	Specifies capture input to CC111. 0: INTP111 1: INTP110

9.2.5 Operation

(1) Basic operation

The following two operation modes can be selected for TM1n (n = 0, 1).

(a) General-purpose timer mode (CMD bit of TUMn register = 0)

In the general-purpose timer mode, the TM1n operates either as a 16-bit interval timer or as a PWM output timer.

The base clock (f_{CLK}) to TM1n is selected with the timer 1n/timer 2n clock selection register (PRM02), and the count clock is selected with the prescaler mode register (PRM1n).

(b) Up/down counter mode (UDC mode) (CMD bit of TUMn register = 1)

In the UDC mode, TM1n operates as a 16-bit up/down counter.

External clock input (TIUDn, TCUDn pins) by PRM1n register setting is used as the TM1n count clock.

The UDC mode is further divided into two modes according to the TM1n clear conditions.

- **UDC mode A (TUMn register's CMD bit = 1, MSEL bit = 0)**

  The TM1n clear cause can be selected as only external clear input (TCLR1n), a match signal between the TM1n count value and the CM1n0 set value during up count operation, or logical sum (OR) of the two signals, using bits CLR1 and CLR0 of the TMC1n register. TM1n can transfer the value of CM1n0 upon occurrence of TM1n underflow.

- **UDC mode B (TUMn register's CMD bit = 1, MSEL bit = 1)**

  The status of TM1n after match of the TM1n count value and CM1n0 set value is as follows.

  <1> In the case of up count operation, TM1n is cleared (0000H), and the INTCM1n0 interrupt is generated.

  <2> In the case of down count operation, the TM1n count value is decremented (–1).

  The status of TM1n after match of the TM1n count value and CM1n1 set value is as follows.

  <1> In the case of up count operation, the TM1n count value is incremented (+1).

  <2> In the case of down count operation, TM1n is cleared (0000H), and the INTCM1n1 interrupt is generated.

(2) Operation in general-purpose timer mode

TM1n can perform the following operations in the general-purpose timer mode.

(a) Interval operation

TM1n and CM1n0 always compare their values and the INTCM1n0 interrupt is generated upon occurrence of a match.

TM1n is cleared (0000H) at the count clock following the match.

Furthermore, when one more count clock is input, TM1n counts up to 0001H. The interval time can be calculated with the following formula.

Interval time = (CM1n0 value + 1) × TM1n count clock rate

Caution Interval operation can be achieved by setting the ENMD bit of the TMC1n register to "1".

(b) Free-running operation

TM1n performs full count operation from 0000H to FFFFH, and after the OVF bit of the STATUSn register is set (to "1"), TM1n is cleared and resumes counting. The free-running cycle can be calculated with the following formula.

Free-running cycle = 65536 × TM1n count clock rate

Caution The free-running operation can be achieved by setting the ENMD bit of the TMC1n register to "0".

(c) Compare function

TM1n connects two compare register (CM1n0, CM1n1) channels and two capture/compare register (CC1n0, CC1n1) channels.

When the TM1n count value and the set value of one of the compare registers match, a match interrupt (INTCM1n0, INTCM1n1, INTCC1n0[Note], INTCC1n1[Note]) is output.

Particularly in the case of interval operation, TM1n is cleared upon generation of the INTCM1n0 interrupt.

Note This match interrupt is generated when CC1n0 and CC1n1 are set to the compare register mode.

(d) Capture function

TM1n connects two capture/compare register (CC1n0, CC1n1) channels.

When CC1n0 and CC1n1 are set to the capture register mode, the value of TM1n is captured in synchronization with the corresponding capture trigger signal.

Furthermore, an interrupt request (INTCC1n0, INTCC1n1) is generated by the INTP1n0, INTP1n1 input signals.

Table 9-6. Capture Trigger Signal (TM1n) to 16-Bit Capture Register

Capture Register	Capture Trigger Signal
CC1n0	INTP1n0
CC1n1	INTP1n0 or INTP1n1

Remarks 1. CC1n0 and CC1n1 are capture/compare registers. Which of these registers is used is specified with capture/compare control register n (CCRn).

2. n = 0, 1

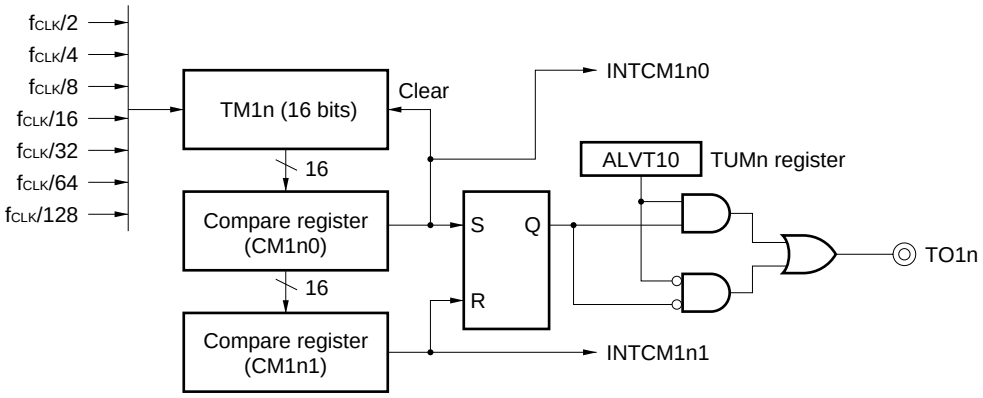
The valid edge of the capture trigger is specified by signal edge selection register n (SESAn). If both the rising edge and the falling edge are selected as the capture triggers, it is possible to measure the input pulse width from external. If a single edge is selected as the capture trigger, the input pulse cycle can be measured.

(e) PWM output operation

PWM output operation is performed from the TO1n pin by setting TM1n to the general-purpose timer mode (CMD bit = 0) using timer unit mode register n (TUMn).

The resolution is 16 bits, and the count clock can be selected from among seven internal clocks ($f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$, $f_{CLK}/128$).

Figure 9-62. TM1n Block Diagram (During PWM Output Operation)



Caution Be sure to set the count clock of TM1n to 8 MHz or lower.

Remarks 1. f_{CLK}: Base clock

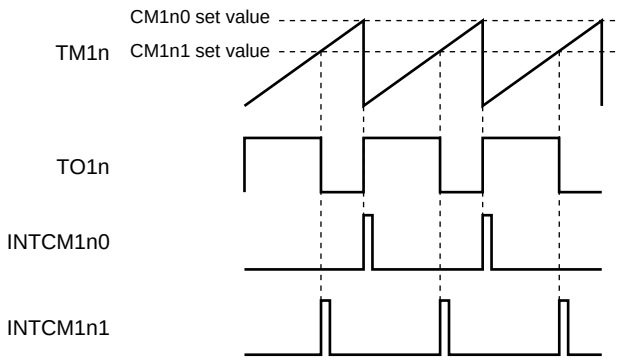
2. n = 0, 1

(i) Description of operation

The CM1n0 register is a compare register used to set the PWM output cycle. When the value of this register matches the value of TM1n, the INTCM1n0 interrupt is generated. Compare match is saved by hardware, and TM1n is cleared at the next count clock after the match.

The CM1n1 register is a compare register used to set the PWM output duty. Set the duty required for the PWM cycle.

Figure 9-63. PWM Signal Output Example (When ALVT10 Bit = 0 Is Set)



Cautions 1. Changing the values of the CM1n0 and CM1n1 registers is prohibited during TM1n operation (CE1 bit of TMC1n register = 1).

2. Changing the value of the ALVT10 bit of the TUMn register is prohibited during TM1n operation.

3. PWM signal output is performed from the second PWM cycle after the CE1 bit is set (to “1”).

(3) Operation in UDC mode

(a) Overview of operation in UDC mode

The count clock input to TM1n in the UDC mode (CMD bit of TUMn register = 1) can only be external input from the TIUD1n and TCUD1n pins. Up/down count judgment in the UDC mode is determined based on the phase difference of the TIUD1n and TCUD1n pin inputs according to the PRM1n register setting (There is a total of four choices).

Table 9-7. List of Count Operations in UDC Mode

PRM1n Register			Operation Mode	TM1n Operation
PRM12	PRM11	PRM10		
1	0	0	Mode 1	Down count when TCUD1n = high level Up count when TCUD1n = low level
1	0	1	Mode 2	Up count upon detection of valid edge of TIUD1n input Down count upon detection of valid edge of TCUD1n input
1	1	0	Mode 3	Automatic judgment in TCUD1n input level upon detection of valid edge of TIUD1n input
1	1	1	Mode 4	Automatic judgment upon detection of both edges of TIUD1n input and both edges of TCUD1n input

The UDC mode is further divided into two modes according to the TM1n clear conditions (Count operation is performed only with TIUD1n, TCUD1n input in both modes).

- **UDC mode A (TUMn register's CMD bit = 1, MSEL bit = 0)**

  The TM1n clear cause can be selected as only external clear input (TCLR1n), a match signal between the TM1n count value and the CM1n0 set value during up count operation, or logical sum (OR) of the two signals, using bits CLR1 and CLR0 of the TMC1n register. TM1n can transfer the value of CM1n0 upon occurrence of TM1n underflow.

- **UDC mode B (TUMn register's CMD bit = 1, MSEL bit = 1)**

  The status of TM1n after match of the TM1n count value and CM1n0 set value is as follows.

  <1> In the case of up count operation, TM1n is cleared (0000H), and the INTCM1n0 interrupt is generated.

  <2> In the case of down count operation, the TM1n count value is decremented (–1).

  The status of TM1n after match of the TM1n count value and CM1n1 set value is as follows.

  <1> In the case of up count operation, the TM1n count value is incremented (+1).

  <2> In the case of down count operation, TM1n is cleared (0000H), and the INTCM1n1 interrupt is generated.

(b) Up/down count operation in UDC mode

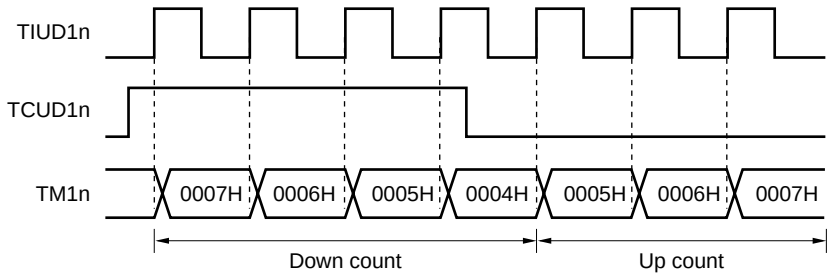
TM1n up/down count judgment in the UDC mode is determined based on the phase difference of the TIUD1n and TCUD1n pin inputs according to the PRM1n register setting.

(i) Mode 1 (PRM12 bit = 1, PRM11 bit = 0, PRM10 bit = 0)

In mode 1, the following count operations are performed based on the level of the TCUD1n pin upon detection of the valid edge of the TIUD1n pin.

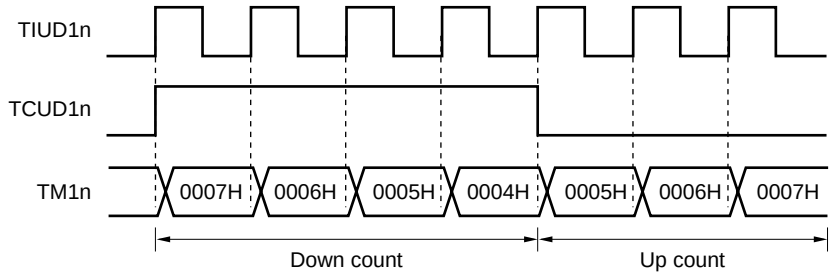
- TM1n down count operation when TCUD1n pin = high level
- TM1n up count operation when TCUD1n pin = low level

Figure 9-64. Mode 1 (When Rising Edge Is Specified as Valid Edge of TIUD1n Pin)



Remark n = 0, 1

Figure 9-65. Mode 1 (When Rising Edge Is Specified as Valid Edge of TIUD1n Pin): In Case of Simultaneous TCUD1n, TCUD1n Pin Edge Timing



Remark n = 0, 1

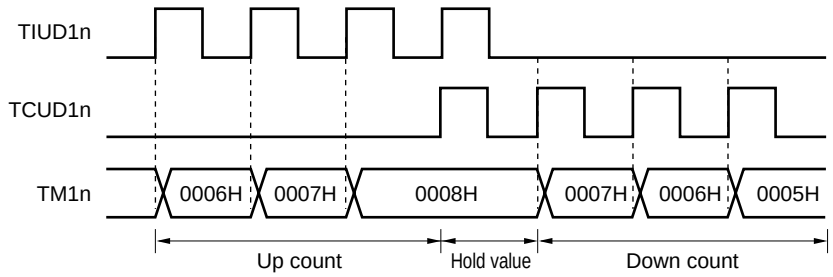
(ii) Mode 2 (PRM12 bit = 1, PRM11 bit = 0, PRM10 bit = 1)

The count conditions in mode 2 are as follows.

- TM1n up count upon detection of valid edge of TIUD1n pin
- TM1n down count upon detection of valid edge of TCUD1n pin

Caution If the count clock is simultaneously input to the TIUD1n pin and the TCUD1n pin, count operation is not performed and the immediately preceding value is held.

Figure 9-66. Mode 2 (When Rising Edge Is Specified as Valid Edge of TIUD1n, TCUD1n Pins)



Remark n = 0, 1

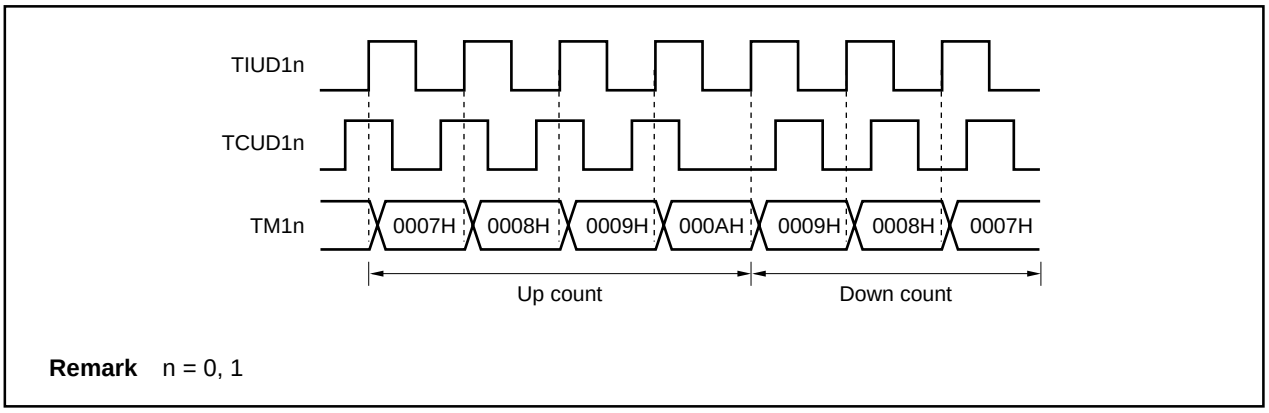
(iii) Mode 3 (PRM12 = 1, PRM11 = 1, PRM10 = 0)

In mode 3, when two signals 90 degrees out of phase are input to the TIUD1n and TCUD1n pins, the level of the TCUD1n pin is sampled at the input of the valid edge of the TIUD1n pin (Refer to **Figure 9-67**).

If the TCUD1n pin level sampled at the valid edge input to the TIUD1n pin is low, TM1n counts down when the valid edge is input to the TIUD1n pin.

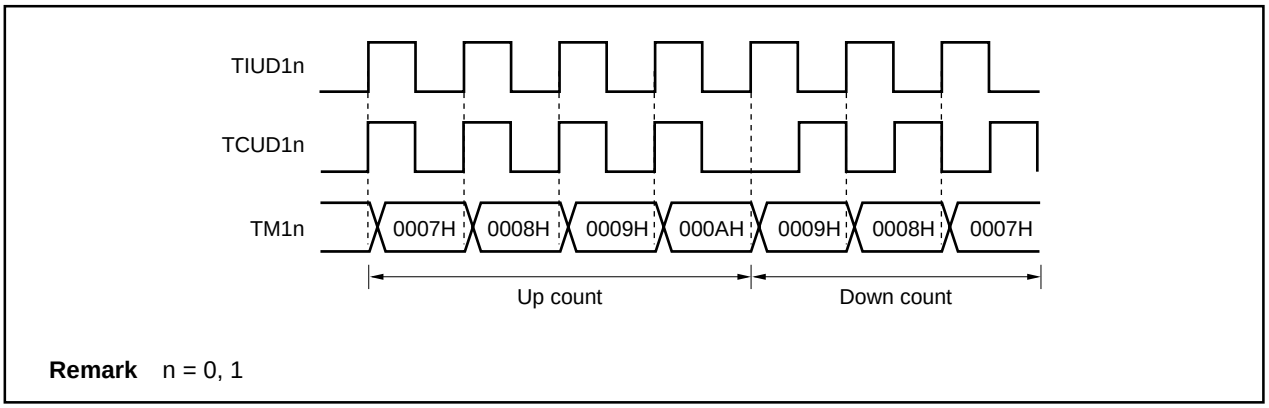
If the TCUD1n pin level sampled at the valid edge input to the TIUD1n pin is high, TM1n counts up when the valid edge is input to the TIUD1n pin.

Figure 9-67. Mode 3 (When Rising Edge Is Specified as Valid Edge of TIUD1n pin)



Remark n = 0, 1

Figure 9-68. Mode 3 (When Rising Edge Is Specified as Valid Edge of TIUD1n Pin): In Case of Simultaneous TIUD1n, TCUD1n Pin Edge Timing



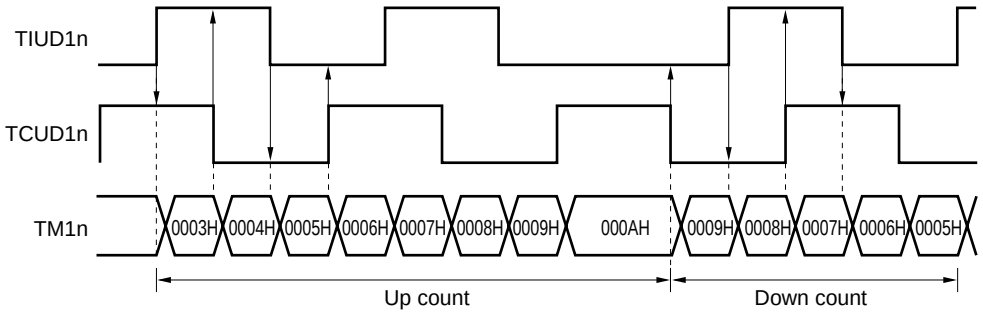
Remark n = 0, 1

(iv) Mode 4 (PRM12 = 1, PRM11 = 1, PRM10 = 1)

In mode 4, when two signals 90 degrees out of phase are input to the TIUD1n and TCUD1n pins, up/down operation is automatically judged and counting is performed according to the timing shown in **Figure 9-69**.

In mode 4, counting is executed at both the rising and falling edges of the two signals input to the TIUD1n and TCUD1n pins. Therefore, TM1n counts four times per cycle of an input signal (x4 count).

Figure 9-69. Mode 4



Cautions 1. When mode 4 is specified as the operation mode of TM1n, the valid edge specifications for pins TIUD1n and TCUD1n are not effective.

2. If the TIUD1n pin edge and TCUD1n pin edge are input simultaneously in mode 4, TM1n continues the same count operation (up or down) it was performing immediately before the input.

(c) Operation in UDC mode A

(i) Interval operation

The operations at the count clock following match of the TM1n count value and the CM1n0 set value are as follows.

- In case of up count operation: TM1n is cleared (0000H) and the INTCM1n0 interrupt is generated.
- In case of down count operation: The TM1n count value is decremented (–1) and the INTCM1n0 interrupt is generated.

Remark The interval operation can be combined with the transfer operation.

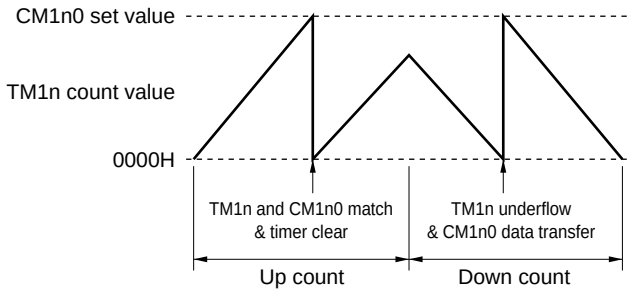
(ii) Transfer operation

The operations at the next count clock after the count value of TM1n becomes 0000H during TM1n count down operation are as follows.

- In case of down count operation: The data held in CM1n0 is transferred.
- In case of up count operation: The TM1n count value is incremented (+1).

Remarks 1. Transfer enable/disable can be set with the RLEN bit of the TMC1 register.
2. The transfer operation can be combined with the interval operation.

Figure 9-70. Example of TM1n Operation When Interval Operation and Transfer Operation Are Combined



Remark n = 0, 1

(iii) Compare function

TM1n connects two compare register (CM1n0, CM1n1) channels and two capture/compare register (CC1n0, CC1n1) channels.

When the TM1n count value and the set value of one of the compare registers match, a match interrupt (INTCM1n0, INTCM1n1, INTCC1n0[Note], INTCC1n1[Note]) is output.

Note This match interrupt is generated when CC1n0 and CC1n1 are set to the compare register mode.

(iv) Capture function

TM1n connects two capture/compare register (CC1n0, CC1n1) channels.

When CC1n0 and CC1n1 are set to the capture register mode, the value of TM1n is captured in synchronization with the corresponding capture trigger signal.

When the TM1n is set to the capture register mode, a capture interrupt (INTCC1n0, INTCC1n1) is generated upon detection of the valid edge.

(d) Operation in UDC mode B

(i) Basic operation

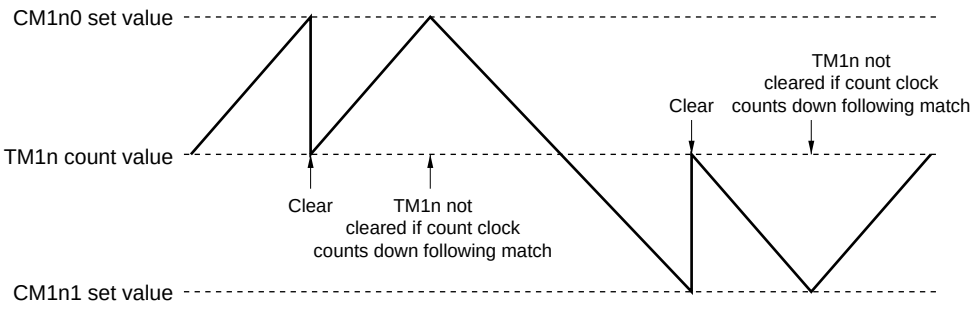
The operations at the next count clock after the count value of TM1n and the CM1n0 set value match when TM1n is in UDC mode B are as follows.

- In case of up count operation: TM1n is cleared (0000H) and the INTCM1n0 interrupt is generated.
- In case of down count operation: The TM1n count value is decremented (–1).

The operations at the next count clock after the count value of TM1n and the CM1n1 set value match when TM1n is in UDC mode B are as follows.

- In case of up count operation: The TM1n count value is incremented (+1).
- In case of down count operation: TM1n is cleared (0000H) and the INTCM1n1 interrupt is generated.

Figure 9-71. Example of TM1n Operation in UDC Mode



Remark n = 0, 1

(ii) Compare function

TM1n connects two compare register (CM1n0, CM1n1) channels and two capture/compare register (CC1n0, CC1n1) channels.

When the TM1n count value and the set value of one of the compare registers match, a match interrupt (INTCM1n0 (only during up count operation), INTCM1n1 (only during down count operation), INTCC1n0[Note], INTCC1n1[Note]) is output.

Note This match interrupt is generated when CC1n0 and CC1n1 are set to the compare register mode.

(iii) Capture function

TM1n connects two capture/compare register (CC1n0, CC1n1) channels.

When CC1n0 and CC1n1 are set to the capture register mode, the value of TM1n is captured in synchronization with the corresponding capture trigger signal.

When the TM1n is set to the capture register mode, a capture interrupt (INTCC1n0, INTCC1n1) is generated upon detection of the valid edge.

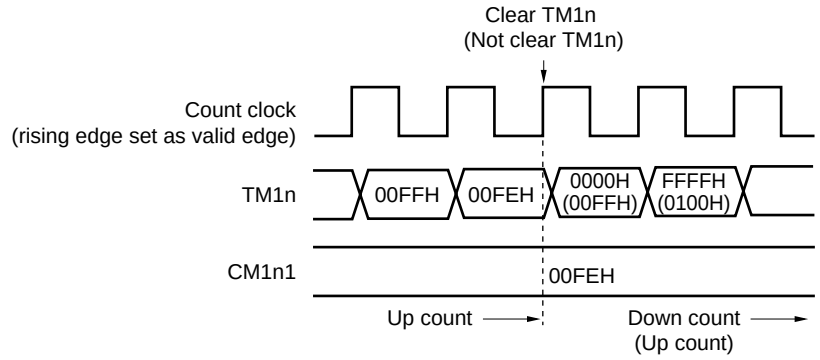
9.2.6 Supplementary description of internal operation

(1) Clearing of count value in UDC mode B

When TM1n is in UDC mode B, the count value clear operation is as follows.

- In case of TM1n up count operation: TM1n is cleared upon match with CM1n0
- In case of TM1n down count operation: TM1n is cleared upon match with CM1n1

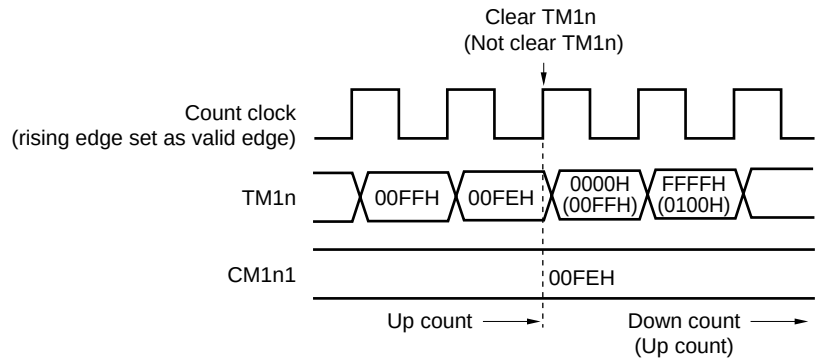
Figure 9-72. Clear Operation upon Match with CM1n0 During TM1n Up Count Operation



Remarks 1. n = 0, 1

2. Items between parentheses in the above figure apply to down count operation.

Figure 9-73. Clear Operation upon Match with CM1n1 During TM1n Down Count Operation



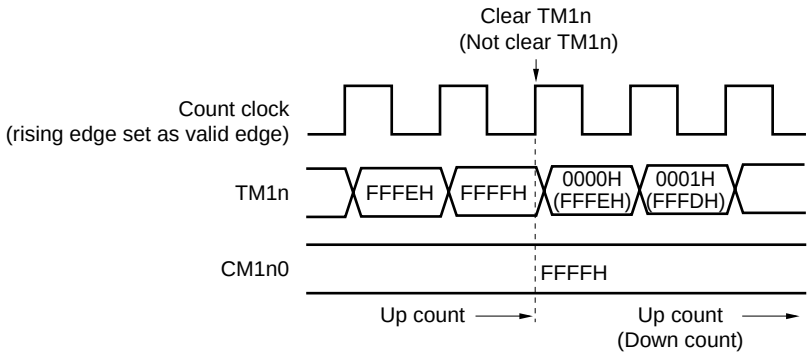
Remarks 1. n = 0, 1

2. Items between parentheses in the above figure apply to up count operation.

(2) Clearing of count value upon occurrence of compare match

The internal operation during TM1n clear operation upon occurrence of a compare match is as follows.

Figure 9-74. Count Value Clear Operation upon Compare Match



Caution The operations at the next count clock after the count value of TM1n and the CM1n0 set value match are as follows.

- **In case of up count: Clear operation is performed.**
- **In case of down count: Clear operation is not performed.**

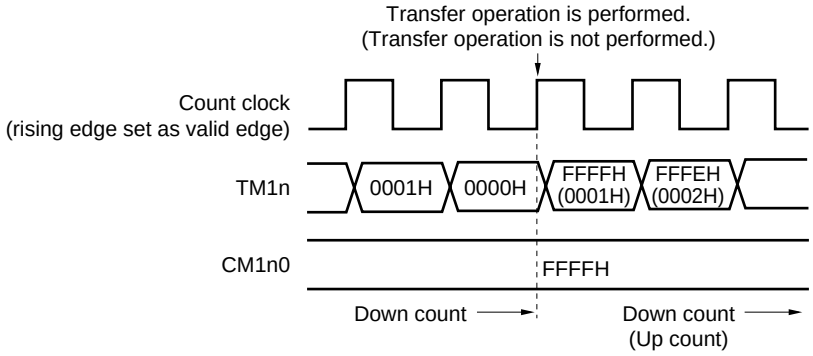
Remarks 1. n = 0, 1

2. Items between parentheses in the above figure apply to down count operation.

(3) Transfer operation

The internal operation during TM1n transfer operation is as follows.

Figure 9-75. Internal Operation During Transfer Operation



Caution The count operations after the TM1n count value becomes 0000H are as follows.

- **In case of down count: Transfer operation is performed.**
- **In case of up count: Transfer operation is not performed.**

Remarks 1. n = 0, 1

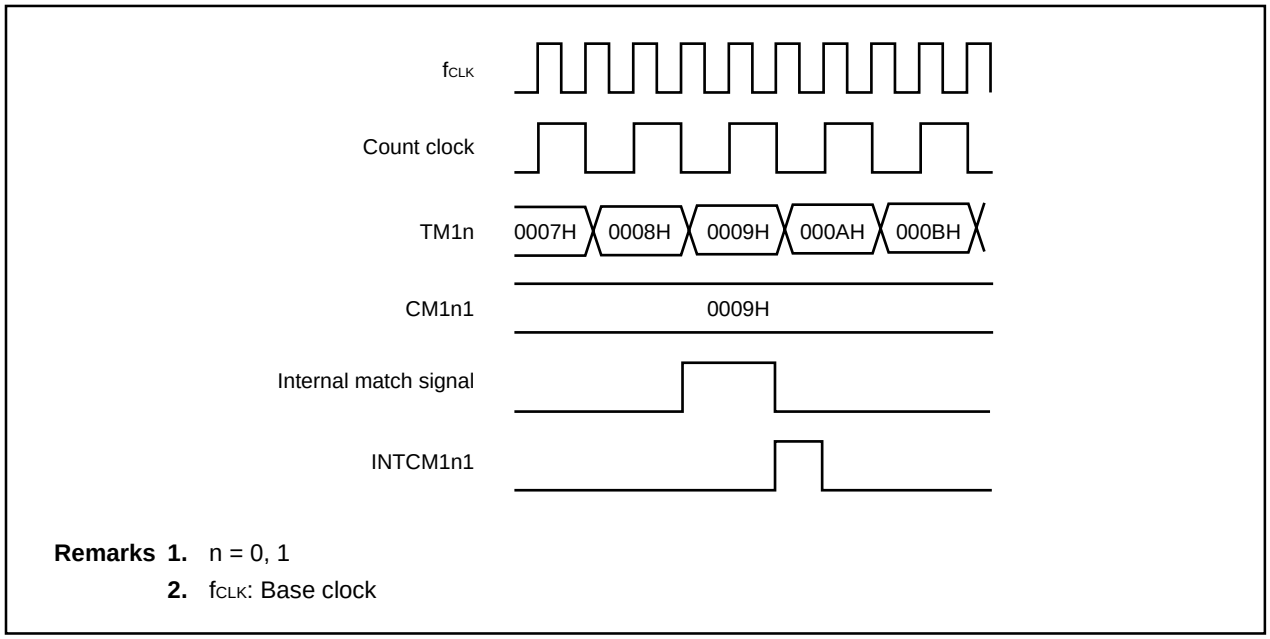
2. Items between parentheses in the above figure apply to up count operation.

(4) Interrupt signal output upon compare match

An interrupt signal is output when the count value of TM1n matches the set value of the CM1n0, CM1n1, CC1n0[Note], or CC1n1[Note] register. The interrupt generation timing is as follows.

Note When CC1n0 and CC1n1 are set to the compare register mode.

Figure 9-76. Interrupt Output upon Compare Match
(CM1n1 with Operation Mode Set to General-Purpose Timer Mode and Count Clock Set to $f_{CLK}/2$)



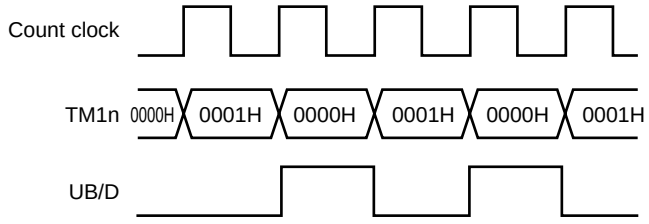
Remarks 1. n = 0, 1
2. f_{CLK}: Base clock

An interrupt signal such as illustrated in Figure 9-76 is output at the next count following match of the TM1n count value and the set value of a corresponding compare register.

(5) UB/D flag (bit 0 of STATUSn register) operation

In the UDC mode (CMD bit of TUMn register = 1), the UB/D flag changes as follows during TM1n up/down count operation at every internal operation clock.

Figure 9-77. UB/D Flag Operation



Remark n = 0, 1

9.3 Timer 2

9.3.1 Features (timer 2)

Timers 20, 21 (TM20, TM21) are 16-bit general-purpose timer units that perform the following operations.

- Pulse interval or frequency measurement and programmable pulse output
- Interval timer
- PWM output timer
- 32-bit capture timer when 2 timer counter channels are connected in cascade
  (In this case, four 32-bit capture register channels can be used.)

9.3.2 Function overview (timer 2)

- 16-bit timer/counter (TM20, TM21): 2 channels
- Bit length
  Timer 2 registers (TM20, TM21): 16 bits
  During cascade operation: 32 bits (higher 16 bits: TM21, lower 16 bits: TM20)
- Capture/compare register
  In 16-bit mode: 6
  In 32-bit mode: 4 (capture mode only)
- Count clock division selectable by prescaler (maximum frequency of count clock: 8 MHz)
- Base clock (f_{CLK}): 2 types (maximum frequency of f_{CLK}: 16 MHz)
  ϕ/2 and ϕ/4 can be selected
- Prescaler divide ratio
  The following divide ratios can be selected according to the base clock (f_{CLK}).

Divide Ratio	Base Clock (f_{CLK})	
	ϕ/2 Selected	ϕ/4 Selected
1/2	ϕ/4	ϕ/8
1/4	ϕ/8	ϕ/16
1/8	ϕ/16	ϕ/32
1/16	ϕ/32	ϕ/64
1/32	ϕ/64	ϕ/128
1/64	ϕ/128	ϕ/256
1/128	ϕ/256	ϕ/512

- Interrupt request sources
  - Compare-match interrupt request: 6 types
    Perform comparison with sub-channel n capture/compare register and generate the INTCC2n interrupt upon compare match.
  - Timer counter overflow interrupt request: 2 types
    The INTTM20 (INTTM21) interrupt is generated when the count value of TM20 (TM21) becomes FFFFH.
- Capture request
  The count values of TM20, TM21 can be latched using external pin (INTP2n)[Note 1, Note 2], TM10, TM11 interrupt signals (INTCM100, INTCM101) and interrupt requests by software as capture triggers.
- PWM output function
  Control of the outputs of pins TO20 through TO23 in the compare mode and PWM output can be performed using the compare match timing of sub-channels 1 to 4 and the zero count signal of the timer counter.
- Timer count operation with external clock input[Note 2]
  Timer count operation can be performed with the pin TI2 clock input signal.
- Timer count enable operation[Note 3] with external pin input[Note 2]
  Timer count enable operation can be performed with the TCLR2 pin input signal.
- Timer counter clear control[Note 3, Note 4] with external pin input[Note 2]
  Timer counter clear operation can be performed with the TCLR2 pin input signal.
- Up/down count control[Note 3, Note 5] with external pin input[Note 2]
  Up/down count operation in the compare mode can be controlled with the TCLR2 pin input signal.
- Output delay operation
  A clock-synchronized output delay can be added to the output signal of pins TO20 through TO23.
  This is effective as an EMI countermeasure.
- Input filter
  An input filter can be inserted at the input stage of external pins (TI2, INTP20 through INTP25, TCLR2) and the TM10, TM11 interrupt signals (Refer to **Figure 14-47**).

Notes 1. For the registers used to specify the valid edge for external interrupt requests (INTP20 through INTP25) to timer 2, refer to **7.3.8 (4) Timer 2 input filter mode registers 0 to 5 (FEM0 to FEM5)**.

2. The pairs TI2 and INTP20, TO21 and INTP21, TO22 and INTP22, TO23 and INTP23, TO24 and INTP24, TCLR2 and INTP25 are each alternate function pins.

3. The count enable operation for the timer counter through external pin input, timer counter clear operation, and up/down count control cannot be performed combined all at the same time.

4. In the case of 32-bit cascade connection, clear operation by external pin input (TCLR2) cannot be performed.

5. Up/down count control using 32-bit cascade connection cannot be performed.

Remark ϕ : Internal system clock
n = 0 to 5

9.3.3 Basic configuration

The basic configuration is shown below.

Table 9-8. Timer 2 Configuration List

Timer	Count Clock		Register	Read/Write	Generated Interrupt Signal	Capture Trigger	Timer Output[Note 3] S/R	Other Functions
	Note 1	**Note 2**						
Timer 2	ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256	ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256, ϕ/512	TM20	–	INTTM20	–	**Note 4**	**Note 5**
			TM21	–	INTTM21	–	**Note 4**	**Note 5**
			CVSE00	Read/write	INTCC20	INTP20/INTP25	–	–
			CVSE10	Read/write	–	INTP21/INTP24	TO20[Note 6]/ TO23[Note 6]	Buffer/**Note 7**
			CVSE20	Read/write	–	INTP22/INTP23	TO21[Note 6]/ TO20[Note 6]	Buffer/**Note 7**
			CVSE30	Read/write	–	INTP23/INTP22	TO22[Note 6]/ TO21[Note 6]	Buffer/**Note 7**
			CVSE40	Read/write	–	INTP24/INTP21	TO23[Note 6]/ TO22[Note 6]	Buffer/**Note 7**
			CVSE50	Read/write	INTCC25	INTP25/INTP20	–	–
			CVPE40	Read	INTCC24	INTP24/INTP21	TO23/TO22	**Note 7**
			CVPE30	Read	INTCC23	INTP23/INTP22	TO22/TO21	**Note 7**
			CVPE20	Read	INTCC22	INTP22/INTP23	TO21/TO20	**Note 7**
			CVPE10	Read	INTCC21	INTP21/INTP24	TO20/TO23	**Note 7**

Notes 1. When ϕ/2 is selected as the base clock input to TM2n

2. When ϕ/4 is selected as the base clock input to TM2n

3. Refer to OTMEn1, OTMEn0 bits in **9.3.4 (6) Timer 2 output control register (OCTLE0)**

4. Reset operation by zero count signal is enabled.

5. Cascade operation with TM20 and TM21 is enabled.

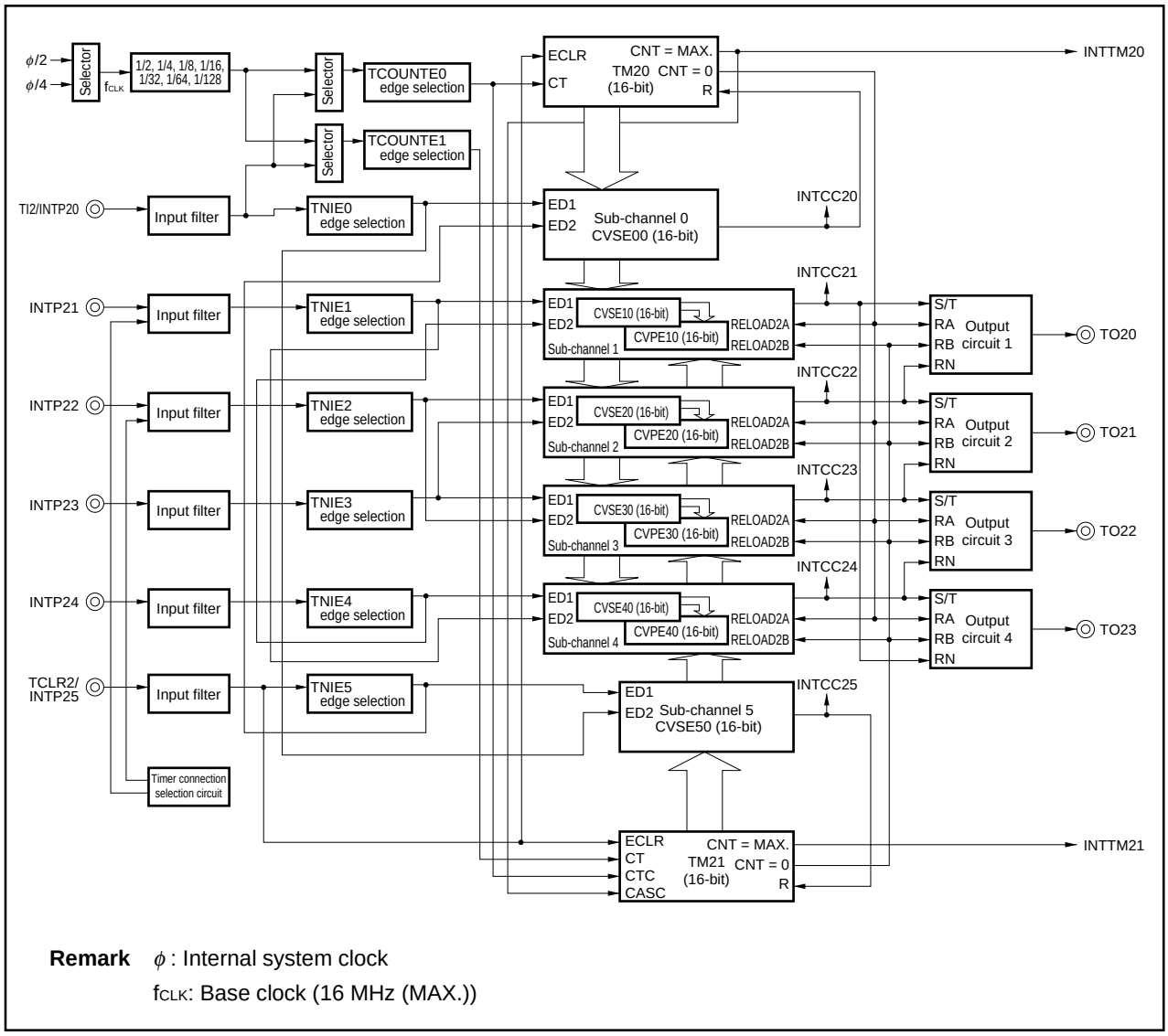
6. Only in buffer-less mode (BFEEy bit of CMSEm0 register = 0)
(m = 12, 34; y: When m = 12, y = 1, 2, and when m = 34, y = 3, 4)

7. Cascade operation using the CVSEn0 register and CVPEn0 register is enabled.

Remark ϕ: Internal system clock
S/R: Set/Reset

Figure 9-78 shows the block diagram of timer 2.

Figure 9-78. Block Diagram of Timer 2



Remark ϕ : Internal system clock

f_{CLK}: Base clock (16 MHz (MAX.))

Table 9-9. Meaning of Signals in Block Diagram

Signal Name	Meaning
CASC[Note 1]	TM21 count signal input in 32-bit mode
CNT	Count value of timer 2 (CNT = MAX.: Maximum value count signal output of timer 2 (generated when TM2n = FFFFH), CNT = 0: Zero count signal output of timer 2 (generated when TM2n = 0000H))
CT	TM2n count signal input in 16-bit mode
CTC	TM21 count signal input in 32-bit mode
ECLR	External control signal input from TCLR2 input
ED1, ED2	Capture event signal input from edge selection circuit
R[Note 2]	Compare match signal input (sub-channel 0/5)
RA	TM20 zero count signal input (reset signal of output circuit)
RB	TM21 zero count signal input (reset signal of output circuit)
RELOAD2A	TM20 zero count signal input (generated when TM20 = 0000H)
RELOAD2B	TM21 zero count signal input (generated when TM21 = 0000H)
RN	Sub-channel x interrupt signal input (reset signal of output circuit)
S/T	Sub-channel x interrupt signal input (set signal of output circuit)
TCOUNTE0, TCOUNTE1	Timer 2 count enable signal input
TNIEm	Timer 2 sub-channel m capture event signal input

Notes 1. TM21 performs count operation when CASC (CNT = MAX. for TM20) is generated and the rising edge of CTC is detected in the 32-bit mode.

2. TM20/TM21 clear by sub-channel 0/5 compare match or count direction can be controlled.

Remark m = 0 to 5
n = 0, 1
x = 1 to 4

(1) Timers 20, 21 (TM20, TM21)

The features of TM2n are listed below.

- Free-running counter that enables counter clearing by compare match of sub-channel 0 and sub-channel 5
- Can be used as a 32-bit capture timer when TM20 and TM21 are connected in cascade.
- Up/down control, counter clear, and count operation enable/disable can be controlled with external pin (TCLR2)
- Counter up/down and clear operation control method can be set by software.
- Stop upon occurrence of count value 0 and count operation start/stop can be controlled by software.

(2) Timer 2 sub-channel 0 capture/compare register (CVSE00)

The CVSE00 register is a 16-bit capture/compare register of sub-channel 0.

In the capture register mode, it captures the TM20 count value.

In the compare register mode, it detects match with TM20.

This register can be read/written in 16-bit units.

Figure 9-79. Timer 2 Sub-Channel 0 Capture/Compare Register (CVSE00)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CVSE00																	FFFFF660H	0000H

(3) Timer 2 sub-channel n main capture/compare register (CVPEn0) (n = 1 to 4)

The CVPEn0 register is a sub-channel n 16-bit main capture/compare register.

In the capture register mode, this register captures the value of TM21 when the BFEEn bit of the CMSEm0 register = 0 (m = 12, 34). When the BFEEn bit = 1, this register holds the value of TM20 or TM21.

If the capture register mode is selected in the 32-bit mode (value of TB1En, TB0En bits of CMSEm0 register = 11B), this register captures the contents of TM21 (higher 16 bits).

This register is read-only in 16-bit units.

Figure 9-80. Timer 2 Sub-Channel n Main Capture/Compare Register (CVPEn0) (n = 1 to 4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CVPE10																	FFFFF652H	0000H
CVPE20																	FFFFF656H	0000H
CVPE30																	FFFFF65AH	0000H
CVPE40																	FFFFF65EH	0000H

(4) Timer 2 sub-channel n sub capture/compare register (CVSEn0) (n = 1 to 4)

The CVSEn0 register is a sub-channel n 16-bit sub capture/compare register.

In the compare register mode, this register can be used as a buffer. In the capture register mode, this register captures the value of TM20 when the BFEEn bit of the CMSEm0 register = 0 (m = 12, 34).

If the capture register mode is selected in the 32-bit mode (value of TB1En and TB0En bits of CMSEm0 register = 11B), this register captures the contents of TM20 (lower 16 bits).

The CVSEn0 register can be written only in the compare register mode. If this register is written in the capture register mode, the contents written to CVSEn0 register will be lost.

This register can be read/written in 16-bit units.

Figure 9-81. Timer 2 Sub-Channel n Sub Capture/Compare Register (CVSEn0) (n = 1 to 4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CVSE10																	FFFFF650H	0000H
CVSE20																	FFFFF654H	0000H
CVSE30																	FFFFF658H	0000H
CVSE40																	FFFFF65CH	0000H

(5) Timer 2 sub-channel 5 capture/compare register (CVSE50)

The CVSE50 register is a sub-channel 5 16-bit capture/compare register.

In the capture register mode, it captures the count value of TM21.

In the compare register mode, it detects match with TM21.

This register can be read/written in 16-bit units.

Figure 9-82. Timer 2 Sub-Channel 5 Capture/Compare Register (CVSE50)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CVSE50																	FFFFF662H	0000H

9.3.4 Control registers

(1) Timer 1n/timer 2n clock selection register (PRM02)

The PRM02 register is used to select the base clock (f_{CLK}) of timer 1 (TM1n) and timer 2 (TM2n).

This register can be read/written in 8- or 1-bit units.

Caution Always set this register before using timer 1 and timer 2.

Figure 9-83. Timer 1n/Timer 2n Clock Selection Register (PRM02)

	7	6	5	4	3	2	1	0	Address	Initial Value
PRM02	0	0	0	0	0	0	0	PRM2	FFFFF5D8H	00H

Bit Position	Bit Name	Function
0	PRM2	Specifies the base clock of timer 1 (TM1n) and timer 2 (TM2n). 0: ϕ/4 (when ϕ > 32 MHz) 1: ϕ/2 (when $\phi \leq$ 32 MHz)

Remark ϕ: Internal system clock

n = 0, 1

(2) Timer 2 clock stop register (STOPTE0)

The STOPTE0 register is used to stop the operation clock input to TM2n (n = 0, 1).

This register can be read/written in 16-, 8-, or 1-bit units.

Figure 9-84. Timer 2 Clock Stop Register (STOPTE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
STOPTE0	STFTE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FFFFF640H	0000H

Bit Position	Bit Name	Function
15	STFTE	Stops the operation clock to TM2n. 0: Normal operation 1: Stop operation clock to TM2n

Cautions 1. Initialize TM2n when the STFTE bit = 0. TM2n cannot be initialized when the STFTE bit = 1.

2. If, following initialization, the value of the STFTE bit is made "1", the initialized state is maintained.

Remark n = 0, 1

(3) Timer 2 count clock/control edge selection register (CSE0)

The CSE0 register is used to specify the TM2n count clock and the control valid edge.

This register can be read/written in 16-, 8-, or 1-bit units.

Figure 9-85. Timer 2 Count Clock/Control Edge Selection Register (CSE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CSE0	0	0	0	0	TES1E1	TES1E0	TES0E1	TES0E0	CESE1	CESE0	CSE12	CSE11	CSE10	CSE02	CSE01	CSE00	FFFFF642H	0000H

Bit Position	Bit Name	Function
11, 10, 9, 8	TESnE1, TESnE0	Specifies the valid edge of the TM2n internal count clock (TCOUNTEn) signal.
7, 6	CESE1, CESE0	Specifies the valid edge of the TM2n external clear input (TCLR2).
5 to 3, 2 to 0	CSEn2, CSEn1, CSEn0	Selects internal count clock of TM2n.

TESnE1	TESnE0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

CESE1	CESE0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Through input
1	1	Both rising and falling edges

CSEn2	CSEn1	CSEn0	Count Clock
0	0	0	$f_{CLK}/2$
0	0	1	$f_{CLK}/4$
0	1	0	$f_{CLK}/8$
0	1	1	$f_{CLK}/16$
1	0	0	$f_{CLK}/32$
1	0	1	$f_{CLK}/64$
1	1	0	$f_{CLK}/128$
1	1	1	Selects input signal from external clock input pin (TI2) as clock.

Remark n = 0, 1

f_{CLK}: Base clock

(4) Timer 2 sub-channel input event edge selection register (SESE0)

The SESE0 register specifies the valid edge of the external capture signal input (TINEn) for the sub-channel n capture/compare register performing capture (n = 0 to 5).

This register can be read/written in 16-, 8-, or 1-bit units.

Figure 9-86. Timer 2 Sub-Channel Input Event Edge Selection Register (SESE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SESE0	0	0	0	0	IESE51	IESE50	IESE41	IESE40	IESE31	IESE30	IESE21	IESE20	IESE11	IESE10	IESE01	IESE00	FFFFF644H	0000H

Bit Position	Bit Name	Function
11 to 0	IESEn1, IESEn0	Specifies the valid edge of external capture signal input (TINEn) for sub-channel n capture/compare register performing capture.

IESEn1	IESEn0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Remark n = 0 to 5

(5) Timer 2 time base control register (TCRE0)

The TCRE0 register controls the operation of TM2n.

This register can be read/written in 16-, 8-, or 1-bit units.

Caution If ECREn bit = 1 and ECEEn bit = 1 have been set, it is not possible to input an external clear signal (TCLR2) for TM2n. In this case, first set CLREn bit = 1, and then clear TM2n by software (n = 0, 1).

Figure 9-87. Timer 2 Time Base Control Register (TCRE0) (1/3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TCRE0	CASE1	CLRE1	CEE1	ECRE1	ECEE1	OSTE1	UDSE11	UDSE10	0	CLRE0	CEE0	ECRE0	ECEE0	OSTE0	UDSE01	UDSE00	FFFFF646H	0000H

Bit Position	Bit Name	Function
15	CASE1	Specifies 32-bit cascade operation mode for TM21 (TM21 counts upon overflow of TM20 (carry count)). 0: Don't connect in cascade[Note 1] 1: 32-bit cascade operation mode[Notes 2, 3] **Notes 1.** TM21 counts with CT signal input in the count enabled state. **2.** TM21 counts with CTC and CASC signal inputs in the count enabled state. **3.** Only the capture register mode can be used for the capture/compare register. **Caution When CASE1 bit = 1, set the TByE1 and TByE0 bits of the CMSEx0 register to 11 (x = 12, 34, y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4).**
14, 6	CLREn	Specifies software clear for TM2n. 0: Continue TM2n operation 1: Clear (0) TM2n count value **Caution Do not perform the software clear and hardware clear operations simultaneously.**
13, 5	CEEn	Specifies TM2n count operation enable/disable. 0: Stop count operation 1: Enable count operation

Remark n = 0, 1

Figure 9-87. Timer 2 Time Base Control Register (TCRE0) (2/3)

Bit Position	Bit Name	Function
12, 4	ECREn	Specifies TM2n external clear (TCLR2) operation enable/disable through ECLR signal input. 0: Don't enable TM2n external clear (TCLR2) operation 1: Enable TM2n external clear (TCLR2) operation **Cautions 1. In the 32-bit cascade operation mode (CASE1 bit = 1), TM2n external clear operation is not enabled.** **2. If the ECLR signal is input when ECREn = 1, TM2n clear operation is performed after 1 internal count clock set with the CSEn2 through CSEn0 bits of the CSE0 register.**
11, 3	ECEEn	Specifies TM2n count operation enable/disable through ECLR signal input. 0: Don't enable TM2n count operation 1: Enable TM2n count operation **Cautions 1. In the 32-bit cascade operation mode (CASE1 bit = 1), control of the TM2n count operation using ECLR signal input is not enabled.** **2. When the ECEEn bit = 1, always set the CESE1 and CESE0 bits of the CSE0 register to "10" (through input).**

Cautions 1. When clearing is performed with the ECLR signal, the TM2n counter is cleared with a delay of (1 internal count clock set with bits CSEn2 through CSEn0 of the CSE0 register) + 2 base clocks. Therefore, if external clock input is selected as the internal count clock, the counter is not cleared until the external clock (TI2) is input.

2. The ECREn bit and the ECEEn bit cannot be set to "1".

3. If the ECEEn bit is set to "1" and the ECREn bit is set to "0", down count operation cannot be performed.

Remark n = 0, 1

Figure 9-87. Timer 2 Time Base Control Register (TCRE0) (3/3)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>10, 2</td><td>OSTEn</td><td>Specifies stop mode.
0: Don’t stop TM2n count when count value is 0.
1: Stop TM2n count when count value is 0.

Caution When TM2n count stop is cancelled when the OSTE1n bit = 1 (TM2n count is stopped when the count value is 0), TM2n counts up except when the UDSEn1, UDSEn0 bits = 10. The count direction when the UDSEn1, UDSEn0 bits = 10 is determined by the value of ECLR.</td></tr>
<tr><td>9, 8, 1, 0</td><td>UDSEn1,
UDSEn0</td><td>Specifies TM2n up/down count.

<table>
<tr><th>UDSEn1</th><th>UDSEn0</th><th>Count</th></tr>
<tr><td>0</td><td>0</td><td>Perform only up count.
Clear TM2n with compare match signal.</td></tr>
<tr><td>0</td><td>1</td><td>Count up after TM2n has become “0”, and count down after a compare match occurs for sub-channels 0, 5 (triangular wave up/down count).</td></tr>
<tr><td>1</td><td>0</td><td>Selects up/down count according to the ECLR signal input.
Up count when ECLR = 1
Down count when ECLR = 0</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table>
Cautions 1. In the 32-bit cascade operation mode (CASE1 bit = 1), set the UDSEn1, UDSEn0 bits to “00”.
2. When the UDSEn1, UDSEn0 bits = “10”, be sure to set the CESE1, CESE0 bits of the CSE0 register to “10” (through input).
3. When the UDSEn1, UDSEn0 bits = “10”, compare match between TM2n and CVSEx0 has no effect on the TM2n count operation (x: 0 when n = 0, 5 when n = 1).</td></tr>
</table>

Caution When UDSEn1, UDSEn0 = 01 and OSTEn = 1, the counter does not count up when the counter value is “0”. Therefore, when the counter value is “0”, set OSTEn = 0, and after the value of the counter ceases to be “0”, set OSTEn = 1. Also, on the application, change the value of OSTEn from “0” to “1” with the sub-channels 0, 5 interrupt signals.

Remark n = 0, 1

(6) Timer 2 output control register (OCTLE0)

The OCTLE0 register controls timer output from the TO2m pin (m = 0 to 3).

This register can be read/written in 16-, 8-, or 1-bit units.

Figure 9-88. Timer 2 Output Control Register (OCTLE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
OCTLE0	SWFE4	ALVE4	OTME41	OTME40	SWFE3	ALVE3	OTME31	OTME30	SWFE2	ALVE2	OTME21	OTME20	SWFE1	ALVE1	OTME11	OTME10	FFFFF648H	0000H

Bit Position	Bit Name	Function
15, 11, 7, 3	SWFEn	Fixes the TO2m pin output level according to the setting of ALVEn bit. 0: Don't fix output level. 1: When ALVEn = 0, fix output level to low level. When ALVEn = 1, fix output level to high level.
14, 10, 6, 2	ALVEn	Specifies the active level of the TO2m pin output. 0: Active level is high level 1: Active level is low level
13, 12, 9, 8, 5, 4, 1, 0	OTMEn1, OTMEn0	Specifies toggle mode.

OTMEn1	OTMEn0	Toggle Mode
0	0	Toggle mode 0: Reverse output level of TO2m output every time a sub-channel n compare match occurs.
0	1	Toggle mode 1: Upon sub-channel n compare match, set TO2m output to active level, and when TM20 is "0", set TO2m output to inactive level.
1	0	Toggle mode 2: Upon sub-channel n compare match, set TO2m output to active level, and when TM21 is "0", set TO2m output to inactive level.
1	1	Toggle mode 3: Upon sub-channel n compare match, set TO2m output to active level, and upon sub-channel n + 1 compare match, set TO2m output to inactive level (when n = "4", n + 1 becomes "1").

Cautions 1. When the OTMEn1, OTMEn0 bits = 11 (toggle mode 3), if the same output delay operation settings are made when setting bits ODLEn2 to ODLEn0 of the ODELE0 register, two outputs change simultaneously upon 1 sub-channel n compare match.

2. If two or more signals are input simultaneously to the same output circuit, S/T signal input has a higher priority than RA, RB, and RN signal inputs.

Remark m = n – 1

n = 1 to 4

(7) Timer 2 sub-channel 0, 5 capture/compare control register (CMSE050)

The CMSE050 register controls timer 2 sub-channel 0 capture/compare register (CVSE00) and timer 2 sub-channel 5 capture/compare register (CVSE50).

This register can be read/written in 16-bit units.

Figure 9-89. Timer 2 Sub-Channel 0, 5 Capture/Compare Control Register (CMSE050)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CMSE050	0	0	EEVE5	0	LNKE5	CCSE5	0	0	0	0	EEVE0	0	LNKE0	CCSE0	0	0	FFFFF64AH	0000H

Bit Position	Bit Name	Function
13, 5	EEVEn	Enables/disables event detection by sub-channel n capture/compare register. 0: Don't detect events 1: Detect events
11, 3	LNKEn	Specifies capture event signal input from edge selection to ED1 or ED2. 0: In capture register mode, select ED1 signal input. In compare register mode, LNKEn bit has no influence. 1: In capture register mode, select ED2 signal input. In compare register mode, LNKEn bit has no influence.
10, 2	CCSEn	Selects capture/compare register operation mode. 0: Operate in capture register mode. The TM20 and TM21 count statuses can be read with sub-channel 0 and sub-channel 5, respectively. 1: Operate in compare register mode. TM2m is cleared upon detection of match between sub-channel n and TM2m.

Remark m = 0, 1
n = 0, 5

(8) Timer 2 sub-channel 1, 2 capture/compare control register (CMSE120)

The CMSE120 register controls the timer 2 sub-channel n sub capture/compare register (CVSEn0) and the timer 2 sub-channel n main capture/compare register (CVPEn0) (n = 0, 1).

This register can be read/written in 16-bit units.

Figure 9-90. Timer 2 Sub-Channel 1, 2 Capture/Compare Control Register (CMSE120) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CMSE120	0	0	EEVE2	BFEE2	LNKE2	CCSE2	TB1E2	TB0E2	0	0	EEVE1	BFEE1	LNKE1	CCSE1	TB1E1	TB0E1	FFFFF64CH	0000H

Bit Position	Bit Name	Function
13, 5	EEVEn	Enables/disables event detection for CMSE120 register. 0: Don't detect events 1: Detect events
12, 4	BFEEn	Specifies the buffer operation of sub-channel n sub capture/compare register (CVSEn0). 0: Don't use sub-channel n sub capture/compare register (CVSEn0) as buffer. 1: Use sub-channel n sub capture/compare register (CVSEn0) as buffer. **Remarks 1.** The operations in the capture register mode and compare register mode when the sub-channel n sub capture/compare register (CVSEn0) is not used as a buffer are shown below. • In capture register mode: The CPU can read both the master register (CVPEn0) and slave register (CVSEn0). The next event is ignored until the CPU finishes reading the master register. TM20 capture is performed by the slave register, and TM21 capture is performed by the master register. • In compare register mode: The CPU writes to the slave register (CVSEn0), and immediately after, the same contents as those of the slave register are written to the master register (CVPEn0). **2.** The operations in the capture register mode and compare register mode when the sub-channel n sub capture/compare register (CVSEn0) is used as a buffer are shown below. • In capture register mode: When the CPU reads the master register (CVPEn0), the master register updates the value held by the slave register (CVSEn0) immediately before the CPU read operation. When a capture event occurs, the timer counter value at that time is always saved in the slave register. • In compare register mode: The CPU writes to the slave register (CVSEn0) and these contents are transferred to the master register (CVPEn0) set with the LNKEn bits.

Remark n = 1, 2

Figure 9-90. Timer 2 Sub-Channel 1, 2 Capture/Compare Control Register (CMSE120) (2/2)

Bit Position	Bit Name	Function
11, 3	LNKEn	Selects capture event signal input from edge selection and specifies transfer operation in compare register mode. 0: Select ED1 signal input in capture register mode. In the compare register mode, the data of the CVSEn0 register is transferred to the CVPEn0 register upon occurrence of TM2x compare match (TM2x = timer counter selected with bits TB1En, TB0En). 1: Select ED2 signal input in capture register mode. In the compare register mode, the data of the CVSEn0 register is transferred to the CVPEn0 register when the TM2x count value becomes “0” (TM2x = timer counter selected with bits TB1En, TB0En).
10, 2	CCSEn	Selects capture/compare register operation mode. 0: Capture register mode 1: Compare register mode
9, 8, 1, 0	TB1En, TB0En	Sets sub-channel n timer counter.

TB1En	TB0En	Sub-Channel n Timer Counter
0	0	Don’t use sub-channel n.
0	1	Set TM20 to sub-channel n.
1	0	Set TM21 to sub-channel n.
1	1	32-bit mode[Note] (Select both TM20 and TM21.)

Note In the 32-bit mode, influence of the BFEEn bit is ignored. Also, the CVSEn0 register cannot be used as a buffer in this mode.

Caution When the TB1En, TB0En bits are set to “11”, set the CASE1 bit of the TCRE0 register to “1”.

Remark n = 1, 2

(9) Timer 2 sub-channel 3, 4 capture/compare control register (CMSE340)

The CMSE340 register controls the timer 2 sub-channel n sub capture/compare register (CVSEn0) and the timer 2 sub-channel n main capture/compare register (CVPEn0).

This register can be read/written in 16-bit units.

Figure 9-91. Timer 2 Sub-Channel 3, 4 Capture/Compare Control Register (CMSE340) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CMSE340	0	0	EEVE4	BFEE4	LNKE4	CCSE4	TB1E4	TB0E4	0	0	EEVE3	BFEE3	LNKE3	CCSE3	TB1E3	TB0E3	FFFFF64EH	0000H

Bit Position	Bit Name	Function
13, 5	EEVEn	Enables/disables event detection by CMSE340 register. 0: Don't detect events 1: Detect events
12, 4	BFEEn	Specifies the sub-channel n sub capture/compare register (CVSEn0) buffer operation. 0: Don't use sub-channel n sub capture/compare register (CVSEn0) as buffer 1: Use sub-channel n sub capture/compare register (CVSEn0) as buffer **Remarks 1.** The operations in the capture register mode and compare register mode when the sub-channel n sub capture/compare register (CVSEn0) is not used as a buffer are shown below. • In capture register mode: The CPU can read both the master register (CVPEn0) and slave register (CVSEn0). The next event is ignored until the CPU finishes reading the master register. TM20 capture is performed by the slave register, and TM21 capture is performed by the master register. • In compare register mode: The CPU writes to the slave register (CVSEn0), and immediately after, the same contents as those of the slave register are written to the master register (CVPEn0). **2.** The operations in the capture register mode and compare register mode when the sub-channel n sub capture/compare register (CVSEn0) is used as a buffer are shown below. • In capture register mode: When the CPU reads the master register (CVPEn0), the master register updates the value held by the slave register (CVSEn0) immediately before the CPU read operation. When a capture event occurs, the timer counter value at that time is always saved in the slave register. • In compare register mode: The CPU writes to the slave register (CVSEn0) and these contents are transferred to the master register (CVPEn0) set with the LNKEn bits.

Remark n = 3, 4

Figure 9-91. Timer 2 Sub-Channel 3, 4 Capture/Compare Control Register (CMSE340) (2/2)

Bit Position	Bit Name	Function
11, 3	LNKEn	Selects capture event signal input from edge selection and specifies transfer operation in compare register mode. 0: Select ED1 signal input in capture register mode. In the compare register mode, the data of the CVSEn0 register is transferred to the CVPEn register upon occurrence of TM2x compare match (TM2x = timer counter selected with bits TB1En, TB0En). 1: Select ED2 signal input in capture register mode. In the compare register mode, the data of the CVSEn0 register is transferred to the CVPEn register when the TM2x count value becomes “0” (TM2x = timer counter selected with bits TB1En, TB0En).
10, 2	CCSEn	Selects capture/compare register operation mode. 0: Capture register mode 1: Compare register mode
9, 8, 1, 0	TB1En, TB0En	Sets sub-channel n timer counter.

TB1En	TB0En	Sub-Channel n Timer Counter
0	0	Don’t use sub-channel n.
0	1	Set TM20 to sub-channel n.
1	0	Set TM21 to sub-channel n.
1	1	32-bit mode[Note] (Select both TM20 and TM21.)

Note In the 32-bit mode, influence of the BFEEn bit is ignored. Also, the CVSEn register cannot be used as a buffer in this mode.

Caution When the TB1En, TB0En bits are set to “11”, set the CASE1 bit of the TCRE0 register to “1”.

Remark n = 3, 4

(10) Timer 2 time base status register (TBSTATE0)

The TBSTATE0 register indicates the status of TM2n (n = 0, 1).

This register can be read/written in 16-, 8-, or 1-bit units.

Caution The ECFEn, RSFEn, and UDFEn bits are read-only bits.

Figure 9-92. Timer 2 Time Base Status Register (TBSTATE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TBSTATE0	0	0	0	0	OVFE1	ECFE1	RSFE1	UDFE1	0	0	0	0	OVFE0	ECFE0	RSFE0	UDFE0	FFFFF664H	0000H

Bit Position	Bit Name	Function
11, 3	OVFEn	Indicates TM2n overflow status. 0: No overflow 1: Overflow **Caution If write access to the TBSTATE0 register is performed while overflow is not detected, the OVFEn bit is cleared (0).**
10, 2	ECFEn	Indicates the ECLR signal input status. 0: Low level 1: High level
9, 1	RSFEn	Indicates the TM2n count status. 0: TM2n is not counting. 1: TM2n is counting (either up or down)
8, 0	UDFEn	Indicates the TM2n up/down count status. 0: TM2n is in the down count mode. 1: TM2n is in the up count mode.

Remark n = 0, 1

(11) Timer 2 capture/compare 1 to 4 status register (CCSTATE0)

The CCSTATE0 register indicates the status of the timer 2 sub-channel sub capture/compare register (CVSEn0) and the timer 2 sub-channel main capture/compare register (CVPEn0) (n = 1 to 4).

This register can be read/written in 16-, 8-, or 1-bit units.

Caution The BFFEn1 and BFFEn0 bits are read-only bits.

Figure 9-93. Timer 2 Capture/Compare 1 to 4 Status Register (CCSTATE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CCSTATE0	0	CEFE4	BFFE41	BFFE40	0	CEFE3	BFFE31	BFFE30	0	CEFE2	BFFE21	BFFE20	0	CEFE1	BFFE11	BFFE10	FFFFF666H	0000H

Bit Position	Bit Name	Function
14, 10, 6, 2	CEFEn	Indicates the capture/compare event occurrence status. 0: In capture register mode: No capture operation has occurred. In compare register mode: No compare match has occurred. 1: In capture register mode: At least one capture operation has occurred. In compare register mode: At least one compare match has occurred. **Caution The CEFEn bit can be cleared (0) by performing write access to the CCSTATE0 register while no capture operation or compare match occurs. When bit manipulation is performed for the CEFE1 (CEFE3) bit and the CEFE2 (CEFE4) bit, both bits are cleared.**
13, 12, 9, 8, 5, 4, 1, 0	BFFEn1, BFFEn0	Indicates the capture buffer status. BFFEn1 / BFFEn0 / Capture Buffer Status 0 / 0 / No value in buffer 0 / 1 / Sub-channel n master register (CVPEn0) contains a capture value. Slave register (CVSEn0) does not contain a value. 1 / 0 / Both sub-channel n master register (CVPEn0) and slave register (CVSEn0) contain a capture value. 1 / 1 / Unused **Caution The BFFEn1 and BFFEn0 bits return a value only when sub-channel n sub capture/compare register (CVSEn0) buffer operation (bit BFEEn of CMSEm0 register = 1) is selected or when capture register mode (bit CCSEn of CMSEm0 register = 0) is selected. "0" is read when the compare register mode (CCSEn bit = 1) is selected.**

Remark m = 12, 34
n = 1 to 4

(12) Timer 2 output delay register (ODELE0)

The ODELE0 register sets the output delay operation synchronized with the clock to the TO2n pin's output delay circuit.

This register can be read/written in 16-, 8-, or 1-bit units.

Figure 9-94. Timer 2 Output Delay Register (ODELE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ODELE0	0	ODLE42	ODLE41	ODLE40	0	ODLE32	ODLE31	ODLE30	0	ODLE22	ODLE21	ODLE20	0	ODLE12	ODLE11	ODLE10	FFFFF668H	0000H

Bit Position	Bit Name	Function
14 to 12, 10 to 8, 6 to 4, 2 to 0	ODLEn2, ODLEn1, ODLEn0	Specifies output delay operation.

ODLEn2	ODLEn1	ODLEn0	Set Output Delay Operation
0	0	0	Don't perform output delay operation.
0	0	1	Set output delay of 1 system clock.
0	1	0	Set output delay of 2 system clocks.
0	1	1	Set output delay of 3 system clocks.
1	0	0	Set output delay of 4 system clocks.
1	0	1	Set output delay of 5 system clocks.
1	1	0	Set output delay of 6 system clocks.
1	1	1	Set output delay of 7 system clocks.

Remark The ODLEn2, ODLEn1, ODLEn0 bits are used for EMI countermeasures.

Remark n = 1 to 4

(13) Timer 2 software event capture register (CSCE0)

The CSCE0 register sets capture operation by software in the capture register mode.

This register can be read/written in 16-bit units.

Figure 9-95. Timer 2 Software Event Capture Register (CSCE0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
CSCE0	0	0	0	0	0	0	0	0	0	0	SEVE5	SEVE4	SEVE3	SEVE2	SEVE1	SEVE0	FFFFF66AH	0000H

Bit Position	Bit Name	Function
5 to 0	SEVEn	Specifies capture operation by software in capture register mode. 0: Continue normal operation. 1: Perform capture operation. **Cautions 1. The SEVEn bit ignores the settings of the EEVEn and the LNKEn bits of the CMSEm0 register.** **2. The SEVEn bit is automatically cleared (0) at the end of an event.** **3. The SEVEn bit ignores all the internal limitation statuses of the timer 2 unit.**

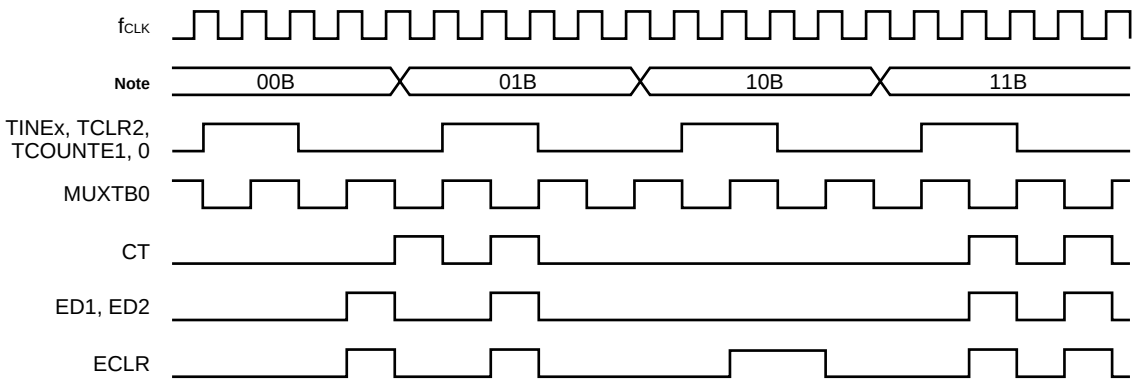
Remark m = 12, 34, 05
n = 0 to 5

9.3.5 Operation

(1) Edge detection

The edge detection timing is shown below.

Figure 9-96. Edge Detection Timing



Note The set values of the TESnE1, TESnE0 bits and the CESE1, CESE0 bits of the CSE0 register, and the IESEn1, IESEn0 bits of the SESE0 register are shown.

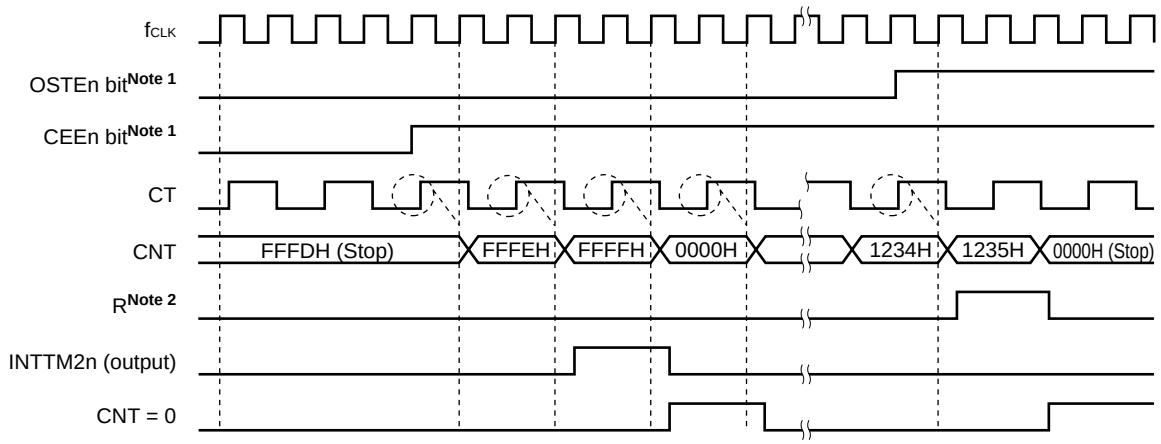
Remarks 1. f_{CLK}: Base clock

2. CT: TM2n count signal input in the 16-bit mode
ECLR: External control signal input from TCLR2 input
ED1, ED2: Capture event signal input from edge selection circuit
MUXTB0: TM20 multiplex signal
TCOUNTE0, TCOUNTE1: Timer 2 count enable signal input
TINEx: Timer 2 sub-channel x capture event signal input (x = 0 to 5)

(2) Basic operation of timer 2

Figures 9-97 to 9-100 show the basic operation of timer 2.

Figure 9-97. Timer 2 Up Count Timing
(When TCRE0 Register's UDSEn1, UDSEn0 Bits = 00B,
ECEEn Bit = 0, ECREn Bit = 0, CLREn Bit = 0, CASE1 Bit = 0)



Notes 1. Bits OSTE, CEE of TCRE0 register

2. Can control TM20/TM21 clear by sub-channel 0/5 compare match or count direction.

Remarks 1. f_{CLK}: Base clock

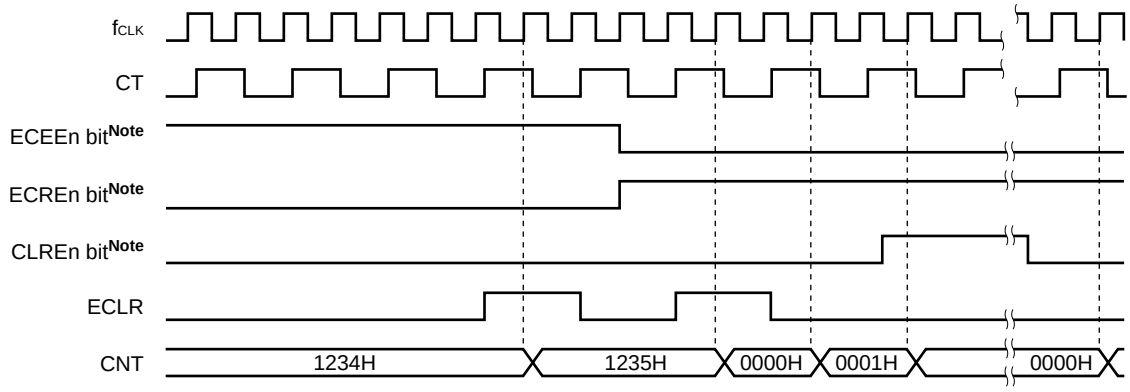
2. CNT: Count value of timer 2

CT: TM2n count signal input in 16-bit mode

R: Compare match signal input (sub-channel 0/5)

3. n = 0, 1

Figure 9-98. External Control Timing of Timer 2 (When TCRE0 Register's UDSEn1, UDSEn0 Bits = 00B, OSTEn Bit = 0, CEEn Bit = 1, CASE1 Bit = 0)



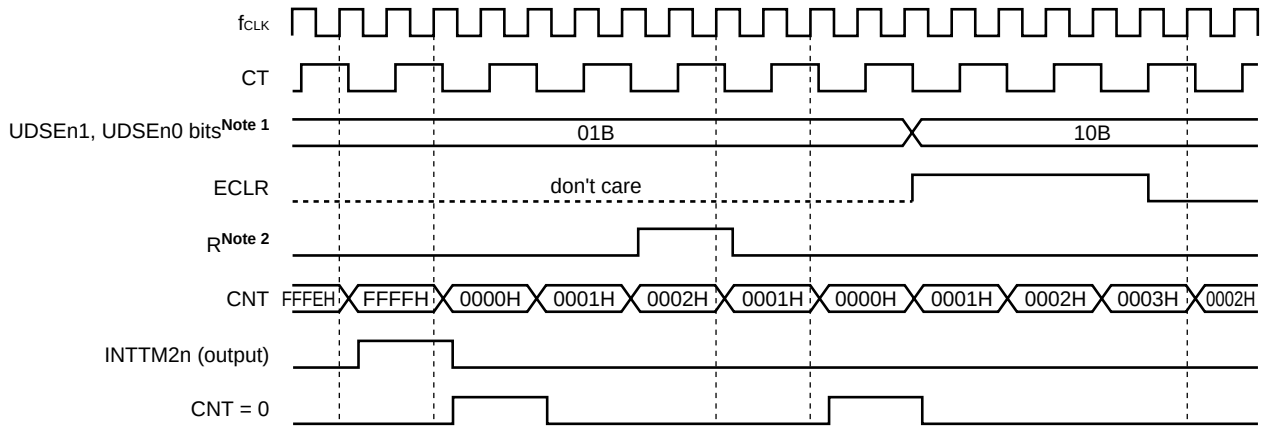
Note Bits ECEEn, ECREn, CLREn of TCRE0 register

Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2
CT: TM2n count signal input in 16-bit mode
ECLR: External control signal input from TCLR2 pin input

3. n = 0, 1

Figure 9-99. Operation in Timer 2 Up/Down Count Mode (When TCRE0 Register's ECEEn bit = 0, ECREn Bit = 0, CLREn Bit = 0, OSTEn Bit = 0, CEEn Bit = 1, CASE1 Bit = 0)



Notes 1. UDSEn1, UDSEn0 bits of TCRE0 register

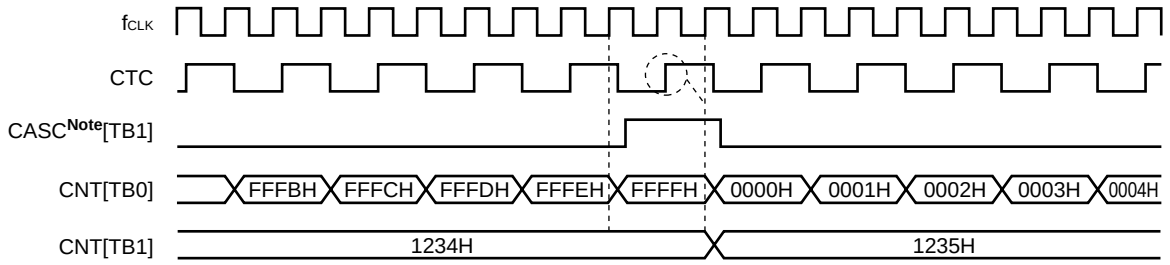
2. Can control TM20/TM21 clear by sub-channel 0/5 compare match or count direction.

Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2
CT: TM2n count signal input in 16-bit mode
ECLR: External control signal input from TCLR2 pin input
R: Compare match signal input (sub-channel 0/5)

3. n = 0, 1

Figure 9-100. Timing in 32-Bit Cascade Operation Mode (When TCRE0 Register's UDSEn1, UDSEn0 Bits = 00B, ECEEn Bit = 0, ECREn Bit = 0, CLREn Bit = 0, OSTEn Bit = 0, CEEn Bit = 1, CASE1 Bit = 1)



Note If, in the 32-bit mode, CASC (CNT = MAX for TM20) is input to TM21 and the CTC rising edge is detected, TM21 performs count operation.

Remarks 1. f_{CLK}: Base clock

2. CASC: TM21 count signal input in 32-bit mode
CNT: Count value of timer 2
CTC: TM21 count signal input in 32-bit mode
TB0: Count value of TM20
TB1: Count value of TM21

3. n = 0, 1

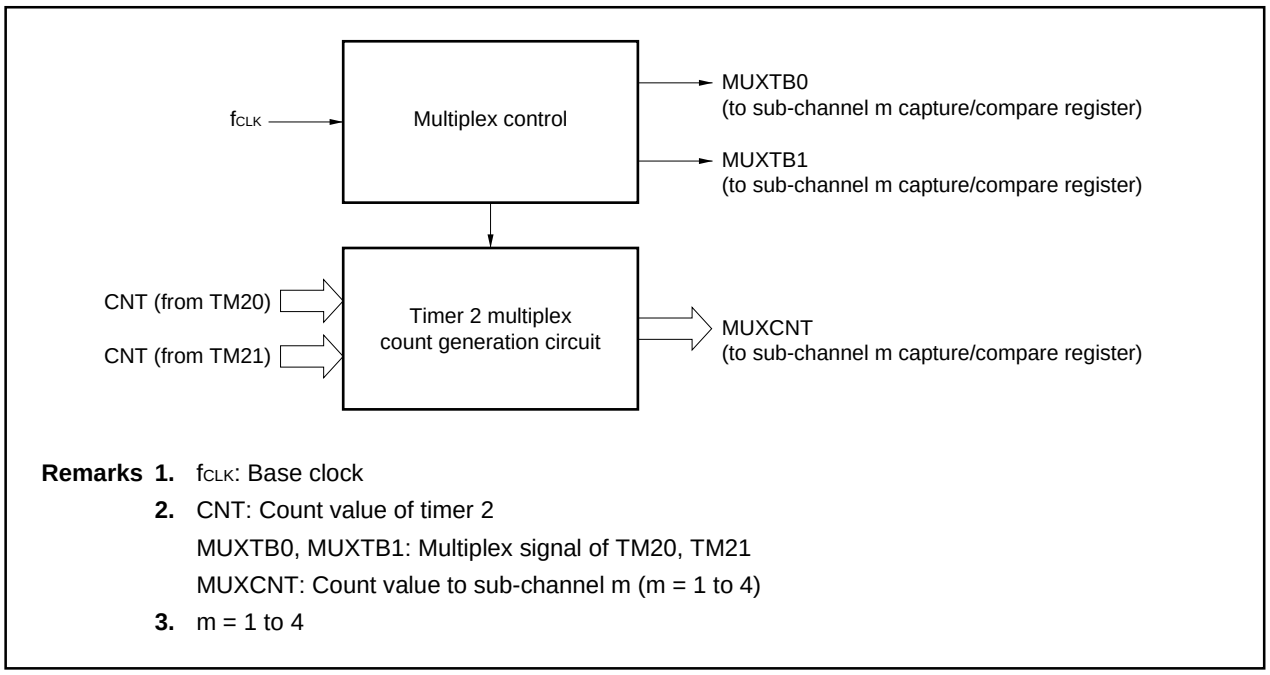
(3) Operation of capture/compare register (sub-channels 1 to 4)

Sub-channels 1 to 4 receive the count value of the timer 2 multiplex count generation circuit.

The multiplex count generation circuit is an internal unit of TM2n that supplies the multiplex count value MUXCNT to sub-channels 1 to 4. The count value of TM20 is output to sub-channels 1 to 4 at the rising edge of MUXTB0, and the count value of TM21 is output to sub-channels 1 to 4 at the rising edge of MUXTB1.

Figure 9-101 shows the block diagram of the timer 2 multiplex count generation circuit, and Figure 9-102 shows the multiplex count timing.

Figure 9-101. Block Diagram of Timer 2 Multiplex Count Generation Circuit

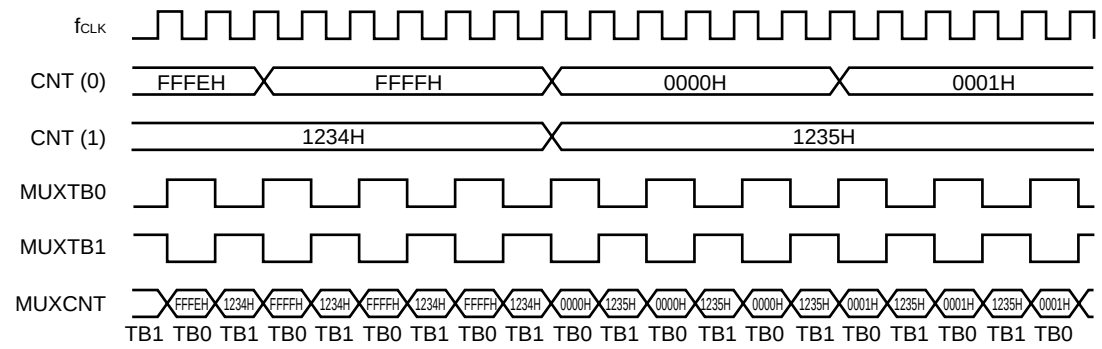


Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
MUXCNT: Count value to sub-channel m (m = 1 to 4)

3. m = 1 to 4

Figure 9-102. Multiplex Count Timing



Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2

MUXTB0, MUXTB1: Multiplex signal of TM20, TM21

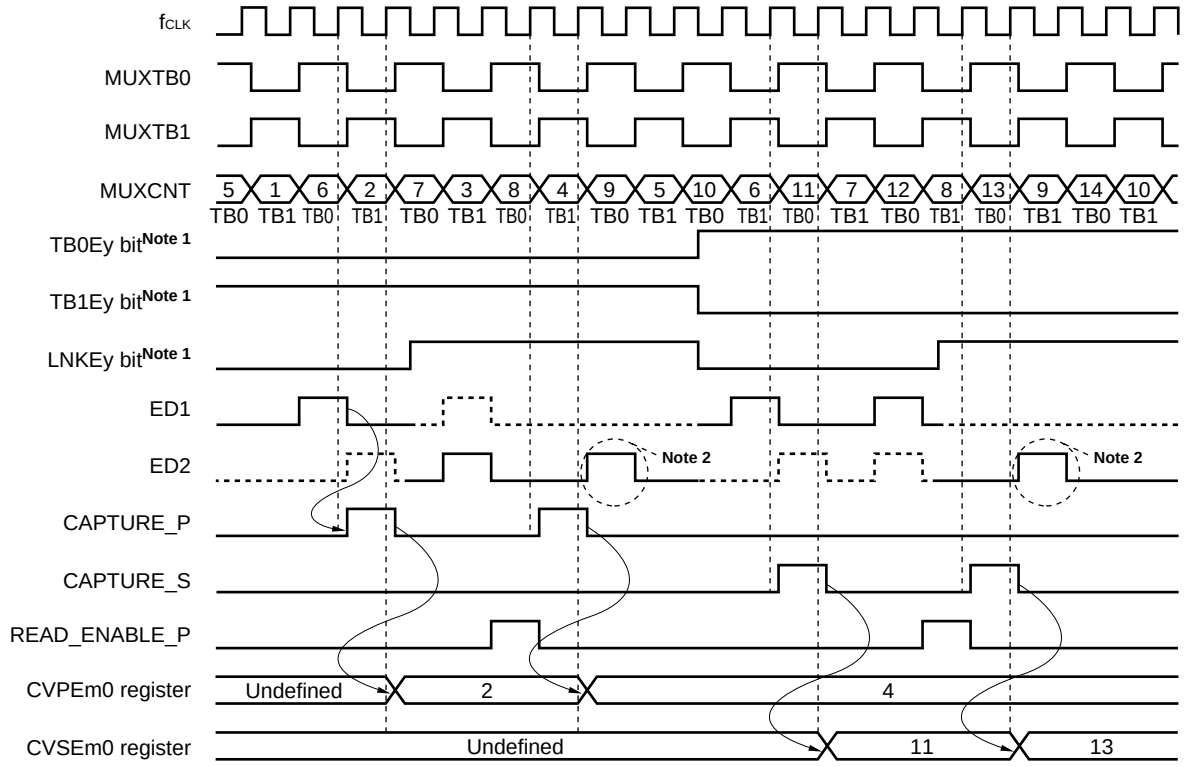
MUXCNT: Count value to sub-channel m (m = 1 to 4)

TB0: Count value of TM20

TB1: Count value of TM21

Figures 9-103 to 9-108 show the operation of the capture/compare register (sub-channels 1 to 4).

Figure 9-103. Capture Operation: 16-Bit Buffer-Less Mode (When Operation Is Delayed Through Setting of LNKEy Bit of CMSEx0 Register, and CMSEx0 Register's CCSEy Bit = 0, BFEEy Bit = 0, EEVEy Bit = 1, and CSCE0 Register's SEVEy Bit = 0)



Notes 1. Bits TB0Ey, TB1Ey of CMSEx register

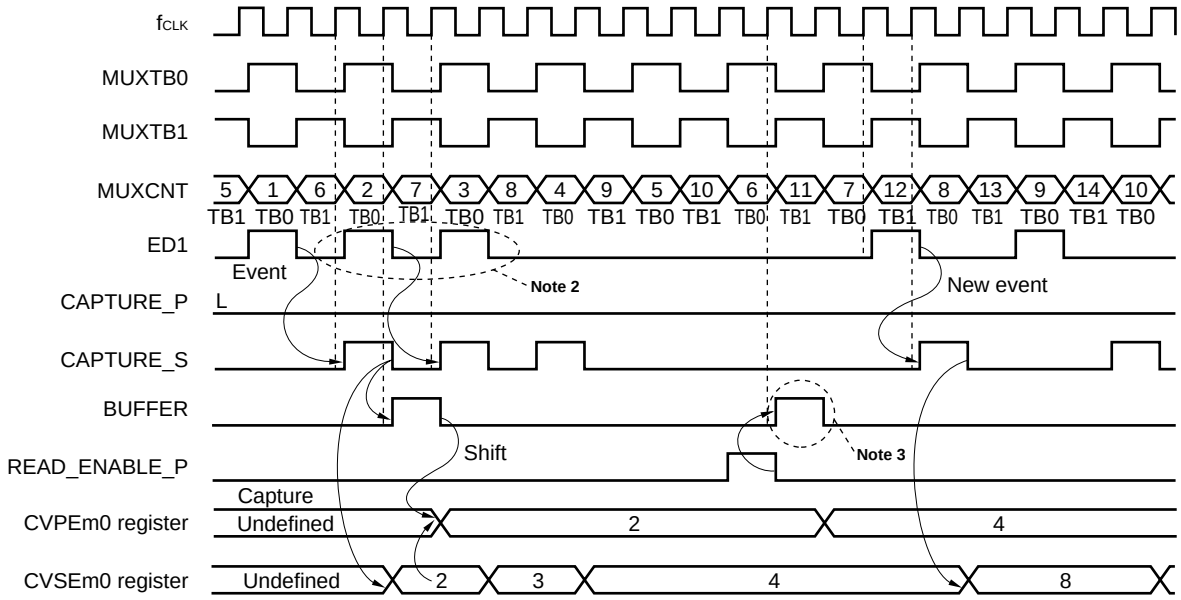
2. If an event occurs in this timing, it is ignored.

Remarks 1. f_{CLK}: Base clock

2. CAPTURE_P: Capture trigger signal of main capture register
CAPTURE_S: Capture trigger signal of sub capture register
ED1, ED2: Capture event signal input from edge selection circuit
MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
READ_ENABLE_P: Read timing for CVPEm0 register (m = 1 to 4)
TB0: Count value of TM20
TB1: Count value of TM21

3. m = 1 to 4, x = 12, 34
y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4

Figure 9-104. Capture Operation: Mode with 16-Bit Buffer[Note 1] (When CMSEx0 Register's TByE1 Bit = 0, TByE0 Bit = 1, CCSEy Bit = 0, LNKEy Bit = 0, BFEEy Bit = 1, EEVEy Bit = 1, and CSCE0 Register's SEVEy Bit = 0)



Notes 1. To operate TM2n in this mode, perform capture at least twice at the start of operation and read the CVPEm0 register. Also, read the CVPEm0 register after performing capture at least once.

2. Write operation to the CVPEn0 register is not performed at these signal inputs because the CVSEm0 register operates as a buffer.

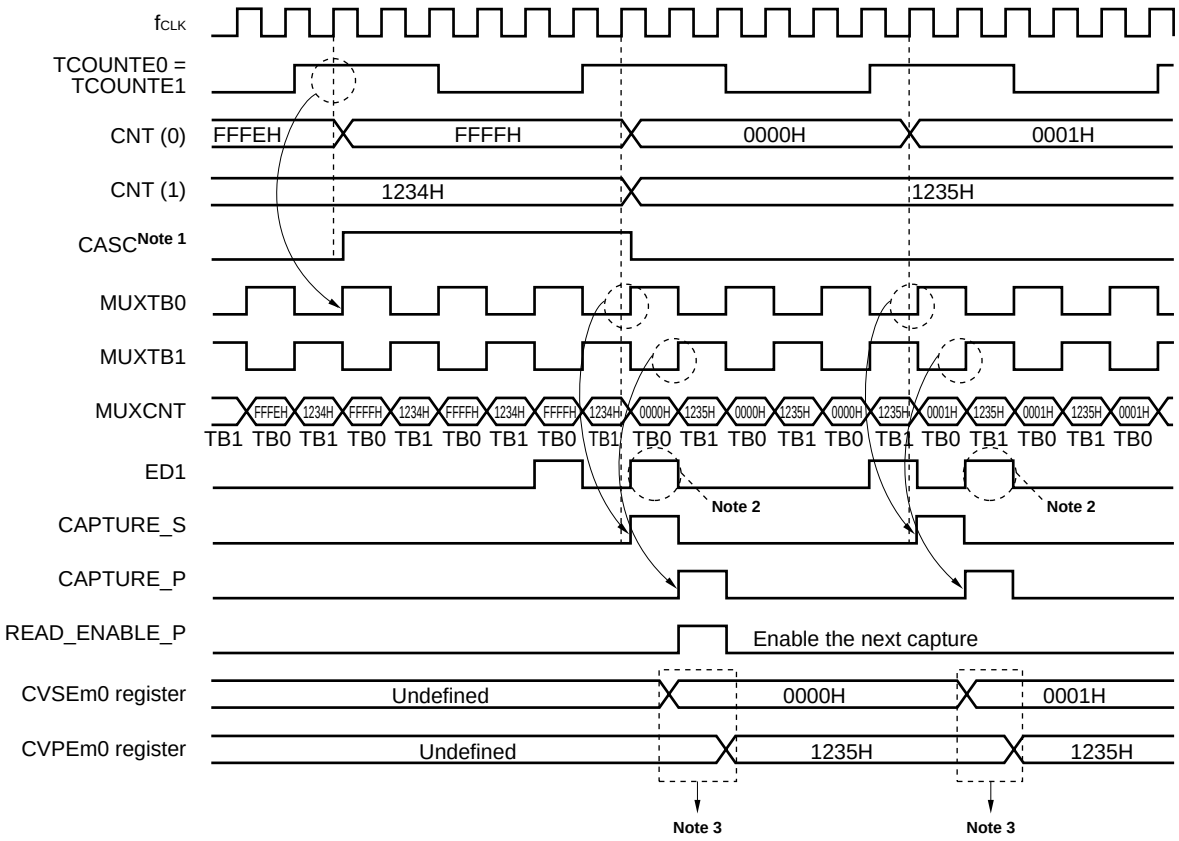
3. After this timing, write operation from the CVSEm0 register to the CVPEm0 register is enabled.

Remarks 1. f_{CLK}: Base clock

2. BUFFER: Timing of write operation from CVSEm0 register to CVPEm0 register
CAPTURE_P: Capture trigger signal of main capture register
CAPTURE_S: Capture trigger signal of sub capture register
ED1: Capture event signal input from edge selection circuit
MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
READ_ENABLE_P: Read timing of CVPEm0 register (m = 1 to 4)
TB0: Count value of TM20; TB1: Count value of TM21

3. m = 1 to 4, x = 12, 34
y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4

Figure 9-105. Capture Operation: 32-Bit Cascade Operation Mode (When CMSEx Register's TByE1 Bit = 1, TByE0 Bit = 1, CCSEy Bit = 0, LNKEy Bit = 0, BFEEy Bit = Arbitrary, EEVEy Bit = 1, and CSCE0 Register's SEVEy Bit = 0)



Notes 1. TM21 performs count operation when, in the 32-bit mode, CASC (CNT = MAX. for TM20) is input to TM21 and the rising edge of CTC is detected.

2. If an event occurs during this timing, it is ignored.

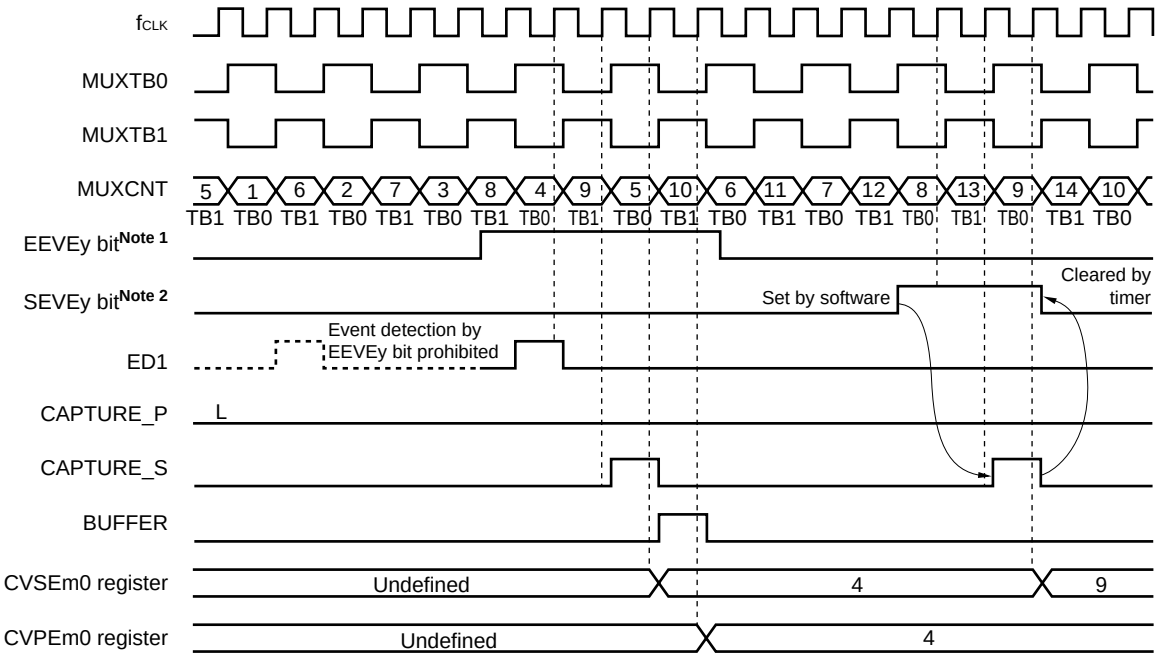
3. CPU read access is not performed in this timing (wait status).

Remarks 1. f_{CLK}: Base clock

2. CAPTURE_P: Capture trigger signal of main capture register
CAPTURE_S: Capture trigger signal of sub capture register
CASC: TM21 count signal in 32-bit mode
CNT: Count value of timer 2
ED1: Capture event signal input from edge selection circuit
MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
READ_ENABLE_P: Read timing of CVPEm0 register (m = 1 to 4)
TB0: Count value of TM20
TB1: Count value of TM21
TCOUNTE0, TCOUNTE1: Count enable signal input of timer 2

3. m = 1 to 4, x = 12, 34
y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4

Figure 9-106. Capture Operation: Capture Control by Software and Trigger Timing (When CMSEx0 Register's TByE1 Bit = 0, TByE0 Bit = 1, CCSEy Bit = 0, LNKEy Bit = 0, BFEEy Bit = 1)



Notes 1. EEVEy bit of CMSEx0 register

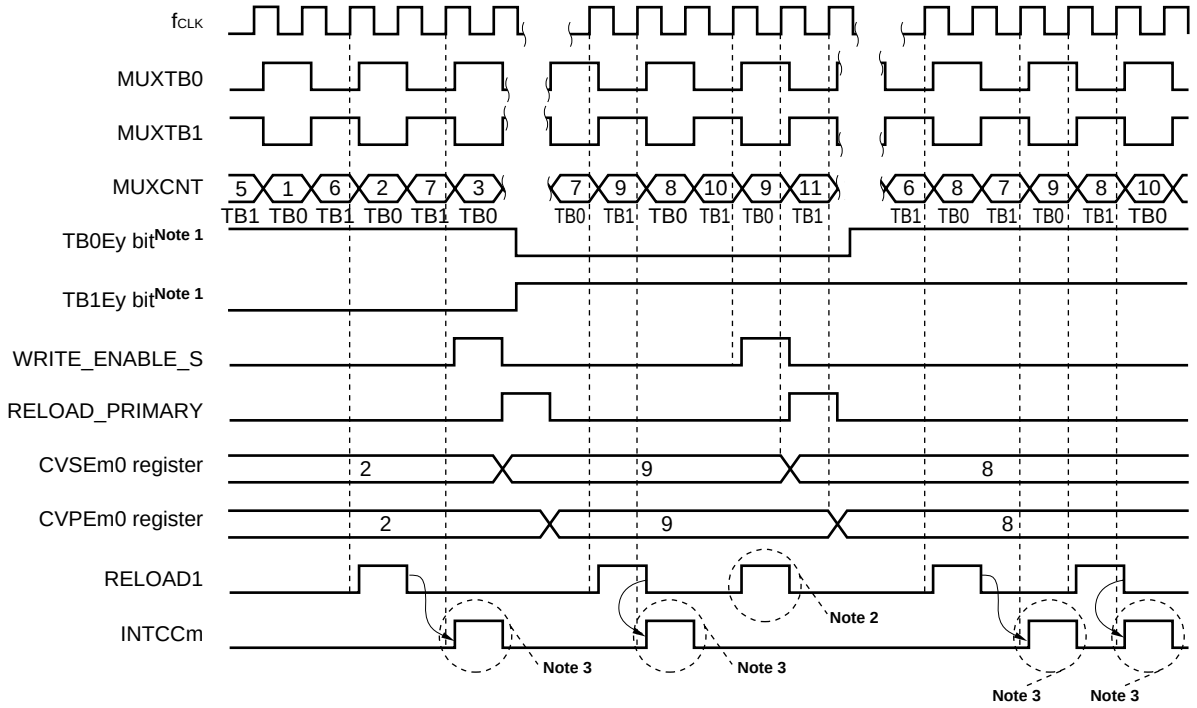
2. SEVEy bit of CSCE0 register

Remarks 1. f_{CLK}: Base clock

2. BUFFER: Timing of write operation from CVSEm0 register to CVPEm0 register
CAPTURE_P: Capture trigger signal of main capture register
CAPTURE_S: Capture trigger signal of sub capture register
ED1: Capture event signal input from edge selection circuit
MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
TB0: Count value of TM20
TB1: Count value of TM21

3. m = 1 to 4, x = 12, 34
y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4

Figure 9-107. Compare Operation: Buffer-Less Mode (When CMSEx0 Register's CCSEy Bit = 1, LNKEy Bit = Arbitrary, BFEEy Bit = 0)



Notes 1. TB1Ey, TB0Ey bits of CMSEx0 register

2. No interrupt is generated due to compare match with counter differing from TB1Ey, TB0Ey bit settings.

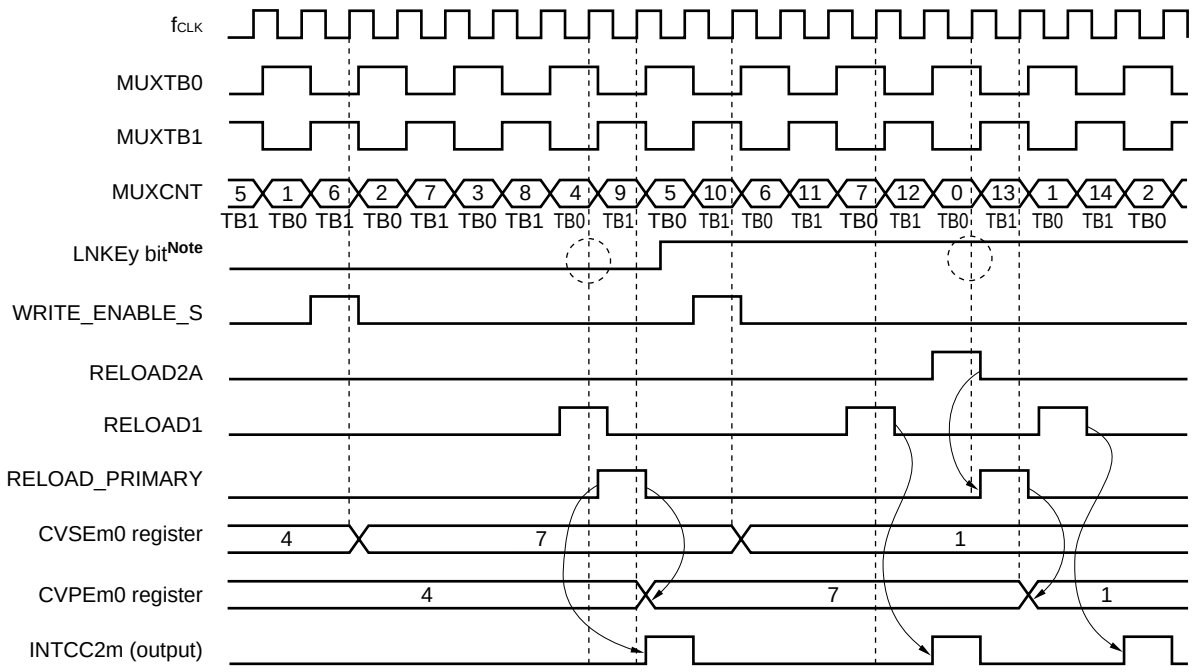
3. INTCC2m is generated to match the cycle from rising edge to falling edge of MUXTB0.

Remarks 1. f_{CLK}: Base clock

2. MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
RELOAD1: Compare match signal
RELOAD_PRIMARY: Timing of write operation from CVSEm0 register to CVPEm0 register
WRITE_ENABLE_S: Timing of CVSEm0 register write operation
TB0: Count value of TM20
TB1: Count value of TM21

3. m = 1 to 4, x = 12, 34

Figure 9-108. Compare Operation: Mode with Buffer (When Operation Is Delayed Through Setting of LNKEy Bit of CMSEx0 Register, CMSEx0 Register's CCSEy Bit = 1, BFEEy Bit = 1)



Note LNKEy bit of CMSEx0 register

Remarks 1. f_{CLK}: Base clock

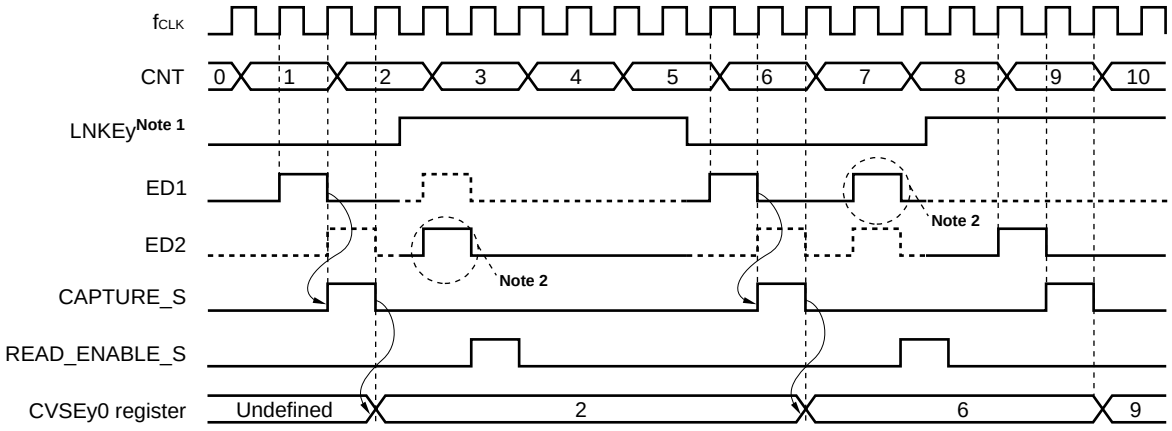
2. MUXCNT: Count value to sub-channel m (m = 1 to 4)
MUXTB0, MUXTB1: Multiplex signal of TM20, TM21
RELOAD1: Compare match signal
RELOAD2A: Zero count signal input of TM20 (occurs when TM20 = 0000H)
RELOAD_PRIMARY: Timing of write operation from CVSEm0 register to CVPEm0 register
WRITE_ENABLE_S: Timing of CVSEm0 register write operation
TB0: Count value of TM20 (In this figure, the maximum count value is 7.)
TB1: Count value of TM21

3. m = 1 to 4, x = 12, 34
y: When x = 12, y = 1, 2, and when x = 34, y = 3, 4

(4) Operation of capture/compare register (sub-channels 0, 5)

Figures 9-109 and 9-110 show the operation of the capture/compare register (sub-channels 0, 5).

Figure 9-109. Capture Operation: Timer 2 Count Value Read Timing (When CMSE050 Register's CCSEy Bit = 0, EEVEy Bit = 1, and CSCE0 Register's SEVEy Bit = 0)



Notes 1. LNKEy bit of CMSE050 register

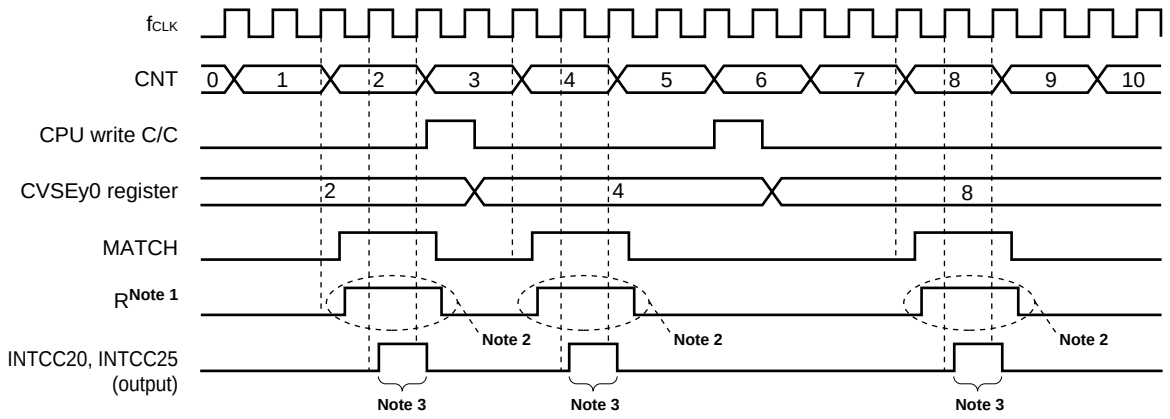
2. If an event occurs in this timing, it is ignored.

Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2
CAPTURE_S: Capture trigger signal of sub capture register
ED1, ED2: Capture event signal inputs from edge selection circuit
READ_ENABLE_S: Read timing for CVSEy0 register

3. y = 0, 5

Figure 9-110. Compare Operation: Timing of Compare Match and Write Operation to Register (When CMSE050 Register's CCSEy Bit = 1, EEVEy Bit = Arbitrary, and CSCE0 Register's SEVEy Bit = Arbitrary)



Notes 1. Can control TM20/TM21 clear by sub-channel 0/5 compare match and count direction

2. When MATCH signal occurs, the same waveform as the MATCH signal is generated.

3. The pulse width is always 1 clock.

Remarks 1. f_{CLK}: Base clock

2. CNT: Count value of timer 2

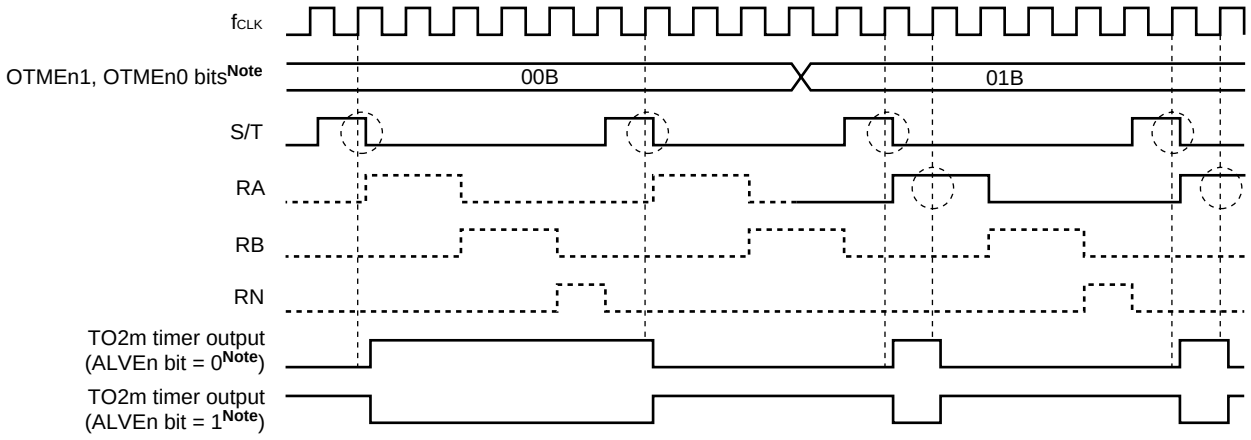
MATCH: CVSEy0 register compare match timing

R: Compare match input (sub-channel 0/5)

(5) Operation of output circuit

Figures 9-111 to 9-114 show the output circuit operation.

Figure 9-111. Signal Output Operation: Toggle Mode 0 and Toggle Mode 1 (When OCTLE0 Register's SWFEn Bit = 0, and ODELE0 Register's ODLEn2 Through ODLEn0 Bits = 0)



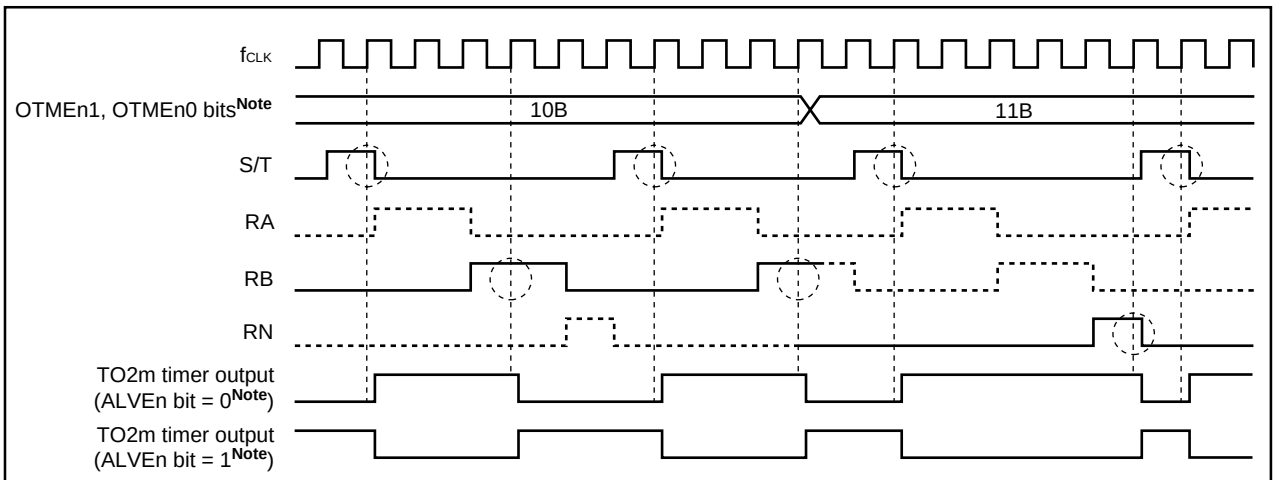
Note OTMEn1, OTMEn0 bits of OCTLE0 register

Remarks 1. f_{CLK}: Base clock

2. RA: Zero count signal input of TM20 (output circuit reset signal)
RB: Zero count signal input of TM21 (output circuit reset signal)
RN: Interrupt signal input of sub-channel n (output circuit reset signal) (n = 1 to 4)
S/T: Interrupt signal input of sub-channel n (output circuit set signal) (n = 1 to 4)

3. n = 1 to 4
m = 0 to 3

Figure 9-112. Signal Output Operation: Toggle Mode 2 and Toggle Mode 3 (When OCTLE0 Register's SWFEn Bit = 0, and ODELE0 Register's ODLEn2 Through ODLEn0 Bits = 0)



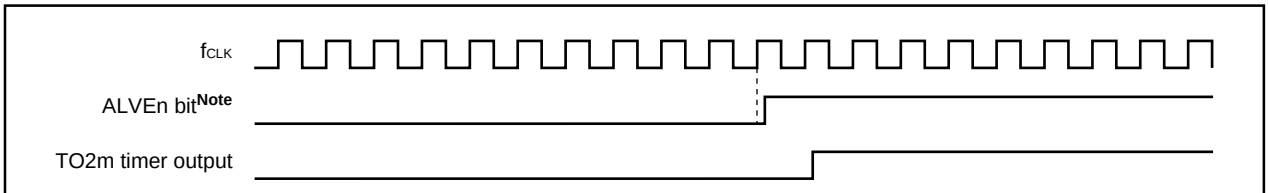
Note OTMEn1, OTMEn0 bits of OCTLE0 register

Remarks 1. f_{CLK}: Base clock

2. RA: Zero count signal input of TM20 (output circuit reset signal)
RB: Zero count signal input of TM21 (output circuit reset signal)
RN: Interrupt signal input of sub-channel n (output circuit reset signal) (n = 1 to 4)
S/T: Interrupt signal input of sub-channel n (output circuit set signal) (n = 1 to 4)

3. n = 1 to 4
m = 0 to 3

Figure 9-113. Signal Output Operation: During Software Control (When OCTLE0 Register's OTMEn1, OTMEn0 Bits = Arbitrary, SWFEn Bit = 1, and ODELE0 Register's ODLEn2 Through ODLEn0 Bits = 0)

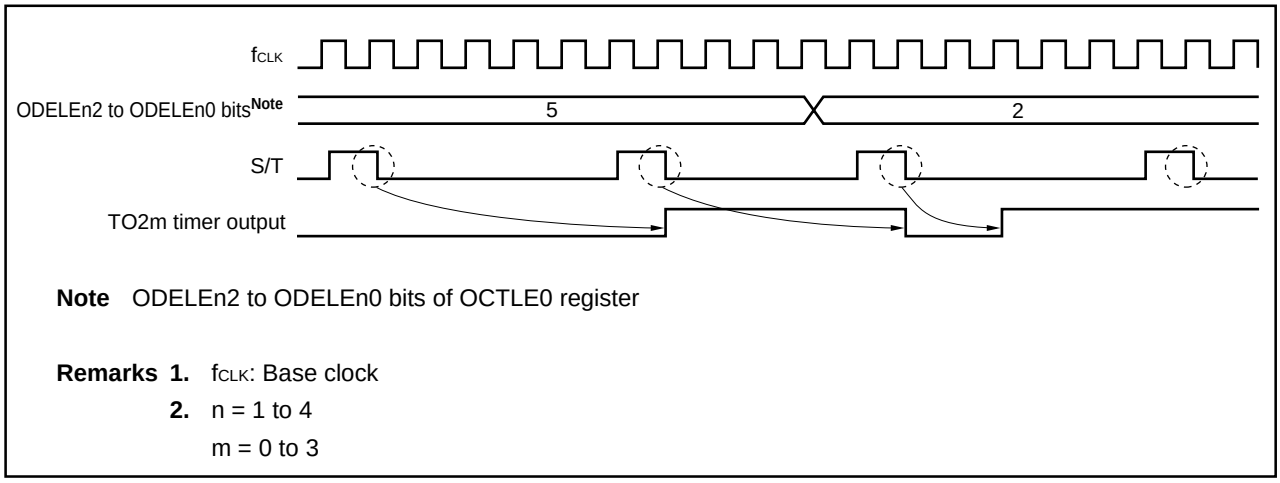


Note ALVEn bit of OCTLE0 register

Remarks 1. f_{CLK}: Base clock

2. n = 1 to 4
m = 0 to 3

Figure 9-114. Signal Output Operation: During Delay Output Operation (When OCTLE0 Register's OTMEn1, OTMEn0 Bits = 0, ALVEn = 0, SWFEn Bit = 0)



Note ODELEn2 to ODELEn0 bits of OCTLE0 register

Remarks 1. f_{CLK}: Base clock

2. n = 1 to 4

m = 0 to 3

9.4 Timer 3

9.4.1 Features (timer 3)

Timer 3 (TM3) is a 16-bit timer/counter that can perform the following operations.

- Interval timer function
- PWM output
- External signal cycle measurement

9.4.2 Function overview (timer 3)

- 16-bit timer/counter (TM3): 1 channel
- Capture/compare registers: 2
- Count clock division selectable by prescaler (maximum frequency of count clock: 16 MHz)
- Base clock (f_{CLK}): 2 types (maximum frequency of f_{CLK}: 32 MHz)
  ϕ and ϕ/2 can be selected
- Prescaler divide ratio
  The following divide ratios can be selected according to the base clock (f_{CLK}).

Divide Ratio	Base Clock (f_{CLK})	
	ϕ Selected	ϕ/2 Selected
1/2	ϕ/2	ϕ/4
1/4	ϕ/4	ϕ/8
1/8	ϕ/8	ϕ/16
1/16	ϕ/16	ϕ/32
1/32	ϕ/32	ϕ/64
1/64	ϕ/64	ϕ/128
1/128	ϕ/128	ϕ/256
1/256	ϕ/256	ϕ/512

- Interrupt request sources
  - Capture/compare match interrupt requests: 2 sources
    In case of capture register: INTCC3n generated by INTP3n input
    In case of compare register: INTCC3n generated by CC3n match signal
  - Overflow interrupt request: 1 source
    INTTM3 generated upon overflow of TM3 register
- Timer/counter count clock sources: 2 types
  (Selection of external pulse input, internal system clock cycle)
- One of two operation modes when the timer/counter overflows can be selected: free-running mode or overflow stop mode
- The timer/counter can be cleared by match of timer/counter and compare register
- External pulse output (TO3): 1

Remarks 1. ϕ: Internal system clock

2. n = 0, 1

9.4.3 Basic configuration

Table 9-10. Timer 3 Configuration List

Timer	Count Clock		Register	Read/Write	Generated Interrupt Signal	Capture Trigger	Timer Output S/R
	Note 1	**Note 2**					
Timer 3	ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256	ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256, ϕ/512	TM3	Read	INTTM3	–	–
			CC30	Read/write	INTCC30	INTP30	TO3 (S)
			CC31	Read/write	INTC31	INTP31	TO3 (R)

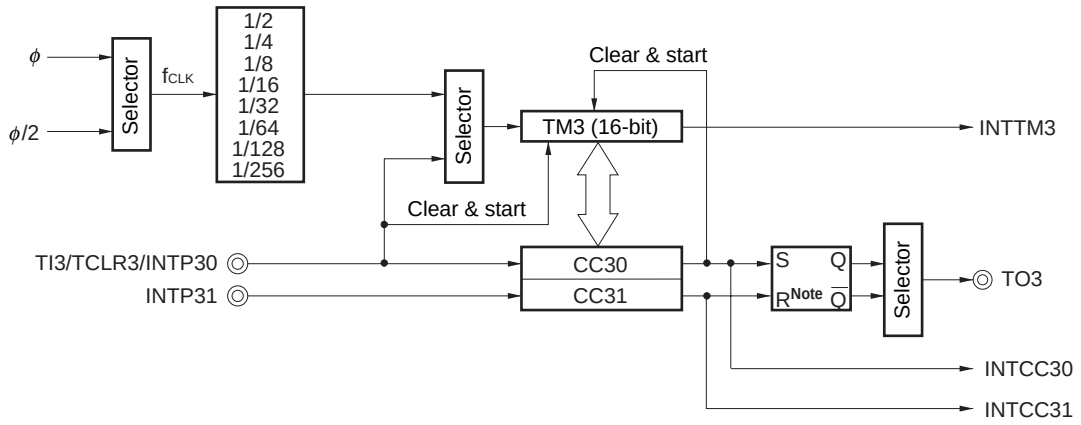
Notes 1. When ϕ is selected as the base clock (f_{CLK}) of TM3

2. When ϕ/2 is selected as the base clock (f_{CLK}) of TM3

Remark ϕ: Internal system clock
S/R: Set/Reset

Figure 9-115 shows the block diagram of timer 3.

Figure 9-115. Block Diagram of Timer 3



Note Reset priority

Remarks 1. TI3 input and TCLR3 input connected to port immediately before edge detection

2. f_{CLK}: Base clock (32 MHz (MAX.))

(1) Timer 3 (TM3)

TM3 functions as a 16-bit free-running timer or as an event counter for an external signal. Besides being mainly used for cycle measurement, TM3 can be used as pulse output.

TM3 is read-only in 16-bit units.

Caution Continuous reading of TM3 is prohibited. If TM3 is continuously read, the second read value may differ from the actual value.

Figure 9-116. Timer 3 (TM3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
TM3																	FFFFF680H	0000H

Cautions 1. The TM3 register can only be read. If writing is performed to the TM3 register, the subsequent operation is undefined.

2. If the CAE bit of the TMC30 register is cleared (0), a reset is performed asynchronously.

TM3 performs the count-up operations of an internal count clock or external count clock. Timer starting and stopping are controlled by the CE bit of timer control register 30 (TMC30).

The internal or external count clock is selected by the ETI bit of timer control register 31 (TMC31).

(a) Selection of the external count clock

TM3 operates as an event counter.

When the ETI bit of timer control register 31 (TMC31) is set (1), TM3 counts the valid edges of the external clock input (TI3), synchronized with the internal count clock. The valid edge is specified by valid edge selection register (SESC).

Caution If the INTP30, TI3, and TCLR3 pins are used as the TI3 and TCLR3, mask the INTP30 interrupt.

(b) Selection of the internal count clock

TM3 operates as a free-running timer.

When an internal clock is specified as a count clock by timer control register 31 (TMC31), TM3 is counted up for each input clock cycle specified by the CS2 to CS0 bits of the TMC30 register.

A division by the prescaler can be selected for the count clock from among $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$, $f_{CLK}/128$ and $f_{CLK}/256$ by the TMC30 register (f_{CLK}: base clock).

An overflow interrupt can be generated if the timer overflows. Also, the timer can be stopped following an overflow by setting the OST bit of the TMC31 register to 1.

Caution The count clock cannot be changed while the timer is operating.

The conditions when the TM3 register becomes 0000H are shown below.

(a) Asynchronous reset

- CAE bit of TMC30 register = 0
- Reset input

(b) Synchronous reset

- CE bit of TMC30 register = 0
- The CC30 register is used as a compare register, and the TM3 and CC30 registers match when clearing the TM3 register is enabled (CCLR bit of the TMC31 register = 1)

(2) Capture/compare registers 30 and 31 (CC30 and CC31)

These capture/compare registers are 16-bit registers.

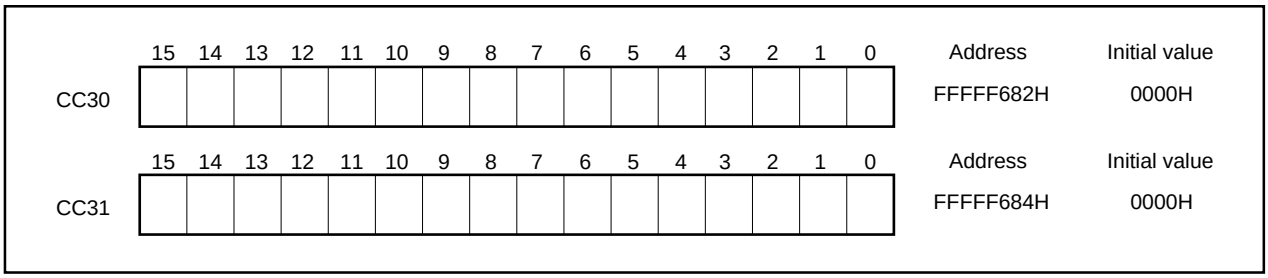
They can be used as capture registers or compare registers according to the CMS1 and CMS0 bit specifications of timer control register 31 (TMC31).

These registers can be read/written in 16-bit units (However, write operations can only be performed in compare mode).

Caution Continuous reading of CC3n is prohibited. If CC3n is continuously read, the second read value may differ from the actual value. If CC3n must be read twice, be sure to read another register between the first and the second read operation.

Correct usage example	Incorrect usage example
CC30 read	CC30 read
CC31 read	CC30 read
CC30 read	CC31 read
CC31 read	CC31 read

Figure 9-117. Capture/Compare Registers 30 and 31 (CC30, CC31)



(a) Setting these registers to capture registers (CMS1 and CMS0 of TMC31 = 0)

When these registers are set to capture registers, the valid edges of the corresponding external interrupt signals INTP30 and INTP31 are detected as capture triggers. The timer TM3 is synchronized with the capture trigger, and the value of TM3 is latched in the CC30 and CC31 registers (capture operation).

The valid edge of the INTP30 pin is specified (rising, falling, or both edges) according to the IES301 and IES300 bits of the SESC register, and the valid edge of the INTP31 pin is specified according to the IES311 and IES310 bits of the SESC register.

The capture operation is performed asynchronously relative to the count clock. The latched value is held in the capture register until the next time the capture operation is performed.

When the CAE bit of timer control register 30 (TMC30) is 0, 0000H is read.

If these registers are specified as capture registers, an interrupt is generated by detecting the valid edge of signals INTP30 and INTP31.

Caution If the capture operation and the TM3 register count prohibit setting (CE bit of TMC30 register = 0) timings conflict, the captured data becomes undefined, and no INTCC3n interrupt is generated (n = 0, 1).

(b) Setting these registers to compare registers (CMS1 and CMS0 of TMC31 = 1)

When these registers are set to compare registers, the TM3 and register values are compared for each timer count clock, and an interrupt is generated by a match. If the CCLR bit of timer control register 31 (TMC31) is set (1), the TM3 value is cleared (0) at the same time as a match with the CC30 register (it is not cleared (0) by a match with the CC31 register).

A compare register is equipped with a set/reset output function. The corresponding timer output (TO3) is set or reset, synchronized with the generation of a match signal.

The interrupt selection source differs according to the function of the selected register.

Cautions 1. To write to capture/compare registers 30 and 31 (CC30, CC31), always set the CAE bit to 1 first. When the CAE bit is 0, even if writing to registers CC30 and CC31, the data that is written will be invalid because the reset is asynchronous.

2. Perform a write operation to capture/compare registers 30 and 31 after setting them to compare registers according to the TMC31 register setting. If they are set to capture registers (CMS1 and CMS0 bits of TMC31 register = 0), no data is written even if a write operation is performed to CC30 and CC31.

3. When these registers are set to compare registers, INTP30 and INTP31 cannot be used as external interrupt input pins.

9.4.4 Control registers

(1) Timer 3 clock selection register (PRM03)

The PRM03 register is used to select the base clock (f_{CLK}) of timer 3 (TM3).

This register can be read/written in 8- or 1-bit units.

Caution Always set this register before setting the timer.

Figure 9-118. Timer 3 Clock Selection Register (PRM03)

	7	6	5	4	3	2	1	0	Address	Initial value
PRM03	0	0	0	0	0	0	0	PRM3	FFFFF690H	00H

Bit Position	Bit Name	Function
0	PRM3	Specifies the base clock (f_{CLK}) of timer 3 (TM3). 0: ϕ/2 (when ϕ > 32 MHz) 1: ϕ (when $\phi \leq$ 32 MHz)

Remark ϕ : Internal system clock

(2) Timer control register 30 (TMC30)

The TMC30 register controls the operation of TM3.

This register can be read/written in 8- or 1-bit units.

Caution The CAE bit and CE bit cannot be set at the same time. Be sure to set the CAE bit prior to setting the CE bit. To use an external pin related to the timer function when using timer 3, be sure to set (1) the CAE bit after setting the external pin to the control mode.

Figure 9-119. Timer Control Register 30 (TMC30) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
TMC30	OVF	CS2	CS1	CS0	0	0	CE	CAE	FFFFF686H	00H

Bit Position	Bit Name	Function
7	OVF	Flag that indicates TM3 overflow. 0: No overflow 1: Overflow The OVF bit becomes “1” when TM3 changes from FFFFH to 0000H. An overflow interrupt request (INTTM3) is generated at the same time. However, if CC30 is set to the compare mode (CMS0 bit of the TMC31 register = 1) and match clear during comparison of TM3 and CC30 is enabled (CCLR bit of TMC31 register = 1), and TM3 is cleared to 0000H following match at FFFFH, TM3 is considered to have been cleared and the OVF bit does not become “1”, nor is the INTTM3 interrupt generated. The OVF bit holds a “1” until “0” is written to it or an asynchronous reset is applied while the CAE bit = 0. Interrupts by overflow and the OVF bit are independent, and even if the OVF bit is manipulated, this does not affect the interrupt request flag for INTTM3 (TM3IF0). If an overflow occurs while the OVF bit is being read, the value of the flag changes and the value is returned at the next read.

Figure 9-119. Timer Control Register 30 (TMC30) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>6 to 4</td><td>CS2 to CS0</td><td>Selects the internal count clock for TM3.
<table>
<tr><th>CS2</th><th>CS1</th><th>CS0</th><th>Count Clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>$f_{CLK}/2$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>$f_{CLK}/4$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>$f_{CLK}/8$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>$f_{CLK}/16$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>$f_{CLK}/32$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>$f_{CLK}/64$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>$f_{CLK}/128$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>$f_{CLK}/256$</td></tr>
</table>
Caution Do not change the CS2 to CS0 bits during timer operation. If they are to be changed, they must be changed after setting the CE bit to “0”. If the CS2 to CS0 bits are overwritten during timer operation, the operation is not guaranteed.
Remark f_{CLK}: Base clock</td></tr>
<tr><td>1</td><td>CE</td><td>Controls the operation of TM3.
0: Disable count (timer stopped at 0000H and does not operate)
1: Perform count operation.
Caution If CE = 0, the external pulse output (TO3) becomes inactive level (The active level of TO3 output is set with the ALV bit of the TMC31 register).</td></tr>
<tr><td>0</td><td>CAE</td><td>Controls the internal count clock.
0: Asynchronously reset entire TM3 unit. Stop base clock supply to TM3 unit.
1: Supply base clock (f_{CLK}) to TM3 unit.
Cautions 1. When CAE = 0 is set, the TM3 unit can be reset asynchronously.
2. When CAE = 0, the TM3 unit is in a reset state. To operate TM3, first set CAE = 1.
3. When the CAE bit is changed from “1” to “0”, all the registers of the TM3 unit are initialized. When again setting CAE = 1, be sure to then again set all the registers of the TM3 unit.</td></tr>
</table>

(3) Timer control register 31 (TMC31)

The TMC31 register controls the operation of TM3.

This register can be read/written in 8- or 1-bit units.

Cautions 1. Do not change the bits of the TMC31 register during timer operation. If they are to be changed, they must be changed after setting the CE bit of the TMC30 register to "0". If the TMC31 register is overwritten during timer operation, the operation is not guaranteed.

2. If the ENT1 bit and the ALV bit are changed simultaneously, a glitch (spike-shaped noise) may be generated in the TO3 pin output. Either design the circuit that will not malfunction even if a glitch is generated, or make sure that the ENT1 bit and the ALV bit do not change at the same time.

3. TO3 output remains unchanged by external interrupt signals (INTP30, INTP31). When using the TO3 signal, set the capture/compare register to the compare register (CMS1, CMS0 bits of TMC31 register = 1).

Remarks 1. A reset takes precedence for the flip-flop of the TO3 output.

2. When the A/D converter is set to the timer trigger mode, the match interrupt of the compare register becomes a start trigger for A/D conversion, and conversion begins. At this time, the compare register match interrupt also functions as a compare register match interrupt for the CPU. To prevent the generation of a compare register match interrupt for the CPU, disable interrupts with the interrupt mask bits (CC3MK0, CC3MK1) of the interrupt control registers (CC3IC0, CC3IC1).

Figure 9-120. Timer Control Register 31 (TMC31) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
TMC31	OST	ENT1	ALV	ETI	CCLR	ECLR	CMS1	CMS0	FFFFF688H	20H

Bit Position	Bit Name	Function
7	OST	Sets the operation when TM3 overflows. 0: Continue count operation after overflow (free-running mode) 1: After overflow, timer holds 0000H and stops count operation (overflow stop mode). At this time, the CE bit of TMC30 remains "1". The count operation is resumed by again writing "1" to the CE bit.

Figure 9-120. Timer Control Register 31 (TMC31) (2/2)

Bit Position	Bit Name	Function
6	ENT1	Enables/disables output of external pulse output (TO3). 0: Disable external pulse output. Output of inactive level of ALV bit to TO3 pin is fixed. TO3 pin level remains unchanged even if match signal from corresponding compare register is generated. 1: Enable external pulse output. Compare register match causes TO3 output to change. However, in capture mode, TO3 output does not change. An ALV bit inactive level is output from the time when timer output is enabled until a match signal is generated. **Caution If either CC30 or CC31 is specified as a capture register, the ENT1 bit must be set to "0".**
5	ALV	Specifies active level of external pulse output (TO3). 0: Active level is low level. 1: Active level is high level. **Caution The initial value of the ALV bit is "1".**
4	ETI	Switches count clock between external clock and internal clock. 0: Specifies input clock (internal). The count clock can be selected with bits CS2 through CS0 of TMC30. 1: Specifies external clock (TI3). Valid edge can be selected with bits TES31, TES30 of SESC.
3	CCLR	Enables/disables TM3 clearing during compare operation. 0: Disable clearing. 1: Enable clearing (TM3 is cleared when CC30 and TM3 match during compare operation).
2	ECLR	Enables TM3 clearing by external clear input (TCLR3). 0: Disable clearing by TCLR3. 1: Enable clearing by TCLR3 (Counting resumes after clearing).
1	CMS1	Selects operation mode of capture/compare register (CC31). 0: Register operates as capture register. 1: Register operates as compare register.
0	CMS0	Selects operation mode of capture/compare register (CC30). 0: Register operates as capture register. 1: Register operates as compare register.

(4) Valid edge selection register (SESC)

This register specifies the valid edge of external interrupt requests (TI3, TCLR3, INTP30, INTP31) from an external pin.

The rising edge, the falling edge, or both rising and falling edges can be specified as the valid edge independently for each pin.

This register can be read/written in 8- or 1-bit units.

Caution Do not change the bits of SESC register during timer operation. If they are to be changed, they must be changed after setting the CE bit of the TMC30 register to "0". If the SESC register is overwritten during timer operation, the operation is not guaranteed.

Figure 9-121. Valid Edge Selection Register (SESC)

	7	6	5	4	3	2	1	0	Address	Initial value
SESC	TES31	TES30	CES31	CES30	IES311	IES310	IES301	IES300	FFFFF689H	00H
	TI3		TCLR3		INTP31		INTP30			

Bit Position	Bit Name	Function
7, 6	TES31, TES30	Specifies the valid edge of INTP30, INTP31 pins, TCLR3, and TI3 pins.
5, 4	CES31, CES30	
3, 2	IES311, IES310	
1, 0	IES301, IES300	

xESn1	xESn0	Operation
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Remark n = 3, 30, 31

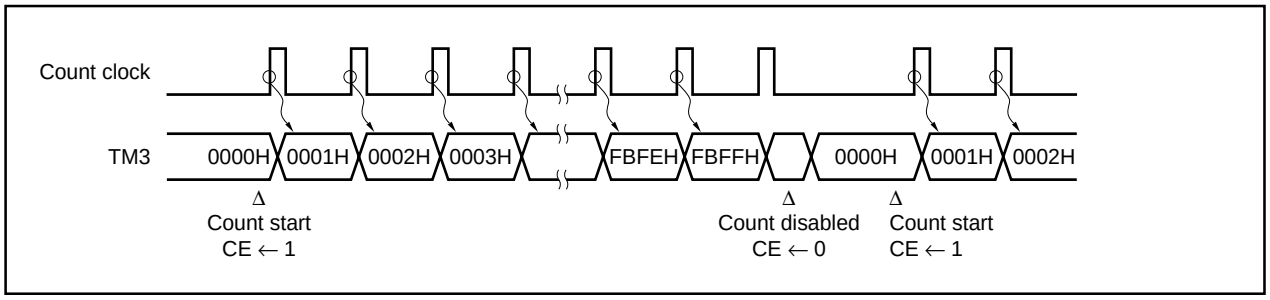
9.4.5 Operation

(1) Count operation

Timer 3 can function as a 16-bit free-running timer or as an external signal event counter. The setting for the type of operation is specified by timer control register 3n (TMC3n) (n = 0, 1).

When it operates as a free-running timer, if the CC30 or CC31 register and the TM3 count value match, an interrupt signal is generated and the timer output signal (TO3) can be set or reset. Also, a capture operation that holds the TM3 count value in the CC30 or CC31 register is performed, synchronized with the valid edge that was detected from the external interrupt request input pin as an external trigger. The capture value is held until the next capture trigger is generated.

Figure 9-122. Basic Operation of Timer 3



(2) Overflow

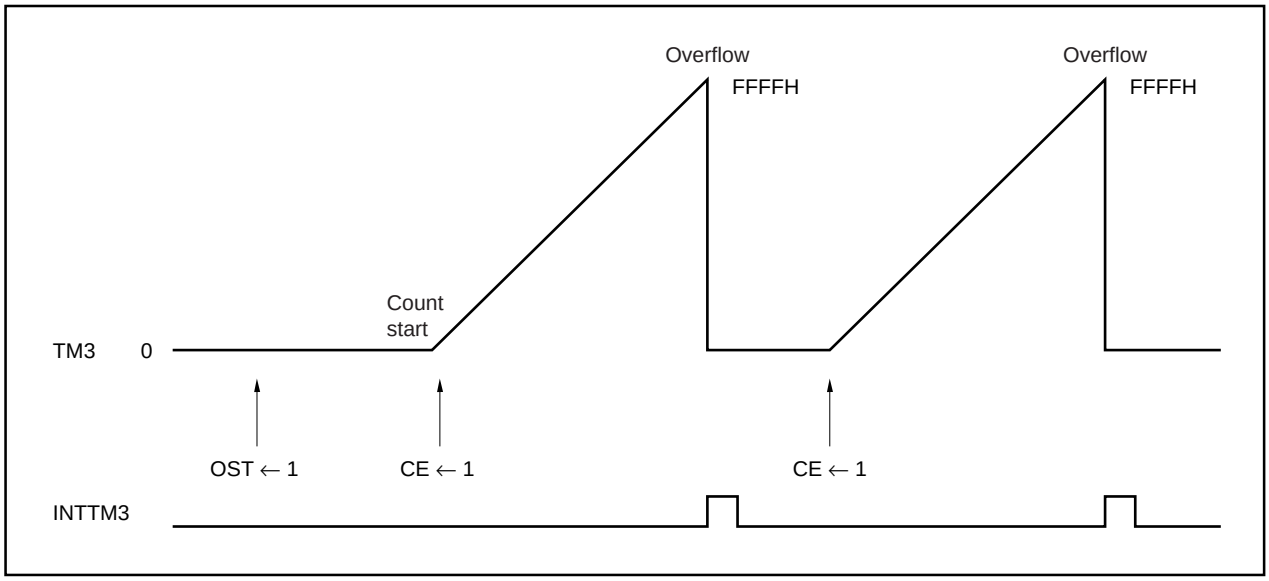
When the TM3 register has counted the count clock from FFFFH to 0000H, the OVF bit of the TMC30 register is set (1), and an overflow interrupt (INTTM3) is generated at the same time. However, if the CC30 register is set to compare mode (CMS0 bit = 1) and to the value FFFFH when match clearing is enabled (CCLR bit = 1), then the TM3 register is considered to be cleared and the OVF bit is not set (1) when the TM3 register changes from FFFFH to 0000H. Also, the overflow interrupt (INTTM3) is not generated .

When the TM3 register is changed from FFFFH to 0000H because the CE bit changes from 1 to 0, the TM3 register is considered to be cleared, but the OVF bit is not set (1) and no INTTM3 interrupt is generated.

Also, timer operation can be stopped after an overflow by setting the OST bit of the TMC31 register to 1. When the timer is stopped due to an overflow, the count operation is not restarted until the CE bit of the TMC30 register is set (1).

Operation is not affected even if the CE bit is set (1) during a count operation.

Figure 9-123. Operation after Overflow (When OST = 1)



(3) Capture operation

The TM3 register has two capture/compare registers. These are the CC30 register and the CC31 register. A capture operation or a compare operation is performed according to the settings of both the CMS1 and CMS0 bits of the TMC31 register. If the CMS1 and CMS0 bits of the TMC31 register are set to 0, the register operates as a capture register.

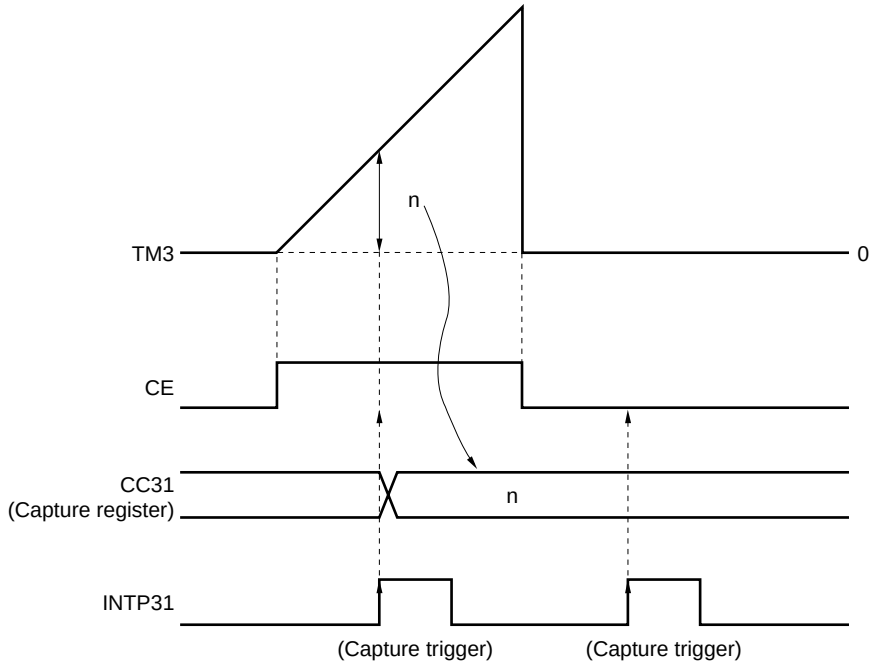
A capture operation that captures and holds the TM3 count value asynchronously relative to the count clock is performed synchronized with an external trigger. The valid edge that is detected from an external interrupt request input pin (INTP30 or INTP31) is used as an external trigger (capture trigger). The TM3 count value during counting is captured and held in the capture register, synchronized with that capture trigger signal. The capture register value is held until the next capture trigger is generated.

Also, an interrupt request (INTCC30 or INTCC31) is generated by INTP30 or INTP31 signal input.

The valid edge of the capture trigger is set by valid edge selection register (SESC).

If both the rising and falling edges are set as capture triggers, the input pulse width from an external source can be measured. Also, if only one of the edges is set as the capture trigger, the input pulse cycle can be measured.

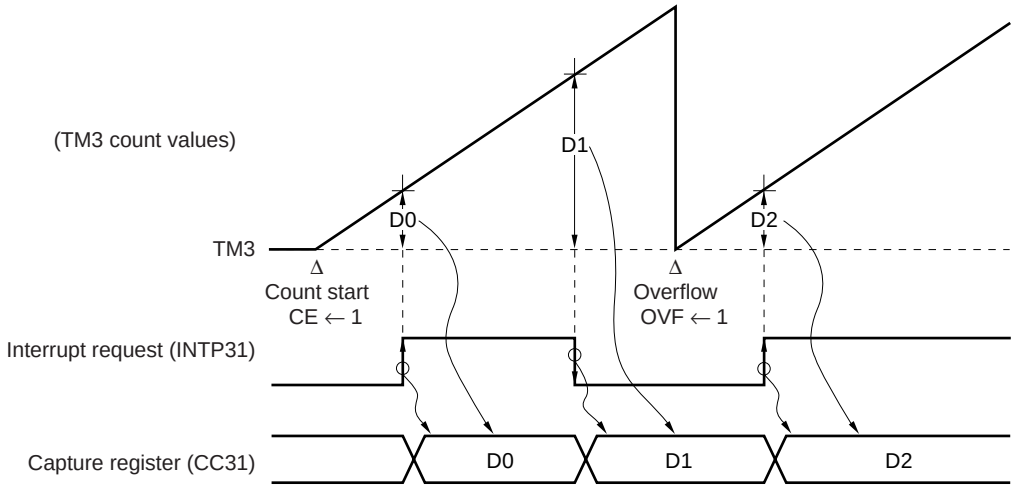
Figure 9-124. Capture Operation Example



Remarks 1. When the CE bit is 0, no capture operation is performed even if INTP31 is input.

2. Valid edge of INTP31: Rising edge

Figure 9-125. TM3 Capture Operation Example (When Both Edges Are Specified)



Remark D0 to D2: TM3 count values

(4) Compare operation

The TM3 register has two capture/compare registers. These are the CC30 register and the CC31 register. A capture operation or a compare operation is performed according to the settings of both the CMS1 and CMS0 bits of the TMC31 register. If 1 is set in the CMS1 and CMS0 bits of the TMC31 register, the register operates as a compare register.

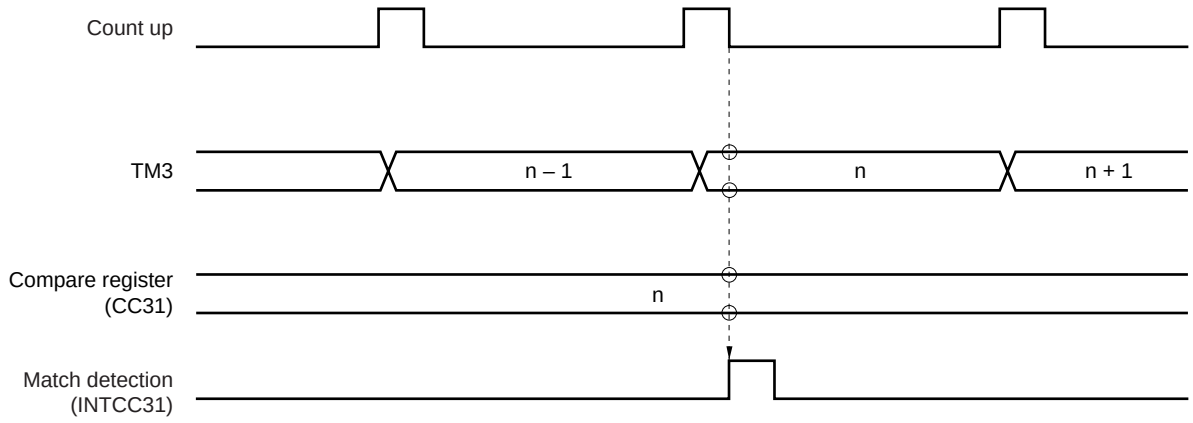
A compare operation that compares the value that was set in the compare register and the TM3 count value is performed.

If the TM3 count value matches the value of the compare register, which had been set in advance, a match signal is sent to the output control circuit. The match signal causes the timer output pin (TO3) to change and an interrupt request signal (INTCC30, INTCC31) to be generated at the same time.

If the CC30 register is set to 0000H, the 0000H after the TM3 register counts up from FFFFH to 0000H is judged as a match. The 0000H when the TM3 register begins counting is not judged as a match.

If match clearing is enabled (CCLR bit = 1) for the CC30 register, the TM3 register is cleared when a match with the TM3 register occurs during a compare operation.

Figure 9-126. Compare Operation Example



Remark The match is detected immediately after the count up, and the match detection signal is generated.

(5) External pulse output

Timer 3 has one timer output pin (TO3).

An external pulse output (TO3) is generated when a match of the two compare registers (CC30 and CC31) and the TM3 register is detected.

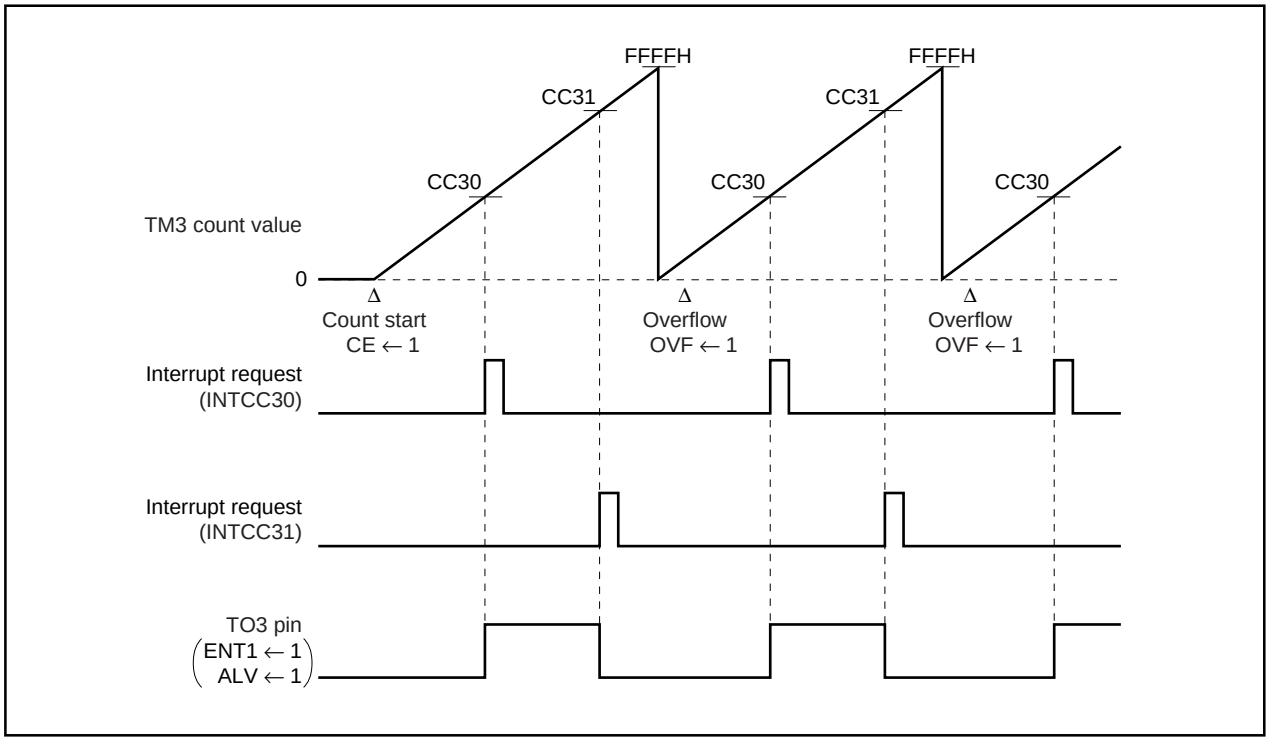
If a match is detected when the TM3 count value and the CC30 value are compared, the output level of the TO3 pin is set. Also, if a match is detected when the TM3 count value and the CC31 value are compared, the output level of the TO3 pin is reset.

The output level of the TO3 pin can be specified by the TMC31 register.

Table 9-11. TO3 Output Control

ENT1	ALV	TO3 Output	
		External Pulse Output	Output Level
0	0	Disable	High level
0	1	Disable	Low level
1	0	Enable	When the CC30 register is matched: Low level When the CC31 register is matched: High level
1	1	Enable	When the CC30 register is matched: High level When the CC31 register is matched: Low level

Figure 9-127. TM3 Compare Operation Example (Set/Reset Output Mode)



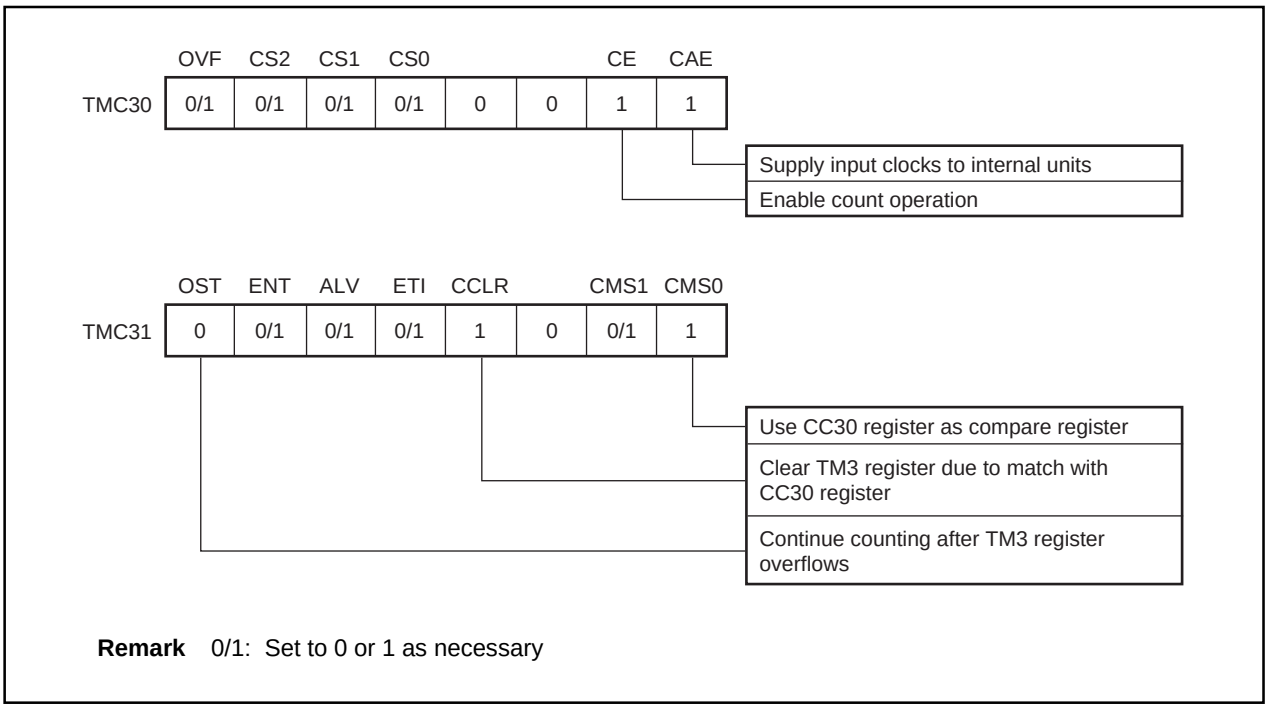
9.4.6 Application examples

(1) Interval timer

By setting the TMC30 and TMC31 registers as shown in Figure 9-128, timer 3 operates as an interval timer that repeatedly generates interrupt requests with the value that was set in advance in the CC30 register as the interval.

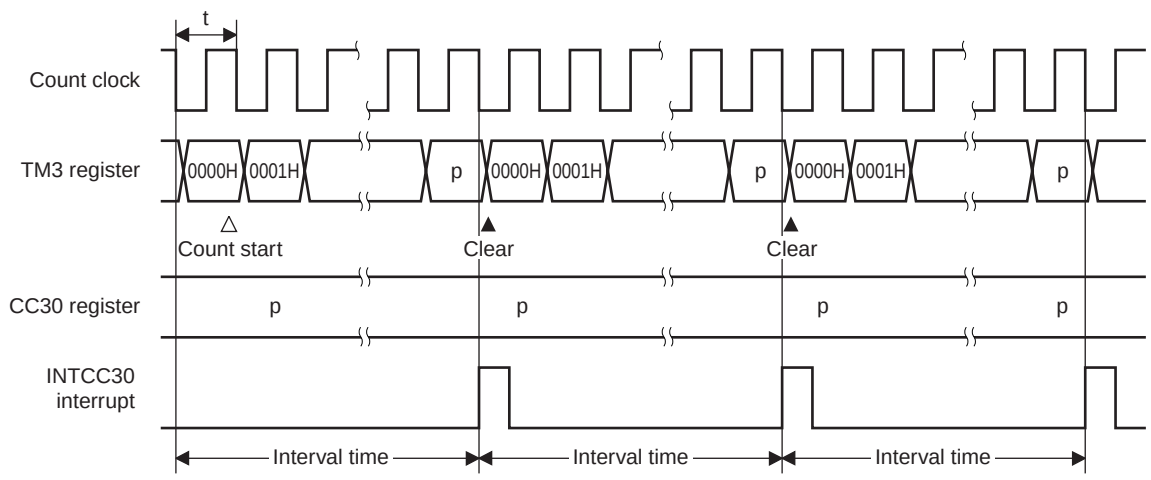
When the counter value of the TM3 register matches the setting value of the CC30 register, the TM3 register is cleared (0000H) and an interrupt request signal (INTCC30) is generated at the same time that the count operation resumes.

Figure 9-128. Contents of Register Settings When Timer 3 Is Used as Interval Timer



Remark 0/1: Set to 0 or 1 as necessary

Figure 9-129. Interval Timer Operation Timing Example



Remark p: Setting value of CC30 register (0000H to FFFFH)

t: Count clock cycle

Interval time = $(p + 1) \times t$

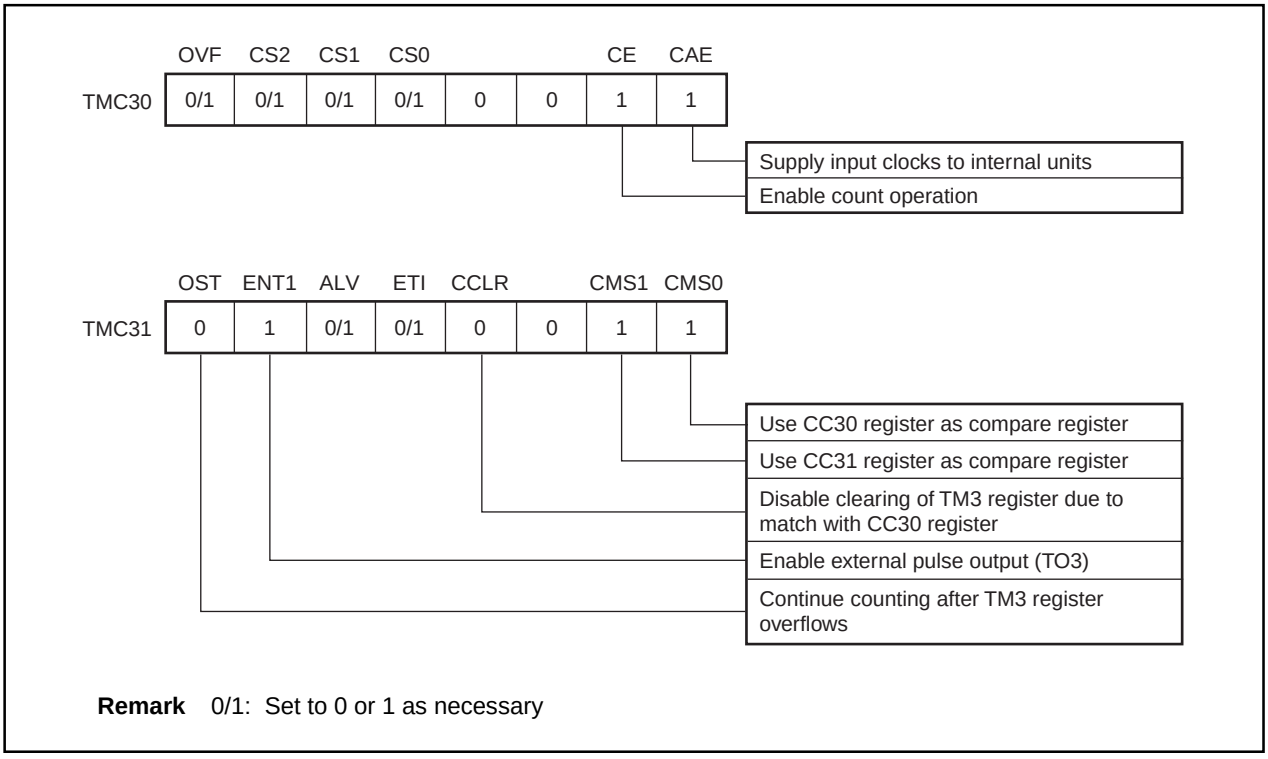
(2) PWM output

By setting the TMC30 and TMC31 registers as shown in Figure 9-130, timer 3 can output a PWM of an arbitrary frequency with the values that were set in advance in the CC30 and CC31 registers determining the intervals.

When the counter value of the TM3 register matches the setting value of the CC30 register, the TO3 output becomes active. Then, when the counter value of the TM3 register matches the setting value of the CC31 register, the TO3 output becomes inactive. This enables a PWM of an arbitrary frequency to be output. When the setting value of the CC30 register and the setting value of the CC31 register are the same, the TO3 output remains inactive and does not change.

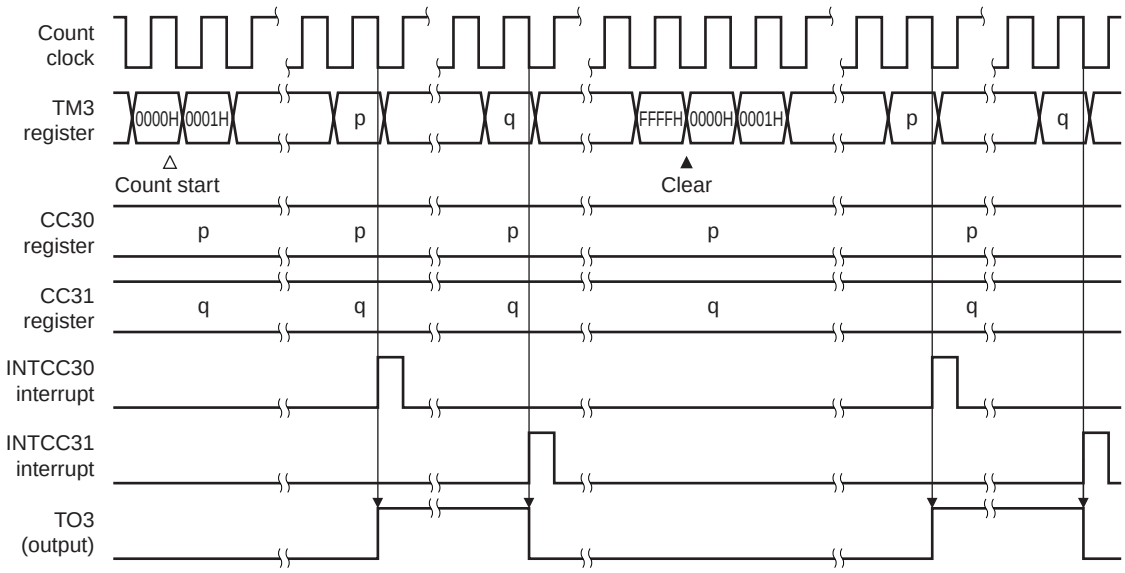
The active level of TO3 output can be set by the ALV bit of the TMC31 register.

Figure 9-130. Contents of Register Settings When Timer 3 Is Used for PWM Output



Remark 0/1: Set to 0 or 1 as necessary

Figure 9-131. PWM Output Operation Timing Example



Remarks 1. p: Setting value of CC30 register (0000H to FFFFH)

q: Setting value of CC31 register (0000H to FFFFH)

$p \neq q$

2. In this example, the active level of TO3 output is set to high level.

(3) Cycle measurement

By setting the TMC30 and TMC31 registers as shown in Figure 9-132, timer 3 can measure the cycle of signals input to the INTP30 pin or INTP31 pin.

The valid edge of the INTP30 pin is selected according to the IES301 and IES300 bits of the SESC register, and the valid edge of the INTP31 pin is selected according to the IES311 and IES310 bits of the SESC register. Either the rising edge, the falling edge, or both edges can be selected as the valid edges of both pins.

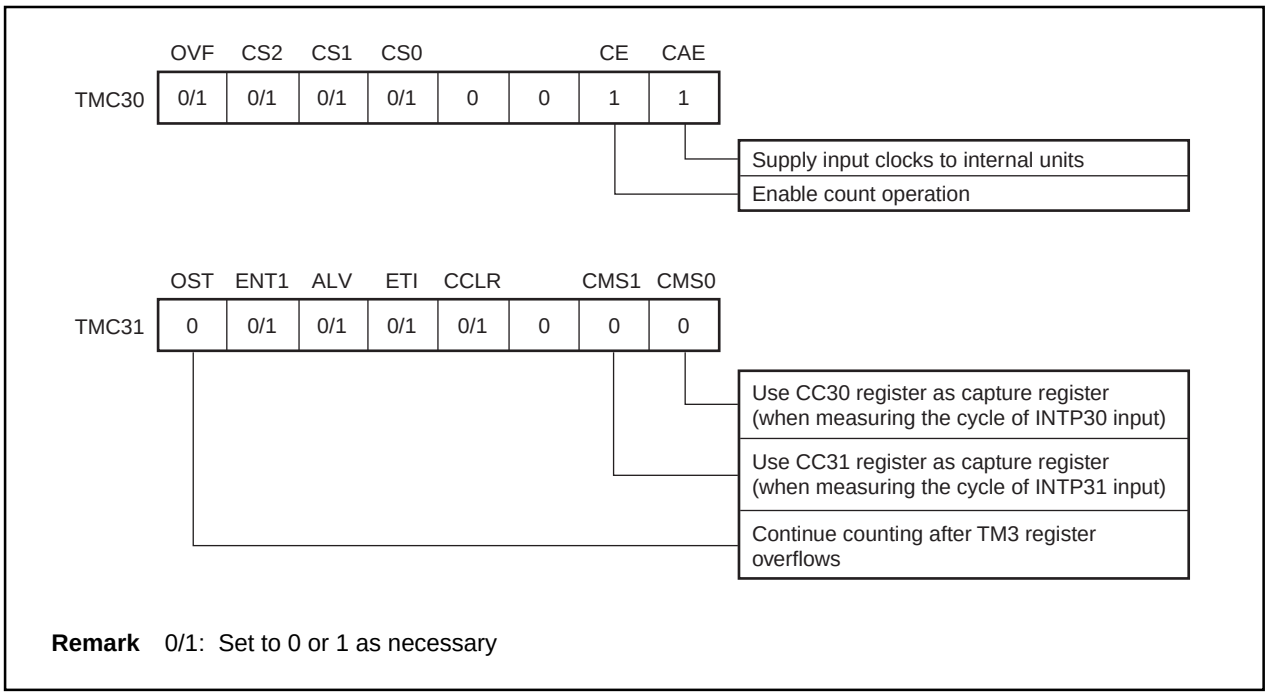
If the CC30 register is set to a capture register and TM3 is started, the valid edge input of the INTP30 pin is set as the trigger for capturing the TM3 register value in the CC30 register. When this value is captured, an INTCC30 interrupt is generated.

Similarly, if the CC31 register is set to a capture register and TM3 is started, the valid edge input of the INTP31 pin is set as the trigger for capturing the TM3 register value in the CC31 register. When this value is captured, an INTCC31 interrupt is generated.

The cycle of signals input to the INTP30 pin is calculated by obtaining the difference between the TM3 register's count value (Dx) that was captured in the CC30 register according to the x-th valid edge input of the INTP30 pin and the TM3 register's count value (D(x+1)) that was captured in the CC30 register according to the (x+1)-th valid edge input of the INTP30 pin and multiplying the value of this difference by the cycle of the clock control signal.

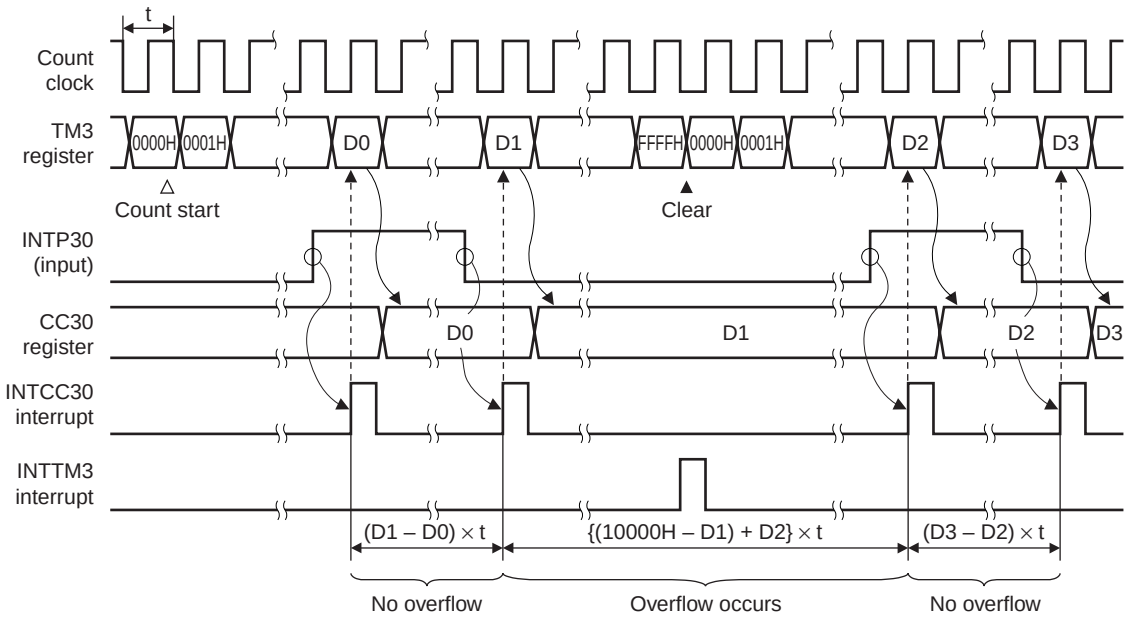
The cycle of signals input to the INTP31 pin is calculated by obtaining the difference between the TM3 register's count value (Dx) that was captured in the CC31 register according to the x-th valid edge input of the INTP31 pin and the TM3 register's count value (D(x+1)) that was captured in the CC31 register according to the (x+1)-th valid edge input of the INTP31 pin and multiplying the value of this difference by the cycle of the clock control signal.

Figure 9-132. Contents of Register Settings When Timer 3 Is Used for Cycle Measurement



Remark 0/1: Set to 0 or 1 as necessary

Figure 9-133. Cycle Measurement Operation Timing Example



Caution An overflow must not be generated more than once between the 1st and 2nd INTCC30 interrupts.

Remarks 1. D0 to D3: TM3 register count values
t: Count clock cycle

2. In this example, the valid edge of INTP30 input has been set to both edges (rising and falling).

9.4.7 Precautions

Various precautions concerning timer 3 are shown below.

(1) If a conflict occurs between the reading of the CC30 register and a capture operation when the CC30 register is used in capture mode, an external trigger (INTP30) valid edge is detected and an external interrupt request signal (INTCC30) is generated however, timer value is not stored in the CC30 register.

(2) If a conflict occurs between the reading of the CC31 register and a capture operation when the CC31 register is used in capture mode, an external trigger (INTP31) valid edge is detected and an external interrupt request signal (INTCC31) is generated however, the timer value is not stored in the CC31 register.

(3) The following bits and registers must not be rewritten during operation (TMC30 register CE = 1).
- CS2 to CS0 bits of TMC30 register
- TMC31 register
- SESC register

(4) The CAE bit of the TMC30 register is a TM3 reset signal. To use TM3, first set (1) the CAE bit.

(5) The analog noise elimination time + two cycles of the input clock are required to detect a valid edge of the external interrupt input (INTP30 or INTP31) and external clock input (TI3). Therefore, edge detection will not be performed normally for changes that are less than the analog noise elimination time + two cycles of the input clock. For the analog noise elimination, refer to **14.4 Noise Eliminator**.

(6) The operation of an external interrupt output (INTCC30 or INTCC31) is automatically determined according to the operating state of the capture/compare registers 30, 31 (CC30, CC31). When the capture/compare register is used for a capture mode, the external trigger (INTP30, INTP31) is used for valid edge detection. When the capture/compare register is used for a compare mode, the external interrupt output is used for a match interrupt indicating a match with the TM3 register.

(7) If the ENT1 and ALV bits of the TMC31 register are changed at the same time, a glitch (spike shaped noise) may be generated in the TO3 pin output. Either create a circuit configuration that will not malfunction even if a glitch is generated or make sure that the ENT1 and ALV bits do not change at the same time.

9.5 Timer 4

9.5.1 Features (timer 4)

Timer 4 (TM4) functions as a 16-bit interval timer.

9.5.2 Function overview (timer 4)

- 16-bit interval timer: 1 channel
- Compare register: 1
- Count clock selected from divisions of internal system clock (maximum frequency of count clock: 16 MHz)
- Base clock (f_{CLK}): 1 type (maximum frequency of f_{CLK}: 32 MHz)
  ϕ/2
- Prescaler divide ratio
  The following divide ratios can be selected according to the base clock (f_{CLK}).

Divide Ratio	Base Clock (f_{CLK})
1/2	ϕ/4
1/4	ϕ/8
1/8	ϕ/16
1/16	ϕ/32
1/32	ϕ/64
1/64	ϕ/128
1/128	ϕ/256
1/256	ϕ/512

- Interrupt request source: 1
  - Compare match interrupt
    INTCM4 generated with CM4 match signal
- Timer clear
  TM4 register can be cleared by CM4 register match.

Remark ϕ: Internal system clock

9.5.3 Basic configuration

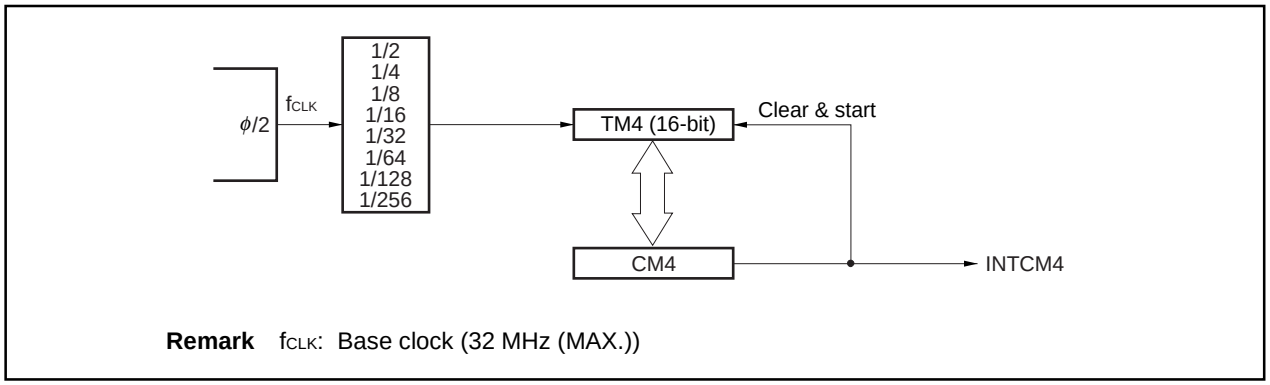
Table 9-12. Timer 4 Configuration List

Timer	Count Clock	Register	Read/Write	Generated Interrupt Signal	Capture Trigger	Timer Output S/R	Other Functions
Timer 4	ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256, ϕ/512	TM4	Read	–	–	–	–
		CM4	Read/write	INTCM4	–	–	–

Remark ϕ: Internal system clock
S/R: Set/Reset

Figure 9-134 shows the block diagram of timer 4.

Figure 9-134. Block Diagram of Timer 4



Remark f_{CLK}: Base clock (32 MHz (MAX.))

(1) Timer 4 (TM4)

TM4 is a 16-bit timer. It is mainly used as an interval timer for software.

Starting and stopping TM4 is controlled by the CE bit of the timer control register 4 (TMC4).

A division by the prescaler can be selected for the count clock from among ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256, and ϕ/512 by the CS2 to CS0 bits of the TMC4 register.

TM4 is read-only in 16-bit units.

Figure 9-135. Timer 4 (TM4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
TM4																	FFFFF540H	0000H

The conditions for which the TM4 register becomes 0000H are shown below.

- Reset input
- CAE bit = 0
- CE bit = 0
- Match of TM4 register and CM4 register
- Overflow

Cautions 1. If the CAE bit of the TMC4 register is cleared (0), a reset is performed asynchronously.

2. If the CE bit of the TMC4 register is cleared (0), a reset is performed, synchronized with the internal clock. Similarly, a synchronized reset is performed after a match with the CM4 register and after an overflow.

3. The count clock must not be changed during a timer operation. If it is to be overwritten, it should be overwritten after the CE bit is cleared (0).

4. Up to ϕ/4 clocks are required after a value is set in the CE bit until the set value is transferred to internal units. When a count operation begins, the count cycle from 0000H to 0001H differs from subsequent count cycles.

5. After a compare match is generated, the timer is cleared at the next count clock. Therefore, if the division ratio is large, the timer value may not be zero even if the timer value is read immediately after a match interrupt is generated.

(2) Compare register 4 (CM4)

CM4 and the TM4 register count value are compared, and an interrupt request signal (INTCM4) is generated when a match occurs. TM4 is cleared, synchronized with this match. If the CAE bit of the TMC4 register is set to 0, a reset is performed asynchronously, and the registers are initialized.

The CM4 register is configured with a master/slave configuration. When a write operation to a CM4 register is performed, data is first written to the master register and then the master register data is transferred to the slave register. In a compare operation, the slave register value is compared with the count value of the TM4 register. When a read operation to a CM4 register is performed, data in the master side is read out.

CM4 can be read/written in 16-bit units.

Figure 9-136. Compare Register 4 (CM4)

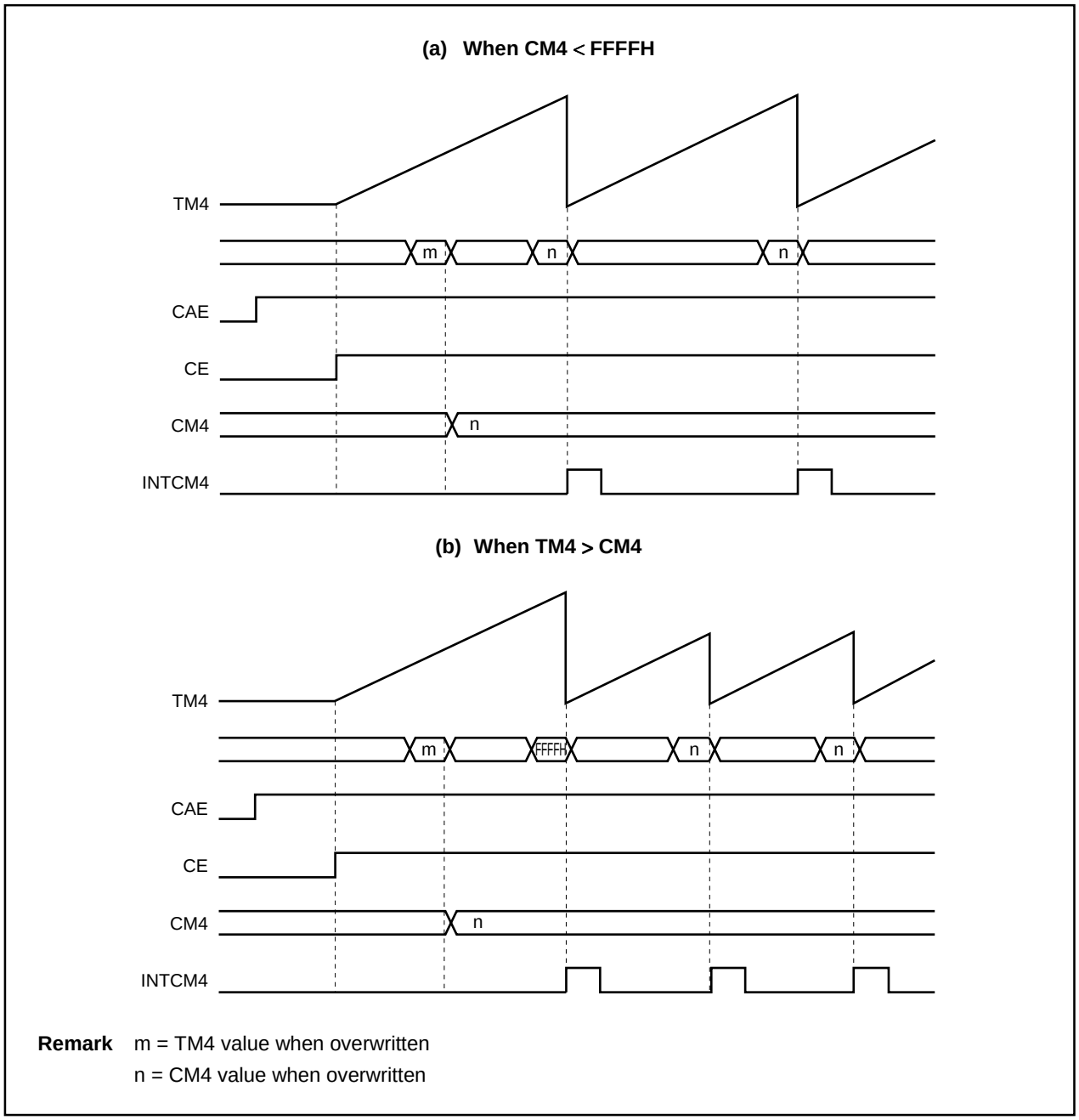
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CM4																	FFFFF542H	0000H

Cautions 1. A write operation to a CM4 register requires ϕ/4 clocks until the value that was set in the CM4 register is transferred to internal units. When writing continuously to the CM4 register, be sure to reserve a time interval of at least ϕ/4 clocks.

2. The CM4 register can be overwritten only once in a single TM4 register cycle (from 0000H until an INTCM4 interrupt is generated due to a match of the TM4 register and CM4 register). If this cannot be secured by the application, make sure that the CM4 register is not overwritten during timer operation.

3. Note that an INTCM4 interrupt will be generated after an overflow if a value less than the counter value is written in the CM4 register during TM4 register operation (Figure 9-137).

Figure 9-137. Example of Timing During TM4 Operation



Remark m = TM4 value when overwritten
n = CM4 value when overwritten

9.5.4 Control register

(1) Timer control register 4 (TMC4)

The TMC4 register controls the operation of timer 4.

This register can be read/written in 8- or 1-bit units.

Caution The CAE bit and CE bit cannot be set at the same time. Be sure to set the CAE bit prior to setting the CE bit.

Figure 9-138. Timer Control Register 4 (TMC4)

	7	6	5	4	3	2	1	0	Address	Initial value
TMC4	0	CS2	CS1	CS0	0	0	CE	CAE	FFFFF544H	00H

Bit Position	Bit Name	Function
6 to 4	CS2 to CS0	Selects the TM4 count clock. CS2 / CS1 / CS0 / Count Clock 0 / 0 / 0 / ϕ/4 0 / 0 / 1 / ϕ/8 0 / 1 / 0 / ϕ/16 0 / 1 / 1 / ϕ/32 1 / 0 / 0 / ϕ/64 1 / 0 / 1 / ϕ/128 1 / 1 / 0 / ϕ/256 1 / 1 / 1 / ϕ/512 **Caution Do not change the CS2 to CS0 bits during timer operation. If they are to be changed, they must be changed after setting the CE bit to 0. If the CS2 to CS0 bits are overwritten during timer operation, the operation is not guaranteed.**
1	CE	Controls the operation of TM4. 0: Disable count (timer stopped at 0000H and does not operate) 1: Perform count operation **Caution CE bit is not cleared even if a match is detected by the compare operation. To stop the count operation, clear the CE bit.**
0	CAE	Controls the internal count clock. 0: Asynchronously reset entire TM4 unit. Stop base clock (f_{CLK}) supply to TM4 unit. 1: Supply base clock (f_{CLK}) to TM4 unit. **Cautions 1. When CAE = 0 is set, the TM4 unit can be reset asynchronously.** **2. When CAE = 0, the TM4 unit is in a reset state. To operate TM4, first set CAE = 1.** **3. When the CAE bit is changed from 1 to 0, all the registers of the TM4 unit are initialized. When again setting CAE = 1, be sure to then again set all the registers of the TM4 unit.**

9.5.5 Operation

(1) Compare operation

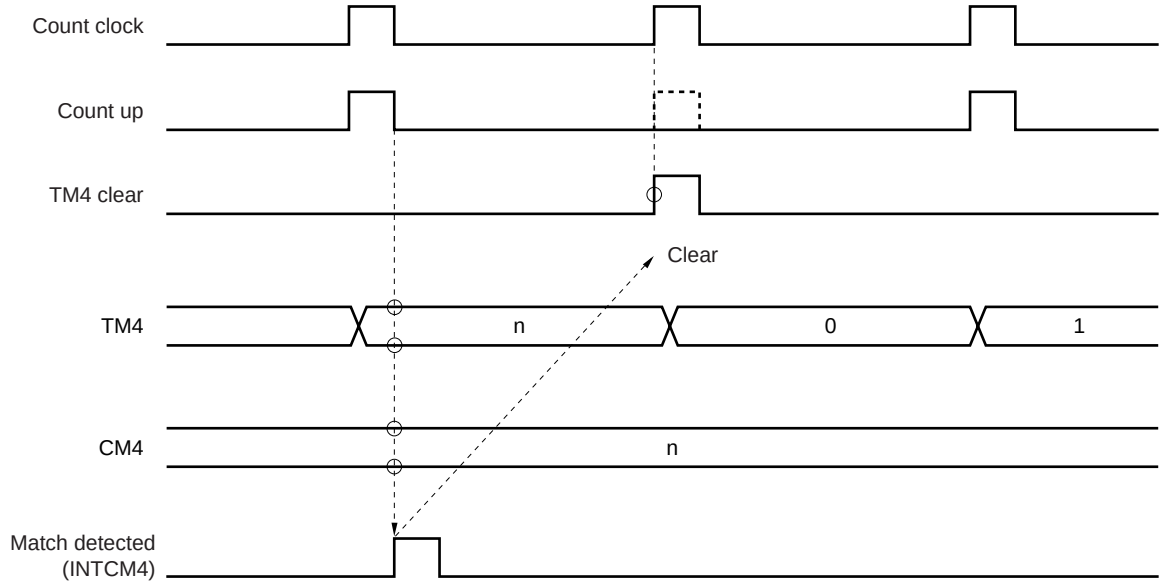
TM4 can be used for a compare operation in which the value that was set in a compare register (CM4) is compared with the TM4 count value.

If a match is detected by the compare operation, an interrupt (INTCM4) is generated. The generation of the interrupt causes TM4 to be cleared (0) at the next count timing. This function enables timer 4 to be used as an interval timer.

CM4 can also be set to 0. In this case, when an overflow occurs and TM4 becomes 0, a match is detected and INTCM4 is generated. Although the TM4 value is cleared (0) at the next count timing, INTCM4 is not generated according to this match.

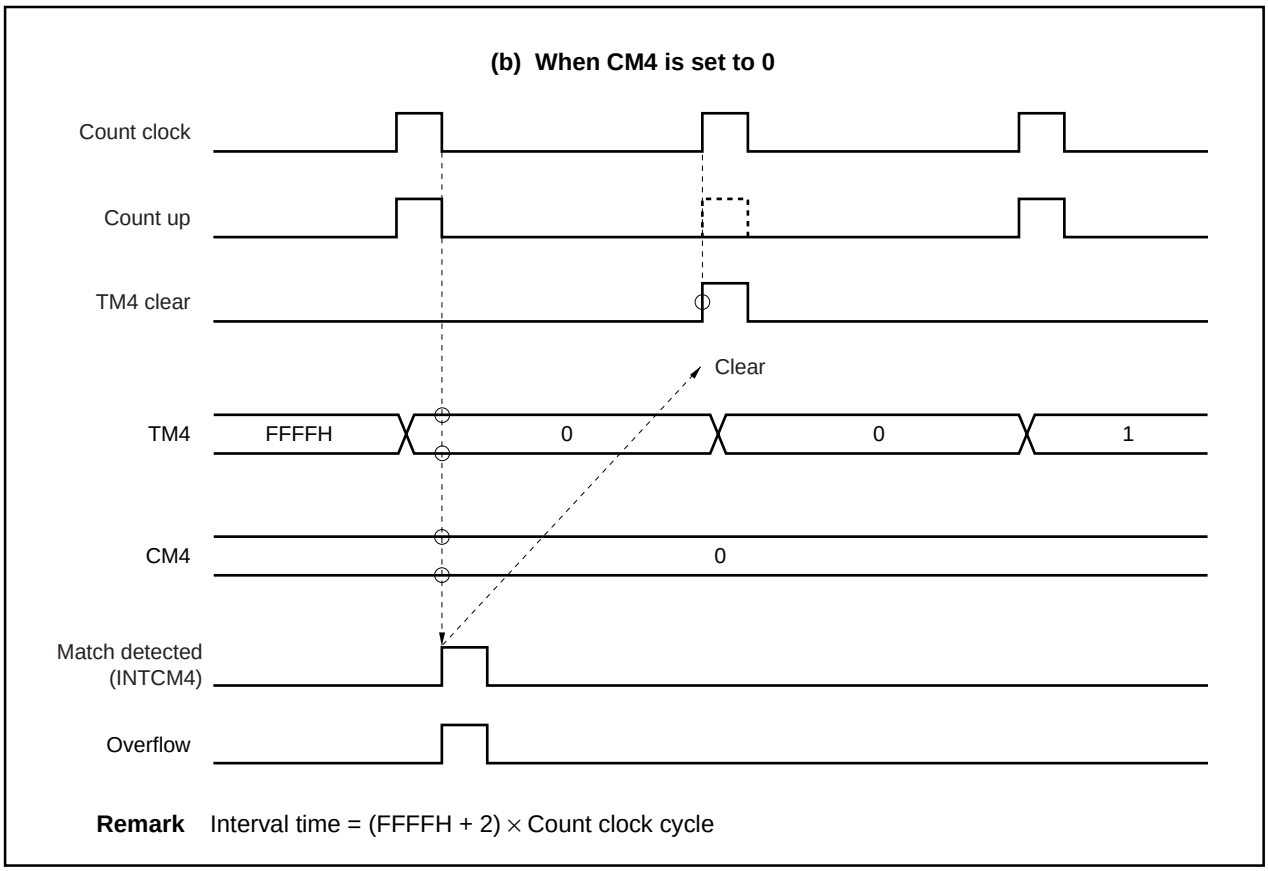
Figure 9-139. TM4 Compare Operation Example (1/2)

(a) When CM4 is set to n (non-zero)



Remark Interval time = (n + 1) × Count clock cycle
n = 1 to 65536 (FFFFH)

Figure 9-139. TM4 Compare Operation Example (2/2)



Remark Interval time = (FFFFH + 2) × Count clock cycle

9.5.6 Application example

(1) Interval timer

This section explains an example in which timer 4 is used as an interval timer with 16-bit precision.
Interrupt requests (INTCM4) are output at equal intervals (refer to **Figure 9-139 TM4 Compare Operation Example**). The setup procedure is shown below.

<1> Set (1) the CAE bit.
<2> Set each register.
- Select the count clock using the CS2 to CS0 bits of the TMC4 register.
- Set the compare value in the CM4 register.

<3> Start counting by setting (1) the CE bit.
<4> If the TM4 register and CM4 register values match, an INTCM4 interrupt is generated.
<5> INTCM4 interrupts are generated thereafter at equal intervals.

9.5.7 Precautions

Various precautions concerning timer 4 are shown below.

(1) To operate TM4, first set (1) the CAE bit of the TMC4 register.

(2) Up to ϕ/4 clocks are required after a value is set in the CE bit of the TMC4 register until the set value is transferred to internal units. When a count operation begins, the count cycle from 0000H to 0001H differs from subsequent count cycles.

(3) To initialize the TM4 register status and start counting again, clear (0) the CE bit and then set (1) the CE bit after an interval of ϕ/4 clocks has elapsed.

(4) Up to ϕ/4 clocks are required until the value that was set in the CM4 register is transferred to internal units. When writing continuously to the CM4 register, be sure to secure a time interval of at least ϕ/4 clocks.

(5) The CM4 register can be overwritten only once during a timer/counter operation (from 0000H until an INTCM4 interrupt is generated due to a match of the TM4 register and CM4 register). If this cannot be secured, make sure that the CM4 register is not overwritten during a timer/counter operation.

(6) The count clock must not be changed during a timer operation. If it is to be overwritten, it should be overwritten after the CE bit is cleared (0). If the count clock is overwritten during a timer operation, operation cannot be guaranteed.

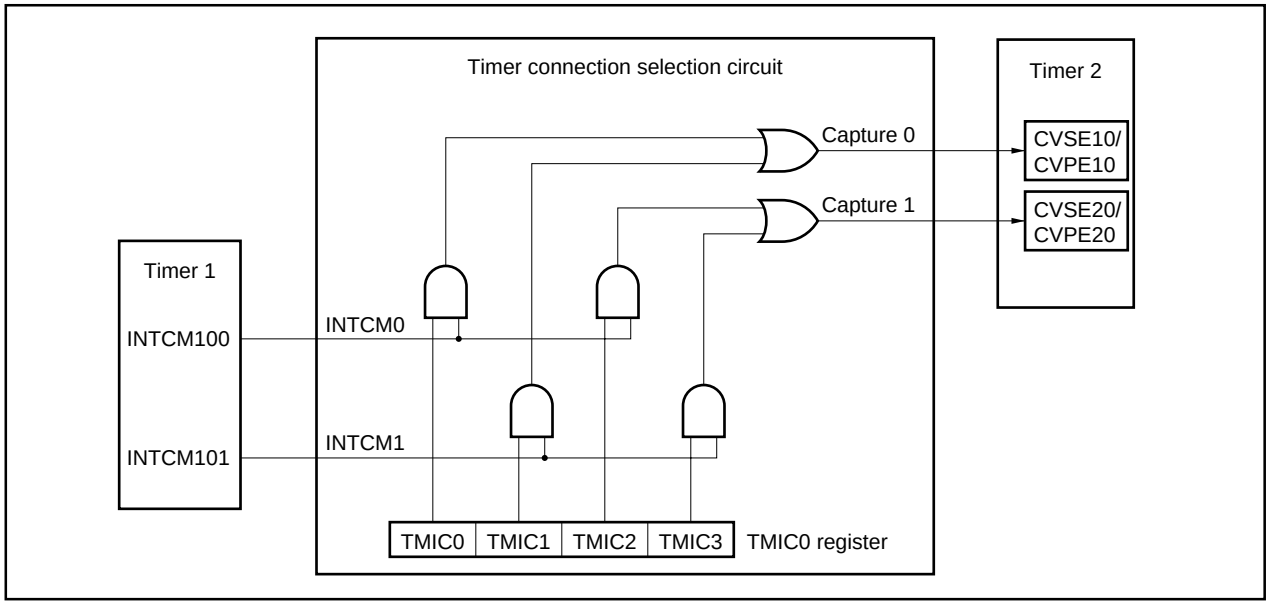
(7) An INTCM4 interrupt will be generated after an overflow if a value less than the counter value is written in the CM4 register during TM4 register operation.

9.6 Timer Connection Function

9.6.1 Overview

The V850E/IA1 provides a function to connect timer 1 and timer 2.

Figure 9-140. Block Diagram of Timer Connection Function



9.6.2 Control register

(1) Timer connection selection register 0 (TMIC0)

The TMIC0 register enables/disables input of the INTCM100, INTCM101 signals to the CVSEn0/CVPEn0 registers (n = 1, 2).

This register can be read/written in 8- or 1-bit units.

Figure 9-141. Timer Connection Selection Register 0 (TMIC0)

	7	6	5	4	3	2	1	0	Address	Initial value
TMIC0	0	0	0	0	TMIC3	TMIC2	TMIC1	TMIC0	FFFFF620H	00H

Bit Position	Bit Name	Function
3	TMIC3	Enables/disables input of INTCM101 signal to CVSE20/CVPE20 registers. 0: Don't input INTCM101 signal to CVSE20/CVPE20 registers. 1: Input INTCM101 signal to CVSE20/CVPE20 registers.
2	TMIC2	Enables/disables input of INTCM100 signal to CVSE20/CVPE20 registers. 0: Don't input INTCM100 signal to CVSE20/CVPE20 registers. 1: Input INTCM100 signal to CVSE20/CVPE20 registers.
1	TMIC1	Enables/disables input of INTCM101 signal to CVSE10/CVPE10 registers. 0: Don't input INTCM101 signal to CVSE10/CVPE10 registers. 1: Input INTCM101 signal to CVSE10/CVPE10 registers.
0	TMIC0	Enables/disables input of INTCM100 signal to CVSE10/CVPE10 registers. 0: Don't input INTCM100 signal to CVSE10/CVPE10 registers. 1: Input INTCM100 signal to CVSE10/CVPE10 registers.

[MEMO]

CHAPTER 10 SERIAL INTERFACE FUNCTION

10.1 Features

The serial interface function provides three types of serial interfaces combining a total of six transmit/receive channels. All six channels can be used simultaneously.

The three interface formats are as follows.

(1) Asynchronous serial interfaces (UART0 to UART2): 3 channels
(2) Clocked serial interfaces (CSI0, CSI1): 2 channels
(3) FCAN controller: 1 channel

Remark For details about the FCAN controller, refer to **CHAPTER 11 FCAN CONTROLLER**.

UART0 to UART2, whereby one byte of serial data is transmitted/received following a start bit, support full-duplex communication. In the UART1 and UART2 interfaces, one higher bit is added to 8 bits of transmit/receive data, enabling communication using 9-bit data.

CSI0 and CSI1 perform data transfer according to three types of signals, namely serial clocks ($\overline{SCK0}$, $\overline{SCK1}$), serial inputs (SI0, SI1), and serial outputs (SO0, SO1) (3-wire serial I/O).

FCAN conforms to CAN specification Ver. 2.0 Part B, and provides a 32-message buffer.

10.2 Asynchronous Serial Interface 0 (UART0)

10.2.1 Features

- Transfer rate: 300 bps to 1562.5 Kbps (using a dedicated baud rate generator and an internal system clock of 50 MHz)
- Full-duplex communications
  On-chip reception buffer register 0 (RXB0)
  On-chip transmission buffer register 0 (TXB0)
- Two-pin configuration[Note]
  TXD0: Transmit data output pin
  RXD0: Receive data input pin
- Reception error detection functions
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 3 types
  - Reception error interrupt (INTSER0): Interrupt is generated according to the logical OR of the three types of reception errors
  - Reception completion interrupt (INTSR0): Interrupt is generated when receive data is transferred from the shift register to the reception buffer register 0 after serial transfer is completed during a reception enabled state
  - Transmission completion interrupt (INTST0): Interrupt is generated when the serial transmission of transmit data (8 or 7 bits) from the shift register is completed
- The character length of transmit/receive data is specified according to the ASIM0 register
- Character length: 7 or 8 bits
- Parity functions: Odd, even, 0, or none
- Transmission stop bits: 1 or 2 bits
- On-chip dedicated baud rate generator

Note The SCK and CTS pins are not available for UART0.

10.2.2 Configuration

UART0 is controlled by the asynchronous serial interface mode register 0 (ASIM0), asynchronous serial interface status register 0 (ASIS0), and asynchronous serial interface transmission status register 0 (ASIF0). Receive data is maintained in the reception buffer register 0 (RXB0), and transmit data is written to the transmission buffer register 0 (TXB0).

Figure 10-1 shows the configuration of the asynchronous serial interface 0 (UART0).

(1) Asynchronous serial interface mode register 0 (ASIM0)

The ASIM0 register is an 8-bit register for specifying the operation of the asynchronous serial interface.

(2) Asynchronous serial interface status register 0 (ASIS0)

The ASIS0 register consists of a set of flags that indicate the error contents when a reception error occurs. The various reception error flags are set (1) when a reception error occurs and are reset (0) when the ASIS0 register is read.

(3) Asynchronous serial interface transmission status register 0 (ASIF0)

The ASIF0 register is an 8-bit register that indicates the status when a transmit operation is performed.

This register consists of a transmission buffer data flag, which indicates the hold status of TXB0 data, and the transmission shift register data flag, which indicates whether transmission is in progress.

(4) Reception control parity check

The receive operation is controlled according to the contents set in the ASIM0 register. A check for parity errors is also performed during a receive operation, and if an error is detected, a value corresponding to the error contents is set in the ASIS0 register.

(5) Reception shift register

This is a shift register that converts the serial data that was input to the RXD0 pin to parallel data. One byte of data is received, and if a stop bit is detected, the receive data is transferred to the reception buffer register 0 (RXB0).

This register cannot be directly manipulated.

(6) Reception buffer register 0 (RXB0)

RXB0 is an 8-bit buffer register for holding receive data. When 7 characters are received, 0 is stored in the MSB.

During a reception enabled state, receive data is transferred from the reception shift register to the RXB0, synchronized with the end of the shift-in processing of one frame.

Also, the reception completion interrupt request (INTSR0) is generated by the transfer of data to the RXB0.

(7) Transmission shift register

This is a shift register that converts the parallel data that was transferred from the transmission buffer register 0 (TXB0) to serial data.

When one byte of data is transferred from the TXB0, the shift register data is output from the TXD0 pin.

This register cannot be directly manipulated.

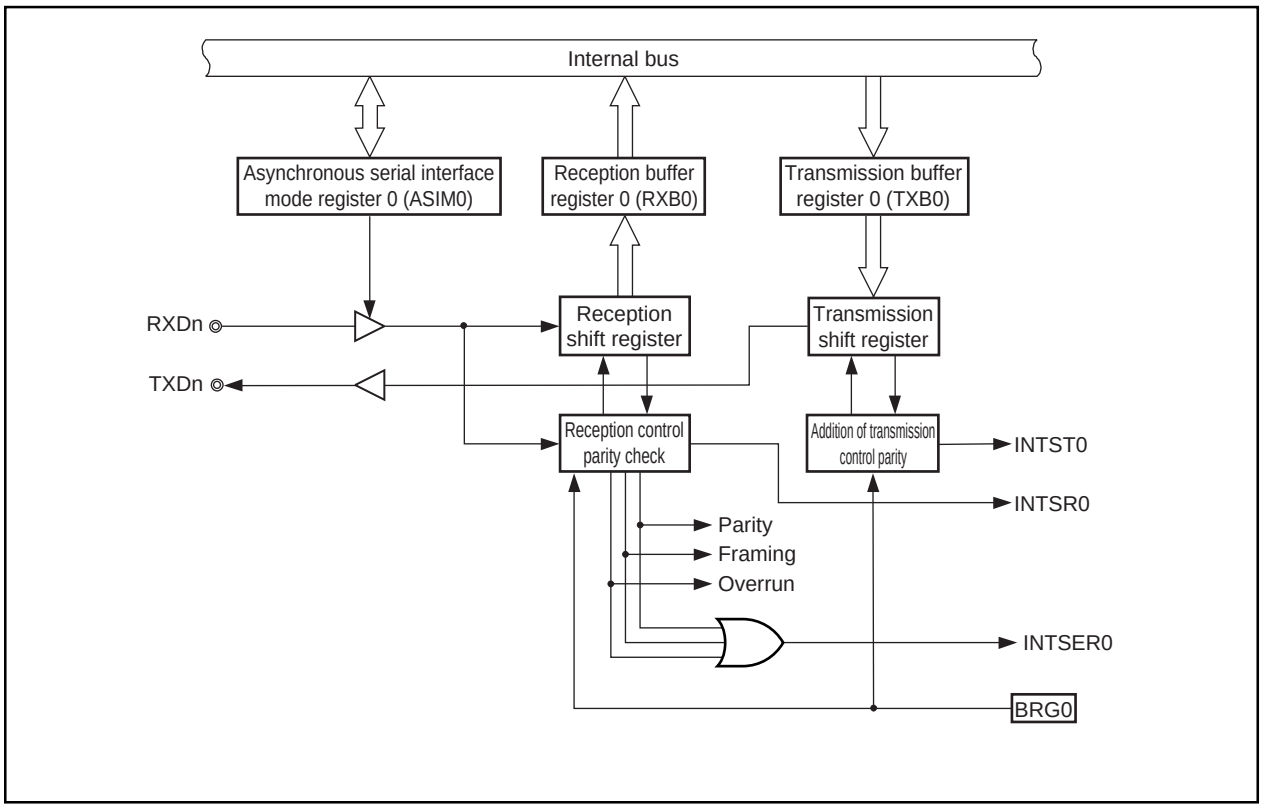
(8) Transmission buffer register 0 (TXB0)

TXB0 is an 8-bit buffer for transmit data. A transmit operation is started by writing transmit data to TXB0. The transmission completion interrupt request (INTST0) is generated synchronized with the completion of transmission of one frame.

(9) Addition of transmission control parity

A transmit operation is controlled by adding a start bit, parity bit, or stop bit to the data that is written to the TXB0 register, according to the contents that were set in the ASIM0 register.

Figure 10-1. Asynchronous Serial Interface 0 Block Diagram



10.2.3 Control registers

(1) Asynchronous serial interface mode register 0 (ASIM0)

The ASIM0 register is an 8-bit register that controls the UART0 transfer operation.

This register can be read/written in 8 bit or 1-bit units.

Figure 10-2. Asynchronous Serial Interface Mode Register 0 (ASIM0) (1/3)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIM0	CAE	TXE	RXE	PS1	PS0	CL	SL	ISRM	FFFFFA00H	01H

Bit Position	Bit Name	Function
7	CAE	Enables/disables clock operation. 0: Disable clock operation (reset internal circuit asynchronously.) 1: Enable clock operation UART0 operation clock control and asynchronous reset of the internal circuit are performed with the CAE bit. When the CAE bit is set to 0, the UART0 operation clock stops (fixed to low level), and an asynchronous reset is applied to internal UART0 latch. The TXD0 pin output is low level when the CAE bit = 0, and high level when the CAE bit = 1. Therefore, perform CAE setting in combination with port 3 mode register (PM3) so as to avoid malfunction on the other side at startup (Set the port to the output mode after setting the CAE bit to 1). Input from the RXD0 pin is fixed to high level with CAE bit = 0.
6	TXE	Enables/disables transfer. 0: Disable transfer (Perform synchronized reset of transfer circuit.) 1: Enable transfer **Cautions 1. Set the TXE bit to 1 after setting the CAE bit to 1 when starting transfer. Set the CAE bit to 0 after setting the TXE bit to 0 when stopping transfer.** **2. To initialize the transfer unit, clear (0) the TXE bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the TXE bit again. If the TXE bit is not set again, initialization may not be successful. (For details about the base clock, refer to 10.2.6 (1) (a) Base clock (Clock).)**

Figure 10-2. Asynchronous Serial Interface Mode Register 0 (ASIM0) (2/3)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>5</td><td>RXE</td><td>Enables/disables reception.
0: Disable reception (Perform synchronous reset of reception circuit)
1: Enable reception

Cautions 1. Set the RXE bit to 1 after setting the CAE bit to 1 when starting transfer. Set the CAE bit to 0 after setting the RXE bit to 0 when stopping transfer.
2. To initialize the reception unit status, clear (0) the RXE bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the RXE bit again. If the RXE bit is not set again, initialization may not be successful. (For details about the base clock, refer to 10.2.6 (1) (a) Base clock (Clock).)</td></tr>
<tr><td>4, 3</td><td>PS1, PS0</td><td>Controls parity bit.

<table>
<tr><th>PS1</th><th>PS0</th><th>Transmit Operation</th><th>Receive Operation</th></tr>
<tr><td>0</td><td>0</td><td>Don’t output parity bit</td><td>Receive with no parity</td></tr>
<tr><td>0</td><td>1</td><td>Output 0 parity</td><td>Receive as 0 parity</td></tr>
<tr><td>1</td><td>0</td><td>Output odd parity</td><td>Judge as odd parity</td></tr>
<tr><td>1</td><td>1</td><td>Output even parity</td><td>Judge as even parity</td></tr>
</table>
Cautions 1. To overwrite the PS1 and PS0 bits, first clear (0) the TXE and RXE bits.
2. If “0 parity” is selected for reception, no parity judgment is performed. Therefore, no error interrupt is generated because the PE bit of the ASIS0 register is not set.

• Even parity
If the transmit data contains an odd number of bits with the value “1”, the parity bit is set (1). If it contains an even number of bits with the value “1”, the parity bit is cleared (0). This controls the number of bits with the value “1” contained in the transmit data and the parity bit so that it is an even number.
During reception, the number of bits with the value “1” contained in the receive data and the parity bit is counted, and if the number is odd, a parity error is generated.

• Odd parity
In contrast to even parity, odd parity controls the number of bits with the value “1” contained in the transmit data and the parity bit so that it is an odd number.
During reception, the number of bits with the value “1” contained in the receive data and the parity bit is counted, and if the number is even, a parity error is generated.</td></tr>
</table>

Remark When reception is disabled, the reception shift register does not detect a start bit. No shift-in processing or transfer processing to the reception buffer register 0 (RXB0) is performed, and the contents of the RXB0 register are retained.

When reception is enabled, the reception shift operation starts, synchronized with the detection of the start bit, and when the reception of one frame is completed, the contents of the reception shift register are transferred to the RXB0 register. A reception completion interrupt (INTSR0) is also generated in synchronization with the transfer to the RXB0 register.

Figure 10-2. Asynchronous Serial Interface Mode Register 0 (ASIM0) (3/3)

Bit Position	Bit Name	Function
4, 3	PS1, PS0	• 0 parity During transmission, the parity bit is cleared (0) regardless of the transmit data. During reception, no parity error is generated because no parity bit is checked. • No parity No parity bit is added to transmit data. During reception, the receive data is considered to have no parity bit. No parity error is generated because there is no parity bit.
2	CL	Specifies character length of transmit/receive data. 0: 7 bits 1: 8 bits **Caution To overwrite the CL bit, first clear (0) the TXE and RXE bits.**
1	SL	Specifies stop bit length of transmit data. 0: 1 bit 1: 2 bits **Cautions 1. To overwrite the SL bit, first clear (0) the TXE bit.** **2. Since reception is always done using a single stop bit, the SL bit setting does not affect receive operations.**
0	ISRM	Enables/disables generation of reception completion interrupt requests when an error occurs. 0: Generate a reception error interrupt request (INTSER0) as an interrupt when an error occurs. In this case, no reception completion interrupt request (INTSR0) is generated. 1: Generate a reception completion interrupt request (INTSR0) as an interrupt when an error occurs. In this case, no reception error interrupt request (INTSER0) is generated. **Caution To overwrite the ISRM bit, first clear (0) the RXE bit.**

(2) Asynchronous serial interface status register 0 (ASIS0)

The ASIS0 register, which consists of 3-bit error flags (PE, FE and OVE), indicates the error status when UART0 reception is completed.

The status flag, which indicates a reception error, always indicates the status of the error that occurred most recently. That is, if the same error occurred several times before the receive data was read, this flag would hold only the status of the error that occurred last.

The ASIS0 register is cleared to 00H by a read operation. When a reception error occurs, the reception buffer register 0 (RXB0) should be read and the error flag should be cleared after the ASIS0 register is read.

This register is read-only in 8-bit or 1-bit units.

Caution When the CAE bit or RXE bit of the ASIM0 register is set to 0, or when the ASIS0 register is read, the PE, FE, and OVE bits of the ASIS0 register are cleared (0).

Figure 10-3. Asynchronous Serial Interface Status Register 0 (ASIS0)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIS0	0	0	0	0	0	PE	FE	OVE	FFFFFA03H	00H

Bit Position	Bit Name	Function
2	PE	This is a status flag that indicates a parity error. 0: When the ASIM0 register's CAE and RXE bits are both set to 0, or when the ASIS0 register has been read 1: When reception was completed, the transmit data parity did not match the parity bit **Caution The operation of the PE bit differs according to the settings of the PS1 and PS0 bits of the ASIM0 register.**
1	FE	This is a status flag that indicates a framing error. 0: When the ASIM0 register's CAE and RXE bits are both set to 0, or when the ASIS0 register has been read 1: When reception was completed, no stop bit was detected **Caution For receive data stop bits, only the first bit is checked regardless of the number of stop bits.**
0	OVE	This is a status flag that indicates an overrun error. 0: When the ASIM0 register's CAE and RXE bits are both 0, or when the the ASIS0 register has been read. 1: UART0 completed the next receive operation before reading the RXB0 receive data. **Caution When an overrun error occurs, the next receive data value is not written to the RXB0 register and the data is discarded.**

(3) Asynchronous serial interface transmission status register 0 (ASIF0)

The ASIF0 register, which consists of 2-bit status flags, indicates the status during transmission.

By writing the next data to the TXB0 register after data is transferred from the TXB0 register to the transmission shift register, transmit operations can be performed continuously without suspension even during an interrupt interval. When transmission is performed continuously, data should be written after referencing the ASIF0 register to prevent writing to the TXB0 register by mistake.

This register is read-only in 8-bit or 1-bit units.

Figure 10-4. Asynchronous Serial Interface Transmit Status Register 0 (ASIF0)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIF0	0	0	0	0	0	0	TXBF0	TXSF0	FFFFFA05H	00H

Bit Position	Bit Name	Function
1	TXBF	This is a transmission buffer data flag. 0: When the ASIM0 register's CAE or TXE bits is 0, or when data has been transferred to the transmission shift register (Data to be transferred next to TXB0 register does not exist). 1: Data exists in TXB0 register when the TXB0 register has been written to (Data to be transferred next exists in TXB0 register).
0	TXSF	This is a transmission shift register data flag. It indicates the transmission status of UART0. 0: When the ASIM0 register's CAE or TXE bits is set to 0, or when following transfer completion, the next data transfer from the TXB0 register is not performed (waiting transmission) 1: When data has been transferred from the TXB0 register (Transmission in progress)

The following table shows relationships between the transmission status and write operations to TXB0 register.

TXBF	TXSF	Transmission Status	Write Operation to TXB0
0	0	Initial status or transmission completed	Writing is permitted
0	1	Transmission in progress (no data is in TXB0)	Writing is permitted
1	0	Waiting transmission (data is in TXB0)	Writing is not permitted
1	1	Transmission in progress (data is in TXB0)	Writing is not permitted

Caution When transmission is performed continuously, data should be written to TXB0 register after confirming the TXBF bit value. If writing is not enabled, transmit data cannot be guaranteed when data is written to TXB0 register.

(4) Reception buffer register (RXB0)

The RXB0 register is an 8-bit buffer register for storing parallel data that had been converted by the reception shift register.

When reception is enabled (RXE bit = 1 in the ASIM0 register), receive data is transferred from the reception shift register to the RXB0 register, synchronized with the completion of the shift-in processing of one frame. Also, a reception completion interrupt request (INTSR0) is generated by the transfer to the RXB0 register. For information about the timing for generating this interrupt request, refer to **10.2.5 (4) Receive operation**.

If reception is disabled (RXE bit = 0 in the ASIM0 register), the contents of the RXB0 register are retained, and no processing is performed for transferring data to the RXB0 register even when the shift-in processing of one frame is completed. Also, no reception completion interrupt is generated.

When 7 bits is specified for the data length, bits 6 to 0 of the RXB0 register are transferred for the receive data and the MSB (bit 7) is always 0. However, if an overrun error (OVE) occurs, the receive data at that time is not transferred to the RXB0 register.

Except when a reset is input, the RXB0 register becomes FFH even when CAE bit = 0 in the ASIM0 register.

This register is read-only in 8-bit or 1-bit units.

Figure 10-5. Reception Buffer Register 0 (RXB0)

	7	6	5	4	3	2	1	0	Address	Initial value
RXB0	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0	FFFFFA02H	FFH

Bit Position	Bit Name	Function
7 to 0	RXB7 to RXB0	Stores receive data. 0 can be read for RXB7 when 7-bit or character data is received.

(5) Transmission buffer register 0 (TXB0)

The TXB0 register is an 8-bit buffer register for setting transmit data.

When transmission is enabled (TXE bit = 1 in the ASIM0 register), the transmit operation is started by writing data to TXB0 register.

When transmission is disabled (TXE bit = 0 in the ASIM0 register), even if data is written to TXB0 register, the value is ignored.

The TXB0 register data is transferred to the transmission shift register, and a transmission completion interrupt request (INTST0) is generated, synchronized with the completion of the transmission of one frame from the transmission shift register. For information about the timing for generating this interrupt request, refer to **10.2.5 (2) Transmit operation**.

When TXBF bit = 1 in the ASIF0 register, writing must not be performed to TXB0 register.

This register can be read or written in 8-bit or 1-bit units.

Figure 10-6. Transmission Buffer Register 0 (TXB0)

	7	6	5	4	3	2	1	0	Address	Initial value
TXB0	TXB7	TXB6	TXB5	TXB4	TXB3	TXB2	TXB1	TXB0	FFFFFA04H	FFH

Bit Position	Bit Name	Function
7 to 0	TXB7 to TXB0	Writes transmit data.

10.2.4 Interrupt requests

The following three types of interrupt requests are generated from UART0.

- Reception error interrupt (INTSER0)
- Reception completion interrupt (INTSR0)
- Transmission completion interrupt (INTST0)

The default priorities among these three types of interrupt requests is, from high to low, reception error interrupt, reception completion interrupt, and transmission completion interrupt.

Table 10-1. Generated Interrupts and Default Priorities

Interrupt	Priority
Reception error	1
Reception completion	2
Transmission completion	3

(1) Reception error interrupt (INTSER0)

When reception is enabled, a reception error interrupt is generated according to the logical OR of the three types of reception errors explained for the ASIS0 register. Whether a reception error interrupt (INTSER0) or a reception completion interrupt (INTSR0) is generated when an error occurs can be specified according to the ISRM bit of the ASIM0 register.

When reception is disabled, no reception error interrupt is generated.

(2) Reception completion interrupt (INTSR0)

When reception is enabled, a reception completion interrupt is generated when data is shifted in to the reception shift register and transferred to the reception buffer register 0 (RXB0).

A reception completion interrupt request can be generated in place of a reception error interrupt according to the ISRM bit of the ASIM0 register even when a reception error has occurred.

When reception is disabled, no reception completion interrupt is generated.

(3) Transmission completion interrupt (INTST0)

A transmission completion interrupt is generated when one frame of transmit data containing 7-bit or 8-bit characters is shifted out from the transmission shift register.

10.2.5 Operation

(1) Data format

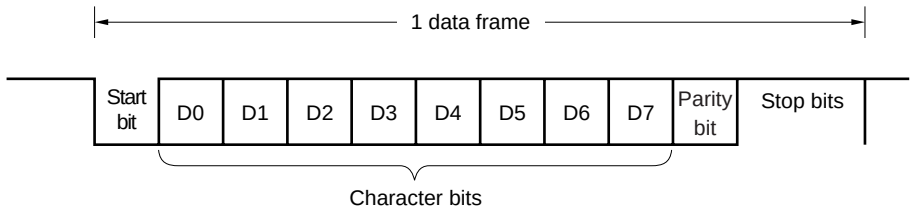
Full-duplex serial data transmission and reception can be performed.

The transmit/receive data format consists of one data frame containing a start bit, character bits, a parity bit, and stop bits as shown in Figure 10-7.

The character bit length within one data frame, the type of parity, and the stop bit length are specified according to the asynchronous serial interface mode register 0 (ASIM0).

Also, data is transferred with LSB first.

Figure 10-7. Asynchronous Serial Interface Transmit/Receive Data Format



- Start bit ⋯ 1 bit
- Character bits ⋯ 7 bits or 8 bits
- Parity bit ⋯ Even parity, odd parity, 0 parity, or no parity
- Stop bits ⋯ 1 bit or 2 bits

(2) Transmit operation

When CAE bit is set to 1 in the ASIM0 register, a high level is output from the TXD0 pin.

Then, when TXE bit is set to 1 in the ASIM0 register, transmission is enabled, and the transmit operation is started by writing transmit data to transmission buffer register 0 (TXB0).

(a) Transmission enabled state

This state is set by the TXE bit in the ASIM0 register.

- TXE = 1: Transmission enabled state
- TXE = 0: Transmission disabled state

Since UART0 does not have a CTS (transmission enabled signal) input pin, a port should be used to confirm whether the destination is in a reception enabled state.

(b) Starting a transmit operation

In transmission enabled state, a transmit operation is started by writing transmit data to transmission buffer register 0 (TXB0). When a transmit operation is started, the data in TXB0 is transferred to transmission shift register. Then, the transmission shift register outputs data to the TXD0 pin (the transmit data is transferred sequentially starting with the start bit). The start bit, parity bit, and stop bits are added automatically.

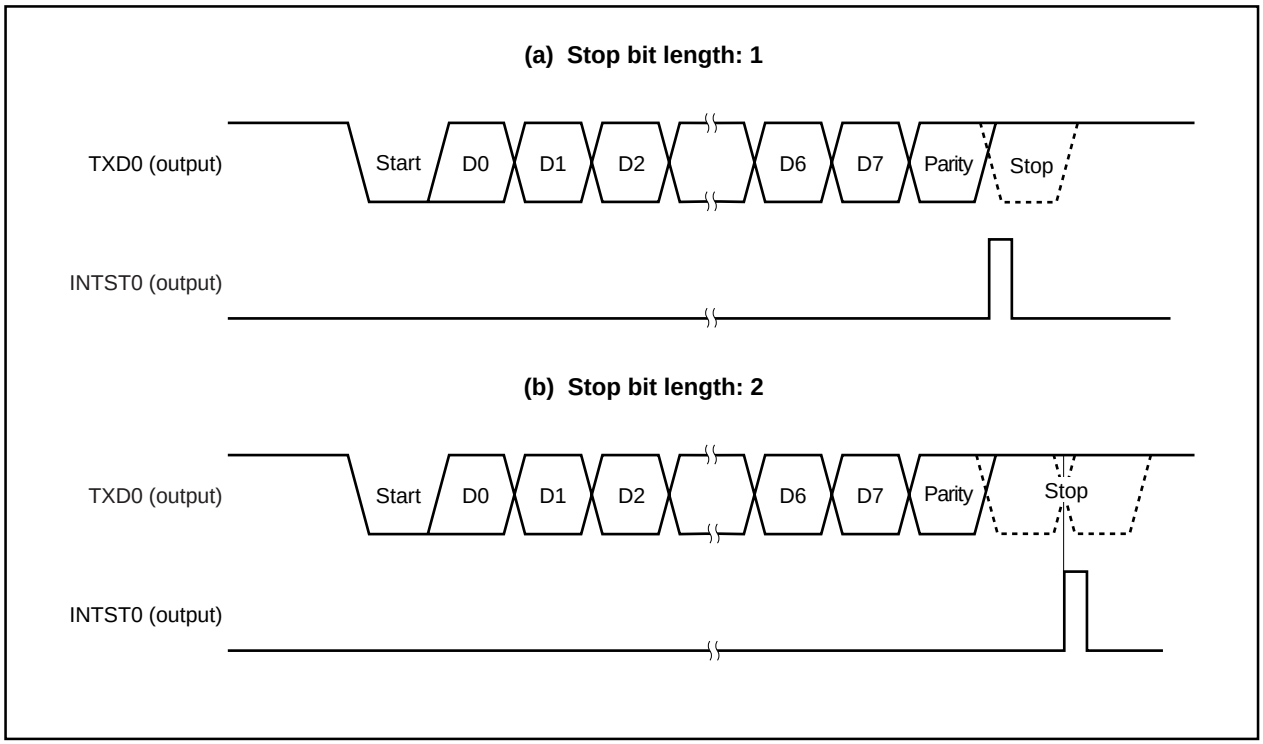
(c) Transmission interrupt request

When the transmission shift register becomes empty, a transmission completion interrupt request (INTST0) is generated. The timing for generating the INTST0 interrupt differs according to the specification of the number of stop bits. The INTST0 interrupt is generated at the same time that the last stop bit is output.

If the data to be transmitted next has not been written to the TXB0 register, the transmit operation is suspended.

Caution Normally, when the transmission shift register becomes empty, a transmission completion interrupt (INTST0) is generated. However, no transmission completion interrupt (INTST0) is generated if the transmission shift register becomes empty due to the input of a $\overline{\text{RESET}}$.

Figure 10-8. Asynchronous Serial Interface Transmission Completion Interrupt Timing



(3) Continuous transmission operation

UART0 can write the next transmit data to the TXB0 register at the time that the transmission shift register starts the shift operation. This enables an efficient transmission rate to be realized by continuously transmitting data even during the INTST0 interrupt service after the transmission of one data frame.

When continuous transmission is performed, data should be written after referencing the ASIF0 register to confirm the transmission status and whether or not data can be written to the TXB0 register.

Caution Transmit data should be written when the TXBF bit is 0. The transmission unit should be initialized when the TXSF bit is 0. If these actions are performed at other times, the transmit data cannot be guaranteed.

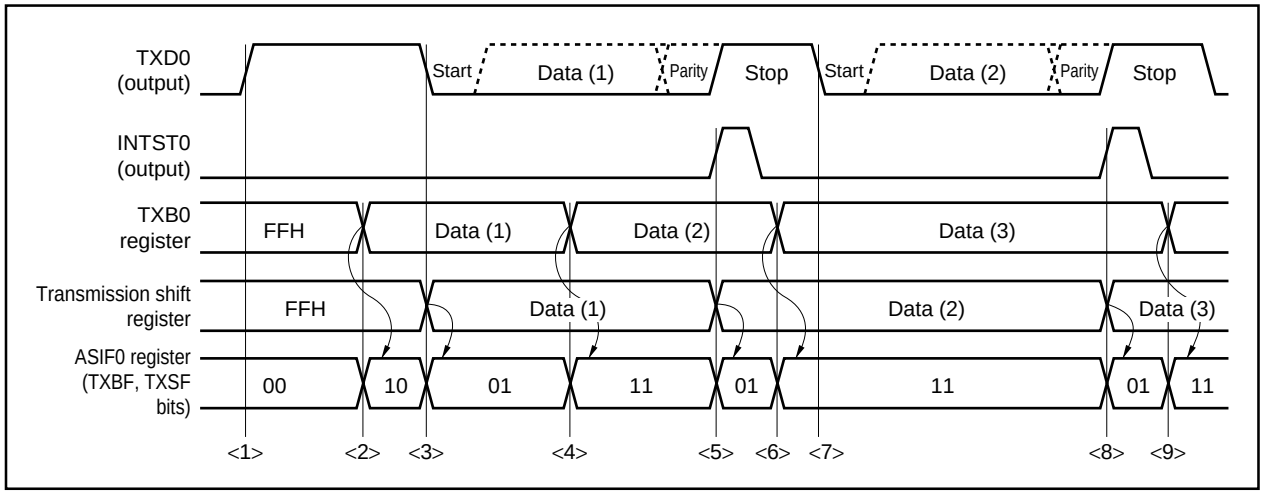
Table 10-2. Transmission Status and Whether or Not Writing Is Enabled

TXBF	TXSF	Transmission Status	Whether or not Write Operation to TXB0 is Enabled
0	0	Initial status or transmission completed	Writing is enabled
0	1	Transmission in progress (no data is in TXB0 register)	Writing is enabled
1	0	Awaiting transmission (data is in TXB0 register)	Writing is not enabled
1	1	Transmission in progress (data is in TXB0 register)	Writing is not enabled

(a) Starting procedure

Figure 10-9 shows the procedure to start continuous transmission.

Figure 10-9. Continuous Transmission Starting Procedure

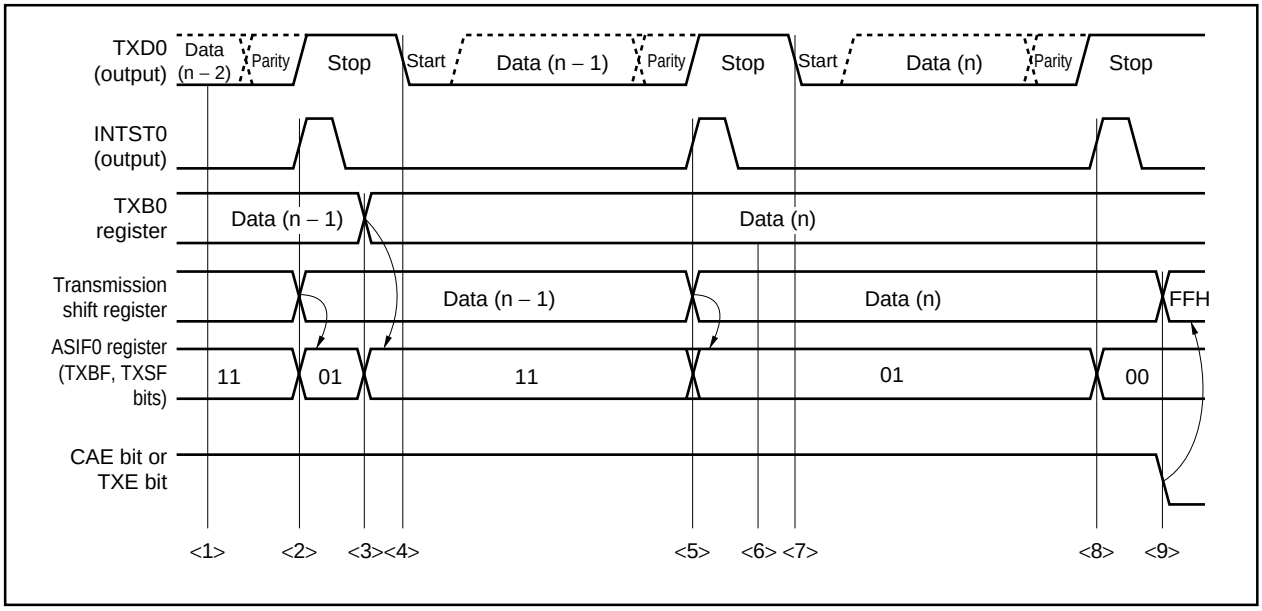


Transmission Starting Procedure	Internal Operation	ASIF0 Register	
		TXBF bit	TXSF bit
<1> Set transmission mode		0	0
<2> Write data (1) to TXB0 register		1	0
	<3> Generate start bit Start data (1) transmission	0	1
<4> Read ASIF0 register (confirm that TXBF bit = 0)			
Write data (2)		1	1
	<<Transmission in progress>>		
	<5> Generate transmission completion interrupt (INTST0)	0	1
<6> Read ASIF0 register (confirm that TXBF bit = 0)			
Write data (3)		1	1
	<7> Generate start bit Start data (2) transmission <<Transmission in progress>>		
	<8> Generate transmission completion interrupt (INTST0)	0	1
<9> Read ASIF0 register (confirm that TXBF bit = 0)			
Write data (4)		1	1

(b) Ending procedure

Figure 10-10 shows the procedure for ending continuous transmission.

Figure 10-10. Continuous Transmission End Procedure



Transmission End Procedure	Internal Operation	ASIF0 Register	
		TXBF Bit	TXSF Bit
	<1> Transmission of data (n – 2) is in progress	1	1
	<5> Generate transmission completion interrupt (INTST0)	0	1
<3> Read ASIF0 register (Confirm that TXBF bit = 0)			
Write data (n)		1	1
	<4> Generate start bit		
	Start data (n – 1) transmission		
	<<Transmission in progress>>		
	<5> Generate transmission completion interrupt (INTST0)	0	1
<6> Read ASIF0 register (Confirm that TXSF bit = 1)			
There is no write data			
	<7> Generate start bit		
	Start data (n) transmission		
	<<Transmission in progress>>		
	<8> Generate transmission completion interrupt (INTST0)	0	0
<9> Read ASIF0 register (Confirm that TXSF bit = 0)			
Clear (0) the CAE bit or TXE bit of ASIM0 register	Initialize internal circuits		

(4) Receive operation

An awaiting reception state is set by setting CAE bit to 1 in the ASIM0 register and then setting RXE bit to 1 in the ASIM0 register. To start a receive operation, detects a start bit first. The start bit is detected by sampling RXD0 pin. When the receive operation begins, serial data is stored sequentially in the reception shift register according to the baud rate that was set. A reception completion interrupt (INTSR0) is generated each time the reception of one frame of data is completed. Normally, the receive data is transferred from the reception buffer register 0 (RXB0) to memory by this interrupt servicing.

(a) Reception enabled state

The receive operation is set to reception enabled state by setting the RXE bit in the ASIM0 register to 1.

- RXE bit = 1: Reception enabled state
- RXE bit = 0: Reception disabled state

In reception disabled state, the reception hardware stands by in the initial state. At this time, the contents of the reception buffer register 0 (RXB0) are retained, and no reception completion interrupt or reception error interrupt is generated.

(b) Starting a receive operation

A receive operation is started by the detection of a start bit.

The RXD0 pin is sampled according to the serial clock from the baud rate generator 0 (BRG0).

(c) Reception completion interrupt

When RXE bit = 1 in the ASIM0 register and the reception of one frame of data is completed (the stop bit is detected), a reception completion interrupt (INTSR0) is generated and the receive data within the reception shift register is transferred to RXB0 at the same time.

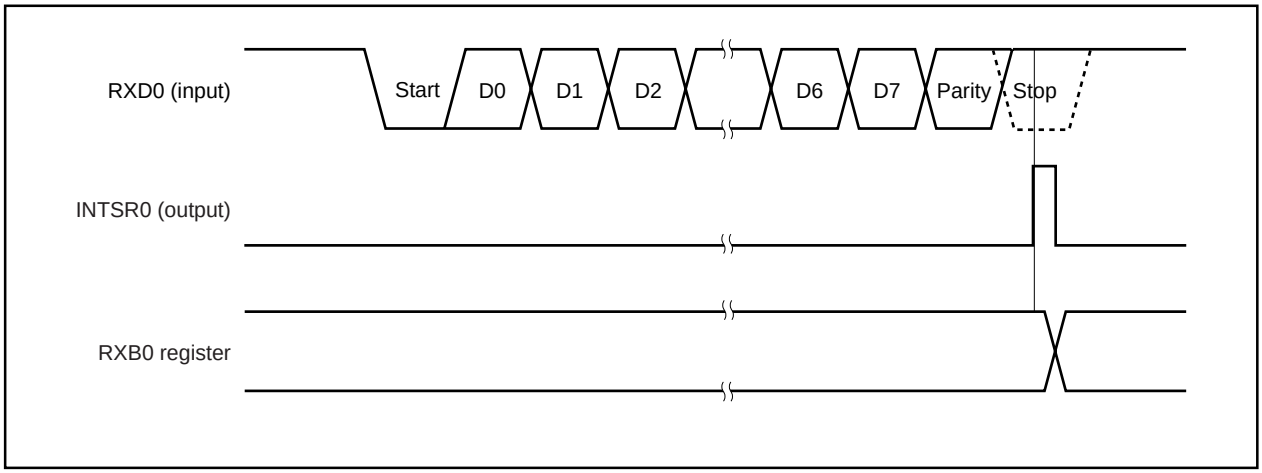
Also, if an overrun error (OVE) occurs, the receive data at that time is not transferred to the reception buffer register 0 (RXB0), and either a reception completion interrupt (INTSR0) or a reception error interrupt (INTSER0) is generated (the receive data within the reception shift register is transferred to RXB0) according to the ISRM bit setting in the ASIM0 register.

Even if a parity error (PE) or framing error (FE) occurs during a reception operation, the receive operation continues until stop bit is received, and after reception is completed, either a reception completion interrupt (INTSR0) or a reception error interrupt (INTSER0) is generated according to the ISRM bit setting in the ASIM0 register.

If the RXE bit is reset (0) during a receive operation, the receive operation is immediately stopped. The contents of the reception buffer register 0 (RXB0) and of the asynchronous serial interface status register (ASIS0) at this time do not change, and no reception completion interrupt (INTSR0) or reception error interrupt (INTSER0) is generated.

No reception completion interrupt is generated when RXE bit = 0 (reception is disabled).

Figure 10-11. Asynchronous Serial Interface Reception Completion Interrupt Timing



(5) Reception error

The three types of error that can occur during a receive operation are a parity error, framing error, or overrun error. The data reception result is that the various flags of the ASIS0 register are set (1), and a reception error interrupt (INTSER0) or a reception completion interrupt (INTSR0) is generated at the same time. The ISRM bit of the ASIM0 register specifies whether INTSER0 or INTSR0 is generated.

The type of error that occurred during reception can be detected by reading the contents of the ASIS0 register during the INTSER0 or INTSR0 interrupt servicing.

The contents of the ASIS0 register are reset (0) by reading the ASIS0 register.

Table 10-3. Reception Error Causes

Error Flag	Reception Error	Cause
PE	Parity error	The parity specification during transmission did not match the parity of the reception data
FE	Framing error	No stop bit was detected
OVE	Overrun error	The reception of the next data was completed before data was read from the reception buffer register 0 (RXB0)

(a) Separation of reception error interrupt

A reception error interrupt can be separated from the INTSR0 interrupt and generated as an INTSER0 interrupt by clearing the ISRM bit of the ASIM0 register to 0.

Figure 10-12. When Reception Error Interrupt Is Separated from INTSR0 Interrupt (ISRM Bit = 0)

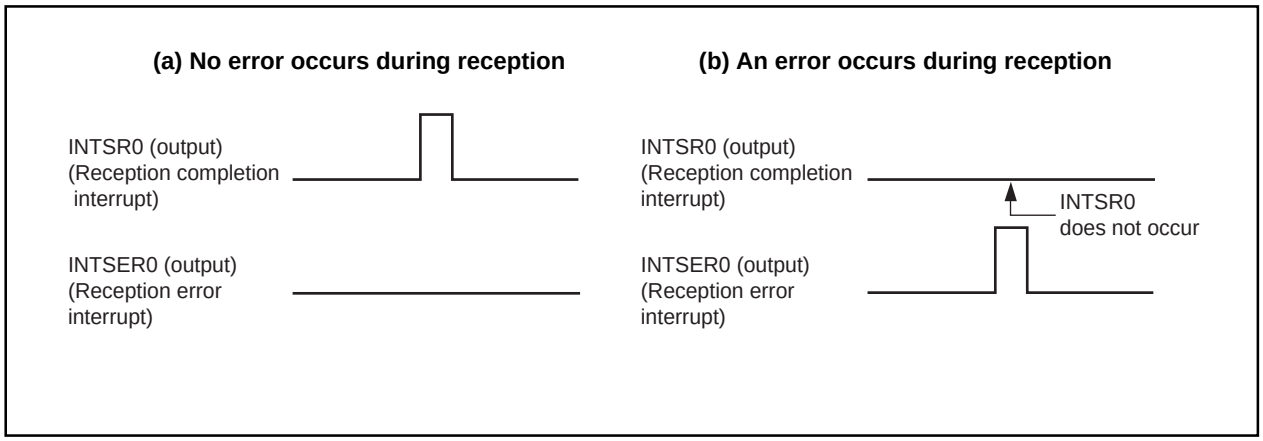
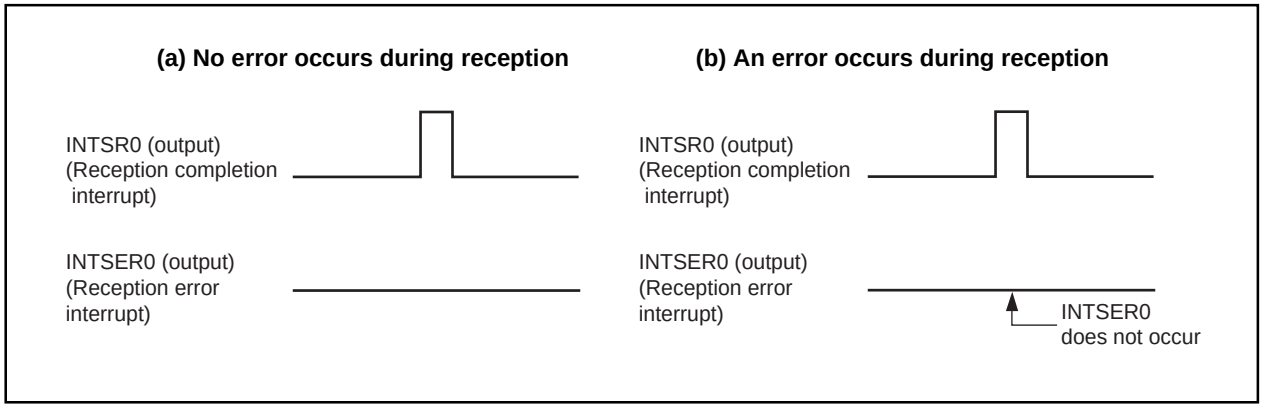


Figure 10-13. When Reception Error Interrupt Is Included in INTSR0 Interrupt (ISRM Bit = 1)



(6) Parity types and corresponding operation

A parity bit is used to detect a bit error in communication data. Normally, the same type of parity bit is used at the transmission and reception sides.

(a) Even parity

(i) During transmission

The parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is even. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 1
- If the number of bits with the value “1” within the transmit data is even: 0

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is odd.

(b) Odd parity

(i) During transmission

In contrast to even parity, the parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is odd. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 0
- If the number of bits with the value “1” within the transmit data is even: 1

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is even.

(c) 0 parity

During transmission the parity bit is set to “0” regardless of the transmit data.

During reception, no parity bit check is performed. Therefore, no parity error is generated regardless of whether the parity bit is “0” or “1”.

(d) No parity

No parity bit is added to the transmit data.

During reception, the receive operation is performed as if there were no parity bit. Since there is no parity bit, no parity error is generated.

(7) Receive data noise filter

The RXD0 signal is sampled at the rising edge of the prescaler output basic clock (Clock). If the same sampling value is obtained twice, the match detector output changes, and this output is sampled as input data. Therefore, data not exceeding one clock width is judged to be noise and is not delivered to the internal circuit (see Figure 10-15). Refer to **10.2.6 (1) (a) Basic clock (Clock)** regarding the basic clock.

Also, since the circuit is configured as shown in Figure 10-14, internal processing during a receive operation is delayed by up to 2 clocks according to the external signal status.

Figure 10-14. Noise Filter Circuit

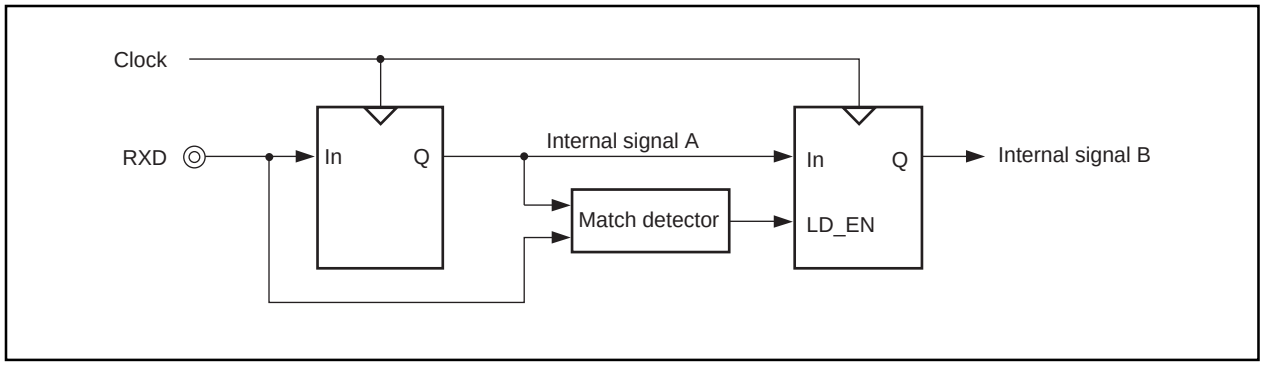
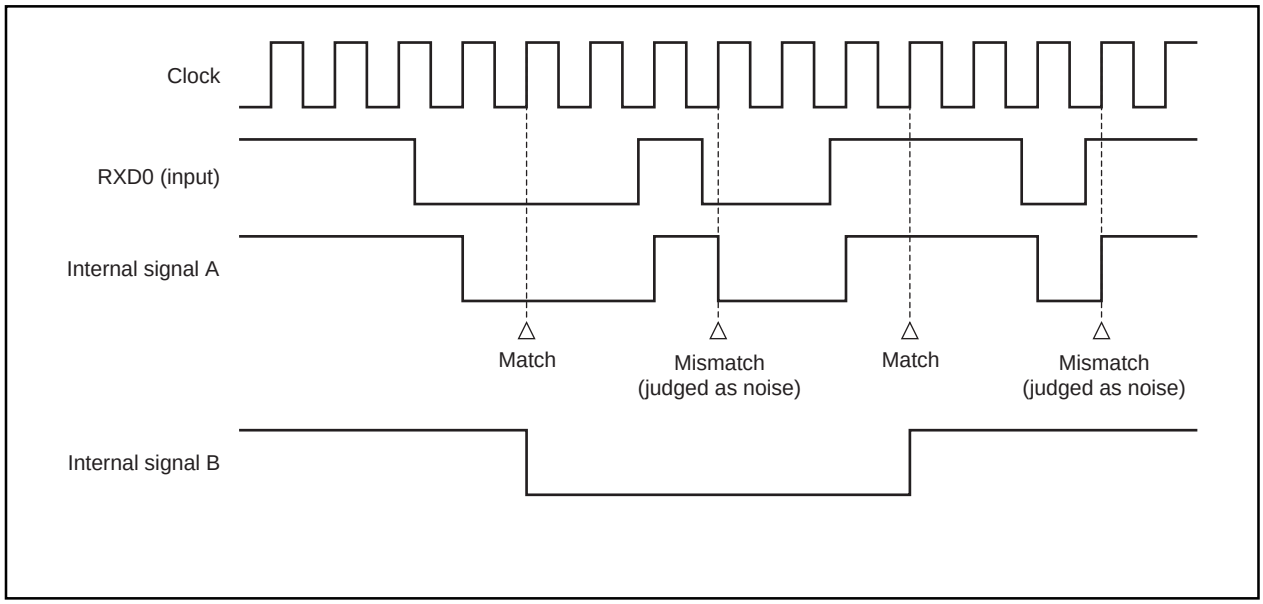


Figure 10-15. Timing of RXD0 Signal Judged as Noise



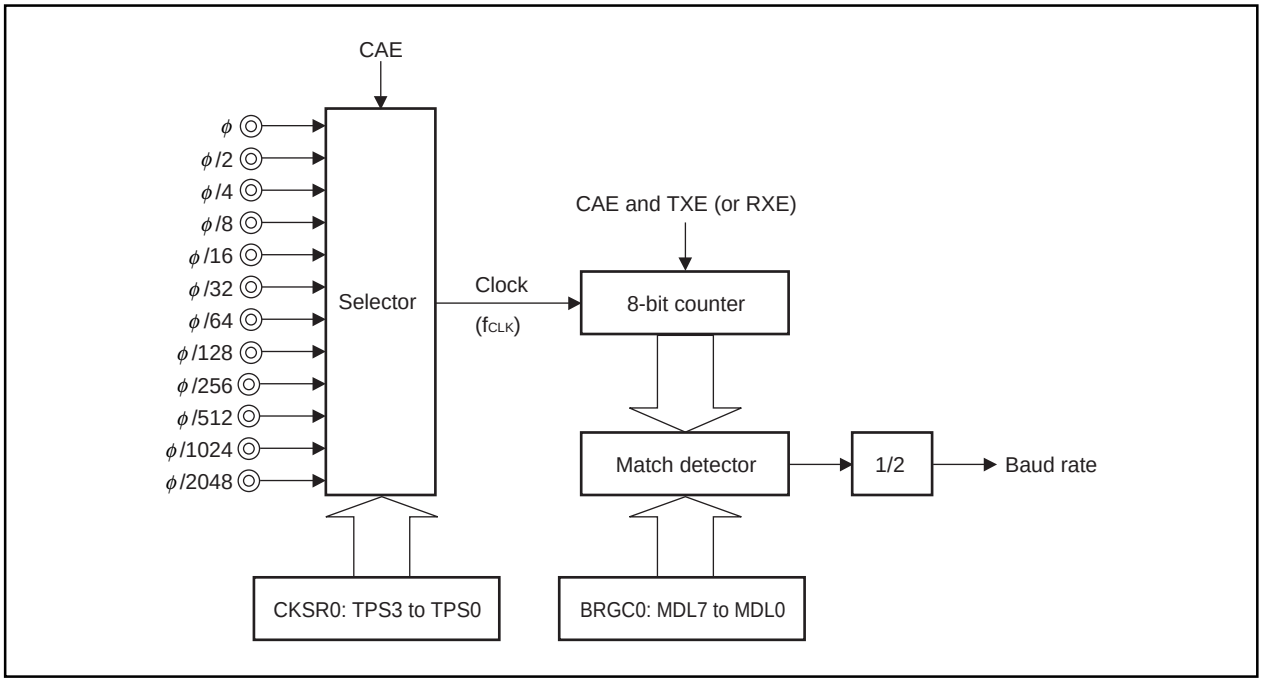
10.2.6 Dedicated baud rate generator 0 (BRG0)

A dedicated baud rate generator, which consists of a source clock selector and an 8-bit programmable counter, generates serial clocks during transmission/reception at UART0. The dedicated baud rate generator output can be selected as the serial clock for each channel.

Separate 8-bit counters exist for transmission and for reception.

(1) Baud rate generator 0 (BRG0) configuration

Figure 10-16. Baud Rate Generator 0 (BRG0) Configuration



(a) Basic clock (Clock)

When CAE bit = 1 in the ASIM0 register, the clock selected according to the TPS3 to TPS0 bits of the CKSR0 register is supplied to the transmission/reception unit. This clock is called the basic clock (Clock), and its frequency is referred to as f_{CLK}. When CAE bit = 0, Clock is fixed at low level.

(2) Serial clock generation

A serial clock can be generated according to the settings of the CKSR0 and BRGC0 registers.

The basic clock to the 8-bit counter is selected according to the TPS3 to TPS0 bits of the CKSR0 register.

The 8-bit counter divisor value can be set according to the MDL7 to MDL0 bits of the BRGC0 register.

(a) Clock select register 0 (CKSR0)

The CKSR0 register is an 8-bit register for selecting the basic block according to the TPS3 to TPS0 bits. The clock selected by the TPS3 to TPS0 bits becomes the basic clock (Clock) of the transmission/ reception module. Its frequency is referred to as f_{CLK}.

This register can be read or written in 8-bit or 1-bit units.

Figure 10-17. Clock Select Register 0 (CKSR0)

	7	6	5	4	3	2	1	0	Address	Initial value
CKSR0	0	0	0	0	TPS3	TPS2	TPS1	TPS0	FFFFFA06H	00H

Bit Position	Bit Name	Function
3 to 0	TPS3 to TPS0	Specifies the basic clock

TPS3	TPS2	TPS1	TPS0	Basic Clock (f_{CLK})
0	0	0	0	ϕ
0	0	0	1	ϕ/2
0	0	1	0	ϕ/4
0	0	1	1	ϕ/8
0	1	0	0	ϕ/16
0	1	0	1	ϕ/32
0	1	1	0	ϕ/64
0	1	1	1	ϕ/128
1	0	0	0	ϕ/256
1	0	0	1	ϕ/512
1	0	1	0	ϕ/1024
1	0	1	1	ϕ/2048
1	1	Arbitrary	Arbitrary	Setting prohibited

Remark ϕ: Internal system clock

Caution The maximum allowable frequency of the basic clock (f_{CLK}) is 25 MHz. Therefore, when the system clock's frequency is 50 MHz, bits TPS3 to TPS0 cannot be set to 0000B.

(b) Baud rate generator control register 0 (BRGC0)

The BRGC0 register is an 8-bit register that controls the baud rate (serial transfer speed) of UART0.

This register can be read or written in 8-bit or 1-bit units.

Figure 10-18. Baud Rate Generator Control Register 0 (BRGC0)

	7	6	5	4	3	2	1	0	Address	Initial value
BRGC0	MDL7	MDL6	MDL5	MDL4	MDL3	MDL2	MDL1	MDL0	FFFFFA07H	FFH

Bit Position	Bit Name	Function
7 to 0	MDL7 to MDL0	Specifies the 8-bit counter's divisor value.

MDL7	MDL6	MDL5	MDL4	MDL3	MDL2	MDL1	MDL0	Divisor Value (k)	Serial Clock
0	0	0	0	0	x	x	x	–	Setting prohibited
0	0	0	0	1	0	0	0	8	$f_{CLK}/8$
0	0	0	0	1	0	0	1	9	$f_{CLK}/9$
0	0	0	0	1	0	1	0	10	$f_{CLK}/10$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	0	250	$f_{CLK}/250$
1	1	1	1	1	0	1	1	251	$f_{CLK}/251$
1	1	1	1	1	1	0	0	252	$f_{CLK}/252$
1	1	1	1	1	1	0	1	253	$f_{CLK}/253$
1	1	1	1	1	1	1	0	254	$f_{CLK}/254$
1	1	1	1	1	1	1	1	255	$f_{CLK}/255$

Caution If the MDL7 to MDL0 bits are to be overwritten, TXE bit and RXE bit should be set to 0 in the ASIM0 register first.

Remarks 1. f_{CLK}: Frequency [Hz] of basic clock (Clock) selected according to TPS3 to TPS0 bits of CKSR0 register

2. k: Value set according to MDL7 to MDL0 bits (k = 8, 9, 10, ..., 255)

3. The baud rate is the output clock for the 8-bit counter divided by 2

4. x: don't care

(c) Baud rate

The baud rate is the value obtained according to the following formula.

$$\text{Baud rate} = \frac{f_{CLK}}{2 \times k} \text{ [bps]}$$

f_{CLK} = Frequency [Hz] of basic clock (Clock) selected according to TPS3 to TPS0 bits of CKSR0 register.
k = Value set according to MDL7 to MDL0 bits of BRGC0 register (k = 8, 9, 10, ..., 255)

(d) Baud rate error

The baud rate error is obtained according to the following formula.

$$\text{Error}\,(\%) = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (normal baud rate)}} - 1 \right) \times 100\,[\%]$$

Cautions 1. Make sure that the baud rate error during transmission does not exceed the allowable error of the reception destination.

2. Make sure that the baud rate error during reception is within the allowable baud rate range during reception, which is described in (4) Allowable baud rate during reception.

Example: Basic clock frequency = 20 MHz = 20,000,000 Hz
Settings of MDL7 to MDL0 bits in BRGC0 register = 01000001B (k = 65)
Target baud rate = 153,600 bps

Baud rate = 20M/(2 × 65)
= 20000000/(2 × 65) = 153,846 [bps]

Error = (153846/153600 – 1) × 100
= 0.160 [%]

(3) Baud rate setting example

Table 10-4. Baud Rate Generator Setting Data

Baud Rate (bps)	ϕ = 50MHz			ϕ = 40 MHz			ϕ = 33 MHz			ϕ = 10 MHz		
	f_{CLK}	k	ERR	f_{CLK}	k	ERR	f_{CLK}	k	ERR	f_{CLK}	k	ERR
300	$\phi/2^9$	163	0.15	$\phi/2^{10}$	65	0.16	$\phi/2^8$	215	–0.07	$\phi/2^7$	130	0.16
600	$\phi/2^8$	163	0.15	$\phi/2^9$	65	0.16	$\phi/2^7$	215	–0.07	$\phi/2^6$	130	0.16
1200	$\phi/2^7$	163	0.15	$\phi/2^8$	65	0.16	$\phi/2^6$	215	–0.07	$\phi/2^5$	130	0.16
2400	$\phi/2^6$	163	0.15	$\phi/2^7$	65	0.16	$\phi/2^5$	215	–0.07	$\phi/2^4$	130	0.16
4800	$\phi/2^5$	163	0.15	$\phi/2^6$	65	0.16	$\phi/2^4$	215	–0.07	$\phi/2^3$	130	0.16
9600	$\phi/2^4$	163	0.15	$\phi/2^5$	65	0.16	$\phi/2^3$	215	–0.07	$\phi/2^2$	130	0.16
19200	$\phi/2^3$	163	0.15	$\phi/2^4$	80	0.16	$\phi/2^2$	215	–0.07	$\phi/2^1$	130	0.16
31250	$\phi/2^3$	100	0	$\phi/2^3$	65	0	$\phi/2^2$	132	0	$\phi/2^1$	80	0
38400	$\phi/2^2$	163	0.15	$\phi/2^3$	65	0.16	$\phi/2^1$	215	–0.07	$\phi/2^0$	130	0.16
76800	$\phi/2^2$	81	0.47	$\phi/2^2$	65	0.16	$\phi/2^1$	107	0.39	$\phi/2^0$	65	0.16
153600	$\phi/2^1$	81	0.47	$\phi/2^1$	65	0.16	$\phi/2^1$	54	–0.54	$\phi/2^0$	33	–1.36
312500	$\phi/2^1$	40	0	$\phi/2^1$	32	0	$\phi/2^1$	26	1.54	$\phi/2^0$	16	0

Caution The maximum allowable frequency of the basic clock (f_{CLK}) is 25 MHz.

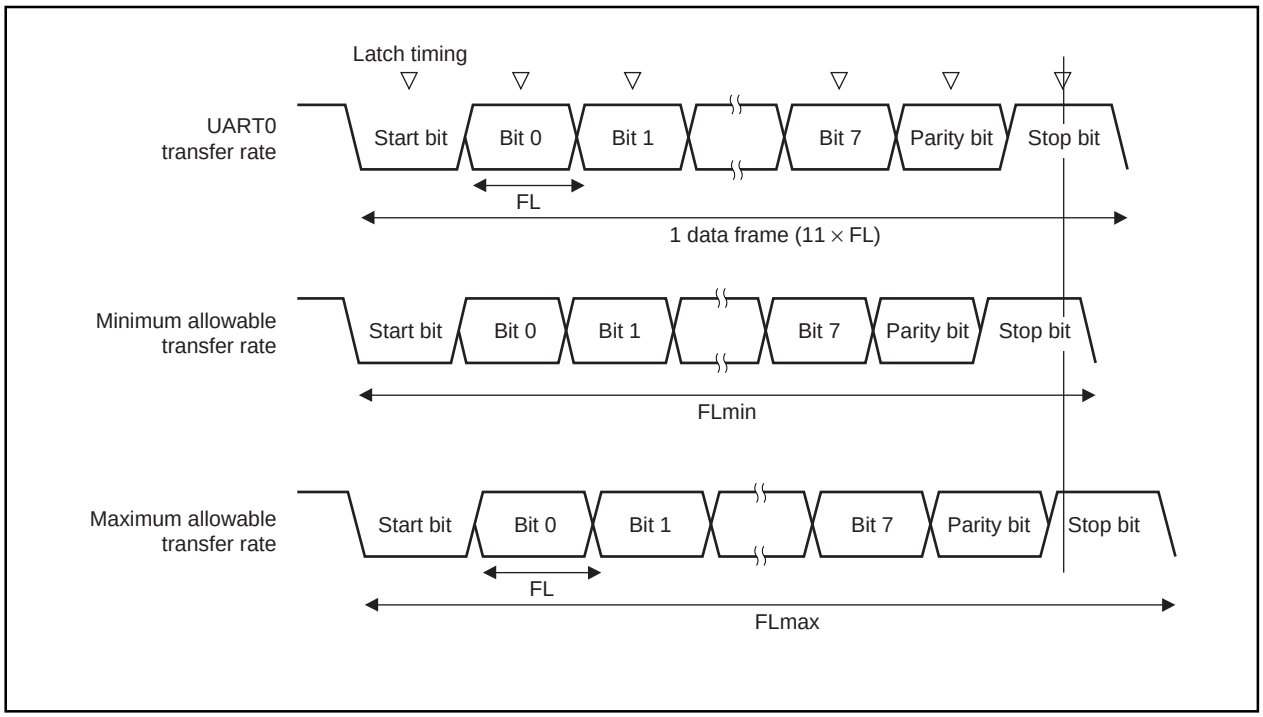
Remarks ϕ: System clock frequency
f_{CLK}: Basic clock frequency
k: Setting values of MDL7 to MDL0 bits in BRGC0 register
ERR: Baud rate error [%]

(4) Allowable baud rate range during reception

The degree to which a discrepancy from the transmission destination's baud rate is allowed during reception is shown below.

Caution The equations described below should be used to set the baud rate error during reception so that it always is within the allowable error range.

Figure 10-19. Allowable Baud Rate Range During Reception



As shown in Figure 10-19, after the start bit is detected, the receive data latch timing is determined according to the counter that was set by the BRGC0 register. If all data up to the final data (stop bit) is in time for this latch timing, the data can be received normally.

Applying this to 11-bit reception is, theoretically, as follows.

$FL = (Brate)^{-1}$

Brate: UART0 baud rate
k: BRGC0 register setting value
FL: 1-bit data length

When the latch timing margin is made 2 basic clocks (Clock), the minimum allowable transfer rate (FLmin) is as follows.

$$FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$$

Therefore, the transfer destination's maximum baud rate (BRmax) that can be received is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} \text{ Brate}$$

Similarly, the maximum allowable transfer rate (FLmax) can be obtained as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k + 2}{2 \times k} \times FL = \frac{21k - 2}{2 \times k} FL$$

$$FLmax = \frac{21k - 2}{20k} FL \times 11$$

Therefore, the transfer destination's minimum baud rate (BRmin) that can be received is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{22k}{21k - 2} \text{ Brate}$$

The allowable baud rate error of UART0 and the transfer destination can be obtained as follows from the expressions described above for computing the minimum and maximum baud rate values.

Table 10-5. Maximum and Minimum Allowable Baud Rate Error

Division Ratio (k)	Maximum Allowable Baud Rate Error	Minimum Allowable Baud Rate Error
8	+3.53%	–3.61%
20	+4.26%	–4.31%
50	+4.56%	–4.58%
100	+4.66%	–4.67%
255	+4.72%	–4.73%

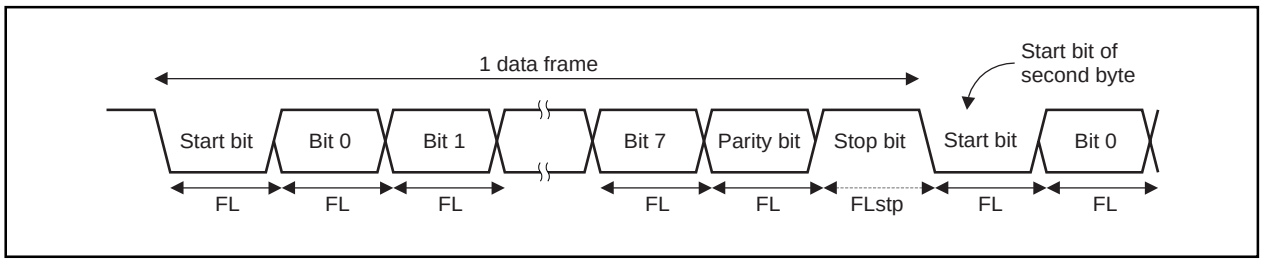
Remarks 1. The reception precision depends on the number of bits in one frame, the basic clock frequency, and the division ratio (k). The higher the basic clock frequency and the larger the division ratio (k), the higher the precision.

2. k: BRGC0 setting value

(5) Transfer rate during continuous transmission

During continuous transmission, the transfer rate from a stop bit to the next start bit is extended two clocks of basic clock (Clock) longer than normal. However, on the reception side, the transfer result is not affected since the timing is initialized by the detection of the start bit.

Figure 10-20. Transfer Rate During Continuous Transmission



Representing the 1-bit data length by FL, the stop bit length by FLstp, and the basic clock frequency by f_{CLK} yields the following equation.

$$FLstp = FL + 2/f_{CLK}$$

Therefore, the transfer rate during continuous transmission is as follows.

$$\text{Transfer rate} = 11 \times FL = 2/f_{CLK}$$

10.2.7 Precautions

When the supply of clocks to UART0 is stopped (for example, IDLE or STOP mode), operation stops with each register retaining the value it had immediately before the supply of clocks was stopped. The TXD0 pin output also holds and outputs the value it had immediately before the supply of clocks was stopped. However, operation is not guaranteed after the supply of clocks is restarted. Therefore, after the supply of clocks is restarted, the circuits should be initialized by setting CAE bit = 0, RXE bit = 0, and TXE bit = 0 in the ASIM0 register.

10.3 Asynchronous Serial Interfaces 1, 2 (UART1, UART2)

10.3.1 Features

- Clocked (synchronous) mode/asynchronous mode can be selected
- Operation clock
  Synchronous mode: Baud rate generator/external clock selectable
  Asynchronous mode: Baud rate generator
- Transfer rate
  600 bps to 153600 bps (in asynchronous mode, ϕ = 50 MHz)
- Full-duplex communications (LSB first)
  On-chip reception buffer register n (RXBn)
- Three-pin configuration
  TXDn: Transmit data output pin
  RXDn: Receive data input pin
  $\overline{\text{ASCK}}$n: Synchronous serial clock I/O
- Reception error detection function
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 2 types
  - Reception completion interrupt (INTSRn): Interrupt is generated when receive data is transferred from the shift register to the reception buffer register n (RXBn) after serial transfer is completed during a reception enabled state.
  - Transmission completion interrupt (INTSTn): Interrupt is generated when the serial transmission of transmit data (8/7 bits) from the shift register is completed.
- The character length of transmit/receive data is specified with the ASIMn0 register (extension bits are specified with the ASIMn1 register)
- Character length: 7 or 8 bits
  9 bits (when extension bit is added)
- Parity functions: Odd, even, 0, or no parity
- Transmission stop bits: 1 or 2 bits
- Communication mode: 1-frame transfer or 2-frame continuous transfer enabled
- On-chip dedicated baud rate generator

Remarks 1. n = 1, 2

2. ϕ : Internal system clock

10.3.2 Configuration

UART1 and UART2 are controlled by asynchronous serial interface mode registers 10, 11, 20, and 21 (ASIM10, ASIM11, ASIM20, ASIM21) and asynchronous serial interface status registers 1 and 2 (ASIS1, ASIS2). Receive data is held in the reception buffer registers (RXB1, RXBL1, RXB2, RXBL2), and transmit data is held in the transmission shift registers (TXS1, TXSL1, TXS2, TXSL2).

Figure 10-21 shows the configuration of asynchronous serial interfaces 1 and 2 (UART1, UART2).

(1) Asynchronous serial interface mode registers 10, 11, 20, 21 (ASIM10, ASIM11, ASIM20, ASIM21)

The ASIMn0 and ASIMn1 registers are 8-bit registers that specify the operation of the asynchronous serial interface (n = 1, 2).

(2) Asynchronous serial interface status registers 1, 2 (ASIS1, ASIS2)

The ASIS1 and ASIS2 registers consist of a transmission status flag (SOT), reception status flag (SIR), a bit (RB8) that indicates the 9th bit when extension bit addition is enabled, and 3-bit error flags (PE, FE, OVE) that indicate the error status at reception end.

(3) Reception control parity check

The receive operation is controlled according to the contents set in the ASIMn0 and ASIMn1 registers. A check for parity errors is also performed during receive operation, and if an error is detected, a value corresponding to the error contents is set in the ASIS1, ASIS2 registers.

(4) 2-frame continuous reception buffer registers (RXB1, RXB2)/reception buffer registers (RXBL1, RXBL2)

RXBn is a 16-bit (during 2-frame continuous reception, 9-bit extension data reception) buffer register that holds receive data. During 7, 8 bit/character reception, 0 is stored in the MSB.

For 16-bit access to this register, specify RXB1, RXB2, and for access to the lower 8 bits, specify RXBL1, RXBL2.

In the reception enabled state, receive data is transferred from the reception shift register to the reception buffer in synchronization with the completion of shift-in processing of one frame.

A reception completion interrupt request (INTSRn) is generated upon transfer to the reception buffer (when 2-frame continuous reception is specified, reception buffer transmission of the second frame).

(5) 2-frame continuous transmission shift registers (TXS1, TXS2)/Transmission shift registers (TXSL1, TXSL2)

TXSn is a 9-bit/2-frame continuous transmission processing shift register. Transmission is started by writing data to this register.

A transmission completion interrupt request (INTSTn) is generated in synchronization with the end of transmission of 1 frame or 2 frames including the TXSn data.

For 16-bit access to this register, specify TXS1, TXS2, and for access to the lower 8 bits, specify TXSL1, TXSL2.

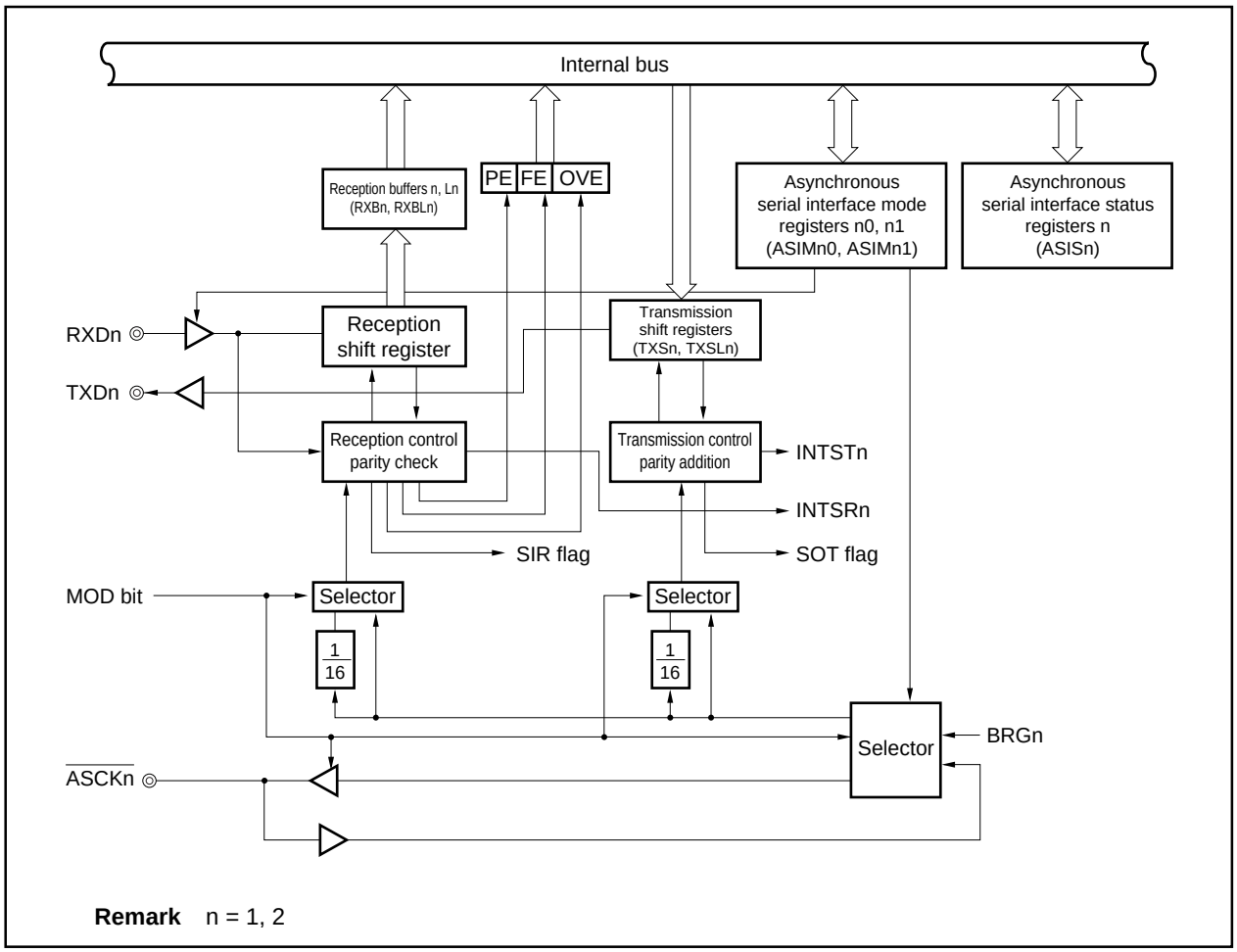
(6) Addition of transmission control parity

A transmission operation is controlled by adding a start bit, parity bit, or stop bit to the data that is written to the TXSn or TXSLn register, according to the contents set in the ASIMn0, ASIMn1 registers.

(7) Selector

The selector selects the serial clock source.

Figure 10-21. Block Diagram of Asynchronous Serial Interfaces 1, 2



Remark n = 1, 2

10.3.3 Control registers

(1) Asynchronous serial interface mode registers 10, 20 (ASIM10, ASIM20)

The ASIMn0 register is an 8-bit register that controls the UART1, UART2 transfer operation (n = 1, 2).

This register can be read/written in 8-bit or 1-bit units.

Cautions 1. If the contents of the ASIMn0 register are changed during UARTn transmission or reception, the UARTn operation cannot be guaranteed (n = 1, 2).

2. Set the ASIMn0 register when the UARTn operation is stopped (when RXE bit = 0 and transmission is completed). Do not change port 3 mode control register (PMC3) after setting the ASIMn0 register.

3. In the case of serial clock output in the clocked (synchronous) mode, ensure that nodes do not output to one another causing conflicts.

Figure 10-22. Asynchronous Serial Interface Mode Registers 10, 20 (ASIM10, ASIM20) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIM10	1	RXE	PS1	PS0	CL	SL	0	SCLS	FFFFFA28H	81H

	7	6	5	4	3	2	1	0	Address	Initial value
ASIM20	1	RXE	PS1	PS0	CL	SL	0	SCLS	FFFFFA48H	81H

Bit Position	Bit Name	Function
6	RXE	Enables/disables reception. 0: Disable reception 1: Enable reception
5, 4	PS1, PS0	Specify parity bit length

PS1	PS0	Operation
0	0	No parity, extension bit operation
0	1	0 parity Transmit side → Transmission with parity bit = 0 Receive side → No parity error generated during reception
1	0	Odd parity
1	1	Even parity

Figure 10-22. Asynchronous Serial Interface Mode Registers 10, 20 (ASIM10, ASIM20) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>3</td><td>CL</td><td>Specifies character length of transmit data (1 frame).
0: 7 bits
1: 8 bits</td></tr>
<tr><td>2</td><td>SL</td><td>Specifies stop bit length of transmit data.
0: 1 bit
1: 2 bits</td></tr>
<tr><td>0</td><td>SCLS</td><td>Specifies serial clock source.
<table>
<tr><th rowspan="2">SCLS</th><th colspan="2">Operation</th></tr>
<tr><th>In Asynchronous Mode</th><th>In Synchronous Mode</th></tr>
<tr><td>0</td><td rowspan="2">Internal baud rate generator</td><td>External clock input</td></tr>
<tr><td>1</td><td></td></tr>
</table>
</td></tr>
</table>

(2) Asynchronous serial interface mode registers 11, 21 (ASIM11, ASIM21)

The ASIMn1 register is an 8-bit register that controls the UART1 and UART2 transfer modes.

This register can be read/written in 8-bit or 1-bit units

Figure 10-23. Asynchronous Serial Interface Mode Registers 11, 21 (ASIM11, ASIM21)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIM11	0	0	0	0	MOD	UMST	UMSR	EBS	FFFFFA2AH	00H

	7	6	5	4	3	2	1	0	Address	Initial value
ASIM21	0	0	0	0	MOD	UMST	UMSR	EBS	FFFFFA4AH	00H

Bit Position	Bit Name	Function
3	MOD	Specifies operation mode (asynchronous/synchronous mode) 0: Asynchronous mode 1: Synchronous mode
2	UMST	Specifies number of continuous frame transmissions. 0: 1-frame data transmission 1: 2-frame continuous data transmission
1	UMSR	Specifies number of continuous frame receptions. 0: 1-frame data reception 1: 2-frame continuous data reception
0	EBS	Specifies extension bit operation for transmit/receive data when no parity is specified (PS0 = PS1 = 0). 0: Disable extension bit addition 1: Enable extension bit addition When the extension bit is specified, 1 data bit is added on top of the 8 bits of transmit/receive data, enabling 9-bit data communication. Extension bit specification is valid only when no parity (ASIMn0 register's PS0 bit = PS1 bit = 0) and 1-frame data transmission (UMST bit = 0) are specified. When 0 parity, odd parity, or even parity are specified, or when 2-frame continuous data transmission (UMST bit = 1) is specified, the EBS bit setting becomes invalid and extension bit addition is not performed. Extension bit addition (EBS bit = 1) and 2-frame continuous data reception (UMSR bit = 1) cannot be set simultaneously.

(3) Asynchronous serial interface status registers 1, 2 (ASIS1, ASIS2)

The ASISn register is a register that is configured of a UARTn transmission status flag (SOT), reception status flag (SIR), a bit (RB8) indicating the 9th bit when extension bit addition is enabled, and 3-bit error flags (PE, FE, OVE) that indicate the error status at reception end (n = 1, 2).

The status flag that indicates reception errors always indicates the most recent error status. In other words, if the same error occurs several times before receive data is read, this flag holds only the status of the error that occurred last.

Each time the ASISn register is read after a receive completion interrupt (INTSRn), read the reception buffer (RXBn or RXBLn). The error flag is cleared when the reception buffer (RXBn or RXBLn) is read.

Also, clear the error flag by reading the reception buffer (RXBn or RXBLn) when a reception error occurs.

This register is read-only in 8-bit or 1-bit units.

Figure 10-24. Asynchronous Serial Interface Status Registers 1, 2 (ASIS1, ASIS2) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
ASIS1	SOT	SIR	0	RB8	0	PE	FE	OVE	FFFFFA2CH	00H

	7	6	5	4	3	2	1	0	Address	Initial value
ASIS2	SOT	SIR	0	RB8	0	PE	FE	OVE	FFFFFA4CH	00H

Bit Position	Bit Name	Function
7	SOT	Status flag indicating transmission status. 0: Transmission end timing (when INTSTn is generated) 1: Indicates transmission status[Note] **Note** The transmission status is the status until the specified number of stop bits has been transmitted following write operation to the transmit register. During 2-frame continuous transmission, this status is until the stop bit of the 2nd frame has been transmitted.
6	SIR	Status flag indicating reception status. 0: Reception end timing (when INTSRn is generated) 1: Indicates reception status[Note] **Note** The reception status is the status until stop bit detection from the start bit detection timing.
4	RB8	Indicates contents of receive data extension bit (1 bit) when 9-bit extended format is specified (EBS bit of ASIMn1 register = 1)

Remark n = 1, 2

Figure 10-24. Asynchronous Serial Interface Status Registers 1, 2 (ASIS1, ASIS2) (2/2)

Bit Position	Bit Name	Function
2	PE	Status flag indicating parity error 0: Processing to read data from reception buffer 1: When transmit parity and receive parity don't match **Caution No parity error is generated if no parity is specified or 0 parity is specified with the PS1, PS0 bits of the ASIMn0 register.**
1	FE	Status flag indicating framing error 0: Processing to read data from reception buffer 1: When stop bit is not detected
0	OVE	Status flag indicating overrun error 0: Processing to read data from reception buffer 1: When UARTn has completed next reception processing prior to loading receive data from reception buffer Since the contents of the reception shift register are transferred to the reception buffer (RXBn, RXBLn) every time 1 frame is received, the following receive data is overwritten to the reception buffer (RXBn, RXBLn) and the previous receive data is discarded.

Remark n = 1 , 2

(4) 2-frame continuous reception buffer registers 1, 2 (RXB1, RXB2)/reception buffer registers L1, L2 (RXBL1, RXBL2)

The RXBn register is a 16-bit buffer register that holds receive data (during 2-frame continuous reception (UMSR bit of ASIMn1 register = 1), during 9-bit extended data reception (EBS bit of ASIMn1 register = 1)). During 7 or 8 bit/character reception, 0 is stored in the MSB.

For 16-bit access to this register, specify RXBn, and for access to the lower 8 bits, specify RXBLn.

In the receive enabled status, receive data is transferred from the reception shift register to the reception buffer in synchronization with the end of shift-in processing for 1 frame of data.

The reception completion interrupt request (INTSRn) is generated upon transfer of data to the reception buffer (when 2-frame reception is specified, reception buffer transmission of the second frame).

In the reception disabled status, transfer processing to the reception buffer is not performed even if shift-in processing for 1 frame of data has been completed, and the contents of the reception buffer are held.

Neither is a reception completion interrupt request generated.

The RXBn register can be read/written in 16-bit units, and the RXBLn register can be read/written in 8-bit or 1-bit units.

Figure 10-25. 2-Frame Continuous Reception Buffer Registers 1, 2 (RXB1, RXB2)/Reception Buffer Registers L1, L2 (RXBL1, RXBL2)

[2-frame continuous buffer register 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
RXB1	RXB15	RXB14	RXB13	RXB12	RXB11	RXB10	RXB9	RXB8	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0	FFFFFA20H	Undefined

[Reception buffer register L1]

	7	6	5	4	3	2	1	0	Address	Initial value
RXBL1	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0	FFFFFA22H	Undefined

[2-frame continuous reception buffer register 2]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
RXB2	RXB15	RXB14	RXB13	RXB12	RXB11	RXB10	RXB9	RXB8	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0	FFFFFA40H	Undefined

[Reception buffer register L2]

	7	6	5	4	3	2	1	0	Address	Initial value
RXBL2	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0	FFFFFA42H	Undefined

Bit Position	Bit Name	Function
15 to 0	RXB15 to RXB0	Stores receive data. 0 can be read for the RXBn register when 7, 8 bit/character data is received. When an extension bit is set during 9 bit/character data reception, the extension bit (RXB8) is stored in RB8 of the ASISn register simultaneously with saving to the reception buffer. 0 can be read for the RXB7 bit of the RXBLn register during 7 bit/character data reception.

(a) When 2-frame continuous reception is set

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBn	RXB15	RXB14	RXB13	RXB12	RXB11	RXB10	RXB9	RXB8	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0

7-/8-bit data of 1st frame　　7-/8-bit data of 2nd frame

(b) When 9-bit extension reception is set

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBn	RXB15	RXB14	RXB13	RXB12	RXB11	RXB10	RXB9	RXB8	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0

9-bit extended data

When 9-bit extension is set, the extension bit (RXB8) is stored in the RB8 bit of the ASISn register simultaneously with saving to the reception buffer.

(c) Cautions

<1> Operation upon occurrence of overrun error during 2-frame continuous reception

- **During normal operation**

Reception completion interrupt (INTSRn) generated upon end of reception of 2nd frame, no error

RXDn	Frame 1	Frame 2

- **Reception of 3rd frame started before performing reception processing**

Reception completion interrupt (INTSRn) generated upon end of reception of 2nd frame, no error

RXDn	Frame 1	Frame 2

Reception interrupt not generated upon end of reception of 3rd frame, occurrence of error

RXDn	Frame 3	Frame 3

Value of OVE bit of ASISn register becomes 1.

- **Start of reception of 3rd frame and 4th frame before performing reception processing**

Reception completion interrupt (INTSRn) generated upon end of reception of 2nd frame, no error

RXDn	Frame 1	Frame 2

No reception completion interrupt generated upon end of reception of 3rd frame, occurrence of error

RXDn	Frame 3	Frame 3

Value of OVE bit of ASISn register becomes 1.

Reception completion interrupt (INTSRn) generated upon end of reception of 4th frame, no error

RXDn	Frame 3	Frame 4

Value of OVE frame of ASISn register remains 1.

- **Start of reception of 3rd frame before performing reception processing, start of reception of 4th frame after reception processing**

Reception completion interrupt (INTSRn) generated upon end of reception of 2nd frame, no error

RXDn	Frame 1	Frame 2

Reception completion interrupt not generated upon end of reception of 3rd frame, occurrence of error

RXDn	Frame 3	Frame 3

Value of OVE bit of ASISn register becomes 1.
Value of OVE flag becomes 0 during reception processing.

Reception completion interrupt (INTSRn) generated upon end of reception of 4th frame, no error

RXDn	Frame 3	Frame 4

No occurrence of error

(5) 2-frame continuous transmission shift registers 1, 2 (TXS1, TXS2)/transmission shift registers L1, L2 (TXSL1, TXSL2)

The TXSn register is a 9-bit/2-frame continuous transmission processing shift register (n = 1, 2). Transmission is started by writing data to this register.

A transmission completion interrupt request (INTSTn) is generated in synchronization with the end of transmission of 1 frame or 2 frames including the TXSn data.

For 16-bit access to this register, specify TXSn, and for access to the lower 8 bits, specify TXSLn.

The TXSn register is write-only in 16-bit units, and the TXSLn register is write-only in 8-bit units.

Figure 10-26. 2-Frame Continuous Transmission Shift Registers 1, 2 (TXS1, TXS2)/Transmission Shift Registers L1, L2 (TXSL1, TXSL2)

[2-frame continuous transmission shift register 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
TXS1	TXS15	TXS14	TXS13	TXS12	TXS11	TXS10	TXS9	TXS8	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0	FFFFFA24H	Undefined

[Transmission shift register L1]

	7	6	5	4	3	2	1	0	Address	Initial value
TXSL1	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0	FFFFFA26H	Undefined

[2-frame continuous transmission shift register 2]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
TXS2	TXS15	TXS14	TXS13	TXS12	TXS11	TXS10	TXS9	TXS8	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0	FFFFFA44H	Undefined

[Transmission shift register L2]

	7	6	5	4	3	2	1	0	Address	Initial value
TXSL2	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0	FFFFFA46H	Undefined

Bit Position	Bit Name	Function
15 to 0	TXB15 to TXB0	Write transmit data.

Caution TXSn, TXSLn can be read, but since shifting is done in synchronization with the shift clock, the data that is read cannot be guaranteed.

10.3.4 Interrupt requests

The following two types of interrupt request are generated from UARTn (n = 1, 2).

- Reception completion interrupt (INTSRn)
- Transmission completion interrupt (INTSTn)

The reception completion interrupt has higher default priority than the transmission completion interrupt.

Table 10-6. Default Priority of Generated Interrupts

Interrupt	Priority
Reception completion	1
Transmission completion	2

(1) Reception completion interrupt (INTSRn)

In the reception enabled state, the reception completion interrupt (INTSRn) is generated when data in the reception shift register undergoes shift-in processing and is transferred to the reception buffer.

The reception completion interrupt request (INTSRn) is generated following stop bit sampling. The reception completion interrupt (INTSRn) is generated upon occurrence of an error.

In the reception disabled state, no reception completion interrupt is generated.

(2) Transmission completion interrupt (INTSTn)

Since UARTn does not have a transmission buffer, a transmission completion interrupt request (INTSTn) is generated when one frames of data containing 7-bit or 8-bit characters or two frames of data containing 9-bit characters are shifted out from the transmission shift register (TXSn, TXSLn).

A transmission completion interrupt (INTSTn) is generated when the last bit of transmit data (stop bit) is transmitted.

10.3.5 Operation

(1) Data format

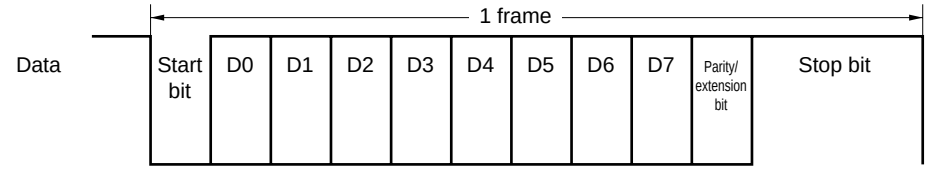
Full-duplex serial data is transmitted and received.

Figure 10-27 shows the format of transmit/receive data. One data frame consists of a start bit, character bits, a parity bit, and a stop bit(s). When 2 data frame transfer is set, both frames have the above-described format.

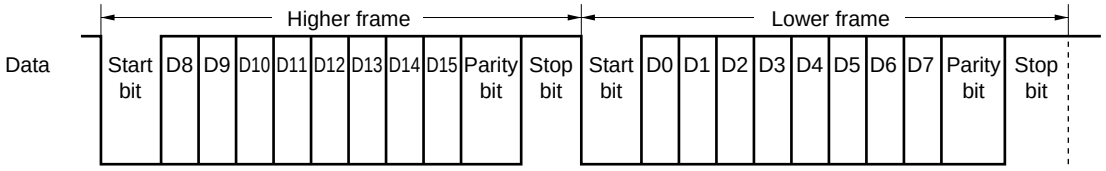
Specification of the character bit length in one data frame, parity selection, and specification of the stop bit length is done using asynchronous serial interface mode registers 10, 20 (ASIM10, ASIM20). Specification of the number of frames and specification of the extension bit is done with asynchronous serial interface mode registers 11, 21 (ASIM11, ASIM21). Data is transmitted LSB first.

Figure 10-27. Asynchronous Serial Interface Transmit/Receive Data Format

(a) 1-frame format



(b) 2-frame format



- Start bit: 1 bit
- Character bits: 7 or 8 bits
- Parity bit: Even parity, odd parity, 0 parity, or no parity
- Stop bit: 1 or 2 bits

Caution The extension bit is invalid in the 2-frame continuous mode or when a parity bit is added.

Table 10-7. ASIMn0, ASIMn1 Register Settings and Data Format

ASIMn0, ASIMn1 Register Settings					Data Format				
CL bit	PS1 bit	PS0 bit	SL bit	EBS bit	D0 to D6	D7	D8	D9	D10
0	0	0	0	0	DATA	Stop bit	—	—	—
0	Other than PS1 = PS0 = 0				DATA	Parity bit	Stop bit	—	—
1	0	0			DATA	DATA	Stop bit	—	—
1	Other than PS1 = PS0 = 0				DATA	DATA	Parity bit	Stop bit	—
0	0	0	1	0	DATA	Stop bit	Stop bit	—	—
0	Other than PS1 = PS0 = 0				DATA	Parity bit	Stop bit	Stop bit	—
1	0	0			DATA	DATA	Stop bit	Stop bit	—
1	Other than PS1 = PS0 = 0				DATA	DATA	Parity bit	Stop bit	Stop bit
0	0	0	0	1	DATA	Stop bit	—	—	—
0	Other than PS1 = PS0 = 0				DATA	Parity bit	Stop bit	—	—
1	0	0			DATA	DATA	DATA	Stop bit	—
1	Other than PS1 = PS0 = 0				DATA	DATA	Parity bit	Stop bit	—
0	0	0	1	1	DATA	Stop bit	Stop bit	—	—
0	Other than PS1 = PS0 = 0				DATA	Parity bit	Stop bit	Stop bit	—
1	0	0			DATA	DATA	DATA	Stop bit	Stop bit
1	Other than PS1 = PS0 = 0				DATA	DATA	Parity bit	Stop bit	Stop bit

(2) Transmission operation

The transmission operation is started by writing data to 2-frame continuous transmission shift registers 1, 2 (TXS1, TXS2)/transmission shift registers (TXSL1, TXSL2).

Following data write, the start bit is transmitted from the next shift timing.

Since the UARTn does not have a CTS (transmission enable signal) input pin, use a port when the other party confirms the reception enabled status (n = 1, 2).

(a) Transmission operation start

The transmission operation is started by writing transmit data to 2-frame continuous transmission shift registers 1, 2 (TXS1, TXS2)/transmission shift registers (TXSL1, TXSL2). Then data is output in sequence from LSB to the TXDn pin (transmission in sequence from the start bit). A start bit, parity bit, and stop bit(s) are automatically added.

(b) Transmission interrupt request

When the transmission shift register becomes empty upon completion of the transmission of 1 or 2 frames of data, a transmission completion interrupt request (INTSTn) is generated. The INTSTn interrupt generation timing differs depending on the number of specified stop bits. The INTSTn interrupt is generated at the same time that the last stop bit is output.

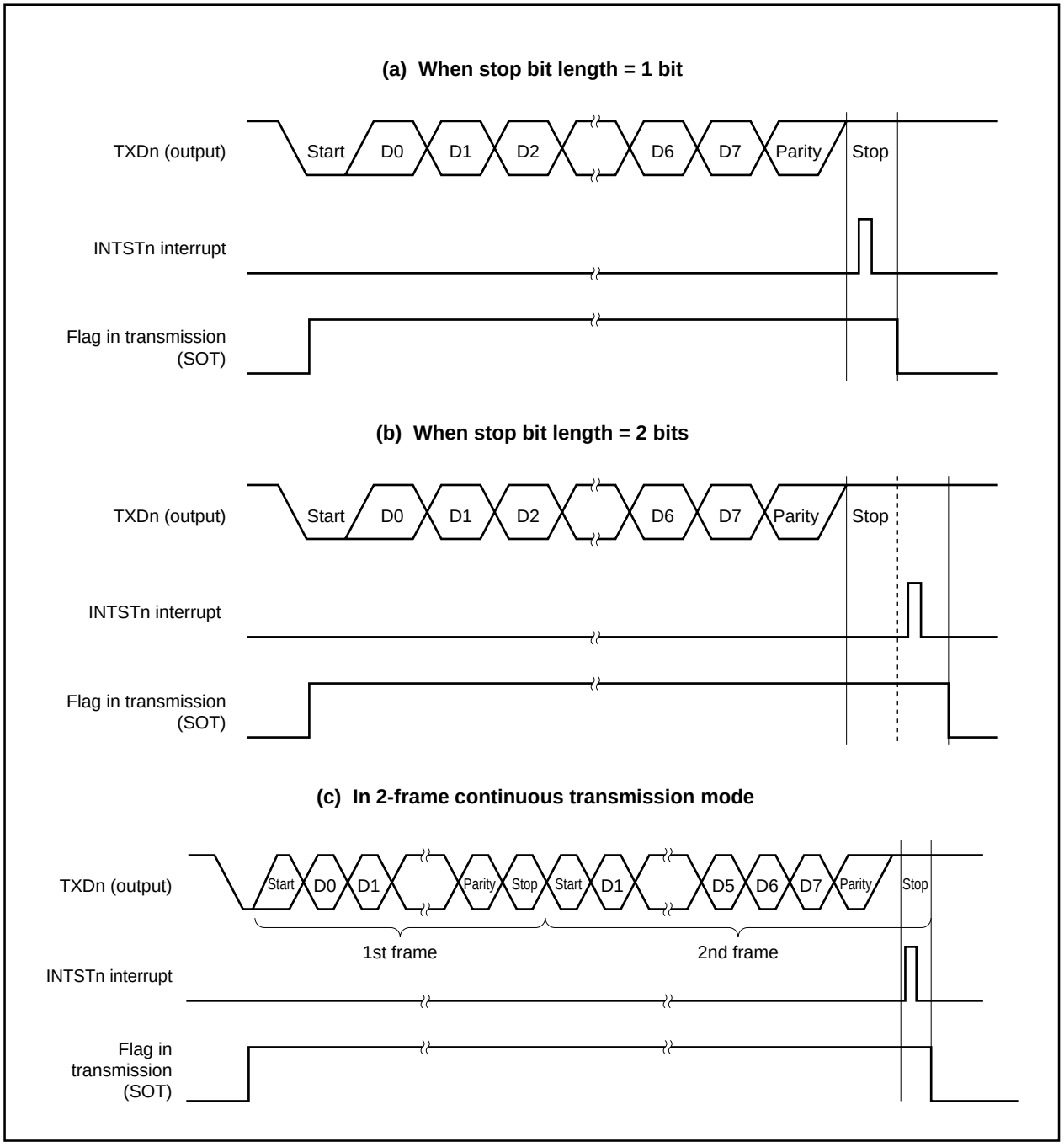
The transmission operation remains stopped until the data to be transmitted next has been written to the TXSn/TXSLn registers.

Figure 10-28 shows the INTSTn interrupt generation timing.

Cautions 1. Normally, the transmission completion interrupt (INTSTn) is generated when the transmission shift register becomes empty. However, if the transmission shift register has become empty due to input of RESET, no transmission completion interrupt (INTSTn) is generated.

2. No data can be written to the TXSn or TXSLn registers during transmission operation until INTSTn is generated. Even if data is written, this does not affect the transmission operation.

Figure 10-28. Asynchronous Serial Interface Transmission Completion Interrupt Timing



(3) Reception operation

The reception wait status is entered by setting the RXE bit of the ASIMn0 register to 1 (n = 1, 2). To start the reception operation, first perform start bit detection. Start bit detection is done by performing sampling of the RXDn pin. When the reception operation is started, serial data is stored to the reception shift register in sequence at the set baud rate. Each time reception of 2 frames or 1 frame of RXBn or RXBLn data has been completed, a reception completion interrupt (INTSRn) is generated. Receive data is transmitted from the reception buffer (RXBn/RXBLn) to memory when this interrupt is processed.

(a) Reception enabled status

The reception operation is enabled by setting (1) the RXE bit of the ASIMn0 register.

- RXE = 1: Reception enabled status
- RXE = 0: Reception disabled status

In the reception disabled status, the reception hardware is in standby in an initialized state. At this time, no reception completion interrupt is generated, and the contents of the reception buffer are held.

(b) Start of reception operation

The reception operation is started through detection of the start bit.

- **In asynchronous mode (MOD bit of ASIMn1 register = 0)**
  The RXDn pin is sampled using the serial clock from the baud rate generator. After 8 serial clocks have been output following detection of the falling edge of the RXDn pin, the RXDn pin is again sampled. If a low level is detected at this time, the falling edge of the RXDn pin is interpreted as a start bit, the operation shifts to reception processing, and the RXDn pin input is sampled from this point on in units of 16 serial clock output.
  If the high level is detected during sampling after 8 serial clocks from detection of the falling edge of the RXDn pin, this falling edge is not recognized as a start bit. The serial clock counter that generates the sample timing is initialized and stops, and input of the next falling edge is waited for.

- **In synchronous mode (MOD bit of ASIMn1 register = 1)**
  The RXDn pin is sampled using the serial clock from the baud rate generator or at the rising edge of serial clock input/output. If the RXDn pin is low level at this time, this is interpreted as a start bit and reception processing starts.

If reception data is interrupted at the fixed low level during reception, reception of this receive data (including error detection) is completed and reception completion interrupt is generated. However, even if the RXD line is fixed at low level, the next reception operation is not started (start bit detection is not performed).
Be sure to set the high level when restarting the reception operation. If the high level is not set, the start bit detection position becomes undefined, and correct reception operation cannot be performed.

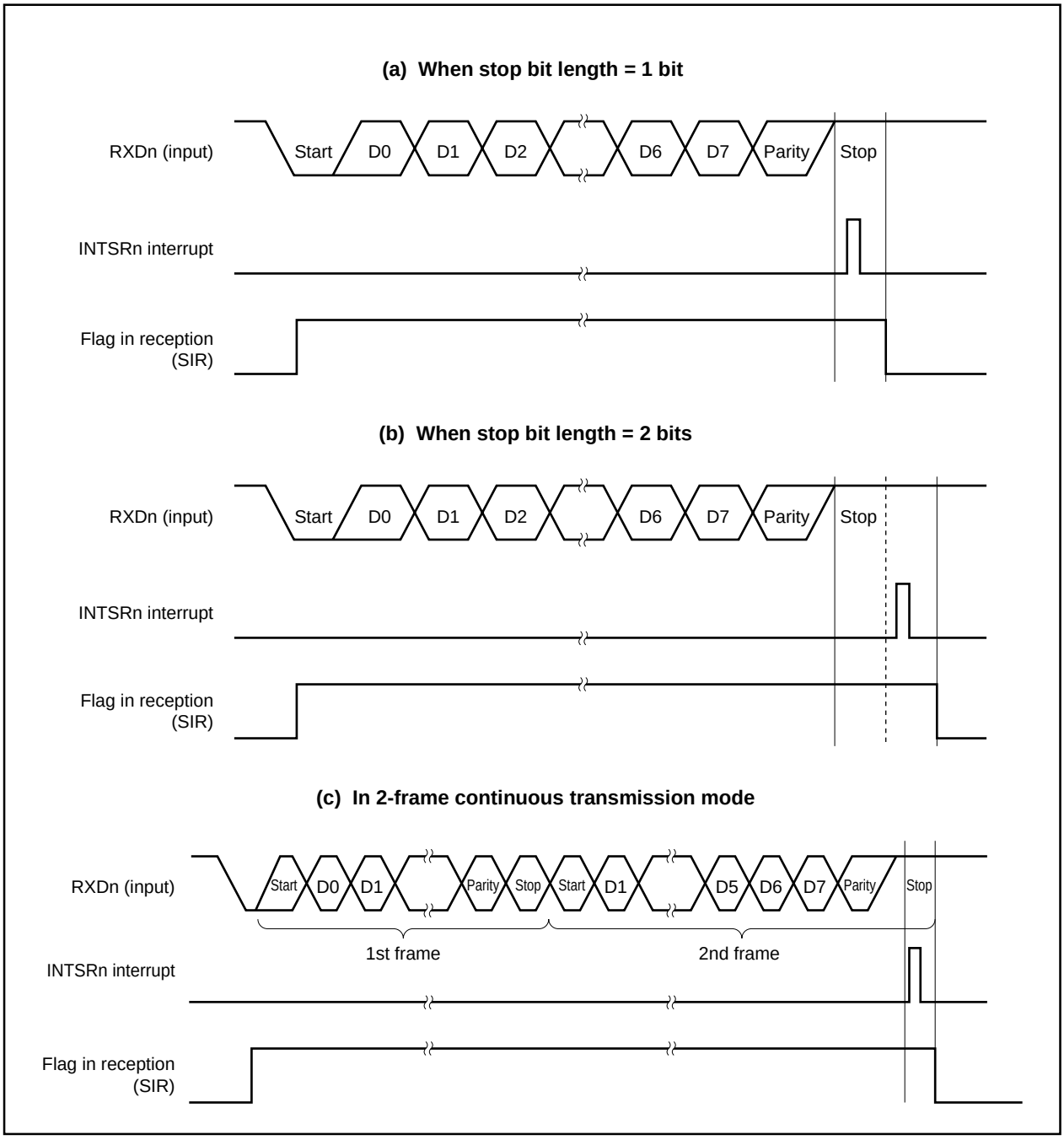
(c) Reception completion interrupt request

When reception of one frame of data has been completed (stop bit detection) when the RXE bit of the ASIMn0 register = 1, the receive data in the shift register is transferred to RXBn/RXBLn and a reception completion interrupt request (INTSRn) is generated after 1 frame or 2 frames of data have been transferred to RXBn/RXBLn.

A reception completion interrupt is also generated upon detection of an error.

When the RXE bit = 0 (reception disabled), no reception completion interrupt is generated.

Figure 10-29. Asynchronous Serial Interface Reception Completion Interrupt Timing



Cautions 1. Even if a reception error occurs, be sure to read the 2-frame continuous reception buffer register n (RXBn)/reception buffer register n (RXBLn). If the RXBn or RXBLn register is not read, an overrun error will occur at the next data reception, and the reception error state will go on indefinitely.

2. Reception is always performed with stop bit length = 1 bit. The second stop bit is ignored.

(4) Reception errors

The three types of error flags of parity errors, framing errors, and overrun errors are affected in synchronization with reception operation. As a result of data reception, the PE, FE, and OVE flags of the ASISn register are set (1) and a reception completion interrupt request (INTSRn) is generated at the same time.

The contents of error that occurred during reception can be detected by reading the contents of the PE, FE, and OVE flags of the ASISn register during the INTSRn interrupt servicing.

The contents of the ASISn register are reset (0) by reading the ASISn register (if the next receive data contains an error, the corresponding error flag is set (1)).

Table 10-8. Reception Error Causes

Error Flag	Reception Error	Causes
PE	Parity error	The parity specification during transmission did not match the parity of the reception data
FE	Framing error	No stop bit was detected
OVE	Overrun error	The reception of the next data was completed before data was read from the reception buffer

(5) Parity types and corresponding operation

A parity bit is used to detect a bit error in communication data. Normally, the same type of parity bit is used at the transmission and reception sides.

(a) Even parity

<1> During transmission

The parity bit is controlled so that number of bits with the value “1” within the transmit data including the parity bit is even. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 1
- If the number of bits with the value “1” within the transmit data is even: 0

<2> During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is odd.

(b) Odd parity

<1> During transmission

In contrast to even parity, the parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is odd. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 0
- If the number of bits with the value “1” within the transmit data is even: 1

<2> During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is even.

(c) 0 parity

During transmission, the parity bit is set to “0” regardless of the transmit data.

During reception, no parity bit check is performed. Therefore, no parity error is generated regardless of whether the parity bit is “0” or “1”.

(d) No parity

No parity bit is added to the transmit data.

During reception, the receive operation is performed as if there were no parity bit. Since there is no parity bit, no parity error is generated.

10.3.6 Synchronous mode

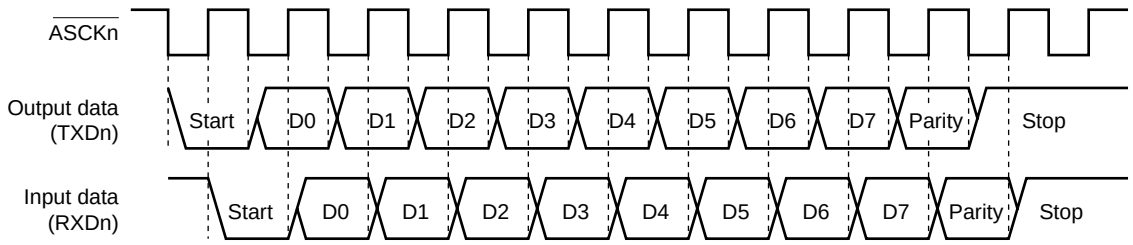
The synchronous mode can be set with the $\overline{\text{ASCKn}}$ pin, which is the serial clock input/output pin (n = 1, 2).

The synchronous mode is set with the MOD bit of the ASIMn1 register, and the serial clock to be used for synchronization is selected with the SCLS bit of the ASIMn0 register.

In the synchronous mode, external clock input is selected when the value of the SCLS bit is 0 (default), and the serial clock output is selected in the case of all other settings. Therefore, when performing settings, make sure that outputs between connection nodes do not conflict.

In the synchronous mode, the falling edge of the serial clock is used as the transmission timing, and the rising edge as the reception timing, but transmit data is output with a delay of 1 system clock (serial clock) (in the external clock synchronous mode, the maximum delay is 2.5 system clocks).

Figure 10-30. Transmission/Reception Timing in Synchronous Mode

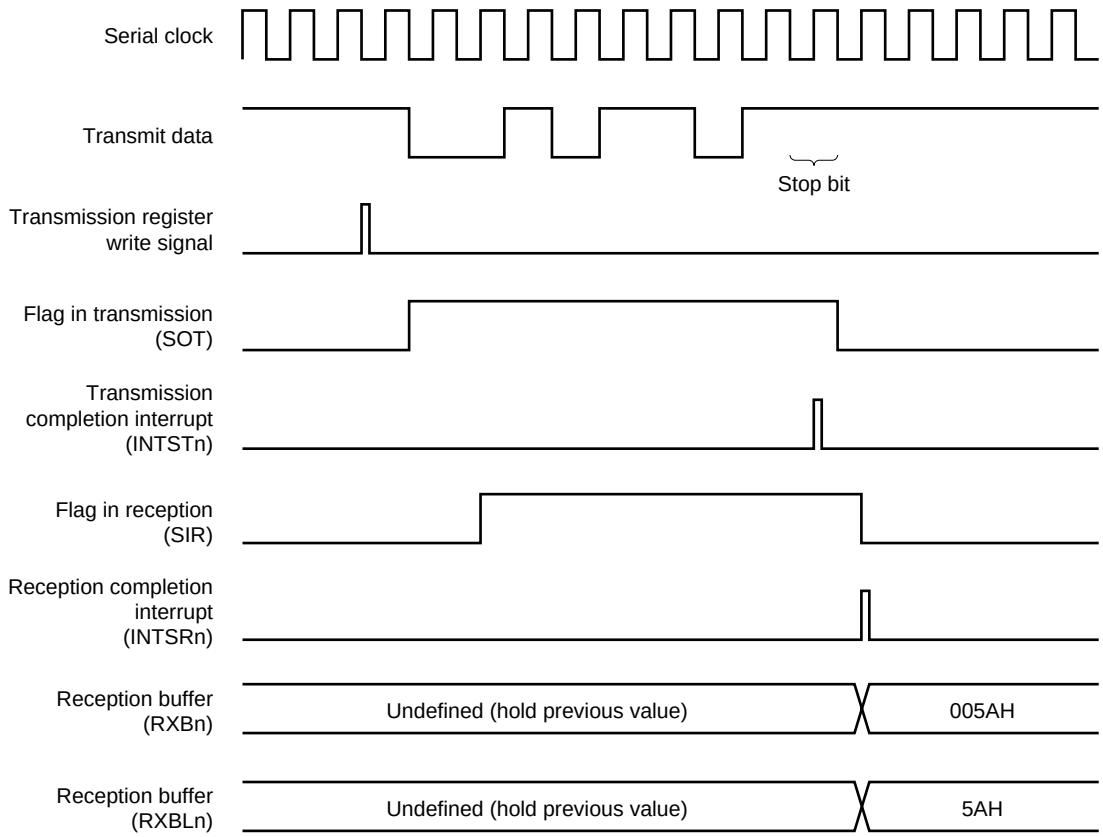


On the data output side, the data changes at the falling edge of the serial clock output.
On the data input side, the data is latched at the rising edge of the serial clock output.
Serial clock output continues as long as the setting is not canceled.

Remark n = 1, 2

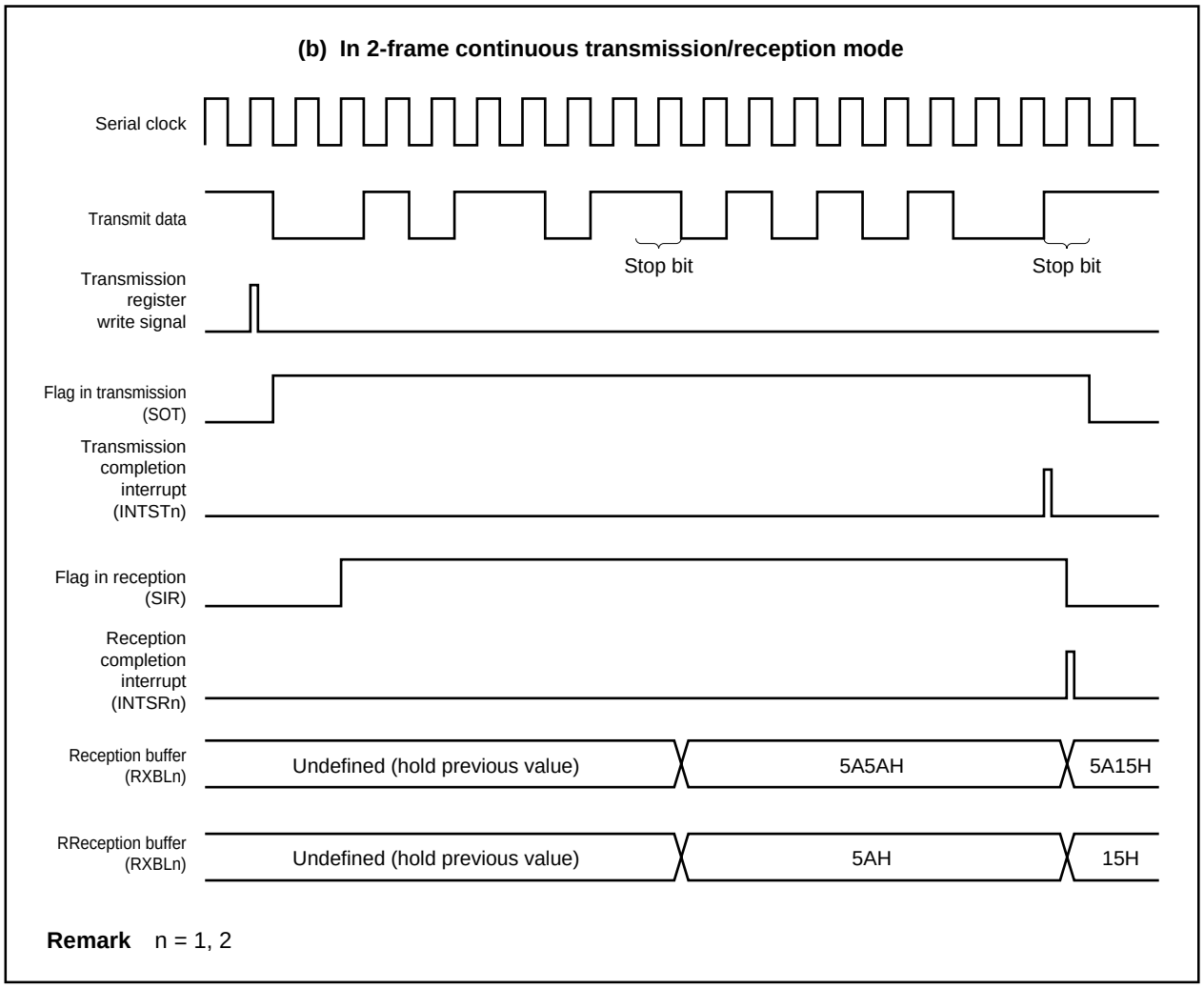
Figure 10-31. Transmission/Reception Timing Chart for Synchronous Mode (1/3)

(a) In 1-frame transmission/reception mode



Remark n = 1, 2

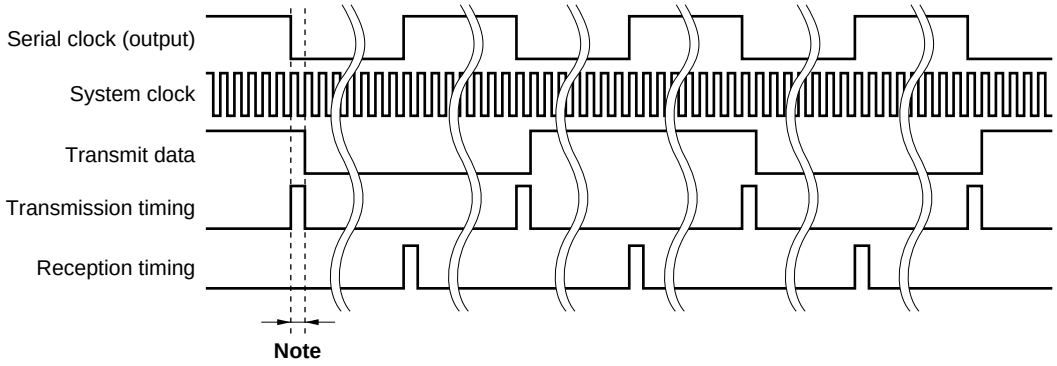
Figure 10-31. Transmission/Reception Timing Chart for Synchronous Mode (2/3)



Remark n = 1, 2

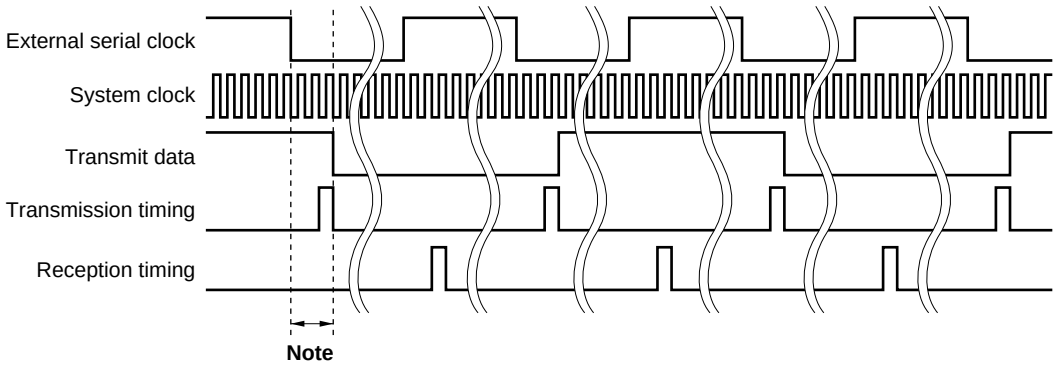
Figure 10-31. Transmission/Reception Timing Chart for Synchronous Mode (3/3)

(c) Transmission/reception timing and transmit data timing during serial clock output



Note The transmit data is delayed by 1 system clock in relation to the serial clock.

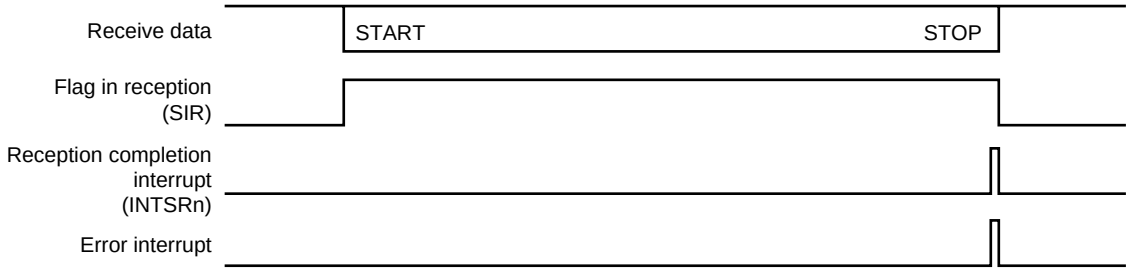
(d) Transmission/reception timing and transmit data timing using external serial clock



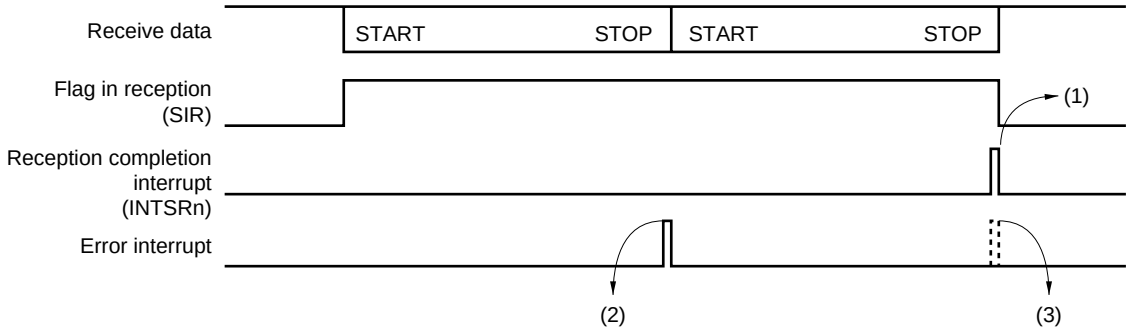
Note Since, during external serial clock synchronization, synchronization is done with the internal system clock when feeding the external serial clock to the internal circuit, a delay ranging from 1 system clock to a maximum of 2.5 system clocks results.

Figure 10-32. Reception Completion Interrupt and Error Interrupt Generation Timing During Synchronous Mode Reception

(a) During normal operation (in 1-frame reception mode)



(b) In 2-frame continuous reception mode



<Explanation>

(1) If the start bit of the second frame is not detected, no reception completion interrupt is generated.

(2) If an error occurs in the first frame, an error interrupt is generated following detection of the stop bit of the first frame (at the calculated position).

(3) If an error occurs in the second frame, an error interrupt is generated simultaneously with a reception completion interrupt.
If an error occurs in the first frame, no error interrupt is generated even if an error occurs in the second frame.

Remark n = 1, 2

10.3.7 Dedicated baud rate generators 1, 2 (BRG1, BRG2)

(1) Configuration of baud rate generators 1, 2 (BRG1, BRG2)

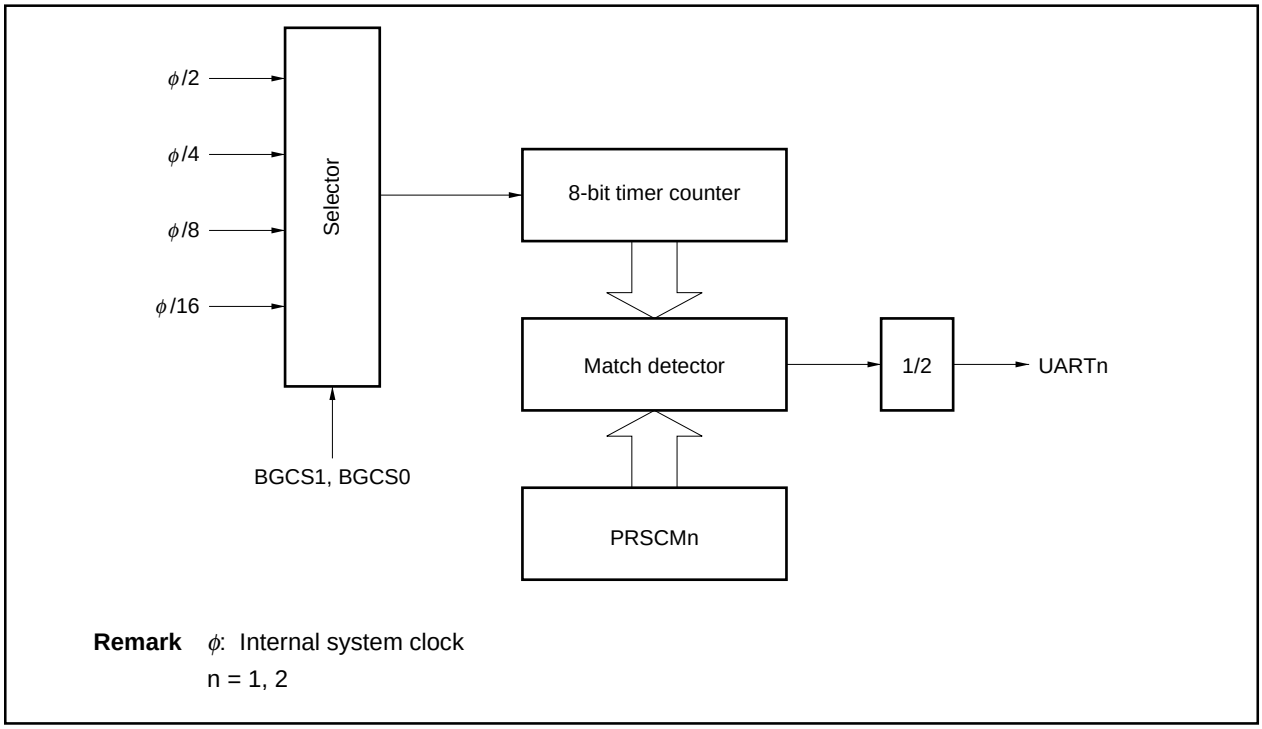
For UART1 and UART2, the serial clock can be selected from the dedicated baud rate generator output or internal system clock (ϕ) for each channel.

The serial clock source is specified with registers ASIM10 and ASIM20.

If dedicated baud rate generator output is specified, BRG1 and BRG2 are selected as the clock sources.

Since the same serial clock can be shared for transmission and reception for one channel, baud rate is the same for the transmission/reception.

Figure 10-33. Block Diagram of Baud Rate Generators 1, 2 (BRG1, BRG2)



Remark ϕ: Internal system clock
n = 1, 2

(2) Dedicated baud rate generators 1, 2 (BRG1, BRG2)

BRGn is configured of an 8-bit timer counter for baud rate signal generation, a prescaler mode register that controls the generation of the baud rate signal (PRSMn), a prescaler compare register that sets the value of the 8-bit timer counter (PRSCMn), and a prescaler (n = 1, 2).

(a) Input clock

The internal system clock (ϕ) is input to BRGn.

(b) Prescaler mode registers 1, 2 (PRSM1, PRSM2)

The PRSMn register controls generation of the UARTn baud rate signal (n = 1, 2).

These registers can be read/written in 8-bit or 1-bit units.

Figure 10-34. Prescaler Mode Registers 1, 2 (PRSM1, PRSM2)

	7	6	5	4	3	2	1	0	Address	Initial value
PRSM1	CE	0	0	0	0	0	BGCS1	BGCS0	FFFFFA2EH	00H

	7	6	5	4	3	2	1	0	Address	Initial value
PRSM2	CE	0	0	0	0	0	BGCS1	BGCS0	FFFFFA4EH	00H

Bit Position	Bit Name	Function
7	CE	Enables baud rate counter operation. 0: Stop baud rate counter operation and fix baud rate output signal to “0: 1: Enable baud rate counter operation and start baud rate output
1, 0	BGCS1, BGCS0	Select count clock to baud rate counter. BGCS1 / BGCS0 / Count Clock Selection 0 / 0 / ϕ/2 0 / 1 / ϕ/4 1 / 0 / ϕ/8 1 / 1 / ϕ/16 **Remark** ϕ: Internal system clock

Cautions 1. Do not change the values of the BGCS1 and BGCS0 bits during transmission/reception operations.

2. Perform PRSMn register settings prior to setting the CE bit to 1 (n = 1, 2).

(c) Prescaler compare registers 1, 2 (PRSCM1, PRSCM2)

PRSCMn is an 8-bit compare register that sets the value of the 8-bit timer counter (n = 1, 2).

These registers can be read/written in 8-bit or 1-bit units.

Figure 10-35. Prescaler Compare Registers 1, 2 (PRSCM1, PRSCM2)

	7	6	5	4	3	2	1	0	Address	Initial value
PRSCM1	PRSCM7	PRSCM6	PRSCM5	PRSCM4	PRSCM3	PRSCM2	PRSCM1	PRSCM0	FFFFFA30H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
PRSCM2	PRSCM7	PRSCM6	PRSCM5	PRSCM4	PRSCM3	PRSCM2	PRSCM1	PRSCM0	FFFFFA50H	00H

Cautions 1. The internal timer counter is cleared by writing to the PRSMn register. Therefore, do not overwrite the PRSCMn register during transmission operation.

2. Perform PRSCMn register settings prior to setting the CE bit to 1. If the contents of the PRSCMn register are overwritten when the value of the CE bit is 1, the cycle of the baud rate signal is not guaranteed.

(d) Baud rate generation

First, when the CE bit of the PRSMn register is overwritten with 1, the 8-bit timer counter for baud rate signal generation starts counting up with the clock selected with bits BGCS1 and BGCS0 of the PRSMn register. The count value of the 8-bit timer counter is compared with the value of the PRSCMn register, and if these values match, a timer count clock pulse of 1 cycle is output to the output control circuit for the baud rate.

The output control circuit for the baud rate reverses the baud rate signal in synchronization with the rising edge of the timer count clock when this pulse is “1”.

(e) Cycle of baud rate signal

The cycle of the baud rate signal is calculated as follows.

- **When setting value of PRSCMn register is 00H**
  (Cycle of signal selected with bits BGCS1, BGCS0 of PRSMn register) × 256 × 2
- **In cases other than above**
  (Cycle of signal selected with bits BGCS1, BGCS0 of PRSMn register) × (setting value of PRSCMn register) × 2

(f) Baud rate setting value

The formulas for calculating the baud rate in the asynchronous mode and the synchronous mode and the formula for calculating the error are as follows.

<1> Formula for calculating baud rate in asynchronous mode

$$\text{Baud rate} = \frac{\phi}{2 \times m \times 2^k \times 16} \text{ [bps]}$$

ϕ = Internal system clock frequency [Hz]

= CPU clock/2 [Hz]

m: Setting value of PRSCMn register ($1 \leq m \leq 256$[Note])

k: Value set with bits BGCS1, BGCS0 of PRSMn register (k = 0, 1, 2, 3)

Note The setting of m = 256 is performed by writing 00H to the PRSCMn register.

<2> Formula for calculating the baud rate in synchronous mode

$$\text{Baud rate} = \frac{\phi}{2 \times m \times 2^k} \text{ [bps]}$$

ϕ = Internal system clock frequency [Hz]

= CPU clock/2 [Hz]

m: Setting value of PRSCMn register ($1 \leq m \leq 256$[Note])

k: Value set with bits BGCS1, BGCS0 of PRSMn register (k = 0, 1, 2, 3)

Note The setting of m = 256 is performed by writing 00H to the PRSCMn register.

<3> Formula for calculating error

$$\text{Error [\%]} = \left(\frac{\text{Actual baud rate} - \text{Desired baud rate}}{\text{Desired baud rate}} \right) \times 100$$

Example (9520 – 9600)/9600 x 100 = –0.833 [%]

Remark Actual baud rate: Baud rate with error
Desired baud rate: Normal baud rate

<4> Baud rate setting example

In an actual system, the output of a prescaler module, etc. is connected to input clock. Table 10-9 shows the baud rate generator setting data at this time.

Table 10-9. Baud Rate Generator Setting Data (BRG = ϕ/2) (1/2)

(a) When ϕ = 32 MHz

Desired Baud Rate		Actual Baud Rate		BGCSm Bit (m = 0, 1)	PRSCMn Register Setting Value (n = 1, 2)	Error
Synchronous Mode	Asynchronous Mode	Synchronous Mode	Asynchronous Mode			
4800	300	4807.692	300.4808	3	208	0.16
9600	600	9615.385	600.9615	3	104	0.16
19200	1200	19230.77	1201.923	3	52	0.16
38400	2400	38461.54	2403.846	3	26	0.16
76800	4800	76923.08	4807.692	3	13	0.16
153600	9600	153846.2	9615.385	2	13	0.16
166400	10400	166666.7	10416.67	1	24	0.16
307200	19200	307692.3	19230.77	1	13	0.16
614400	38400	615384.6	38461.54	0	13	0.16
748800	76800	1142857	71428.57	0	7	–6.99
2457600	153600	2666667	166666.7	0	3	8.51

Table 10-9. Baud Rate Generator Setting Data (BRG = ϕ/2) (2/2)

(b) When ϕ = 40 MHz

Desired Baud Rate		Actual Baud Rate		BGCSm Bit (m = 0, 1)	PRSCMn Register Setting Value (n = 1, 2)	Error
Synchronous Mode	Asynchronous Mode	Synchronous Mode	Asynchronous Mode			
4800	300	4882.813	305.1758	3	256	1.73
9600	600	9615.385	600.9615	3	130	0.16
19200	1200	19230.77	1201.923	3	65	0.16
38400	2400	38461.54	2403.846	2	65	0.16
76800	4800	76923.08	4807.692	1	65	0.16
153600	9600	153846.2	9615.385	0	65	0.16
166400	10400	166666.7	10416.67	0	60	0.16
307200	19200	303030.3	18939.39	0	33	–1.36
614400	38400	625000	39062.5	0	16	1.73
748800	76800	1250000	78125	0	8	1.73
2457600	153600	2500000	156250	0	4	1.73

(c) When ϕ = 50 MHz

Desired Baud Rate		Actual Baud Rate		BGCSm Bit (m = 0, 1)	PRSCMn Register Setting Value (n = 1, 2)	Error
Synchronous Mode	Asynchronous Mode	Synchronous Mode	Asynchronous Mode			
9600	600	9585.89	599.1181	3	163	–0.15
19200	1200	19171.78	1198.236	2	163	–0.15
38400	2400	38343.56	2396.472	1	163	–0.15
76800	4800	76687.12	4792.945	0	163	–0.15
153600	9600	154321	9645.062	0	81	0.47
166400	10400	166666.7	10416.67	0	75	0.16
307200	19200	312500	19531.25	0	40	1.73
614400	38400	625000	39062.5	0	20	1.73
748800	76800	1250000	78125	0	10	1.73
2457600	153600	2500000	156250	0	5	1.73

10.4 Clocked Serial Interfaces 0, 1 (CSI0, CSI1)

10.4.1 Features

- High-speed transfer: Maximum 4 Mbps
- Half-duplex communications
- Master mode or slave mode can be selected
- Transmission data length: 8 bits or 16 bits can be set
- Transfer data direction can be switched between MSB first and LSB first
- Eight clock signals can be selected (7 master clocks and 1 slave clock)
- 3-wire type SOn : Serial transmit data output
  SIn : Serial transmit data input
  $\overline{\text{SCK}}$n: Serial clock input/output
- Interrupt sources: 1 type
  - Transmission/reception completion interrupt (INTCSIn)
- Transmission/reception mode and reception-only mode can be specified
- Two transmission buffers (SOTBFn/SOTBFLn, SOTBn/SOTBLn) and two reception buffers (SIRBn/SIRBLn, SIRBEn/SIRBELn) are provided on chip
- Single transfer mode and repeat transfer mode can be specified

Remark n = 0, 1

10.4.2 Configuration

CSIn is controlled via the clocked serial interface mode register (CSIMn) (n = 0, 1). Transmission/reception of data is performed with reading SIOn register (n = 0, 1).

(1) Clocked serial interface mode registers 0, 1 (CSIM0, CSIM1)

The SCIMn register is an 8-bit register that specifies the operation of CSIn.

(2) Clocked serial interface clock selection registers 0, 1 (CSIC0, CSIC1)

The CSICn register is an 8-bit register that controls the CSIn serial transfer operation.

(3) Serial I/O shift registers 0, 1 (SIO0, SIO1)

The SIOn register is a 16-bit shift register that converts parallel data into serial data.
The SIOn register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by access of the buffer register.

(4) Serial I/O shift registers L0, L1 (SIOL0, SIOL1)

The SIOLn register is an 8-bit shift register that converts parallel data into serial data.
The SIOLn register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by access of the buffer register .

(5) Clocked serial interface reception buffer registers 0, 1 (SIRB0, SIRB1)

The SIRBn register is a 16-bit buffer register that stores receive data.

(6) Clocked serial interface reception buffer registers L0, L1 (SIRBL0, SIRBL1)

The SIRBLn register is an 8-bit buffer register that stores receive data.

(7) Clocked serial interface read-only reception buffer registers 0, 1 (SIRBE0, SIRBE1)

The SIRBEn register is a 16-bit buffer register that stores receive data.
The SIRBEn register is the same as the SIRBn register. It is used to read the contents of the SIRBn register.

(8) Clocked serial interface read-only reception buffer registers L0, L1 (SIRBEL0, SIRBEL1)

The SIRBELn register is an 8-bit buffer register that stores receive data.
The SIRBELn register is the same as the lower bytes of the SIRBn register. It is used to read the contents of the SIRBLn register.

(9) Clocked serial interface transmission buffer registers 0, 1 (SOTB0, SOTB1)

The SOTBn register is a 16-bit buffer register that stores transmit data.

(10) Clocked serial interface transmission buffer registers L0, L1 (SOTBL0, SOTBL1)

The SOTBLn register is an 8-bit buffer register that stores transmit data.

(11) Clocked serial interface initial transmission buffer registers (SOTBF0, SOTBF1)

The SOTBFn register is a 16-bit buffer register that stores the initial transmit data in the repeat transfer mode.

(12) Clocked serial interface initial transmission buffer register L (SOTBFL0, SOTBFL1)

The SOTBFLn register is an 8-bit buffer register that stores initial transmit data in the repeat transfer mode.

(13) Selector

The selector selects the serial clock to be used.

(14) Serial clock control circuit

Controls the serial clock supply to the shift register. Also controls the clock output to the $\overline{\text{SCKn}}$ pin when the internal clock is used.

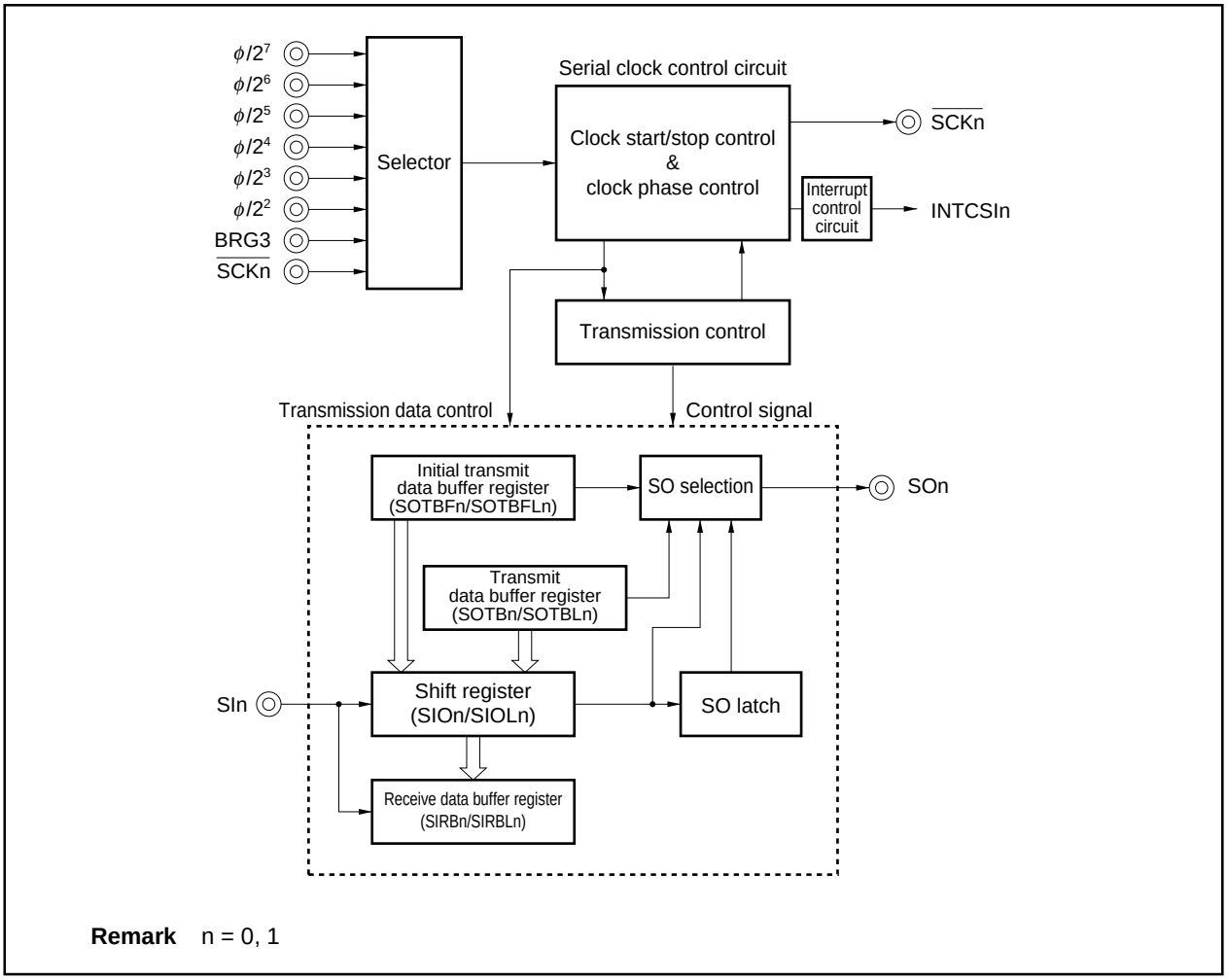
(15) Serial clock counter

Counts the serial clock output or input during transmission/reception operation, and checks whether 8-bit data transmission/reception has been performed.

(16) Interrupt control circuit

Controls the interrupt request timing.

Figure 10-36. Block Diagram of Clocked Serial Interface



Remark n = 0, 1

10.4.3 Control registers

(1) Clocked serial interface mode registers 0, 1 (CSIM0, CSIM1)

The CSIMn register controls the CSIn operation (n = 0, 1).

These registers can be read/written in 8-bit or 1-bit units (however, bit 0 is read-only).

Caution Overwriting the TRMD, CCL, DIR, CSIT, and AUTO bits of the CSIMn register can be done only when the CSOT bit = 0. If these bits are overwritten at any other time, the operation cannot be guaranteed.

Figure 10-37. Clocked Serial Interface Mode Registers 0, 1 (CSIM0, CSIM1) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
CSIM0	CSIE	TRMD	CCL	DIR	CSIT	AUTO	0	CSOT	FFFFF900H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
CSIM1	CSIE	TRMD	CCL	DIR	CSIT	AUTO	0	CSOT	FFFFF910H	00H

Bit Position	Bit Name	Function
7	CSIE	Enables/disables CSIn operation. 0: Enable CSIn operation. 1: Disable CSIn operation. The internal CSIn circuit can be reset asynchronously by setting the CSIE bit to 0. For the $\overline{\text{SCK}}$n and SOn pin output status when the CSIE bit = 0, refer to **10.4.5 Output pins**.
6	TRMD	Specifies transmission/reception mode. 0: Receive-only mode 1: Transmission/reception mode When the TRMD bit = 0, receive-only transfer is performed and the SOn pin output is fixed to low level. Data reception is started by reading the SIRBn register. When the TRMD bit = 1, transmission/reception is started by writing data to the SOTBn register.
5	CCL	Specifies data length. 0: 8 bits 1: 16 bits
4	DIR	Specifies transfer direction mode (MSB/LSB). 0: First bit of transfer data is MSB 1: First bit of transfer data is LSB

Remark n = 0, 1

Figure 10-37. Clocked Serial Interface Mode Registers 0, 1 (CSIM0, CSIM1) (2/2)

Bit Position	Bit Name	Function
3	CSIT	Controls delay of interrupt request signal. 0: No delay 1: Delay mode (interrupt request signal is delayed 1/2 cycle). The delay mode (CSIT bit = 1) is effective only in the master mode (CKS2 to CSK0 bits of the CSICn register are not 11B). In the slave mode (CKS2 to CKS0 bits are 11B), do not set the delay mode. **Caution The delay mode (CSIT bit = 1) is effective only in the master mode (CKS2 to CSK0 bits of the CSICn register are not 111B). In the slave mode (CKS2 to CKS0 bits are 111B), do not set the delay mode.**
2	AUTO	Specifies single transfer mode or repeat transfer mode. 0: Single transfer mode 1: Repeat transfer mode
0	CSOT	Flag indicating transfer status. 0: Idle status 1: Transfer execution status **Caution The CSOT bit is cleared (0) by writing 0 to the CSIE bit.**

Remark n = 0, 1

(2) Clocked serial interface clock selection registers 0, 1 (CSIC0, CSIC1)

The CSICn register is an 8-bit register that controls the CSIn transfer operation (n = 0, 1).

These registers can be read/written in 8-bit or 1-bit units.

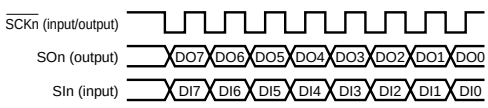
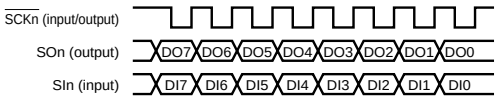
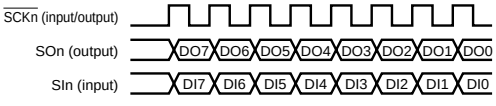
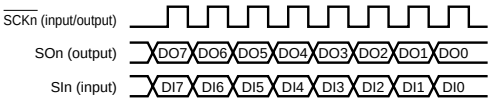
Caution The CSICn register can be overwritten only when the CSIE bit of the CSIMn register = 0.

Figure 10-38. Clocked Serial Interface Clock Selection Registers 0, 1 (CSIC0, CSIC1) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
CSIC0	0	0	0	CKP	DAP	CKS2	CKS1	CKS0	FFFFF901H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
CSIC1	0	0	0	CKP	DAP	CKS2	CKS1	CKS0	FFFFF911H	00H

Bit Position	Bit Name	Function
4, 3	CKP, DAP	Specifies operation mode.

CKP	DAP	Operation Mode
0	0	
0	1	
1	0	
1	1	

Remark n = 0, 1

Figure 10-38. Clocked Serial Interface Clock Selection Registers 0, 1 (CSIC0, CSIC1) (2/2)

Bit Position	Bit Name	Function
2 to 0	CKS2 to CKS0	Specifies input clock.

CKS2	CKS1	CKS0	Input Clock	Mode
0	0	0	$\phi/2^7$	Master mode
0	0	1	$\phi/2^6$	Master mode
0	1	0	$\phi/2^5$	Master mode
0	1	1	$\phi/2^4$	Master mode
1	0	0	$\phi/2^3$	Master mode
1	0	1	$\phi/2^2$	Master mode
1	1	0	Clock generated by BRG3	Master mode
1	1	1	External clock ($\overline{\text{SCKn}}$)	Slave mode

Remark ϕ: Internal system clock frequency

n = 0, 1

(3) Clocked serial interface reception buffer registers 0, 1 (SIRB0, SIRB1)

The SIRBn register is a 16-bit buffer register that stores receive data (n = 0, 1).

When the receive-only mode is set (TRMD bit of CSIMn register = 0), the reception operation is started by reading data from the SIRBn register.

These registers are read-only, in 16-bit units.

In addition to reset input, these registers can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

Figure 10-39. Clocked Serial Interface Reception Buffer Registers 0, 1 (SIRB0, SIRB1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIRB0	SIRB 15	SIRB 14	SIRB 13	SIRB 12	SIRB 11	SIRB 10	SIRB 9	SIRB 8	SIRB 7	SIRB 6	SIRB 5	SIRB 4	SIRB 3	SIRB 2	SIRB 1	SIRB 0	FFFFF902H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIRB1	SIRB 15	SIRB 14	SIRB 13	SIRB 12	SIRB 11	SIRB 10	SIRB 9	SIRB 8	SIRB 7	SIRB 6	SIRB 5	SIRB 4	SIRB 3	SIRB 2	SIRB 1	SIRB 0	FFFFF912H	0000H

Bit Position	Bit Name	Function
15 to 0	SIRB15 to SIRB0	Store receive data.

Cautions 1. Read the SIRBn register only when the 16-bit data length has been set (CCL bit of CSIMn register = 1).

2. When the single transfer mode has been set (AUTO bit of CSIMn register = 0), perform read operation only in the idle state (CSOT bit of CSIMn register = 0). If the SIRBn register is read during data transfer, the data cannot be guaranteed.

(4) Clocked serial interface reception buffer registers L0, L1 (SIRBL0, SIRBL1)

The SIRBLn register is an 8-bit buffer register that stores receive data (n = 0, 1).

When the receive-only mode is set (TRMD bit of CSIMn register = 0), the reception operation is started by reading data from the SIRBLn register.

These registers are read-only, in 8-bit units.

In addition to reset input, these registers can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

The SIRBLn register is the same as the lower bytes of the SIRBn register.

Figure 10-40. Clocked Serial Interface Reception Buffer Registers L0, L1 (SIRBL0, SIRBL1)

	7	6	5	4	3	2	1	0	Address	Initial value
SIRBL0	SIRB7	SIRB6	SIRB5	SIRB4	SIRB3	SIRB2	SIRB1	SIRB0	FFFFF902H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
SIRBL1	SIRB7	SIRB6	SIRB5	SIRB4	SIRB3	SIRB2	SIRB1	SIRB0	FFFFF912H	00H

Bit Position	Bit Name	Function
7 to 0	SIRB7 to SIRB0	Stores receive data.

Cautions 1. Read the SIRBLn register only when the 8-bit data length has been set (CCL bit of CSIMn register = 0).

2. When the single transfer mode is set (AUTO bit of CSIMn register = 0), perform read operation only in the idle state (CSOT bit of CSIMn register = 0). If the SIRBLn register is read during data transfer, the data cannot be guaranteed.

(5) Clocked serial interface read-only reception buffer registers 0, 1 (SIRBE0, SIRBE1)

The SIRBEn register is a 16-bit buffer register that stores receive data (n = 0, 1).

These registers are read-only, in 16-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

The SIRBEn register is the same as the SIRBn register. It is used to read the contents of the SIRBn register.

Figure 10-41. Clocked Serial Interface Read-Only Reception Buffer Registers 0, 1 (SIRBE0, SIRBE1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIRBE0	SIRBE 15	SIRBE 14	SIRBE 13	SIRBE 12	SIRBE 11	SIRBE 10	SIRBE 9	SIRBE 8	SIRBE 7	SIRBE 6	SIRBE 5	SIRBE 4	SIRBE 3	SIRBE 2	SIRBE 1	SIRBE 0	FFFFF906H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIRBE1	SIRBE 15	SIRBE 14	SIRBE 13	SIRBE 12	SIRBE 11	SIRBE 10	SIRBE 9	SIRBE 8	SIRBE 7	SIRBE 6	SIRBE 5	SIRBE 4	SIRBE 3	SIRBE 2	SIRBE 1	SIRBE 0	FFFFF916H	0000H

Bit Position	Bit Name	Function
15 to 0	SIRBE15 to SIRBE0	Store receive data.

Cautions 1. The receive operation is not started even if data is read from the SIRBEn register.

2. The SIRBEn register can be read only if the 16-bit data length is set (CCL bit of CSIMn register = 1).

(6) Clocked serial interface read-only reception buffer registers L0, L1 (SIRBEL0, SIRBEL1)

The SIRBELn register is an 8-bit buffer register that stores receive data (n = 0, 1).

These registers are read-only, in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

The SIRBELn register is the same as the lower byte of the SIRBn register. It is used to read the contents of the SIRBLn register.

Figure 10-42. Clocked Serial Interface Read-Only Reception Buffer Registers L0, L1 (SIRBEL0, SIRBEL1)

	7	6	5	4	3	2	1	0	Address	Initial value
SIRBEL0	SIRBE7	SIRBE6	SIRBE5	SIRBE4	SIRBE3	SIRBE2	SIRBE1	SIRBE0	FFFFF906H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
SIRBEL1	SIRBE7	SIRBE6	SIRBE5	SIRBE4	SIRBE3	SIRBE2	SIRBE1	SIRBE0	FFFFF916H	00H

Bit Position	Bit Name	Function
7 to 0	SIRBE7 to SIRBE0	Store receive data.

Cautions 1. The receive operation is not started even if data is read from the SIRBELn register.

2. The SIRBELn register can be read only if the 8-bit data length has been set (CCL bit of CSIMn register = 0).

(7) Clocked serial interface transmission buffer registers 0, 1 (SOTB0, SOTB1)

The SOTBn register is a 16-bit buffer register that stores transmit data (n = 0, 1).

When the transmission/reception mode is set (TRMD bit of CSIMn register = 1), the transmission operation is started by writing data to the SOTBn register.

This register can be read/written in 16-bit units.

Figure 10-43. Clocked Serial Interface Transmission Buffer Registers 0, 1 (SOTB0, SOTB1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SOTB0	SOTB15	SOTB14	SOTB13	SOTB12	SOTB11	SOTB10	SOTB9	SOTB8	SOTB7	SOTB6	SOTB5	SOTB4	SOTB3	SOTB2	SOTB1	SOTB0	FFFFF904H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SOTB1	SOTB15	SOTB14	SOTB13	SOTB12	SOTB11	SOTB10	SOTB9	SOTB8	SOTB7	SOTB6	SOTB5	SOTB4	SOTB3	SOTB2	SOTB1	SOTB0	FFFFF914H	0000H

Bit Position	Bit Name	Function
15 to 0	SOTB15 to SOTB0	Store transmit data.

Cautions 1. Access the SOTBn register only when the 16-bit data length is set (CCL bit of CSIMn register = 1).

2. When the single transfer mode is set (AUTO bit of CSIMn register = 0), perform access only in the idle state (CSOT bit of CSIMn register = 0). If the SOTBn register is accessed during data transfer, the data cannot be guaranteed.

(8) Clocked serial interface transmission buffer registers L0, L1 (SOTBL0, SOTBL1)

The SOTBLn register is an 8-bit buffer register that stores transmit data (n = 0, 1).

When the transmission/reception mode is set (TRMD bit of CSIMn register = 1), the transmission operation is started by writing data to the SOTBLn register.

These registers can be read/written in 8-bit units.

The SOTBLn register is the same as the lower bytes of the SOTBn register.

Figure 10-44. Clocked Serial Interface Transmission Buffer Registers L0, L1 (SOTBL0, SOTBL1)

	7	6	5	4	3	2	1	0	Address	Initial value
SOTBL0	SOTB7	SOTB6	SOTB5	SOTB4	SOTB3	SOTB2	SOTB1	SOTB0	FFFFF904H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
SOTBL1	SOTB7	SOTB6	SOTB5	SOTB4	SOTB3	SOTB2	SOTB1	SOTB0	FFFFF914H	00H

Bit Position	Bit Name	Function
7 to 0	SOTB7 to SOTB0	Store transmit data.

Cautions 1. Access the SOTBLn register only when the 8-bit data length has been set (CCL bit of CSIMn register = 0).

2. When the single transfer mode is set (AUTO bit of CSIMn register = 0), perform access only in the idle state (CSOT bit of CSIMn register = 0). If the SOTBLn register is accessed during data transfer, the data cannot be guaranteed.

(9) Clocked serial interface initial transmission buffer registers 0, 1 (SOTBF0, SOTBF1)

The SOTBFn register is a 16-bit buffer register that stores initial transmission data in the repeat transfer mode (n = 0, 1).

The transmission operation is not started even if data is written to the SOTBFn register.

These registers can be read/written in 16-bit units.

Figure 10-45. Clocked Serial Interface Initial Transmission Buffer Registers 0, 1 (SOTBF0, SOTBF1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SOTBF0	SOTBF 15	SOTBF 14	SOTBF 13	SOTBF 12	SOTBF 11	SOTBF 10	SOTBF 9	SOTBF 8	SOTBF 7	SOTBF 6	SOTBF 5	SOTBF 4	SOTBF 3	SOTBF 2	SOTBF 1	SOTBF 0	FFFFF908H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SOTBF1	SOTBF 15	SOTBF 14	SOTBF 13	SOTBF 12	SOTBF 11	SOTBF 10	SOTBF 9	SOTBF 8	SOTBF 7	SOTBF 6	SOTBF 5	SOTBF 4	SOTBF 3	SOTBF 2	SOTBF 1	SOTBF 0	FFFFF918H	0000H

Bit Position	Bit Name	Function
15 to 0	SOTBF15 to SOTBF0	Stores initial transmission data in repeat transfer mode.

Caution Access the SOTBFn register only when the 16-bit data length has been set (CCL bit of CSIMn register = 1), and only in the idle state (CSOT bit of CSIMn register = 0). If the SOTBFn register is accessed during data transfer, the data cannot be guaranteed.

(10) Clocked serial interface initial transmission buffer registers L0, L1 (SOTBFL0, SOTBFL1)

The SOTBFLn register is an 8-bit buffer register that stores initial transmission data in the repeat transfer mode (n = 0, 1).

The transmission operation is not started even if data is written to the SOTBFLn register.

These registers can be read/written in 8-bit units.

The SOTBFLn register is the same as the lower bytes of the SOTBFn register.

Figure 10-46. Clocked Serial Interface Initial Transmission Buffer Registers L0, L1 (SOTBFL0, SOTBFL1)

	7	6	5	4	3	2	1	0	Address	Initial value
SOTBFL0	SOTBF7	SOTBF6	SOTBF5	SOTBF4	SOTBF3	SOTBF2	SOTBF1	SOTBF0	FFFFF908H	00H

	7	6	5	4	3	2	1	0	Address	Initial value
SOTBFL1	SOTBF7	SOTBF6	SOTBF5	SOTBF4	SOTBF3	SOTBF2	SOTBF1	SOTBF0	FFFFF918H	00H

Bit Position	Bit Name	Function
7 to 0	SOTBF7 to SOTBF0	Store initial transmission data in repeat transfer mode.

Caution Access the SOTBFLn register only when the 8-bit data length has been set (CCL bit of CSIMn register = 0), and only in the idle state (CSOT bit of CSIMn register = 0). If the SOTBFLn register is accessed during data transfer, the data cannot be guaranteed.

(11) Serial I/O shift registers 0, 1 (SIO0, SIO1)

The SIOn register is a 16-bit shift register that converts parallel data into serial data (n = 0, 1).

The transfer operation is not started even if the SIOn register is read.

These registers are read-only, in 16-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

Figure 10-47. Serial I/O Shift Registers 0, 1 (SIO0, SIO1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIO0	SIO15	SIO14	SIO13	SIO12	SIO11	SIO10	SIO9	SIO8	SIO7	SIO6	SIO5	SIO4	SIO3	SIO2	SIO1	SIO0	FFFFF90AH	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SIO1	SIO15	SIO14	SIO13	SIO12	SIO11	SIO10	SIO9	SIO8	SIO7	SIO6	SIO5	SIO4	SIO3	SIO2	SIO1	SIO0	FFFFF91AH	0000H

Bit Position	Bit Name	Function
15-0	SIO15- SIO0	Data is shifted in (reception) or shifted out (transmission) from the MSB or LSB side.

Caution Access the SIOn register only when the 16-bit data length has been set (CCL bit of CSIMn register = 1), and only in the idle state (CSOT bit of CSIMn register = 0). If the SIOn register is accessed during data transfer, the data cannot be guaranteed.

(12) Serial I/O shift registers L0, L1 (SIOL0, SIOL1)

The SIOLn register is an 8-bit shift register that converts parallel data into serial data (n = 0, 1).

The transfer operation is not started even if the SIOLn register is read.

These registers are read-only, in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIE bit of the CSIMn register.

The SIOLn register is the same as the lower bytes of the SIOn register.

Figure 10-48. Serial I/O Shift Registers L0, L1 (SIOL0, SIOL1)

	7	6	5	4	3	2	1	0	Address	Initial value
SIOL0	SIO7	SIO6	SIO5	SIO4	SIO3	SIO2	SIO1	SIO0	FFFFF90AH	00H

	7	6	5	4	3	2	1	0	Address	Initial value
SIOL1	SIO7	SIO6	SIO5	SIO4	SIO3	SIO2	SIO1	SIO0	FFFFF91AH	00H

Bit Position	Bit Name	Function
7 to 0	SIO7 to SIO0	Data is shifted in (reception) or shifted out (transmission) from the MSB or LSB side.

Caution Access the SIOLn register only when the 8-bit data length has been set (CCL bit of CSIMn register = 0), and only in the idle state (CSOT bit of CSIMn register = 0). If the SIOLn register is accessed during data transfer, the data cannot be guaranteed.

10.4.4 Operation

(1) Single transfer mode

(a) Usage

In the receive-only mode (TRMD bit of CSIMn register = 0), transfer is started by reading[Note 1] the receive data buffer register (SIRBn/SIRBLn) (n = 0, 1).

In the transmission/reception mode (TRMD bit of CSIMn register = 1), transfer is started by writing[Note 2] to the transmit data buffer register (SOTBn/SOTBLn).

In the slave mode, the operation must be enabled beforehand (CSIE bit of CSIMn register = 1).

When transfer is started, the value of the CSOT bit of the CSIMn register becomes 1 (transmission execution status).

Upon transfer completion, the transmission/reception completion interrupt (INTCSIn) is set (1), and the CSOT bit is cleared (0). The next data transfer request is then waited for.

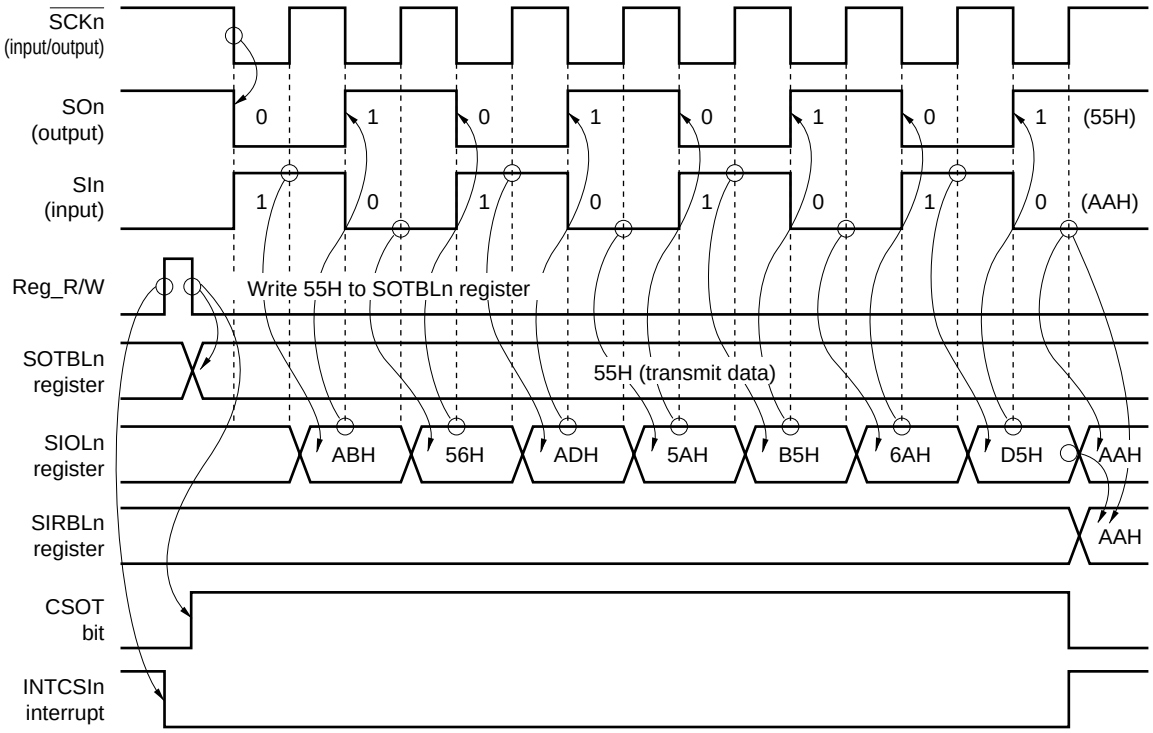
Notes 1. When the 16-bit data length (CCL bit of CSIMn register = 1) has been set, read the SIRBn register. When the 8-bit data length (CCL bit of CSIMn register = 0) has been set, read the SIRBLn register.

2. When the 16-bit data length (CCL bit of CSIMn register = 1) has been set, write to the SOTBn register. When the 8-bit data length (CCL bit of CSIMn register = 0) has been set, write to the SOTBLn register.

Caution When the CSOT bit of the CSIMn register = 1, do not manipulate the CSIn register.

Figure 10-49. Timing Chart in Single Transfer Mode (1/2)

(a) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, operation mode: CKP bit = 0, DAP bit = 0

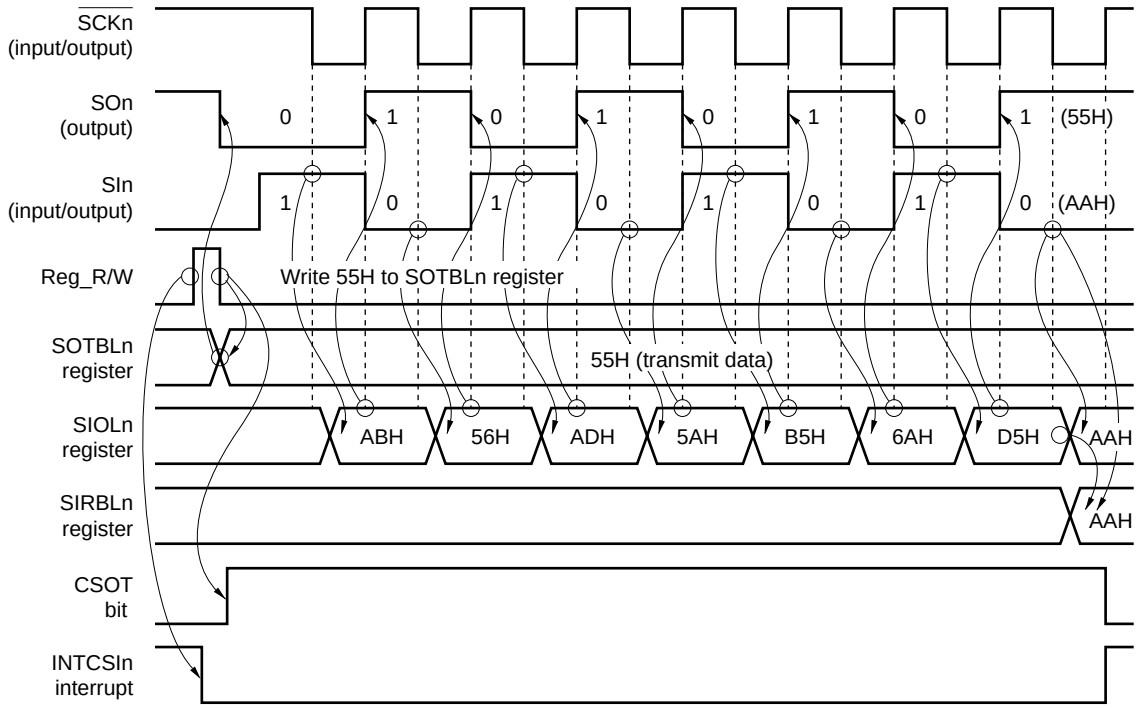


Remarks 1. n = 0, 1

2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed**.**

Figure 10-49. Timing Chart in Single Transfer Mode (2/2)

(b) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, operation mode: CKP bit = 0, DAP bit = 1



Remarks 1. n = 0, 1

2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

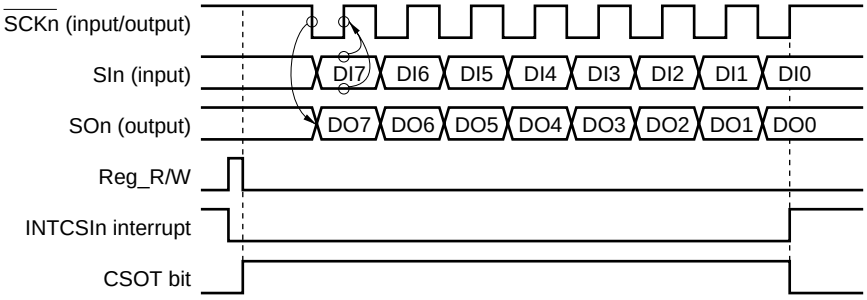
(b) Clock phase selection

The following shows the timing when changing the conditions for clock phase selection (CKP bit of CSICn register) and data phase selection (DAP bit of CSICn register) under the following conditions.

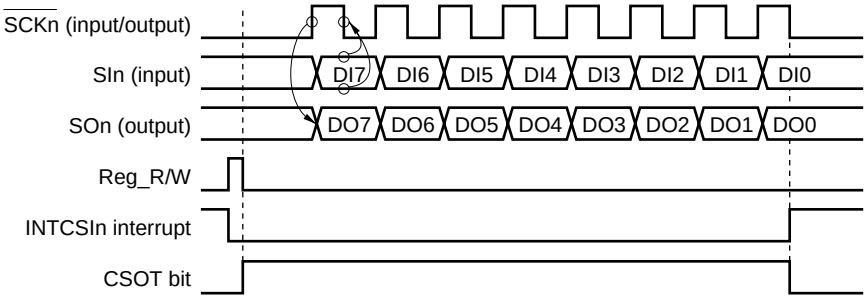
- Data length = 8 bits (CCL bit of CSIMn register = 0)
- First bit of transfer data = MSB (DIR bit of CSIMn register = 0)
- No interrupt request signal delay control (CSIT bit of CSIMn register = 0)

Figure 10-50. Timing Chart According to Clock Phase Selection (1/2)

(a) When CKP bit = 0, DAP bit = 0



(b) When CKP bit = 1, DAP bit = 0

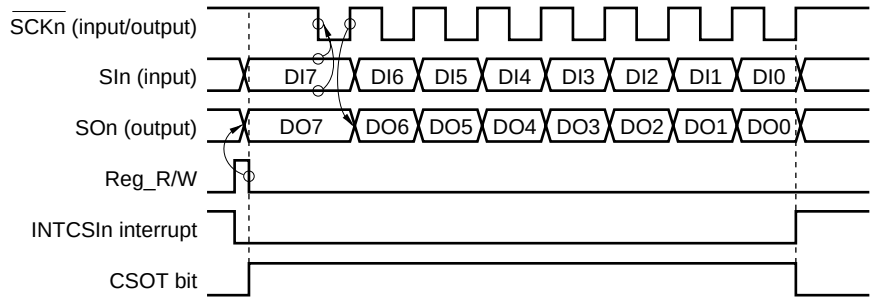


Remarks 1. n = 0, 1

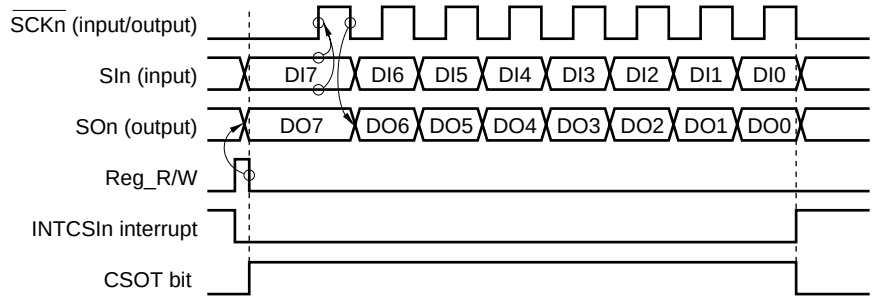
2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

Figure 10-50. Timing Chart According to Clock Phase Selection (2/2)

(c) When CKP bit = 0, DAP bit = 1



(d) When CKP bit = 1, DAP bit = 1



Remarks 1. n = 0, 1

2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

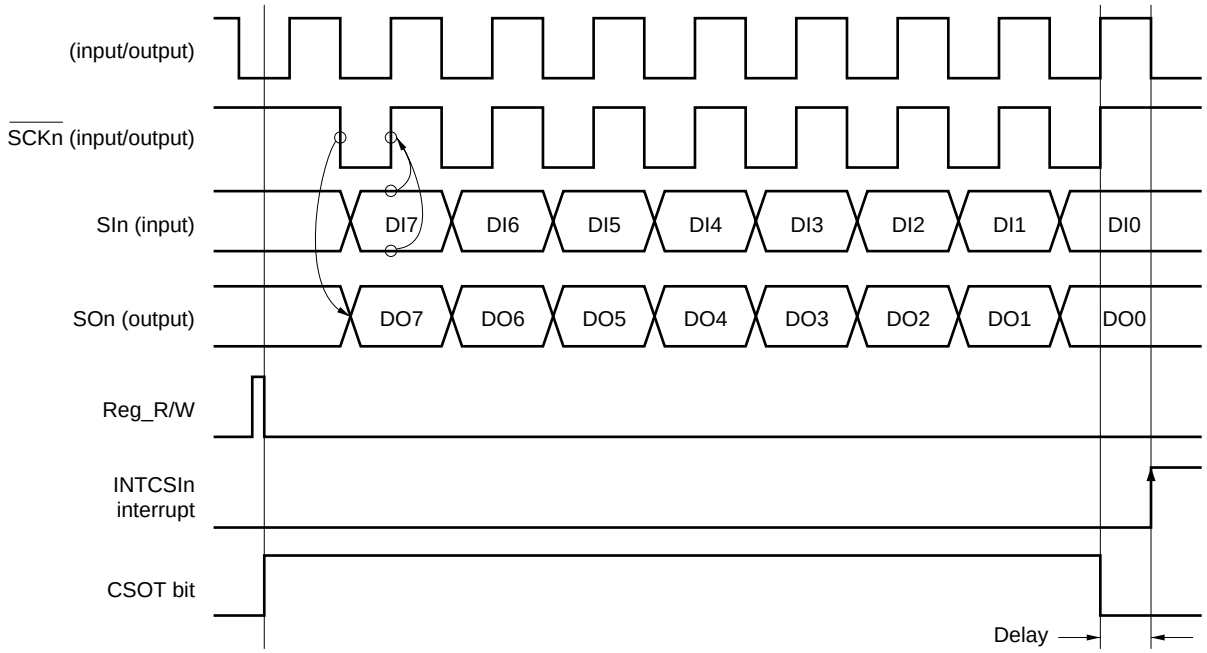
(c) Transmission/reception completion interrupt request signals (INTCSI0, INTCSI1)

INTCSIn is set (1) upon completion of data transmission/reception.

Caution The delay mode (CSIT bit = 1) is valid only in the master mode (bits CKS2 to CKS0 of the CSICn register are not 111B). The delay mode cannot be set when the slave mode is set (bits CKS2 to CKS0 = 111B).

Figure 10-51. Timing Chart of Interrupt Request Signal Output in Delay Mode (1/2)

(a) When CKP bit = 0, DAP bit = 0

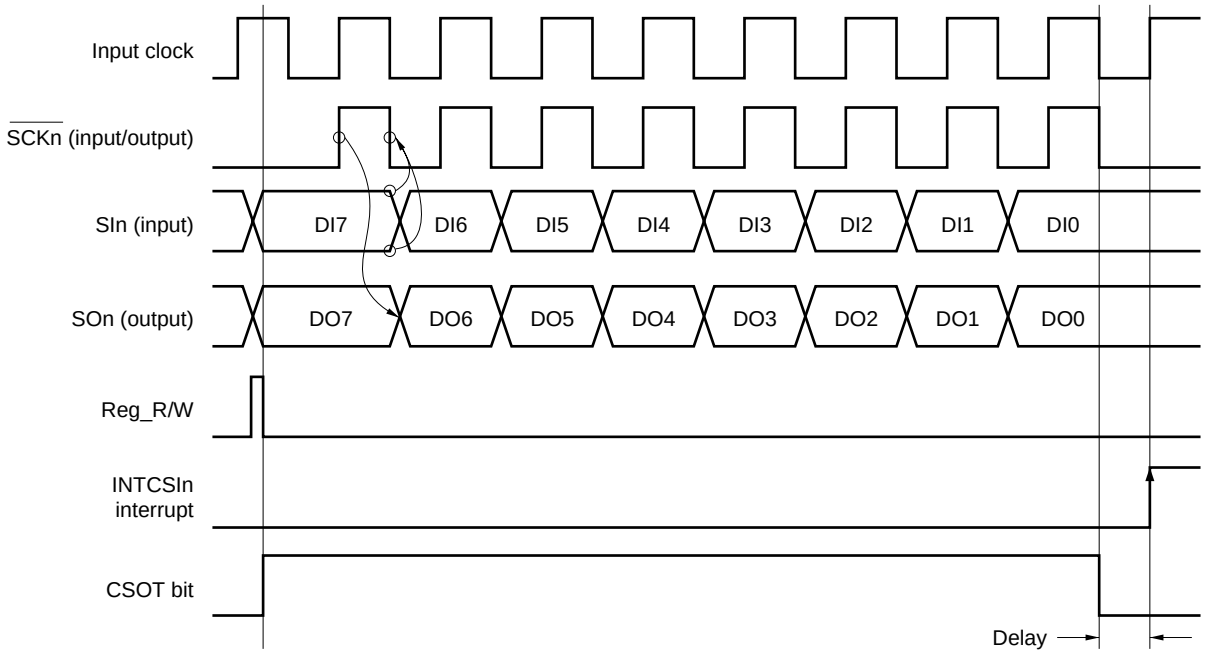


Remarks 1. n = 0, 1

2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed**.**

Figure 10-51. Timing Chart of Interrupt Request Signal Output in Delay Mode (2/2)

(b) When CKP bit = 1, DAP bit = 1



Remarks 1. n = 0, 1

2. Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

(2) Repeat transfer mode

(a) Usage (receive-only)

<1> Set the repeat transfer mode (AUTO bit of CSIMn register = 1) and the receive-only mode (TRMD bit of CSIMn register = 0).

<2> Read SIRBn register (start transfer with dummy read).

<3> Wait for transmission/reception completion interrupt request (INTCSIn).

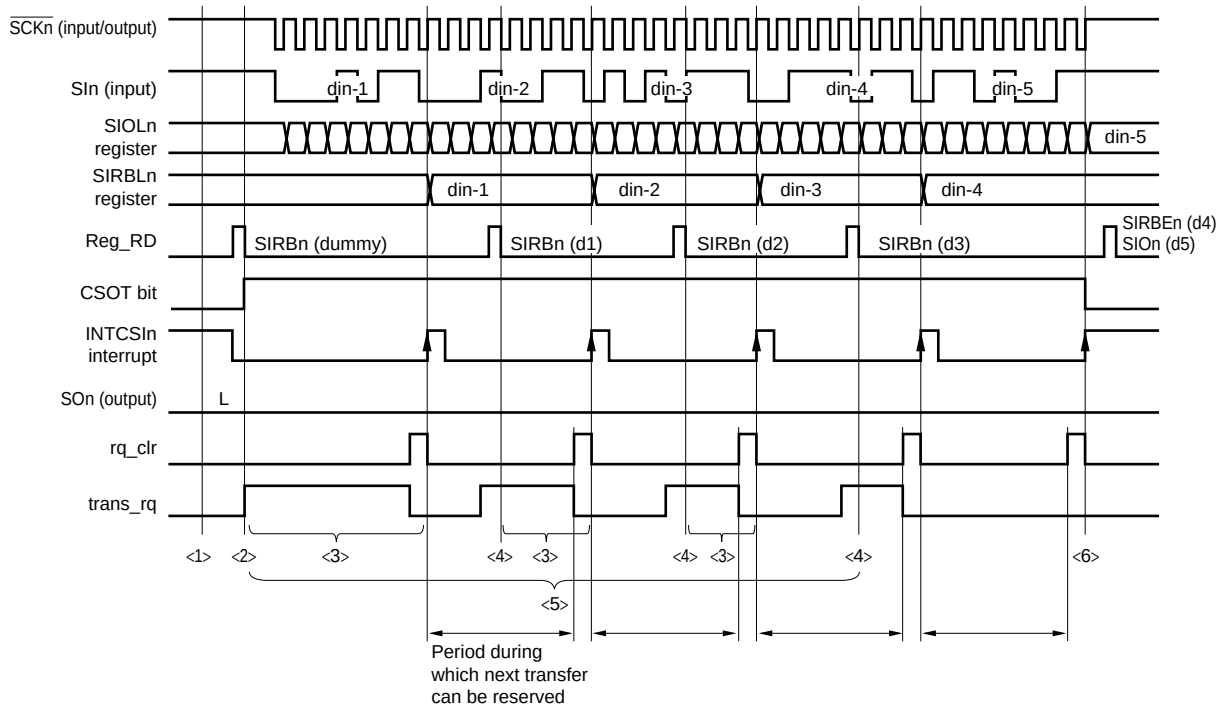
<4> When the transmission/reception completion interrupt request (INTCSIn) has been set (1), read the SIRBn register[Note] (reserve next transfer).

<5> Repeat steps <3> and <4> (n – 2) times. (n: Number of transfer data)

<6> Following output of the last transmission/reception completion interrupt request (INTCSIn), read the SIRBEn register and the SIOn register[Note].

Note When transferring n number of data, receive data is loaded by reading the SIRBn register from the first data to the (n – 2)th data. The (n – 1)th data is loaded by reading the SIRBEn register, and the nth (last) data is loaded by reading the SIOn register.

Figure 10-52. Repeat Transfer (Receive-Only) Timing Chart



Remarks 1. n = 0, 1

2. Reg_RD: Internal signal. This signal indicates that the receive data buffer register (SIRBn/SIRBLn) has been read.

rq_clr: Internal signal. Transfer request clear signal.

trans_rq: Internal signal. Transfer request signal.

In the case of the repeat transfer mode, two transfer requests are set at the start of the first transfer. Following the transmission/reception completion interrupt request (INTCSIn), transfer is continued if the SIRBn register can be read within the next transfer reservation period. If the SIRBn register cannot be read, transfer ends and the SIRBn register does not receive the new value of the SIOn register.

The last data can be obtained by reading the SIOn register following completion of the transfer.

(b) Usage (transmission/reception)

<1> Set the repeat transfer mode (AUTO bit of CSIMn register = 1) and the transmission/reception mode (TRMD bit of CSIMn register = 1)

<2> Write the first data to the SOTBFn register.

<3> Write the 2nd data to the SOTBn register (start transfer).

<4> Wait for a transmission/reception completion interrupt request (INTCSIn).

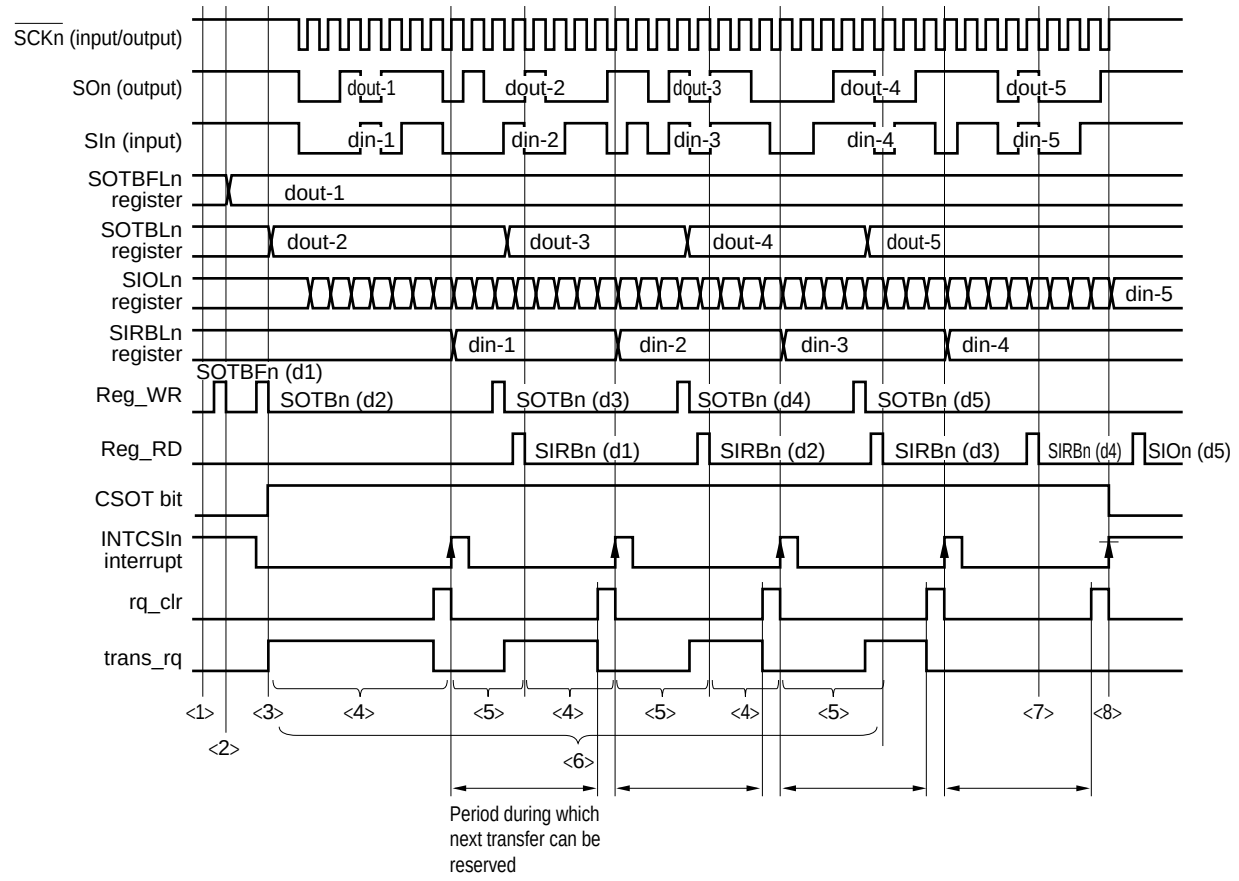
<5> When the transmission/reception completion interrupt request (INTCSIn) has been set (1), write the next data to the SOTBn register (reserve next transfer), and read the SIRBn register to load the receive data.

<6> Repeat steps <4> and <5> as long as data to be sent remains.

<7> Wait for the INTCSIn interrupt. When the interrupt request signal is set (1), read the SIRBn register to load the (n – 1)th receive data.

<8> Following the last transmission/reception completion interrupt request (INTCSIn), read the SIOn register to load the nth (last) receive data.

Figure 10-53. Repeat Transfer (Transmission/Reception) Timing Chart



Remarks 1. n = 0, 1

2. Reg_WR: Internal signal. This signal indicates that the transmit data buffer register (SOTBn/SOTBLn) has been written.

Reg_RD: Internal signal. This signal indicates that the receive data buffer register (SIRBn/SIRBLn) has been read.

rq_clr: Internal signal. Transfer request clear signal.

trans_rq: Internal signal. Transfer request signal.

In the case of the repeat transfer mode, two transfer requests are set at the start of the first transfer. Following the transmission/reception completion interrupt request (INTCSIn), transfer is continued if the SOTBn register can be written within the next transfer reservation period. If the SOTBn register cannot be written, transfer ends and the SIRBn register does not receive the new value of the SIOn register.

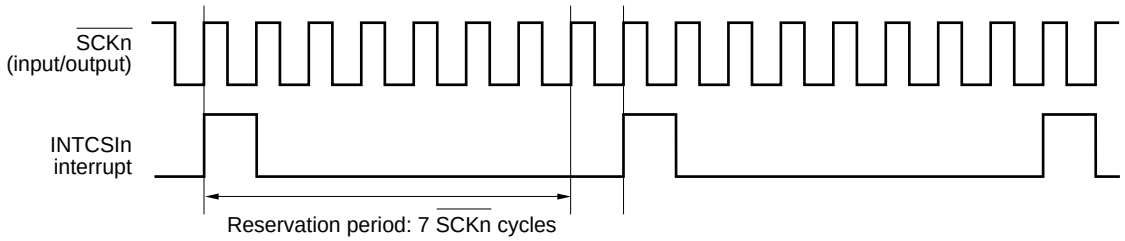
The last receive data can be obtained by reading the SIOn register following completion of the transfer.

(c) Next transfer reservation period

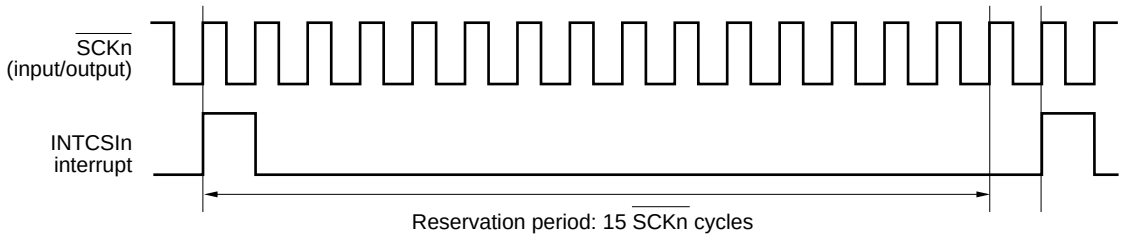
In the repeat transfer mode, the next transfer must be prepared with the period shown in Figure 10-54.

Figure 10-54. Timing Chart of Next Transfer Reservation Period (1/2)

(a) When data length: 8 bits, operation mode: CKP bit = 0, DAP bit = 0



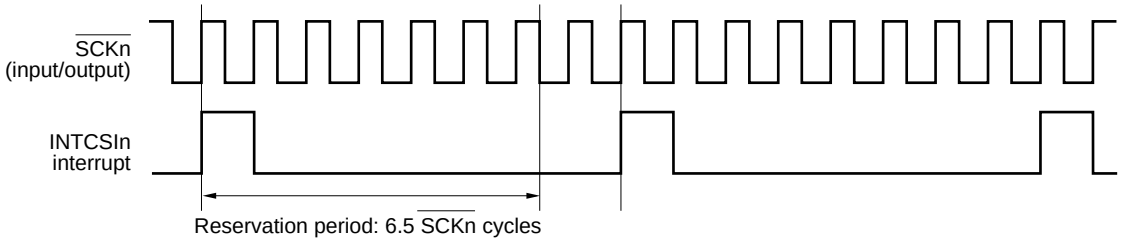
(b) When data length: 16 bits, operation mode: CKP bit = 0, DAP bit = 0



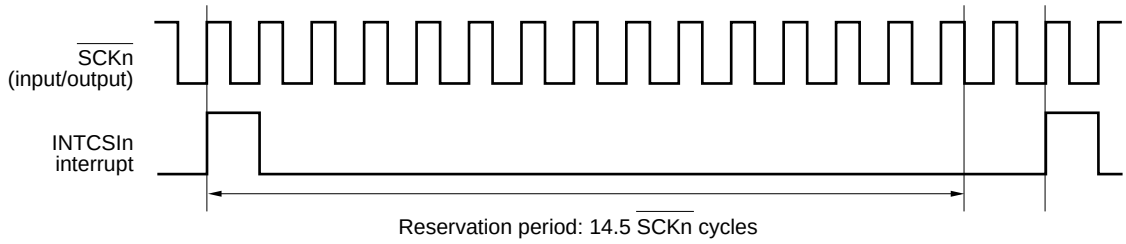
Remark n = 0, 1

Figure 10-54. Timing Chart of Next Transfer Reservation Period (2/2)

(c) When data length: 8 bits, operation mode: CKP bit = 0, DAP bit = 1



(d) When data length: 16 bits, operation mode: CKP bit = 0, DAP bit = 1



Remark n = 0, 1

(d) Cautions

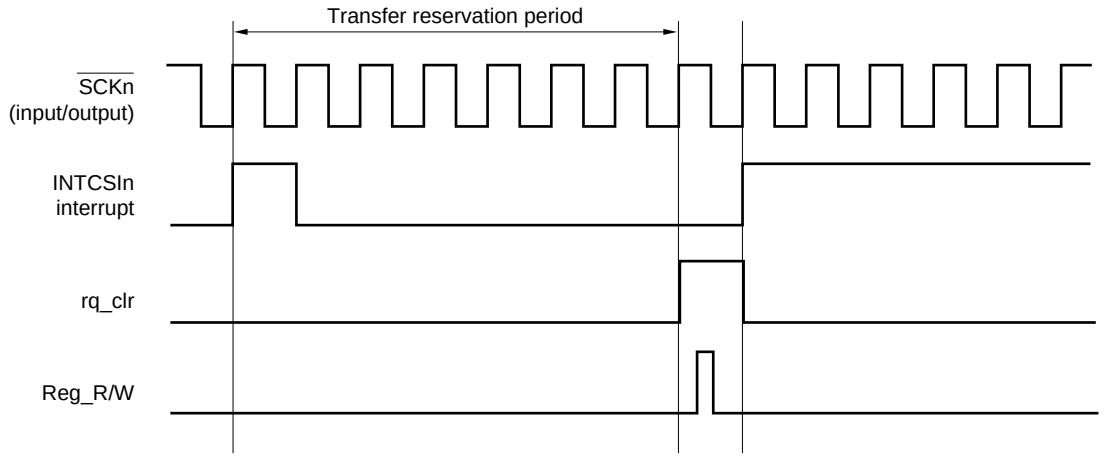
To continue repeat transfers, it is necessary to either read the SIRBn register or write to the SOTBn register during the transfer reservation period.

If access is performed to the SIRBn register or the SOTBn register when the transfer reservation period is over, the following occurs.

(i) In case of contention between transfer request clear and register access

Since request cancellation has higher priority, the next transfer request is ignored. Therefore, transfer is interrupted, and normal data transfer cannot be performed.

Figure 10-55. Transfer Request Clear and Register Access Contention



Remarks 1. n = 0, 1

2. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that the receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

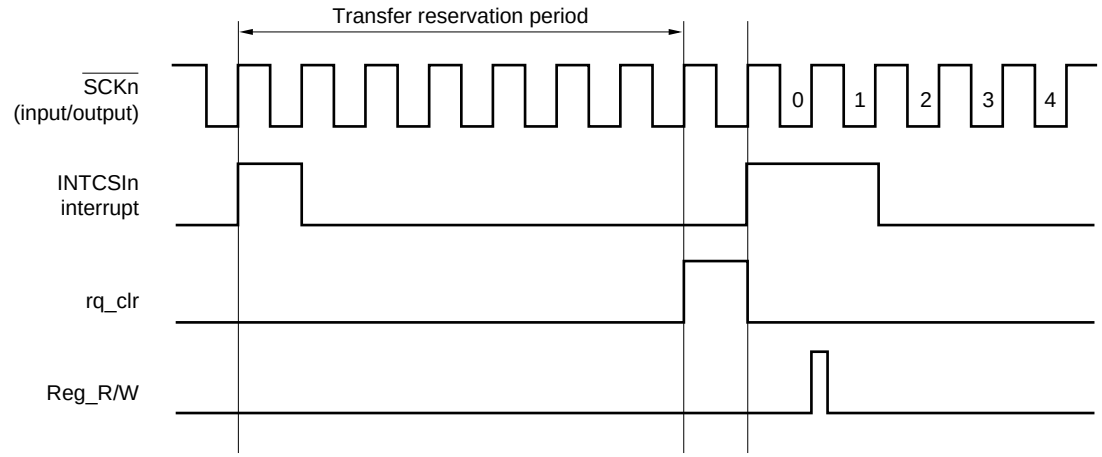
(ii) In case of contention between interrupt request and register access

Since continuous transfer has stopped once, executed as a new repeat transfer.

In the slave mode, a bit phase error transfer error results (refer to Figure 10-56).

In the transmission/reception mode, the value of the SOTBFn register is retransmitted, and illegal data is sent.

Figure 10-56. Interrupt Request and Register Access Contention



Remarks 1. n = 0, 1

2. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that receive data buffer register (SIRBn/SIRBLn) read or transmit data buffer register (SOTBn/SOTBLn) write was performed.

10.4.5 Output pins

(1) $\overline{\text{SCKn}}$ pin

When the CSIn operation is disabled (CSIE bit of CSIMn register = 0), the $\overline{\text{SCKn}}$ pin output status is as follows (n = 0, 1).

Table 10-10. $\overline{\text{SCKn}}$ Pin Output Status

CKP	CKS2	CKS1	CKS0	$\overline{\text{SCKn}}$ Pin Output
0	Don't care	Don't care	Don't care	Fixed to high level
1	1	1	1	Fixed to high level
	Other than above			Fixed to low level

Remarks 1. n = 0, 1

2. When any of bits CKP and CKS2 to CKS0 of the CSICn register is overwritten, the $\overline{\text{SCKn}}$ pin output changes.

(2) SOn pin

When the CSIn operation is disabled (CSIE bit of CSIMn register = 0), the SOn pin output status is as follows (n = 0, 1).

Table 10-11. SOn Pin Output Status

TRMD	DAP	AUTO	CCL	DIR	SOn Pin Output
0	Don't care	Don't care	Don't care	Don't care	Fixed at low level
1	0	Don't care	Don't care	Don't care	SO latch value (low level)
	1	0	0	0	SOTB7 value
				1	SOTB0 value
			1	0	SOTB15 value
				1	SOTB0 value
		1	0	0	SOTBF7 value
				1	SOTBF0 value
			1	0	SOTBF15 value
				1	SOTBF0 value

Remarks 1. n = 0, 1

2. When any of bits TRMD, CCL, DIR, AUTO, and CSICn of the CSIMn register or DAP bit of the CSICn register is overwritten, the SOn pin output changes.

3. SOTBm: Bit m of SOTBn register (m = 0, 7, 15)

4. SOTBFm: Bit m of SOTBFn register (m = 0, 7, 15)

10.4.6 Dedicated baud rate generator 3 (BRG3)

(1) Configuration of baud rate generator 3 (BRG3)

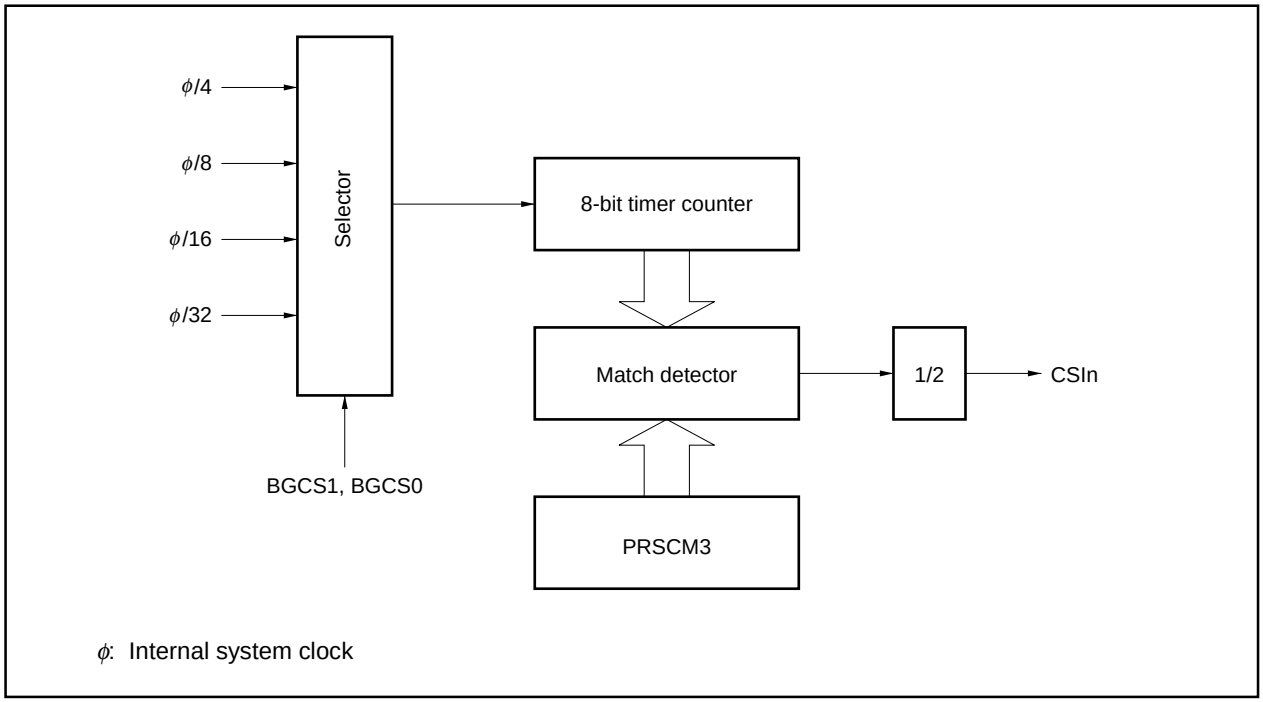
The CSI0 and CSI1 serial clocks can be selected between dedicated baud rate generator output or internal system clock (ϕ).

The serial clock source is specified with registers CSIC0 and CSIC1.

If dedicated baud rate generator output is specified, BRG3 is selected as the clock source.

Since the same serial clock can be shared for transmission and reception, baud rate is the same for the transmission/reception.

Figure 10-57. Baud Rate Generator 3 (BRG3) Block Diagram



ϕ: Internal system clock

(2) Dedicated baud rate generator 3 (BRG3)

BRG3 is configured of an 8-bit timer counter that generates the baud rate signal, a prescaler mode register 3 (PRSM3) that controls baud rate signal generation, a prescaler compare register 3 (PRSCM3) that sets the value of the 8-bit timer counter, and a prescaler.

(a) Input clock

The internal system clock (ϕ) is input to BRG3.

(b) Prescaler mode register 3 (PRSM3)

The PRSM3 register controls generation of the CSI0 and CSI1 baud rate signals.

This register can be read/written in 8-bit or 1-bit units.

Figure 10-58. Prescaler Mode Register 3 (PRSM3)

	7	6	5	4	3	2	1	0	Address	Initial value
PRSM3	0	0	0	CE	0	0	BGCS1	BGCS0	FFFFF920H	00H

Bit Position	Bit Name	Function
4	CE	Enables baud rate counter operation. 0: Stop baud rate counter operation and fix baud rate output signal to 0. 1: Enable baud rate counter operation and start baud rate output operation.
1, 0	BGCS1, BGCS0	Selects count clock for baud rate counter.

BGCS1	BGCS0	Count Clock Selection
0	0	ϕ/4
0	1	ϕ/8
1	0	ϕ/16
1	1	ϕ/32

Remark ϕ: Internal system clock

Cautions 1. Do not change the value of the BGCS1, BGCS0 bits during transmission/reception operation.

2. Set the PRSM3 register prior to setting the CE bit to 1.

(c) Prescaler compare register 3 (PRSCM3)

PRSCM3 is an 8-bit compare register that sets the value of the 8-bit timer counter.

This register can be read/written in 8-bit or 1-bit units.

Figure 10-59. Prescaler Compare Register 3 (PRSCM3)

	7	6	5	4	3	2	1	0	Address	Initial value
PRSCM3	PRSCM7	PRSCM6	PRSCM5	PRSCM4	PRSCM3	PRSCM2	PRSCM1	PRSCM0	FFFFF922H	00H

Cautions 1. The internal timer counter is cleared by writing to the PRSM3 register. Therefore, do not write to the PRSCM3 register during transmission.

2. Set the PRSCM3 register prior to setting the CE bit of the PRSM3 register to 1. If the contents of the PRSCM3 register are overwritten when the value of the CE bit is 1, the cycle of the baud rate signal is not guaranteed.

(d) Baud rate signal cycle

The baud rate signal cycle is calculated as follows.

- **When setting value of PRSCM3 register is 00H**
  (Cycle of signal selected with bits BGCS1, BGCS0 of PRSM3 register) × 256 × 2
- **In cases other than above**
  (Cycle of signal selected with bits BGCS1, BGCS2 of PRSM3 register) × (setting value of PRSCM3 register) × 2

(e) Baud rate setting value

Table 10-12. Baud Rate Generator Setting Data

<1> When ϕ = 32 MHz

BGCS1	BGCS0	PRSCM Register Value	Clock (Hz)
0	0	1	4000000
0	0	2	2000000
0	0	4	1000000
0	0	8	500000
0	0	16	250000
0	0	40	100000
0	0	80	50000
0	0	160	25000
0	1	200	10000
1	0	200	5000

<2> When ϕ = 40 MHz

BGCS1	BGCS0	PRSCM Register Value	Clock (Hz)
0	0	2	2500000
0	0	5	1000000
0	0	10	500000
0	0	20	250000
0	0	50	100000
0	0	100	50000
0	0	200	25000
0	1	250	10000
1	0	250	5000

<3> When ϕ = 50 MHz

BGCS1	BGCS0	PRSCM Register Value	Clock (Hz)
0	0	2	3125000
0	0	4	1562500
0	0	5	1250000
0	0	10	625000
0	0	25	250000
0	0	50	125000
0	0	125	50000
0	0	250	25000
0	1	250	12500
1	0	250	6250

Caution Set the transfer clock so that it does not fall below the minimum value of 250 ns of the $\overline{\text{SCKn}}$ cycle (t_{CYSK1}) prescribed in the electrical specifications.

CHAPTER 11 FCAN CONTROLLER

The V850E/IA1 features a 1channel on-chip FCAN (Full Controller Area Network) controller that complies with the CAN specification Ver. 2.0, Part B.

11.1 Function Overview

Table 11-1 presents an overview of V850E/IA1 functions.

Table 11-1. Overview of Functions

Function	Description
Protocol	CAN Protocol Ver. 2.0, Part B (standard and extended frame transmission/reception)
Baud rate	Maximum 1 Mbps (during 16 MHz clock input)
Data storage	• Allocated to common access-enabled RAM area • RAM that is mapped to an unused message byte can be used for CPU processing or other processing
Mask functions	• Four • Both global masks and local masks can be used
Message configuration	Can be declared as transmit or receive messages
No. of messages	32
Message storage method	• Storage to reception buffer corresponding to ID • Storage to buffer specified by receive mask function
Remote reception	• Remote frames can be received in either the receive message buffer or the transmit message buffer • If a remote frame arrives during a transmit message, there is a choice between having the remote request processed by the CPU or starting the auto transmit function.
Remote transmission	The remote frame can be sent either by setting the transmit message's RTR bit (M_CTRLn register) or by setting the receive message's send request.
Time stamp function	A time stamp function can be set for receive messages and transmit messages.
Diagnostic functions	• Read-enabled error counter is provided. • "Valid protocol operation flag" is provided for verification of bus connections. • Receive-only mode (with auto baud rate detection) is provided. • Diagnostic processing mode is provided.
Low-power mode	• CAN sleep mode (wake up function using CAN bus is enabled) • CAN stop mode (wake up function using CAN bus is disabled)

Remark n = 00 to 31

11.2 Configuration

FCAN is composed of the following four blocks.

(1) NPB interface

This functional block provides an NPB (NEC peripheral I/O bus) interface and a means of transmitting and receiving signals.

(2) MAC (Memory Access Controller)

This functional block controls access to the CAN module within the FCAN and to the CAN RAM.

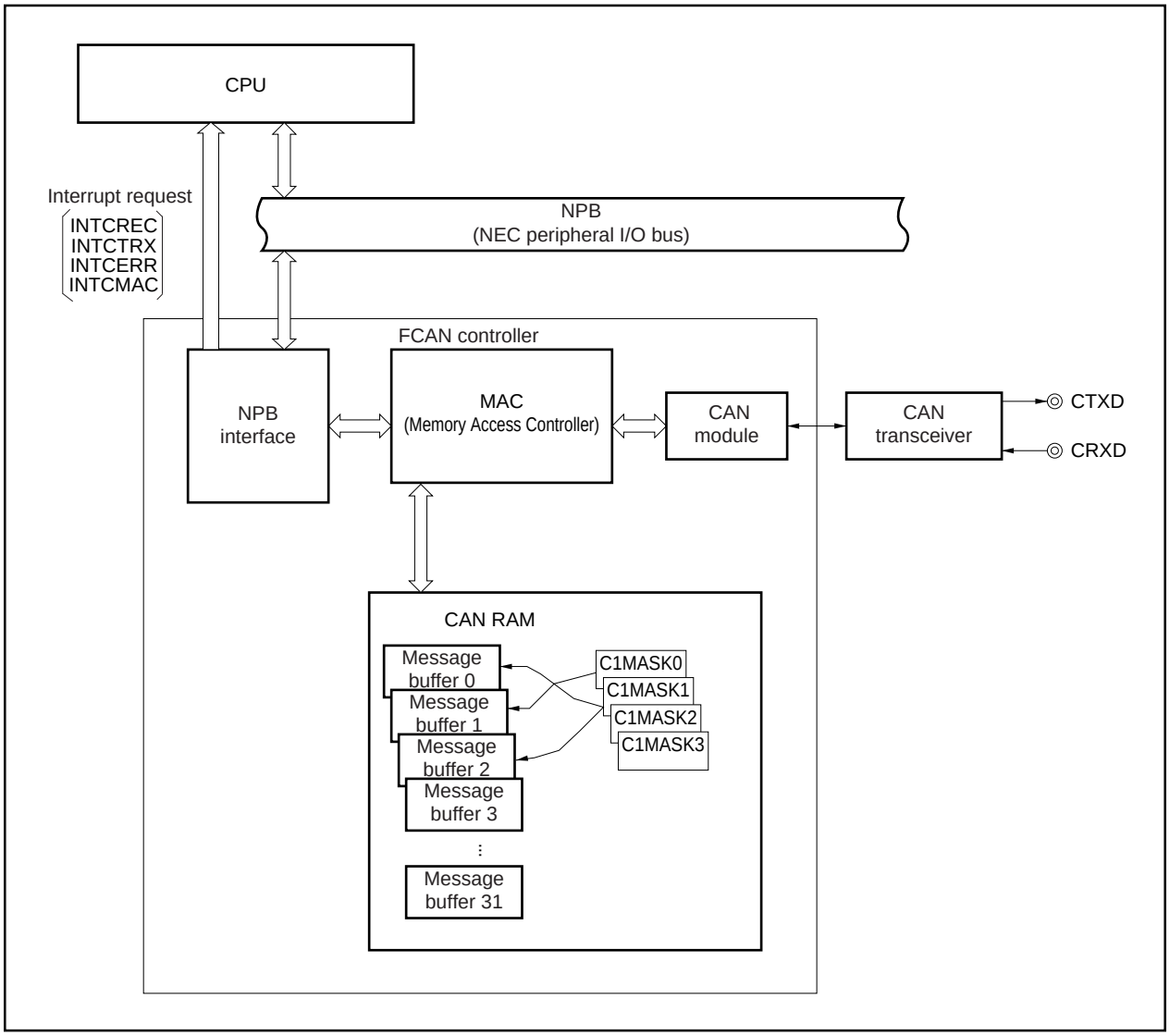
(3) CAN module

This functional block is involved in the operation of the CAN protocol layer and its related settings.

(4) CAN RAM

This is the CAN memory functional block, which is used to store message IDs, message data, etc.

Figure 11-1. Block Diagram of FCAN



11.3 Configuration of Messages and Buffers

Table 11-2. Configuration of Messages and Buffers

Address[Note] (m = 2, 6, A, E)	Register Name
xxxxm800H to xxxxm81FH	Message buffer 0 field
xxxxm820H to xxxxm83FH	Message buffer 1 field
xxxxm840H to xxxxm85FH	Message buffer 2 field
xxxxm860H to xxxxm87FH	Message buffer 3 field
xxxxm880H to xxxxm89FH	Message buffer 4 field
xxxxm8A0H to xxxxm8BFH	Message buffer 5 field
xxxxm8C0H to xxxxm8DFH	Message buffer 6 field
xxxxm8E0H to xxxxm8FFH	Message buffer 7 field
xxxxm900H to xxxxm91FH	Message buffer 8 field
xxxxm920H to xxxxm93FH	Message buffer 9 field
xxxxm940H to xxxxm95FH	Message buffer 10 field
xxxxm960H to xxxxm97FH	Message buffer 11 field
xxxxm980H to xxxxm99FH	Message buffer 12 field
xxxxm9A0H to xxxxm9BFH	Message buffer 13 field
xxxxm9C0H to xxxxm9DFH	Message buffer 14 field
xxxxm9E0H to xxxxm9FFH	Message buffer 15 field
xxxxmA00H to xxxxmA1FH	Message buffer 16 field
xxxxmA20H to xxxxmA3FH	Message buffer 17 field
xxxxmA40H to xxxxmA5FH	Message buffer 18 field
xxxxmA60H to xxxxmA7FH	Message buffer 19 field
xxxxmA80H to xxxxmA9FH	Message buffer 20 field
xxxxmAA0H to xxxxmABFH	Message buffer 21 field
xxxxmAC0H to xxxxmADFH	Message buffer 22 field
xxxxmAE0H to xxxxmAFFH	Message buffer 23 field
xxxxmB00H to xxxxmB1FH	Message buffer 24 field
xxxxmB20H to xxxxmB3FH	Message buffer 25 field
xxxxmB40H to xxxxmB5FH	Message buffer 26 field
xxxxmB60H to xxxxmB7FH	Message buffer 27 field
xxxxmB80H to xxxxmB9FH	Message buffer 28 field
xxxxmBA0H to xxxxmBBFH	Message buffer 29 field
xxxxmBC0H to xxxxmBDFH	Message buffer 30 field
xxxxmBE0H to xxxxmBFFH	Message buffer 31 field

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

Remark For details of message buffers, see **3.4.9 List of programmable peripheral I/O registers**.

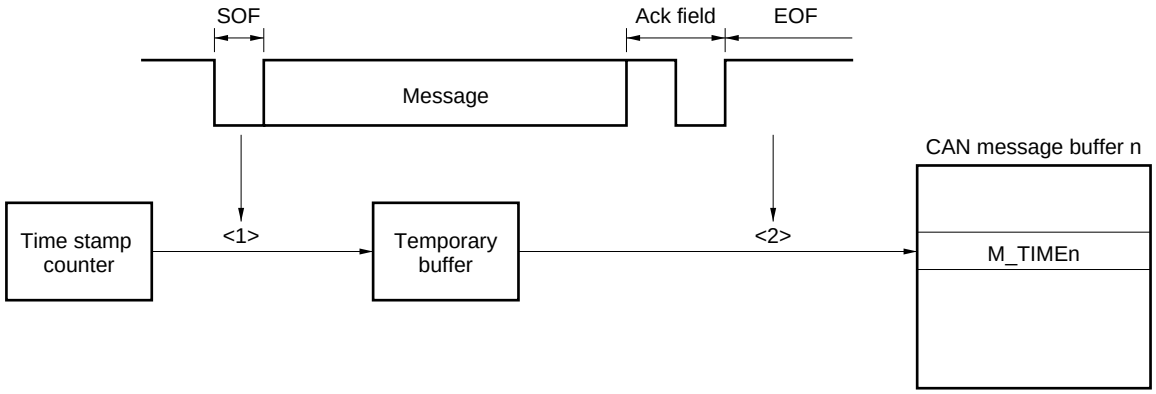
11.4 Time Stamp Function

The FCAN controller supports a time stamp function. This function is needed to build a global time system.

The time stamp function is implemented using a 16-bit free-running time stamp counter.

Two types of time stamp function can be selected for message reception in the FCAN controller. Use bit 3 (TMR) of the CAN1 control register (C1CTRL) to set the desired time stamp function. When the TMRT bit is 0, the time stamp counter value is captured after the SOF is sent via the CAN bus (see **Figure 11-2**) and when the TMR bit is 1, the time stamp counter value is captured after the EOF is sent via the CAN bus (a valid message is confirmed) (see **Figure 11-3**).

Figure 11-2. Time Stamp Function Setting for Message Reception (When C1CTRL Register's TMR Bit = 0)



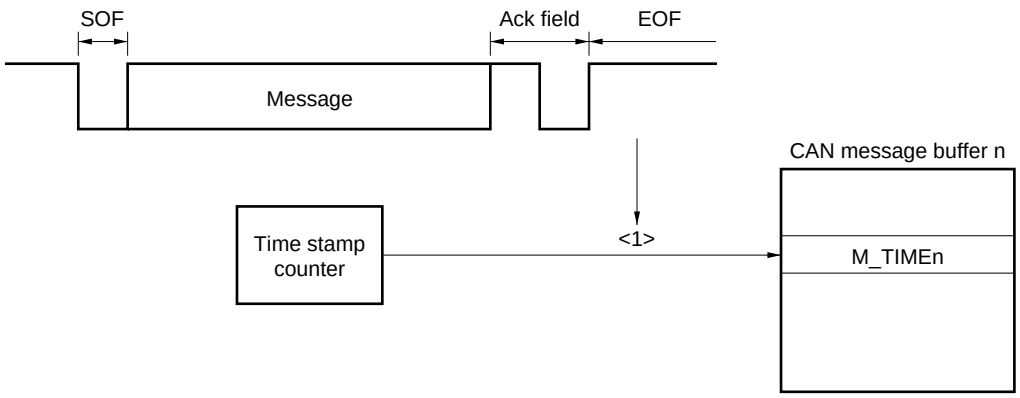
<Explanation>

<1> The time stamp counter value is captured when the SOF is sent via the CAN bus.

<2> A message is stored in CAN message buffer n and the value in the temporary buffer is copied to the M_TIMEn register in CAN message buffer n when the EOF is sent via the CAN bus.

Remark n = 00 to 31

Figure 11-3. Time Stamp Function Setting for Message Reception (When C1CTRL Register's TMR Bit = 1)



<Explanation>

<1> When the EOF is sent via the CAN bus (a valid message is acknowledged), the captured time stamp counter value is copied to the M_TIMEn register in CAN message buffer n when a message is stored in CAN message buffer n.

Remark n = 00 to 31

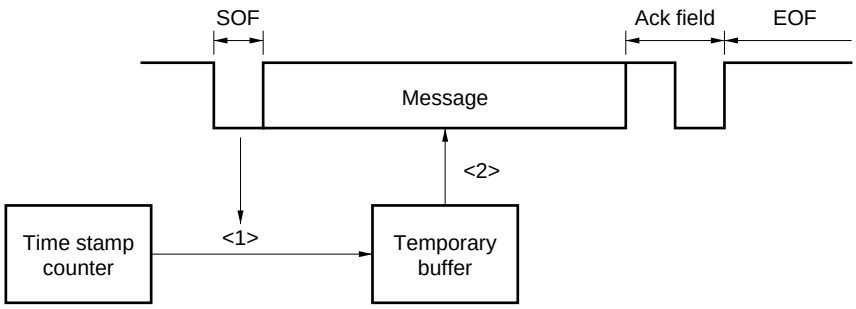
In a global time system, the time value must be captured using the SOF.

In addition, the ability to capture the counter value when data is stored in a message buffer is useful for evaluating the FCAN controller's performance.

The captured time stamp counter value is stored in CAN message buffer n, so CAN message buffer n has its own time stamp function.

When the SOF is sent via the CAN bus while transmitting a message, there is an option to replace the last two bytes of the message with the time stamp counter value by setting bit 5 (ATS) of CAN message control register n (M_CTRLn). This function can be selected for CAN message buffer n on a buffer by buffer basis. Figure 11-4 shows the time stamp setting when the ATS bit = 1.

Figure 11-4. Time Stamp Function Setting for Message Transmission (When M_CTRL Register's ATS Bit = 1)



<Explanation>

<1> The time stamp counter value is captured to the temporary buffer when the SOF is detected on the CAN bus.

<2> The value of the temporary buffer is added to the last 2 bytes of the data length code[Note] specified by bits DLC3 to DLC0 of the M_DLCn register.

Note The ATS bit of the M_CTRLn register must be 1 and the data length must be more than 2 bytes to add the time stamp counter value to the transmit message.

Remark n = 00 to 31

Table 11-3. Example When Adding Captured Time Stamp Counter Value to Last 2 Bytes of Transmit Message

Data Field / DLC Bit Value[Note 1]	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 8
1	M_DATAn0 register value	–	–	–	–	–	–	–
2	**Note 2**	**Note 3**	–	–	–	–	–	–
3	M_DATAn0 register value	**Note 2**	**Note 3**	–	–	–	–	–
4	M_DATAn0 register value	M_DATAn1 register value	**Note 2**	**Note 3**	–	–	–	–
5	M_DATAn0 register value	M_DATAn1 register value	M_DATAn2 register value	**Note 2**	**Note 3**	–	–	–
6	M_DATAn0 register value	M_DATAn1 register value	M_DATAn2 register value	M_DATAn3 register value	**Note 2**	**Note 3**	–	–
7	M_DATAn0 register value	M_DATAn1 register value	M_DATAn2 register value	M_DATAn3 register value	M_DATAn4 register value	**Note 2**	**Note 3**	–
8	M_DATAn0 register value	M_DATAn1 register value	M_DATAn2 register value	M_DATAn3 register value	M_DATAn4 register value	M_DATAn5 register value	**Note 2**	**Note 3**
9 to 15	M_DATAn0 register value	M_DATAn1 register value	M_DATAn2 register value	M_DATAn3 register value	M_DATAn4 register value	M_DATAn5 register value	**Note 2**	**Note 3**

Notes 1. See **11.10 (2) CAN message data length registers 00 to 31 (M_DLC00 to M_DLC31)**.

2. The lower 8 bits of the time stamp counter value when the SOF is detected on the CAN bus

3. The higher 8 bits of the time stamp counter value when the SOF is detected on the CAN bus

Remark n = 00 to 31

11.5 Message Processing

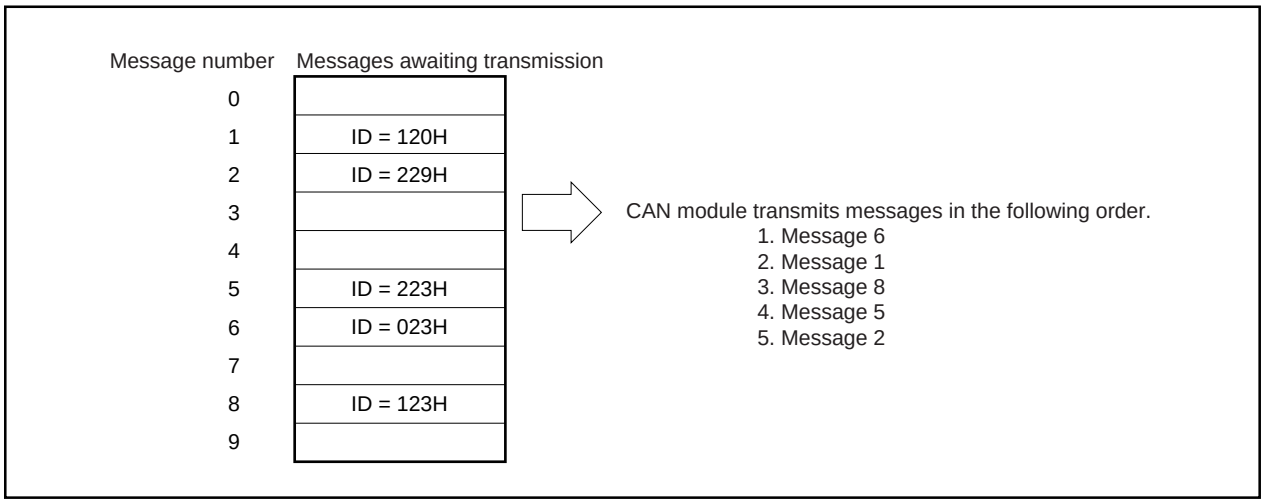
The messages can be linked to mask functions that are in turn linked to CAN modules.

The FCAN system is a multiplexed communication system. The priority of message transmission within this system is determined based on message identifiers (IDs).

To facilitate communication processing by application software when there are several messages awaiting transmission, the CAN module uses hardware to check the message IDs and automatically determine whether or not linked messages are prioritized.

This eliminates the need for software-based priority control.

Figure 11-5. Example of Message Processing



This auto priority control function can be canceled. When it is canceled, the priority among messages is determined based on the locations of the messages in memory (the message that has the lowest message number among the messages in the message buffer has the highest priority).

When several messages have been received in the CAN module's message buffers, priority control for storing received messages is as follows.

Priority rank 1: Remote frame reception in the transmit message buffer.
Priority rank 2: Non-masked message, for which M_STATn register's DN bit has not been set (to 1)
Priority rank 3: Non-masked message, for which M_STATn register's DN bit has been set (to 1)
Priority rank 4: Masked 0 message, for which M_STATn register's DN bit has not been set (to 1)
Priority rank 5: Mask 0 message, for which M_STATn register's DN bit has been set (to 1)
Priority rank 6: Mask 1 message, for which M_STATn register's DN bit has not been set (to 1)
Priority rank 7: Mask 1 message, for which M_STATn register's DN bit has been set (to 1)
Priority rank 8: Mask 2 message, for which M_STATn register's DN bit has not been set (to 1)
Priority rank 9: Mask 2 message, for which M_STATn register's DN bit has been set (to 1)
Priority rank 10: Mask 3 message, for which M_STATn register's DN bit has not been set (to 1)
Priority rank 11: Mask 3 message, for which M_STATn register's DN bit has been set (to 1)

Remark n = 00 to 31

If priority based on location in memory is the same for multiple messages, the message buffer having the lowest message number is selected.

11.6 Mask Function

A mask linkage function can be defined for each received message.

This means that there is no need to distinguish between local masks and global masks.

When the mask function is used, the received message's identifier is compared with the message buffer's identifier and the desired bits can be defined.

When the mask function is operating, a bit whose value is defined as "1" by masking is not subject to the abovementioned comparison between the received message's identifier and the message buffer's identifier.

However, this comparison is performed for any bit whose value is defined as "0" by masking.

For example, let us assume that all messages that have a standard-format ID in which bits ID27 to ID25 = 0 and bits ID24 and ID22 = 1 are to be stored in message buffer 14 (which is linked by mask 1 as explained in **11.10 (7)**). The procedure for this example is shown below.

<1> Identifier bits to be stored in message buffer

ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18
x	0	0	0	1	x	1	x	x	x	x

Remark x = don't care

Messages with an ID in which bits ID27 to ID25 = 0 and bits ID24 and ID22 = 1 are registered (initialized) in message buffer 14 (see section **11.10 (7)**).

<2> Identifier bits set to message buffer 14 (example)
(Using CAN message ID registers L14 and H14 (M_IDL14 and M_IDH14))

ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18
0	0	0	0	1	0	1	0	0	0	0

ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
0	0	0	0	0	0	0	0	0	0	0

ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0

Message buffer 14 is set as a standard-format identifier linked to mask 1 (see section **11.10 (7)**).

<3> Mask setting for CAN module 1 (mask 1)(example)
(Using CAN1 address mask registers L1 and H1 (C1MASKL1 and C1MASKH1))

CM28	CM27	CM26	CM25	CM24	CM23	CM22	CM21	CM20	CM19	CM18
1	0	0	0	0	1	0	1	1	1	1

CM17	CM16	CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7
1	1	1	1	1	1	1	1	1	1	1

CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	1	1	1	1

Remark 0: Do not compare (mask)
1: Compare

Values are written to mask 1 (see section **11.10 (19)**), bits CMID28 to CMID24 and CMID22 are set to 0 and bits CMID28, CMID23, and CMID21 to CMID0 are set to 1. Be sure to set bits CMID17 to CMID0 to 1 wen receiving a standard-format ID message by mask.

11.7 Protocol

FCAN is a high-speed multiplex communication protocol designed to enable real-time communications in automotive applications. The CAN specification is generally divided into two layers (physical layer and data link layer). The data link layer is further divided into logical link control and medium access control. The composition of these layers is illustrated in Figure 11-6 below.

Figure 11-6. Composition of Layers

Higher	Application layer		Not applicable
↕	Data link layer	▪ Logical link control (LLC)	Message and status handling rules
		▪ Medium access control (MAC)	Protocol rules
Lower	Physical layer		Signal level and bit expression rules

11.7.1 Protocol mode function

(1) Standard format mode

2032 different identifiers can be set in this mode.

The standard format mode uses 11-bit identifiers, which means that it can handle up to 2032 messages.

(2) Extended format mode

This mode is used to extend the number of identifiers that can be set.

- While the standard format mode uses 11-bit identifiers, the extended format mode uses 29-bit (11 bits + 18 bits) identifiers which expands the amount of messages that can be handled to 2032×2^{18} messages.
- Extended format mode is set when "recessive (R): recessive in wired OR" is set for both the SRR and IDE bits in the arbitration field.
- When an extended format mode message and a standard format mode remote frame are transmitted at the same time, the node that transmitted the extended format mode message is set to receive mode.

11.7.2 Message formats

Four types of frames are used in CAN protocol messages. The output conditions for each type of frame are as follows.

- Data frame: Frame used for transmit data
- Remote frame: Frame used for transmit requests from receiving side
- Error frame: Frame that is output when an error has been detected
- Overload frame: Frame that is output when receiving side is not ready

Remark Dominant (D): Dominant in wired OR
Recessive (R): recessive in wired OR
In the figure shown below, (D) = 0 and (R) = 1.

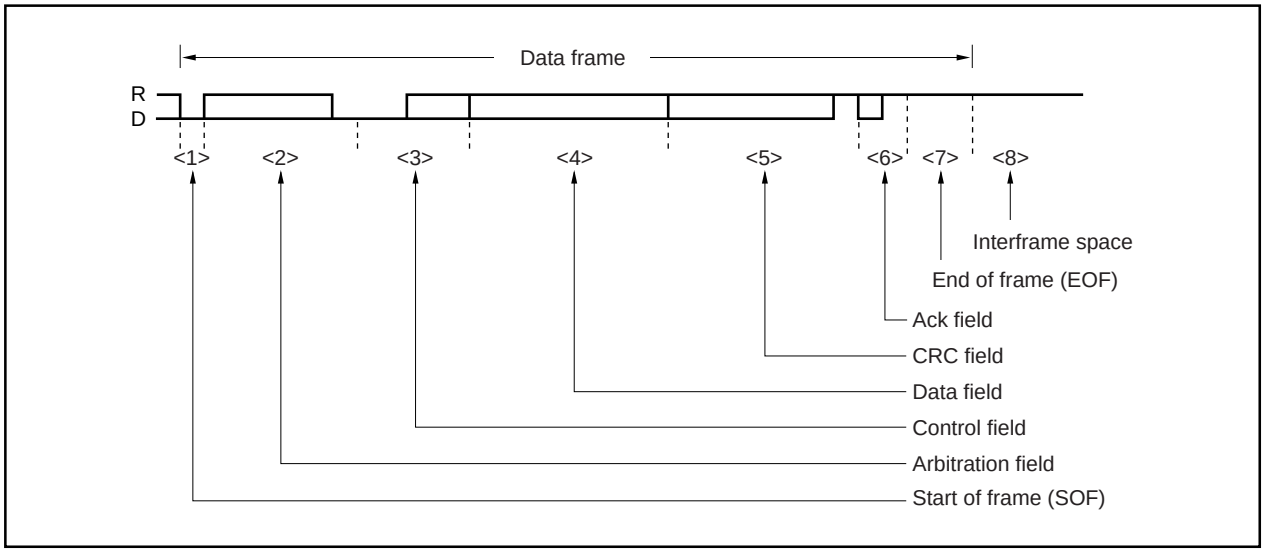
(1) Data frame and remote frame

<1> Data frame

A data frame is the frame used for transmit data.

This frame is composed of seven fields.

Figure 11-7. Data Frame

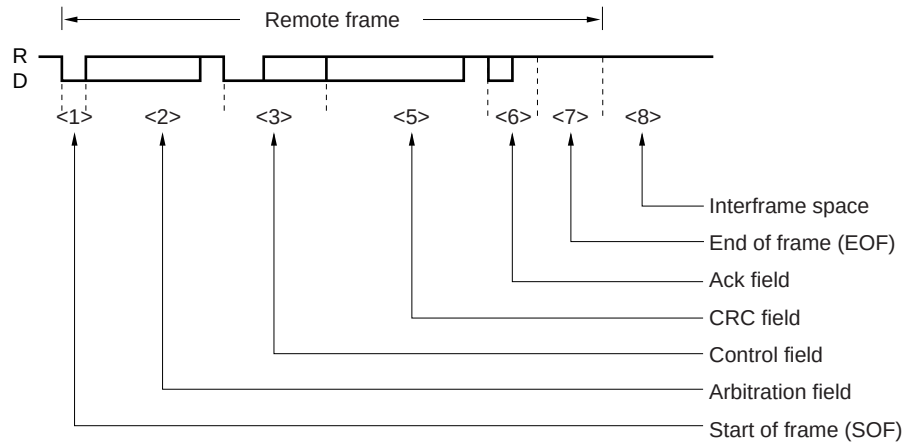


<2> Remote frame

A remote frame is transmitted when the receiving node issues a transmit request.

A remote frame is similar to a data frame, except that the "data field" is deleted and the RTR bit of the "arbitration field" is recessive.

Figure 11-8. Remote Frame



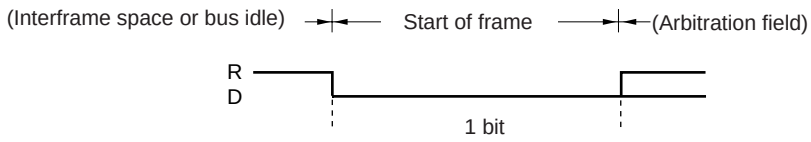
Remark The data field is not transferred even if the control field's data length code is not "0000B".

(2) Description of fields

<1> Start of frame (SOF)

The start of frame field is a 1-bit dominant (D) field that is located at the start of a data frame or remote frame.

Figure 11-9. Start of Frame (SOF)



- The start of frame field starts when the bus line level changes.
- When "dominant (D)" is detected at the sample point, reception continues.
- When "recessive (R)" is detected at the sample point, bus idle mode is set.

<2> Arbitration field

The arbitration field is used to set the priority, data frame or remote frame, and control mode. This field includes an identifier, frame setting (RTR bit), and protocol setting bit.

Figure 11-10. Arbitration Field (In Standard Format Mode)

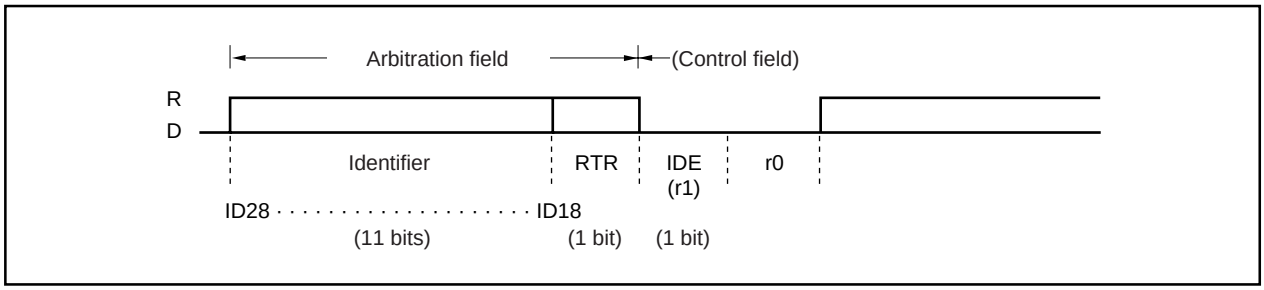
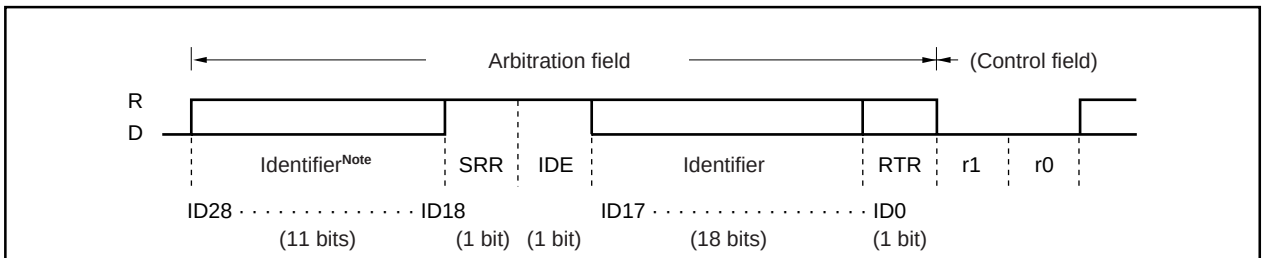


Figure 11-11. Arbitration Field (In Extended Format Mode)



Note Setting the higher 7 bits of the identifier as 1111111B is prohibited.

Cautions 1. ID28 to ID0 are identifier bits.

2. Identifier bits are transferred in MSB-first order.

Table 11-4. RTR Bit Settings

Frame Type	RTR Bit
Data frame	Dominant
Remote frame	Recessive

Table 11-5. Protocol Mode Setting and Number of Identifier (ID) Bits

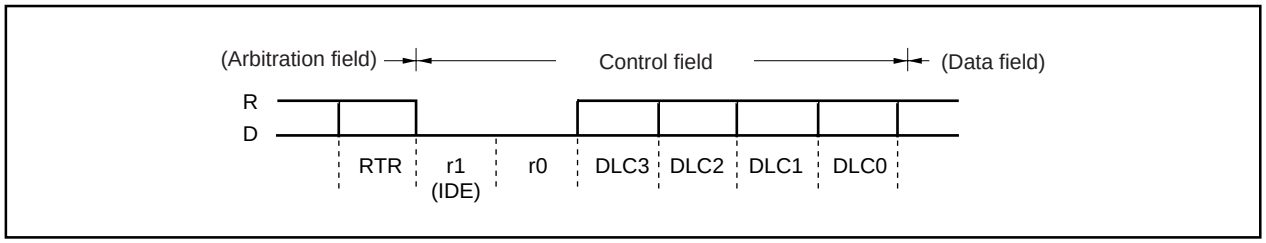
Protocol Mode	SRR Bit	IDE Bit	No. of Bits
Standard format mode	None	Dominant (D)	11 bits
Extended format mode	Recessive (R)	Recessive (R)	29 bits

<3> Control field

The control field sets "N" as the number of data bytes in the data field (N = 0 to 8).

r1 and r0 are fixed as dominant (D). The data length code bits (DLC3 to DLC0) set the byte count.

Figure 11-12. Control Field



In standard format mode, the arbitration field's IDE bit is the same bit as the r1 bit.

Table 11-6. Data Length Code Settings

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0 bytes
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	0	0	0	8 bytes
Other than above				Setting prohibited

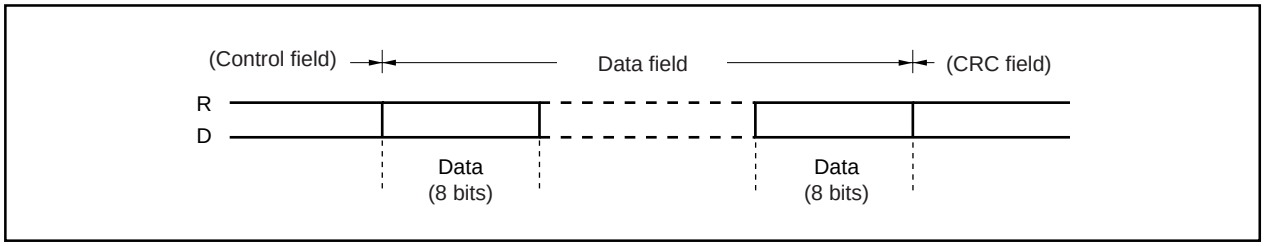
Caution In the remote frame, there is no data field even if the data length code is not 0000B.

<4> Data field

The data field contains the amount of data set by the control field. Up to 8 units of data can be set.

Remark Data units in the data field are each 8 bits long and are ordered MSB first.

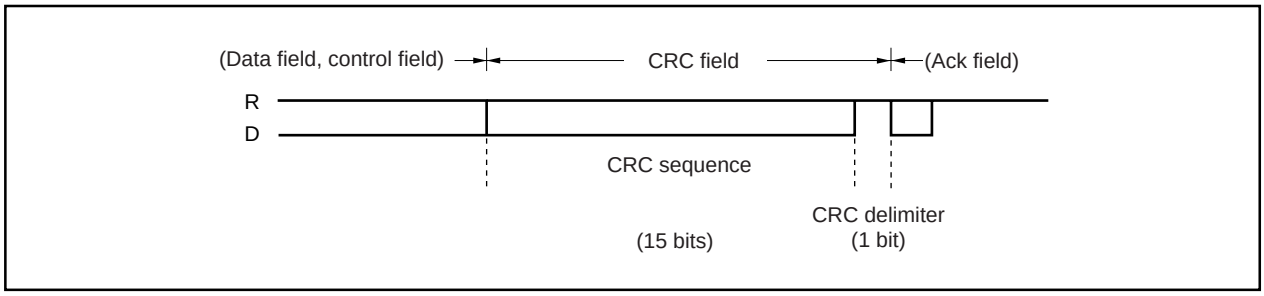
Figure 11-13. Data Field



<5> CRC field

The CRC field is a 16-bit field that is used to check for errors in transmit data. It includes a 15-bit CRC sequence and a 1-bit CRC delimiter.

Figure 11-14. CRC Field



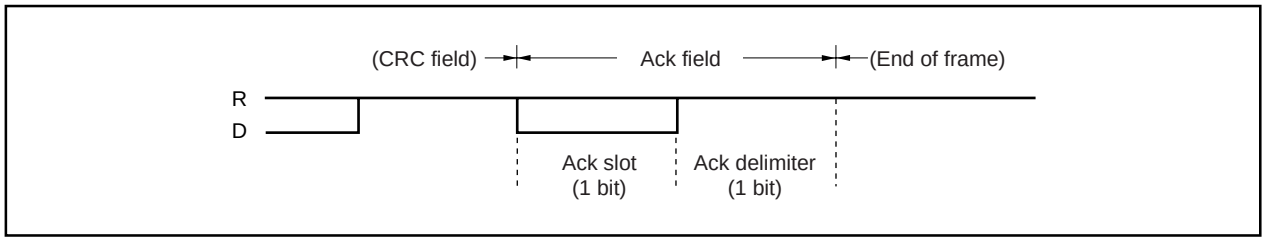
- The polynomial P(X) used to generate the 15-bit CRC sequence is expressed as: $X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + X^3 + 1$
- Transmitting node: No bit stuffing in start of frame, arbitration field, control field, or data field: The transferred CRC sequence is calculated entirely from basic data bits.
- Receiving node: The CRC sequence calculated using data bits that exclude the stuffing bits in the receive data is compared with the CRC sequence in the CRC field. If the two CRC sequences do not match, the node is passed to an error frame.

<6> Ack field

The Ack field is used to confirm normal reception.

It includes a 1-bit Ack slot and a 1-bit Ack delimiter.

Figure 11-15. Ack Field



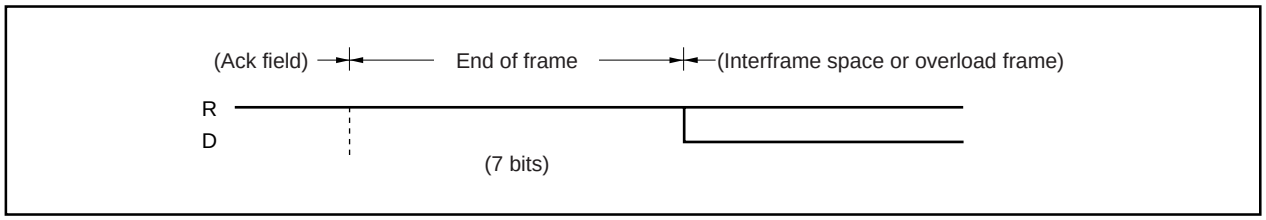
- The receiving node outputs the following depending on whether or not an error is detected between the start of frame field and the CRC field.
  - If an error is detected: Ack slot = Recessive (R)
  - If no error is detected: Ack slot = Dominant (D)
- The transmitting node outputs two "recessive(R)" bits and confirms the receiving node's receive status.

<7> End of frame (EOF)

The end of frame field indicates the end of transmission or reception.

It includes 7 "recessive(R)" bits.

Figure 11-16. End of Frame (EOF)



<8> Interframe space

The interframe space is inserted after the data frame, remote frame, error frame, and overload frame to separate one frame from the next one.

- Error active node

  When the bus is idle, transmit enable mode is set for each node. Transmission then starts from a node that has received a transmit request.

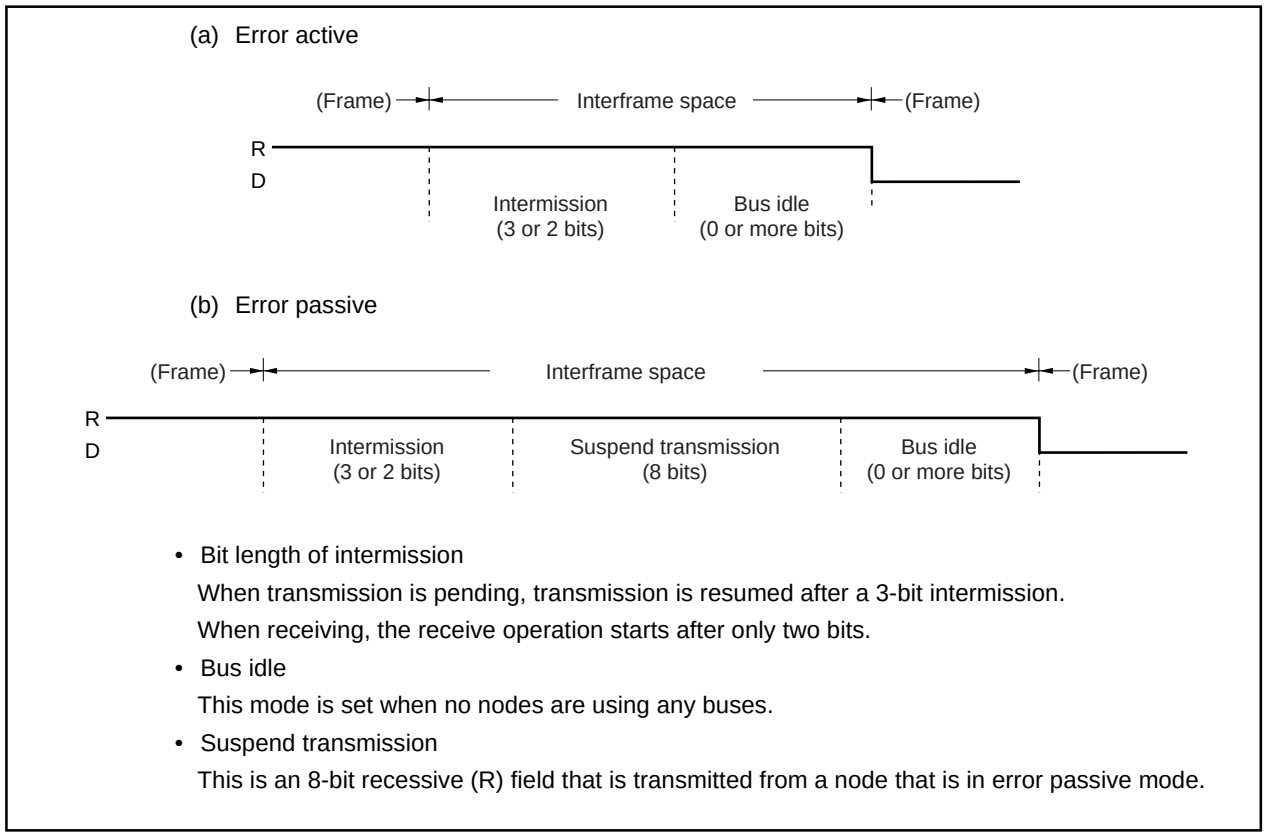
  If the node is an error active node, the interframe space is composed of a 3- or 2-bit intermission field and bus idle field.

- Error passive node

  After an 8-bit bus idle field, transmit enable mode is set. Receive mode is set if a transmission starts from a different node in bus idle mode.

  The error passive node is composed of an intermission field, suspend transmission field, and bus idle field.

Figure 11-17. Interframe Space



- Bit length of intermission

  When transmission is pending, transmission is resumed after a 3-bit intermission.

  When receiving, the receive operation starts after only two bits.

- Bus idle

  This mode is set when no nodes are using any buses.

- Suspend transmission

  This is an 8-bit recessive (R) field that is transmitted from a node that is in error passive mode.

Table 11-7. Operation When Third Bit of Intermission Is “Dominant (D)”

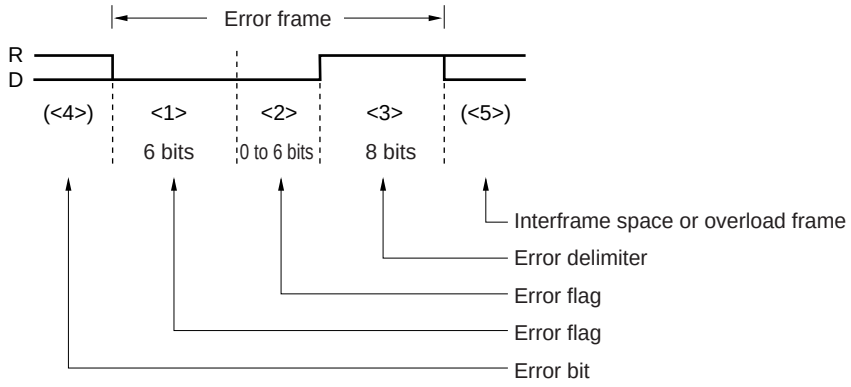
Transmit Status	Operation
No pending transmissions	Receive operation is performed when start of frame output by other node is detected.
Pending transmission exists	Identifier is transmitted when start of frame output by local node is detected.

<9> Error frame

An error frame is used to output from a node in which an error has been detected.

When a passive error flag is being output, if there is “dominant (D)” output from another node, the passive error flag does not end until 6 consecutive bits are detected on the same level. If the bit following the 6 consecutive “recessive (R)” bits is “dominant (D)”, the error frame ends when the next “recessive (R)” bit is detected.

Figure 11-18. Error Frame



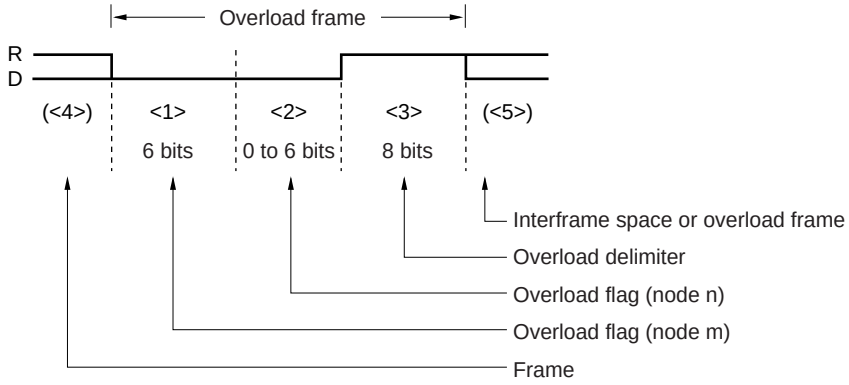
No	Name	Bit Count	Definition	
<1>	Error flag	6	Error active node	Consecutive output of 6 “dominant (D)” bits
			Error passive node	Consecutive output of 6 “recessive (R)” bits
<2>	Error flag	0 to 6	A node that receives an error flag is a node in which bit stuffing errors are detected, after which an error flag is output.	
<3>	Error delimiter	8	8 consecutive “recessive(R)” bits are output. If a “dominant (D)” bit is detected as the eighth bit, an overload frame is sent starting at the next bit.	
<4>	Error bit	–	This bit is output following the bit where an error occurred. If the error is a CRC error, it is output following an Ack delimiter.	
<5>	Interframe space or overload frame	3/10 20 MAX.	An interframe space or overload frame starts from here.	

<10> Overload frame

An overload frame is output starting from the first bit in an intermission in cases where the receiving node is not yet ready to receive.

If a bit error is detected in intermission mode, it is output starting from the bit following the bit where the bit error was detected.

Figure 11-19. Overload Frame



No	Name	Bit count	Definition
<1>	Overload flag starting from node m	6	Consecutive output of 6 “dominant (D)” bits. Output when node m is not ready to receive.
<2>	Overload flag starting from node n	0 to 6	Node n, which has received an overload flag in the interframe space, outputs an overload flag
<3>	Overload delimiter	8	8 consecutive “recessive (R)” bits are output. If a “dominant (D)” bit is detected as the eighth bit, an overload frame is sent starting at the next bit.
<4>	Frame	–	Output following an end of frame, error delimiter, or overload delimiter.
<5>	Interframe space or overload frame	3/10 20 MAX.	An interframe space or overload frame starts from here.

Remark $n \neq m$

11.8 Functions

11.8.1 Determination of bus priority

(1) When one node has started transmitting

- In bus idle mode, the node that outputs data first starts transmission.

(2) When several nodes have started transmitting

- The node that has the longest string of consecutive "dominant (D)" bits starting from the first bit in the arbitration field has top priority for bus access (“dominant (D)” bits take precedence due to wired OR bus arbitration).
- The transmitting node compares the arbitration field which it has output and the bus data level

Table 11-8. Determination of Bus Priority

Matched levels	Transmission continues
Mismatched levels	When a mismatch is detected, data output stops at the next bit, and the operation switches to receiving.

(3) Priority between data frame and remote frame

- If a bus conflict occurs between a data frame and a remote frame, the data frame takes priority because its last bit (RTR) is “dominant (D)”.

11.8.2 Bit stuffing

Bit stuffing is when one bit of inverted data is added for resynchronization to prevent burst errors when the same level is maintained for at least five consecutive bits.

Table 11-9. Bit Stuffing

Transmit	When transmitting data frames and remote frames, if the same level is maintained for at least five bits between the start of frame and CRC fields, one bit of data whose level is inverted from the previous level is inserted before the next bit.
Receive	When receiving data frames and remote frames, if the same level is maintained for at least five bits between the start of frame and CRC fields, the next bit of data is deleted before receiving is resumed.

11.8.3 Multi-master

Since bus priority is determined based on the identifier, any node can be used as the bus master.

11.8.4 Multi-cast

Even when there is only one transmitting node, the same identifier can be set for several nodes, so that the same data can be received by several nodes at the same time (this is called "multi-casting").

11.8.5 CAN sleep mode/CAN stop mode function

The CAN sleep mode/CAN stop mode function is able to set the FCAN controller to sleep (standby) mode to reduce power consumption.

CAN sleep mode is set via the procedure stipulated in the CAN specification. CAN sleep mode can be set to either wake up or not wake up when the bus is operated (this is controlled via CPU access).

11.8.6 Error control function

(1) Types of errors

Table 11-10. Types of Errors

Error Type	Description of Error		Detected Status	
	Detection Method	Detection Condition	Transmit/ Receive	Field/Frame
Bit error	Comparison of output level and bus level (excludes stuff bits)	Mismatch between levels	Transmitting/ receiving nodes	Bus output of data from bits in start of frame to end of frame, error frame, or overload frame
Stuff error	Use stuff bits to check receive data	Six consecutive bits of same-level data	Transmitting/ receiving nodes	Start of frame to CRC sequence
CRC error	Comparison of CRC generated from receive data and received CRC sequence	CRC mismatch	Receiving node	Start of frame to data field
Form error	Check fixed-format field/frame	Detection of inverted fixed format	Receiving node	• CRC delimiter • Ack field • End of frame • Error frame • Overload frame
Ack error	Use transmitting node to check Ack slot	Use Ack slot to detect recessive	Transmitting node	Ack slot

(2) Error frame output timing

Table 11-11. Error Frame Output Timing

Error Type	Output Timing
Bit error, stuff error, form error, Ack error	Error frame is output at the next bit following the bit where error was detected
CRC error	Error frame is output at the next bit following the Ack delimiter

(3) Handling of errors

The transmitting node retransmits the data frame or remote frame after the error frame has been transmitted.

(4) Error statuses

(a) Types of error statuses

The three types of error statuses are listed below.

Error active
Error passive
Bus off

- Error status is controlled by the transmit error counter and receive error counter.
- The various error statuses are categorized according to their error counter values.
- When the error counter value reaches 96 or more, the bus status must be tested since the bus may become seriously damaged.
- During start-up, if only one node is active, the error frame and data are repeatedly resent because no Ack is returned even data has been transmitted.
  In such cases, the error-passive status continues and the bus off mode cannot be set.

Table 11-12. Types of Error Statuses

Error Status Type	Operation	Error Counter Value	Type of Output Error Flag
Error active	Transmit/ receive	0 to 127	Active error flag (6 consecutive “dominant (D)” bits)
Error passive	Transmit	128 to 255	Passive error flag (6 consecutive “recessive (R)” bits)
	Receive	128 or more	
Bus off	Transmit	256 or more	Transfer is not possible. When a string of at least 11 consecutive “recessive (R)” bits occurs 128 times, the error counter is zero-cleared and the error active status can be resumed.

(b) Error counter

The error counter value is incremented each time an error occurs and is decremented when a transmit or receive operation ends normally. The count up/count down timing occurs at the first bit of the error delimiter.

Table 11-13. Error Counter

Status	Transmit Error Counter	Receive Error Counter
When receiving node has detected an error (except for bit errors that occur in an active error flag or overload flag)	No change	+1
When "dominant (D)" is detected following error frame's overload flag output by the receiving node	No change	+8
When transmitting node has sent an error flag [When error counter = ±0] <1> When an Ack error was detected during error passive status and a "dominant (D)" was not detected during error flag output <2> When a stuff error occurs in the arbitration field	+8	No change
Detection of bit error during output of active error flag or overload flag (transmitting node with error active status)	+8	No change
Detection of bit error during output of active error flag or overload flag (receiving node with error active status)	No change	+8
When 14 consecutive "dominant (D)" bits were detected from the start of each node's active error flag or overload flag, followed by detection of eight consecutive dominant bits. Each node has detected eight consecutive dominant bits after a passive error flag.	+8	+8
The transmitting node has completed a transmit operation without any errors (±0 if error counter value is 0).	–1	No change
The receiving node has completed a receive operation without any errors.	No change	• - 1 (1 ≦ REC[Note] ≦ 127) • ±0 (REC = 0) • 127 is set (REC > 127)

Note REC: Receive error counter.

(c) Occurrence of bit error during intermission

In this case, an overload frame occurs.

Caution When an error occurs, error control is performed according to the contents of the transmitting and receiving error counters as they existed prior to the error's occurrence. The error counter value is incremented only after an error flag has been output.

11.8.7 Baud rate control function

(1) Prescaler

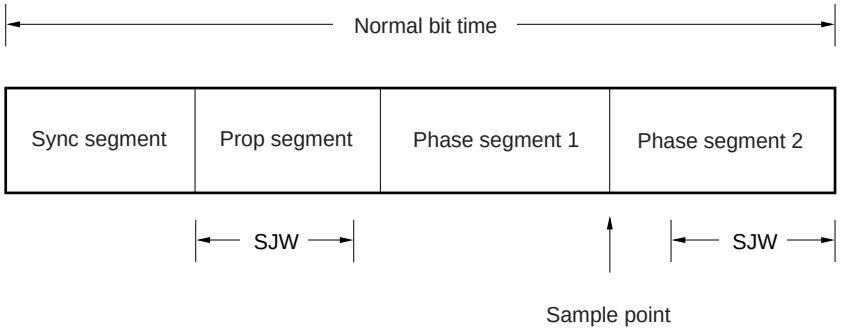
The V850E/IA1 includes a prescaler for dividing the system clock (main clock). This prescaler generates a clock (CK_{TQ}) that is based on a division ratio ranging from 2 to 128 applied to the system clock when the C1BRP register's TLM bit = 0 and based on a division ratio ranging from 2 to 256 applied to the system clock when the TLM bit = 1 (Refer to **11.10 (26) CAN1 bit rate prescaler register (C1BRP)**).

(2) Normal bit time (8 to 25 time quantum)

A definition of 1 data bit time (1 time quantum) is shown below.

Remark 1 time quantum = $1/CK_{TQ}$

Figure 11-20. Normal Bit Time (8 to 25 Time Quantum)



Segment Name	Segment Length	Description
Sync segment (Synchronization Segment)	1	This segment begins when resynchronization occurs.
Prop segment (Propagation Segment)	1 to 8 (programmable)	This segment is used to absorb the delays caused by the output buffer, CAN bus, and input buffer. It is set to return an Ack signal until phase segment 1 begins. Prop segment time $\geqq$ (output buffer delay) + (CAN bus delay) + (input buffer delay)
Phase segment 1 (Phase Buffer Segment 1)	1 to 8 (programmable)	This segment is used to compensate for errors in the data bit time. It accommodates a wide margin or error but slows down communication speed.
Phase segment 2 (Phase Buffer Segment 2)	Maximum value from phase segment 1 + IPT[Note] (IPT = 0 to 2)	
SJW (reSynchronization Jump Width)	1 to 4 (programmable)	This sets the range for bit synchronization.

Note IPT: Information Processing Time

(3) Data bit synchronization

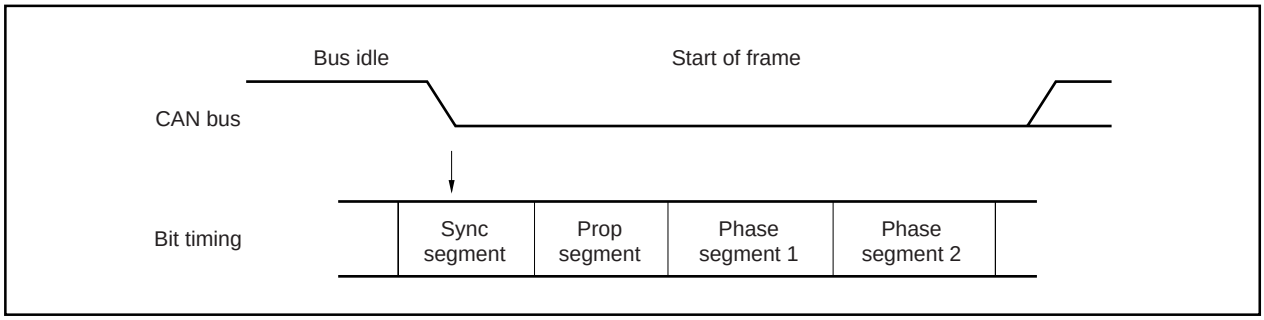
- Since the receiving node has no synchronization signal, synchronization is performed using level changes that occur on the bus.
- As for the transmitting node, data is transmitted in sync with the transmitting node's bit timing.

(a) Hardware synchronization

This is bit synchronization that is performed when the receiving node has detected a start of frame in bus idle mode.

- When a falling edge is detected on the bus, the current bit is assigned to the sync segment and the next bit is assigned to the prop segment. In such cases, synchronization is performed regardless of the SJW (reSynchronization Jump Width).
- Since bit synchronization must be established after a reset or after a wake-up, hardware synchronization is performed only at the first level change that occurs on the bus (for the second and subsequent level changes, bit synchronization is performed as shown below).

Figure 11-21. Coordination of Data Bit Synchronization

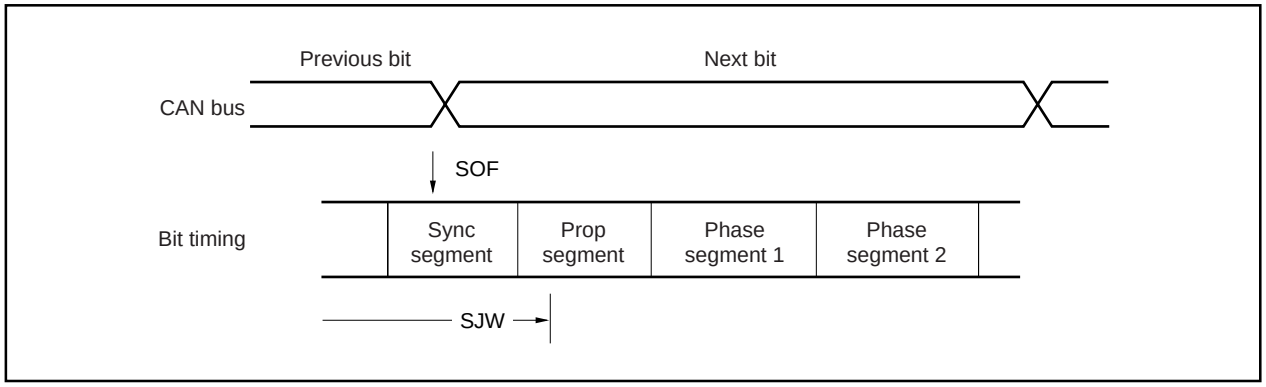


(b) Resynchronization

Resynchronization is performed when a level change is detected on the bus during a receive operation.

- The edge's phase error is produced by the relative positions of the detected edge and sync segment.
  <Phase error symbols>
  0: When edge is within sync segment
  Positive: Edge is before sample point (phase error)
  Negative: Edge is after sample point (phase error)
- When the edge is detected as within the bit timing specified by the SJW, synchronization is performed in the same way as hardware synchronization.
- When the edge is detected as extending beyond the bit timing specified by the SJW, synchronization is performed on the following basis.
  When phase error is positive: Phase segment 1 is lengthened to equal the SJW
  When phase error is negative: Phase segment 2 is shortened to equal the SJW
- A "shifting" of the baud rate for the transmitting and receiving nodes moves the relative position of the sample point for data on the receiving node.

Figure 11-22. Resynchronization



11.9 Caution Points on Bit Set/Clear Function

The FCAN control registers include registers whose bits can be set or cleared via the CPU and via the CAN interface. An operation error occurs if the following registers are written to directly, so do not directly write (via bit manipulation, read/modify/write, or direct writing of target values) values to them.

- CAN global status register (CGST)
- CAN global interrupt enable register (CGIE)
- CAN1 control register (C1CTRL)
- CAN1 definition register (C1DEF)
- CAN1 interrupt enable register (C1IE)

All 16 bits in the above registers can be read via the usual method. Use the procedure described in Figure 11-23 below to set or clear the lower 8 bits in these registers.

Setting or clearing of lower 8 bits in the above registers is performed in combination with the higher 8 bits (see **Figure 11-24**). Figure 11-23 shows how the values of set bits or clear bits relate to set/clear/no change operations in the corresponding register.

Figure 11-23. Example of Bit Setting/Clearing Operations

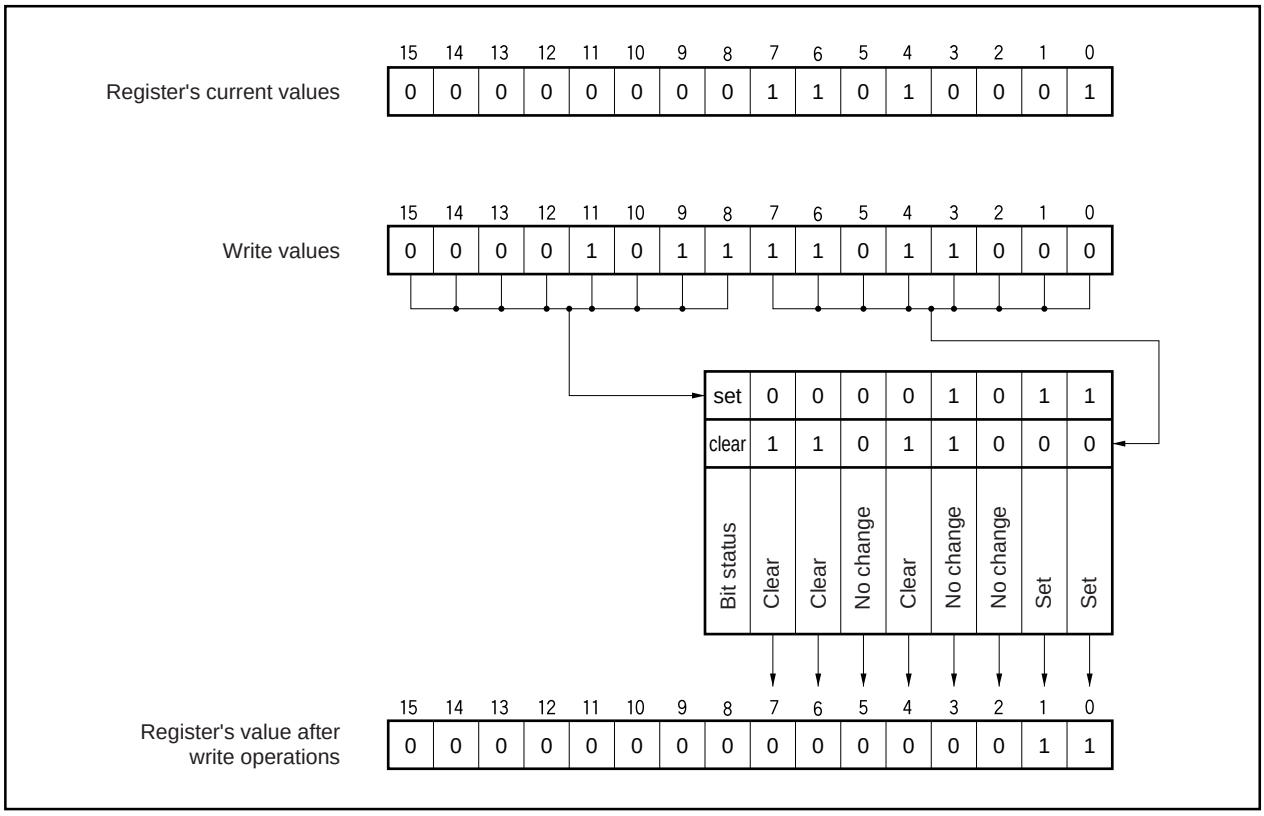


Figure 11-24. 16-Bit Data During Write Operation

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
set 7	set 6	set 5	set 4	set 3	set 2	set 1	set 0	clear 7	clear 6	clear 5	clear 4	clear 3	clear 2	clear 1	clear 0

set n	clear n	Status of clear n Bit After Bit Set/Clear Operation
0	0	No change
0	1	0
1	0	1
1	1	No change

Remark n = 0 to 7

11.10 Control Registers

(1) FCAN clock selection register (PRM04)

The PRM04 register is used to select the main clock (f_{MEM1}).

The clock is selected according to the clock frequency.

This register can be read/written in 8-bit or 1-bit units.

Caution Set this register before using FCAN.

Figure 11-25. FCAN Clock Selection Register (PRM04)

	7	6	5	4	3	2	1	0	Address	Initial value
PRM04	0	0	0	0	0	0	PRM5	PRM4	FFFFF930H	00H

Bit Position	Bit Name	Function
1, 0	PRM5, PRM4	Specifies FCAN main clock (f_{MEM1})

PRM5	PRM4	Input Clock Specification
0	0	ϕ/4 (when ϕ > 48 MHz)
0	1	ϕ/2 (when 16 MHz < ϕ ≤ 32 MHz)
1	0	ϕ/3 (when 32 MHz < ϕ ≤ 48 MHz)
1	1	ϕ (when ϕ ≤ 16 MHz)

Remark ϕ: Internal system clock

(2) CAN message data length registers 00 to 31 (M_DLC00 to M_DLC31)

The M_DLCn register sets the byte count in the data field of CAN message buffer n (n = 00 to 31). When receiving, the receive data field's byte count is set (to 1).

These registers can be read/written in 8-bit units.

Figure 11-26. CAN Message Data Length Registers 00 to 31 (M_DLC00 to M_DLC31)

	7	6	5	4	3	2	1	0	Address	Initial value
M_DLCn (n = 00 to 31)	RFU[Note]	RFU[Note]	RFU[Note]	RFU[Note]	DLC3	DLC2	DLC1	DLC0	See **Table 11-14**	Underfined

Bit Position	Bit Name	Function
3 to 0	DLC3 to DLC0	Control field data for setting the number of bytes in the data field

DLC3	DLC2	DLC1	DLC0	Data Length Code of Transmit/Receive Message
0	0	0	0	0 bytes
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	0	0	0	8 bytes
Other than above				Setting prohibited (If specified during transfer, 8-byte transfer is performed regardless of DLC value.)

Note The RFU bits are reserved for future use. Be sure to set these bits to 0 when writing to the M_DLCn register.

Table 11-14. Addresses of M_DLCn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_DLC00	xxxxmFF804H	M_DLC16	xxxxmFFA04H
M_DLC01	xxxxmFF824H	M_DLC17	xxxxmFFA24H
M_DLC02	xxxxmFF844H	M_DLC18	xxxxmFFA44H
M_DLC03	xxxxmFF864H	M_DLC19	xxxxmFFA64H
M_DLC04	xxxxmFF884H	M_DLC20	xxxxmFFA84H
M_DLC05	xxxxmFF8A4H	M_DLC21	xxxxmFFAA4H
M_DLC06	xxxxmFF8C4H	M_DLC22	xxxxmFFAC4H
M_DLC07	xxxxmFF8E4H	M_DLC23	xxxxmFFAE4H
M_DLC08	xxxxmFF904H	M_DLC24	xxxxmFFB04H
M_DLC09	xxxxmFF924H	M_DLC25	xxxxmFFB24H
M_DLC10	xxxxmFF944H	M_DLC26	xxxxmFFB44H
M_DLC11	xxxxmFF964H	M_DLC27	xxxxmFFB64H
M_DLC12	xxxxmFF984H	M_DLC28	xxxxmFFB84H
M_DLC13	xxxxmFF9A4H	M_DLC29	xxxxmFFBA4H
M_DLC14	xxxxmFF9C4H	M_DLC30	xxxxmFFBC4H
M_DLC15	xxxxmFF9E4H	M_DLC31	xxxxmFFBE4H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(3) CAN message control registers 00 to 31 (M_CTRLC00 to M_CTRL31)

The M_CTRLn register is used to set the frame format of the data field in messages stored in CAN message buffer n (n = 00 to 31).

These registers can be read/written in 8-bit units.

Figure 11-27. CAN Message Control Registers 00 to 31 (M_CTRLC00 to M_CTRL31) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
M_CTRLn (n = 00 to 31)	RMDE1	RMDE0	ATS	IE	MOVR	RFU[Notes1, 2]	RFU[Notes1, 3]	RTR	See **Table 11-15**	Underfined

Notes 1. The RFU bits are reserved for future use. Be sure to set these bits to 0 when writing to this register.

2. The value of the r1 bit on the CAN bus is set during reception.

3. The value of the r0 bit on the CAN bus is set during reception.

Bit Position	Bit Name	Function
7	RMDE1	Specifies operation of the DN flag when a remote frame is received during a transmit message. 0: DN flag not set when remote frame is received 1: DN flag set when remote frame is received **Cautions 1. When the RMDE1 bit is set, the setting of the RMDE0 bit is irrelevant.** **2. If a remote frame arrives at the transmit message buffer when the RMDE1 bit has not been set, the CPU is not notified, nor are other operations performed.**
6	RMDE0	Specifies setting/clearing status of remote frame auto acknowledge function. 0: Remote frame auto acknowledge function cleared 1: Remote frame auto acknowledge function set **Cautions 1. The RMDE0 bit's setting is used only for transmit messages.** **2. When the RTR bit has been set (to 1) (when the receive message or transmit message has a remote frame), the RMDE0 bit is processed as RMDE0 = 0. This prevents a worst-case scenario (in which transmission of a remote frame draws a 100 % bus load due to reception of the same remote frame).**

Remark DN: Bit 2 of M_STATn (see **Figure 11-32**)

Figure 11-27. CAN Message Control Registers 00 to 31 (M_CTRLC00 to M_CTRL31) (2/2)

Bit Position	Bit Name	Function
5	ATS	Specifies whether or not to add a time stamp when transmitting. 0: Time stamp not added when transmitting 1: Time stamp added when transmitting **Cautions 1. The ATS bit is used only for transmit messages.** **2. When the ATS bit has been set (to 1) and the data length code specifies at least two bytes, the last two bytes are replaced by a time stamp (see Table 11-3 Example When Adding Captured Time Stamp Value to Last 2 Bytes of Transmit Message). The added time stamp counter value is sent over the bus via the SOF of the message. When this occurs, the last two bytes (which are defined as a data field) are ignored.**
4	IE	Specifies the enable/disable setting for interrupt requests. 0: Interrupt requests disabled 1: Interrupt requests enabled **Cautions 1. When IE bit = 1, an interrupt request is generated when interrupts are enabled under the following conditions.** **• When a message has been sent from the transmit message buffer** **• When a message has been received by the receive message buffer** **• When the transmit message buffer receives a remote frame when the auto acknowledge function is not set (RMDE0 bit = 0)** **2. When the IE bit = 1, an interrupt request is not generated 0 when interrupts are enabled under the following conditions.** **• When a remote frame has been received for a transmit message when the auto acknowledge function has been set (RMDE0 bit = 1)** **• When a remote frame has been transmitted from the receive message buffer**
3	MOVR	This is the flag that indicates a message buffer overwrite. 0: Overwrite does not occur after DN bit is cleared 1: Overwrite occurs at least once after DN bit is cleared **Caution An overrun of the message buffer occurs when the CAN module writes new data to the message buffer or when the DN bit has already been set (to 1). The MOVR bit is updated each time new data is stored in the message buffer.**
0	RTR	Specifies frame type. 0: Data frame transmit/receive 1: Remote frame transmit/receive **Caution When the RTR bit has been set (to 1) for a transmit message, a remote frame is transmitted instead of a data frame.**

Remark DN: Bit 2 of M_STATn (see **Figure 11-32**)

Table 11-15. Addresses of M_CTRLn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_CTRL00	xxxxmFF805H	M_CTRL16	xxxxmFFA05H
M_CTRL01	xxxxmFF825H	M_CTRL17	xxxxmFFA25H
M_CTRL02	xxxxmFF845H	M_CTRL18	xxxxmFFA45H
M_CTRL03	xxxxmFF865H	M_CTRL19	xxxxmFFA65H
M_CTRL04	xxxxmFF885H	M_CTRL20	xxxxmFFA85H
M_CTRL05	xxxxmFF8A5H	M_CTRL21	xxxxmFFAA5H
M_CTRL06	xxxxmFF8C5H	M_CTRL22	xxxxmFFAC5H
M_CTRL07	xxxxmFF8E5H	M_CTRL23	xxxxmFFAE5H
M_CTRL08	xxxxmFF905H	M_CTRL24	xxxxmFFB05H
M_CTRL09	xxxxmFF925H	M_CTRL25	xxxxmFFB25H
M_CTRL10	xxxxmFF945H	M_CTRL26	xxxxmFFB45H
M_CTRL11	xxxxmFF965H	M_CTRL27	xxxxmFFB65H
M_CTRL12	xxxxmFF985H	M_CTRL28	xxxxmFFB85H
M_CTRL13	xxxxmFF9A5H	M_CTRL29	xxxxmFFBA5H
M_CTRL14	xxxxmFF9C5H	M_CTRL30	xxxxmFFBC5H
M_CTRL15	xxxxmFF9E5H	M_CTRL31	xxxxmFFBE5H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(4) CAN message time stamp registers 00 to 31 (M_TIME00 to M_TIME31)

The M_TIMEn register is the area where the time stamp counter value is written upon completion of data reception (n = 00 to 31).

These registers can be read/written in 16-bit units.

Figure 11-28. CAN Message Time Stamp Registers 00 to 31 (M_TIME00 to M_TIME31)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
M_TIMEn	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	TS	See **Table 11-16**	Underfined
(n = 00 to 31)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Bit Position	Bit Name	Function
15 to 0	TS15 to TS0	Indicates the time stamp counter value. **Caution When a data frame or remote frame is received in the receive message buffer, the new data is stored in the message buffer and a 16-bit time tag (time stamp counter value) is stored in the M_TIMEn register. This time tag is set according to the FCAN's time stamp setting, which is either the time stamp counter value that was captured when the SOF was sent via the bus or the value captured when the CAN module writes data to the message buffer.**

Table 11-16. Addresses of M_TIMEn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_TIME00	xxxxmFF806H	M_TIME16	xxxxmFFA06H
M_TIME01	xxxxmFF826H	M_TIME17	xxxxmFFA26H
M_TIME02	xxxxmFF846H	M_TIME18	xxxxmFFA46H
M_TIME03	xxxxmFF866H	M_TIME19	xxxxmFFA66H
M_TIME04	xxxxmFF886H	M_TIME20	xxxxmFFA86H
M_TIME05	xxxxmFF8A6H	M_TIME21	xxxxmFFAA6H
M_TIME06	xxxxmFF8C6H	M_TIME22	xxxxmFFAC6H
M_TIME07	xxxxmFF8E6H	M_TIME23	xxxxmFFAE6H
M_TIME08	xxxxmFF906H	M_TIME24	xxxxmFFB06H
M_TIME09	xxxxmFF926H	M_TIME25	xxxxmFFB26H
M_TIME10	xxxxmFF946H	M_TIME26	xxxxmFFB46H
M_TIME11	xxxxmFF966H	M_TIME27	xxxxmFFB66H
M_TIME12	xxxxmFF986H	M_TIME28	xxxxmFFB86H
M_TIME13	xxxxmFF9A6H	M_TIME29	xxxxmFFBA6H
M_TIME14	xxxxmFF9C6H	M_TIME30	xxxxmFFBC6H
M_TIME15	xxxxmFF9E6H	M_TIME31	xxxxmFFBE6H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(5) CAN message data registers n0 to n7 (M_DATAn0 to M_DATAn7) (n = 00 to 31)

The M_DATAnx registers are areas where up to 87 bytes of transmit or receive data is stored (n = 00 to 31). These registers can be read/written in 8-bit units.

Figure 11-29. CAN Message Data Registers n0 to n7 (M_DATAn0 to M_DATAn7) (n = 00 to 31)

	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn0 (n = 00 to 31)	D0_7	D0_6	D0_5	D0_4	D0_3	D0_2	D0_1	D0_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn1 (n = 00 to 31)	D1_7	D1_6	D1_5	D1_4	D1_3	D1_2	D1_1	D1_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn2 (n = 00 to 31)	D2_7	D2_6	D2_5	D2_4	D2_3	D2_2	D2_1	D2_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn3 (n = 00 to 31)	D3_7	D3_6	D3_5	D3_4	D3_3	D3_2	D3_1	D3_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn4 (n = 00 to 31)	D4_7	D4_6	D4_5	D4_4	D4_3	D4_2	D4_1	D4_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn5 (n = 00 to 31)	D5_7	D5_6	D5_5	D5_4	D5_3	D5_2	D5_1	D5_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn6 (n = 00 to 31)	D6_7	D6_6	D6_5	D6_4	D6_3	D6_2	D6_1	D6_0	See **Table 11-17**	Underfined
	7	6	5	4	3	2	1	0	Address	Initial value
M_DATAn7 (n = 00 to 31)	D7_7	D7_6	D7_5	D7_4	D7_3	D7_2	D7_1	D7_0	See **Table 11-17**	Underfined

Bit Position	Bit Name	Function
7 to 0	D7_7 to D0_0	Indicates the contents of the message data. **Cautions 1. The M_DATAn0 to M_DATAn7 registers are fields used to hold receive data and transmit data. When data is transmitted, the number of messages defined by the DLC3 to DLC0 bits in the M_DLCn register are transmitted via the CAN bus.** **2. When the M_CTRLn register's ATS bit has been set (to 1) and the value of the DLC3 to DLC0 bits in the M_DLCn register is at least two bytes, the last two bytes that are sent normally via the CAN bus are ignored and the time stamp value is sent.** **3. When a new message is received, all data fields are updated, even when the value of the DLC3 to DLC0 bits in the M_DLCn register is less than 8 bytes. The values of data bytes that have not been received may be updated, but they are ignored.**

Remark n = 00 to 31

Table 11-17. Addresses of M_DATAnx (n = 00 to 31, x = 0 to 7)

n \ Register Name	M_DATAn0[Note] (m = 2, 6, A, E)	M_DATAn1[Note] (m = 2, 6, A, E)	M_DATAn1[Note] (m = 2, 6, A, E)	M_DATAn3[Note] (m = 2, 6, A, E)	M_DATAn4[Note] (m = 2, 6, A, E)	M_DATAn5[Note] (m = 2, 6, A, E)	M_DATAn6[Note] (m = 2, 6, A, E)	M_DATAn7[Note] (m = 3, 7, B)
00	xxxxmFF808H	xxxxmFF809H	xxxxmFF80AH	xxxxmFF80BH	xxxxmFF80CH	xxxxmFF80DH	xxxxmFF80EH	xxxxmFF80FH
01	xxxxmFF828H	xxxxmFF829H	xxxxmFF82AH	xxxxmFF82BH	xxxxmFF82CH	xxxxmFF82DH	xxxxmFF82EH	xxxxmFF82FH
02	xxxxmFF848H	xxxxmFF849H	xxxxmFF84AH	xxxxmFF84BH	xxxxmFF84CH	xxxxmFF84DH	xxxxmFF84EH	xxxxmFF84FH
03	xxxxmFF868H	xxxxmFF869H	xxxxmFF86AH	xxxxmFF86BH	xxxxmFF86CH	xxxxmFF86DH	xxxxmFF86EH	xxxxmFF86FH
04	xxxxmFF888H	xxxxmFF889H	xxxxmFF88AH	xxxxmFF88BH	xxxxmFF88CH	xxxxmFF88DH	xxxxmFF88EH	xxxxmFF88FH
05	xxxxmFF8A8H	xxxxmFF8A9H	xxxxmFF8AAH	xxxxmFF8ABH	xxxxmFF8ACH	xxxxmFF8ADH	xxxxmFF8AEH	xxxxmFF8AFH
06	xxxxmFF8C8H	xxxxmFF8C9H	xxxxmFF8CAH	xxxxmFF8CBH	xxxxmFF8CCH	xxxxmFF8CDH	xxxxmFF8CEH	xxxxmFF8CFH
07	xxxxmFF8E8H	xxxxmFF8E9H	xxxxmFF8EAH	xxxxmFF8EBH	xxxxmFF8ECH	xxxxmFF8EDH	xxxxmFF8EEH	xxxxmFF8EFH
08	xxxxmFF908H	xxxxmFF909H	xxxxmFF90AH	xxxxmFF90BH	xxxxmFF90CH	xxxxmFF90DH	xxxxmFF90EH	xxxxmFF90FH
09	xxxxmFF928H	xxxxmFF929H	xxxxmFF92AH	xxxxmFF92BH	xxxxmFF92CH	xxxxmFF92DH	xxxxmFF92EH	xxxxmFF92FH
10	xxxxmFF948H	xxxxmFF949H	xxxxmFF94AH	xxxxmFF94BH	xxxxmFF94CH	xxxxmFF94DH	xxxxmFF94EH	xxxxmFF94FH
11	xxxxmFF968H	xxxxmFF969H	xxxxmFF96AH	xxxxmFF96BH	xxxxmFF96CH	xxxxmFF96DH	xxxxmFF96EH	xxxxmFF96FH
12	xxxxmFF988H	xxxxmFF989H	xxxxmFF98AH	xxxxmFF98BH	xxxxmFF98CH	xxxxmFF98DH	xxxxmFF98EH	xxxxmFF98FH
13	xxxxmFF9A8H	xxxxmFF9A9H	xxxxmFF9AAH	xxxxmFF9ABH	xxxxmFF9ACH	xxxxmFF9ADH	xxxxmFF9AEH	xxxxmFF9AFH
14	xxxxmFF9C8H	xxxxmFF9C9H	xxxxmFF9CAH	xxxxmFF9CBH	xxxxmFF9CCH	xxxxmFF9CDH	xxxxmFF9CEH	xxxxmFF9CFH
15	xxxxmFF9E8H	xxxxmFF9E9H	xxxxmFF9EAH	xxxxmFF9EBH	xxxxmFF9ECH	xxxxmFF9EDH	xxxxmFF9EEH	xxxxmFF9EFH
16	xxxxmFFA08H	xxxxmFFA09H	xxxxmFFA0AH	xxxxmFFA0BH	xxxxmFFA0CH	xxxxmFFA0DH	xxxxmFFA0EH	xxxxmFFA0FH
17	xxxxmFFA28H	xxxxmFFA29H	xxxxmFFA2AH	xxxxmFFA2BH	xxxxmFFA2CH	xxxxmFFA2DH	xxxxmFFA2EH	xxxxmFFA2FH
18	xxxxmFFA48H	xxxxmFFA49H	xxxxmFFA4AH	xxxxmFFA4BH	xxxxmFFA4CH	xxxxmFFA4DH	xxxxmFFA4EH	xxxxmFFA4FH
19	xxxxmFFA68H	xxxxmFFA69H	xxxxmFFA6AH	xxxxmFFA6BH	xxxxmFFA6CH	xxxxmFFA6DH	xxxxmFFA6EH	xxxxmFFA6FH
20	xxxxmFFA88H	xxxxmFFA89H	xxxxmFFA8AH	xxxxmFFA8BH	xxxxmFFA8CH	xxxxmFFA8DH	xxxxmFFA8EH	xxxxmFFA8FH
21	xxxxmFFAA8H	xxxxmFFAA9H	xxxxmFFAAAH	xxxxmFFAABH	xxxxmFFAACH	xxxxmFFAADH	xxxxmFFAAEH	xxxxmFFAAFH
22	xxxxmFFAC8H	xxxxmFFAC9H	xxxxmFFACAH	xxxxmFFACBH	xxxxmFFACCH	xxxxmFFACDH	xxxxmFFACEH	xxxxmFFACFH
23	xxxxmFFAE8H	xxxxmFFAE9H	xxxxmFFAEAH	xxxxmFFAEBH	xxxxmFFAECH	xxxxmFFAEDH	xxxxmFFAEEH	xxxxmFFAEFH
24	xxxxmFFB08H	xxxxmFFB09H	xxxxmFFB0AH	xxxxmFFB0BH	xxxxmFFB0CH	xxxxmFFB0DH	xxxxmFFB0EH	xxxxmFFB0FH
25	xxxxmFFB28H	xxxxmFFB29H	xxxxmFFB2AH	xxxxmFFB2BH	xxxxmFFB2CH	xxxxmFFB2DH	xxxxmFFB2EH	xxxxmFFB2FH
26	xxxxmFFB48H	xxxxmFFB49H	xxxxmFFB4AH	xxxxmFFB4BH	xxxxmFFB4CH	xxxxmFFB4DH	xxxxmFFB4EH	xxxxmFFB4FH
27	xxxxmFFB68H	xxxxmFFB69H	xxxxmFFB6AH	xxxxmFFB6BH	xxxxmFFB6CH	xxxxmFFB6DH	xxxxmFFB6EH	xxxxmFFB6FH
28	xxxxmFFB88H	xxxxmFFB89H	xxxxmFFB8AH	xxxxmFFB8BH	xxxxmFFB8CH	xxxxmFFB8DH	xxxxmFFB8EH	xxxxmFFB8FH
29	xxxxmFFBA8H	xxxxmFFBA9H	xxxxmFFBAAH	xxxxmFFBABH	xxxxmFFBACH	xxxxmFFBADH	xxxxmFFBAEH	xxxxmFFBAFH
30	xxxxmFFBC8H	xxxxmFFBC9H	xxxxmFFBCAH	xxxxmFFBCBH	xxxxmFFBCCH	xxxxmFFBCDH	xxxxmFFBCEH	xxxxmFFBCFH
31	xxxxmFFBE8H	xxxxmFFBE9H	xxxxmFFBEAH	xxxxmFFBEBH	xxxxmFFBECH	xxxxmFFBEDH	xxxxmFFBEEH	xxxxmFFBEFH

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(6) CAN message ID registers L00 to L31 and H00 to H31 (M_IDL00 to M_IDL31 and M_IDH00 to M_IDH31)

The M_IDLn and M_IDHn registers are areas used to set identifiers (n = 00 to 31).
These registers can be read/written in 16-bit units.

When in standard format mode, any data can be stored in the following areas.

Bits ID0 to ID7: First byte of receive data[Note] is stored.
Bits ID8 to ID15: Second byte of receive data[Note] is stored.
Bits ID16, ID17: Third byte (higher two bits) of receive data[Note] is stored.

Note See **11.10 (5) CAN message data registers n0 to n7 (M_DATAn0 to M_DATAn7) (n = 00 to 31)**.

Figure 11-30. CAN Message ID Registers L00 to L31 and H00 to H31 (M_IDL00 to M_IDL31 and M_IDH00 to M_IDH31)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
M_IDHn (n = 00 to 31)	IDE	0	0	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16	See **Table 11-19**	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
M_IDLn (n = 00 to 31)	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	See **Table 11-18**	Undefined

Bit Position	Bit Name	Function
15 (M_IDHn)	IDEn (M_IDHn)	Specifies format setting mode. 0: Standard format mode (ID28 to ID18: 11 bits) 1: Extended format mode (ID28 to ID0: 29 bits)
12 to 0 (M_IDHn) 15 to 0 (M_IDLn)	ID28 to ID16 (M_IDHn) ID15 to ID0 (M_IDLn)	Indicates the contents of ID28 to ID0.

Remark n = 00 to 31

Table 11-18. Addresses of M_IDLn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_IDL00	xxxxm810H	M_IDL16	xxxxmA10H
M_IDL01	xxxxm830H	M_IDL17	xxxxmA30H
M_IDL02	xxxxm850H	M_IDL18	xxxxmA50H
M_IDL03	xxxxm870H	M_IDL19	xxxxmA70H
M_IDL04	xxxxm890H	M_IDL20	xxxxmA90H
M_IDL05	xxxxm8B0H	M_IDL21	xxxxmAB0H
M_IDL06	xxxxm8D0H	M_IDL22	xxxxmAD0H
M_IDL07	xxxxm8F0H	M_IDL23	xxxxmAF0H
M_IDL08	xxxxm910H	M_IDL24	xxxxmB10H
M_IDL09	xxxxm930H	M_IDL25	xxxxmB30H
M_IDL10	xxxxm950H	M_IDL26	xxxxmB50H
M_IDL11	xxxxm970H	M_IDL27	xxxxmB70H
M_IDL12	xxxxm990H	M_IDL28	xxxxmB90H
M_IDL13	xxxxm9B0H	M_IDL29	xxxxmBB0H
M_IDL14	xxxxm9D0H	M_IDL30	xxxxmBD0H
M_IDL15	xxxxm9F0H	M_IDL31	xxxxmBF0H

Note CAN message buffer registers can be allocated to the addresses xxxx as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

Table 11-19. Addresses of M_IDHn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_IDH00	xxxxm812H	M_IDH16	xxxxmA12H
M_IDH01	xxxxm832H	M_IDH17	xxxxmA32H
M_IDH02	xxxxm852H	M_IDH18	xxxxmA52H
M_IDH03	xxxxm872H	M_IDH19	xxxxmA72H
M_IDH04	xxxxm892H	M_IDH20	xxxxmA92H
M_IDH05	xxxxm8B2H	M_IDH21	xxxxmAB2H
M_IDH06	xxxxm8D2H	M_IDH22	xxxxmAD2H
M_IDH07	xxxxm8F2H	M_IDH23	xxxxmAF2H
M_IDH08	xxxxm912H	M_IDH24	xxxxmB12H
M_IDH09	xxxxm932H	M_IDH25	xxxxmB32H
M_IDH10	xxxxm952H	M_IDH26	xxxxmB52H
M_IDH11	xxxxm972H	M_IDH27	xxxxmB72H
M_IDH12	xxxxm992H	M_IDH28	xxxxmB92H
M_IDH13	xxxxm9B2H	M_IDH29	xxxxmBB2H
M_IDH14	xxxxm9D2H	M_IDH30	xxxxmBD2H
M_IDH15	xxxxm9F2H	M_IDH31	xxxxmBF2H

Note CAN message buffer registers can be allocated to the addresses xxxx as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(7) CAN message configuration registers 00 to 31 (M_CONF00 to M_CONF31)

The M_CONFn register is used to set group messages (n = 00 to 31).

These registers can be read/written in 8-bit units.

Figure 11-31. CAN Message Configuration Registers 00 to 31 (M_CONF00 to M_CONF31)

	7	6	5	4	3	2	1	0	Address	Initial value
M_CONFn (n = 00 to 31)	0	0	MT2	MT1	MT0	0	0	MA	See **Table 11-20**	Undefined

Bit Position	Bit Name	Function
5 to 3	MT2 to MT0	Specifies message type and mask setting.

MT2	MT1	MT0	Operation
0	0	0	Transmit message
0	0	1	Receive message (no mask setting)
0	1	0	Receive message (mask 0 is set)
0	1	1	Receive message (mask 1 is set)
1	0	0	Receive message (mask 2 is set)
1	0	1	Receive message (mask 3 is set)
1	1	0	Setting prohibited
1	1	1	Receive message (diagnostic processing mode)

Caution For the standard format setting, the mask function can be used not only to mask the identifier (ID) but also the first 18 data bits. However, in this case, the byte configuration of the expected data must be set to the ID field. When bits MT2 to MT0 have been set as "111", processing can be performed only when the FCAN has been set to diagnostic mode. In such cases, all messages received are stored regardless of the following conditions.

- **Storage to other message buffer**
- **Identifier type (standard frame or extended frame)**
- **Data frame or remote frame**

Bit Position	Bit Name	Function
0	MA	Specifies message buffer's address.

MA	Operation
0	Message buffer is not used
1	Used as message buffer

Caution When the MA0 bit has been set to "000", message buffer area is used for application RAM or for event processing as a temporary buffer.

Table 11-20. Addresses of M_CONFn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_CONF00	xxxxm814H	M_CONF16	xxxxmA14H
M_CONF01	xxxxm834H	M_CONF17	xxxxmA34H
M_CONF02	xxxxm854H	M_CONF18	xxxxmA54H
M_CONF03	xxxxm874H	M_CONF19	xxxxmA74H
M_CONF04	xxxxm894H	M_CONF20	xxxxmA94H
M_CONF05	xxxxm8B4H	M_CONF21	xxxxmAB4H
M_CONF06	xxxxm8D4H	M_CONF22	xxxxmAD4H
M_CONF07	xxxxm8F4H	M_CONF23	xxxxmAF4H
M_CONF08	xxxxm914H	M_CONF24	xxxxmB14H
M_CONF09	xxxxm934H	M_CONF25	xxxxmB34H
M_CONF10	xxxxm954H	M_CONF26	xxxxmB54H
M_CONF11	xxxxm974H	M_CONF27	xxxxmB74H
M_CONF12	xxxxm994H	M_CONF28	xxxxmB94H
M_CONF13	xxxxm9B4H	M_CONF29	xxxxmBB4H
M_CONF14	xxxxm9D4H	M_CONF30	xxxxmBD4H
M_CONF15	xxxxm9F4H	M_CONF31	xxxxmBF4H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(8) CAN message status registers 00 to 31 (M_STAT00 to M_STAT31)

The M_STATn register indicates group message transmit/receive status information (n = 00 to 31).
These registers are read-only in 8-bit units.

Cautions 1. Writing to M_STATn register is performed using CAN status set/clear register n (SC_STATn).

2. Messages are transmitted only when the M_STATn registers' TRQ and RDY bits have been set (to 1).

Figure 11-32. CAN Message Status Registers 00 to 31 (M_STAT00 to M_STAT31)

	7	6	5	4	3	2	1	0	Address	Initial value
M_STATn (n = 00 to 31)	0	0	0	0	RFU[Note]	DN	TRQ	RDY	See **Table 11-21**	Underfined

Note The RFU bit is reserved for future use. Be sure to set this bit to 0 when writing to the M_STATn register.

Bit Position	Bit Name	Function
2	DN	This is the message update flag. 0: No message was received after DN bit was cleared. 1: At least one message was received after DN bit was cleared. When the DN bit has been set (to 1) by the transmit message buffer, it indicates that the message buffer has received a remote frame. When this message is sent, the DN bit is automatically cleared (to 0). When a frame is again received in the message buffer for which the DN bit has been set (to 1), an overrun condition occurs and the M_CTRLn register's MOVR bit is set (to 1) (n = 00 to 31).
1	TRQ	This is the transmit request flag. 0: Message transmission disabled 1: Message transmission enabled
0	RDY	This is the message ready flag. 0: Message is not ready. 1: Message is ready. A receive operation is performed only for a message buffer in which the RDY bit is set to 1 during reception. A transmit operation is performed only for a message buffer in which the RDY bit is set to 1 and the TRQ bit is set to 1 during transmission.

Caution The FCAN controller incorporated in the V850E/IA1 can receive messages even if RDY bit is not set. However, there are some products other than the V850E/IA1 that cannot receive messages without the RDY setting. Be sure to set RDY bit before a receive operation even when using the V850E/IA1's FCAN controller to retain software compatibility.

Table 11-21. Addresses of M_STATn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
M_STAT00	xxxxm815H	M_STAT16	xxxxmA15H
M_STAT01	xxxxm835H	M_STAT17	xxxxmA35H
M_STAT02	xxxxm855H	M_STAT18	xxxxmA55H
M_STAT03	xxxxm875H	M_STAT19	xxxxmA75H
M_STAT04	xxxxm895H	M_STAT20	xxxxmA95H
M_STAT05	xxxxm8B5H	M_STAT21	xxxxmAB5H
M_STAT06	xxxxm8D5H	M_STAT22	xxxxmAD5H
M_STAT07	xxxxm8F5H	M_STAT23	xxxxmAF5H
M_STAT08	xxxxm915H	M_STAT24	xxxxmB15H
M_STAT09	xxxxm935H	M_STAT25	xxxxmB35H
M_STAT10	xxxxm955H	M_STAT26	xxxxmB55H
M_STAT11	xxxxm975H	M_STAT27	xxxxmB75H
M_STAT12	xxxxm995H	M_STAT28	xxxxmB95H
M_STAT13	xxxxm9B5H	M_STAT29	xxxxmBB5H
M_STAT14	xxxxm9D5H	M_STAT30	xxxxmBD5H
M_STAT15	xxxxm9F5H	M_STAT31	xxxxmBF5H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(9) CAN status set/clear registers 00 to 31 (SC_STAT00 to SC_STAT31)

The SC_STATn register is used to set/clear the transmit/receive status information (n = 00 to 31). These registers are write-only in 16-bit units.

Figure 11-33. CAN Status Set/Clear Registers 00 to 31 (SC_STAT00 to SC_STAT31)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
SC_STATn (n = 00 to 31)	0	0	0	0	0	set DN	set TRQ	set RDY	0	0	0	0	0	clear DN	clear TRQ	clear RDY	See **Table 11-22**	Undefined

Bit Position	Bit Name	Function
10, 2	set DN, clear DN	Specifies setting/clearing of the message update flag.
9,1	set TRQ, clear TRQ	Specifies setting/clearing of the transmit request flag.
8, 0	set RDY, clear RDY	Specifies setting of the message ready flag.

set DN	clear DN	Message Update Flag Setting
0	1	Cleared (DN bit cleared)
1	0	Set (DN bit set)
Other than above		No change in DN bit value

set TRQ	clear TRQ	Transmit Request Flag Setting
0	1	Cleared (TRQ bit cleared)
1	0	Set (TRQ bit set)
Other than above		No change in TRQ bit value

set RDY	clear RDY	Message Ready Flag Setting
0	1	Cleared (RDY bit cleared)
1	0	Set (RDY bit set)
Other than above		No change in RDY bit value

Remark DN: Bit 2 of CAN message status register n (M_STATn)
TRQ: Bit 1 of CAN message status register n (M_STATn)
RDY: Bit 0 of CAN message status register n (M_STATn)

Table 11-22. Addresses of SC_STATn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)	Register Name	Address[Note] (m = 2, 6, A, E)
SC_STAT00	xxxxm816H	SC_STAT16	xxxxmA16H
SC_STAT01	xxxxm836H	SC_STAT17	xxxxmA36H
SC_STAT02	xxxxm856H	SC_STAT18	xxxxmA56H
SC_STAT03	xxxxm876H	SC_STAT19	xxxxmA76H
SC_STAT04	xxxxm896H	SC_STAT20	xxxxmA96H
SC_STAT05	xxxxm8B6H	SC_STAT21	xxxxmAB6H
SC_STAT06	xxxxm8D6H	SC_STAT22	xxxxmAD6H
SC_STAT07	xxxxm8F6H	SC_STAT23	xxxxmAF6H
SC_STAT08	xxxxm916H	SC_STAT24	xxxxmB16H
SC_STAT09	xxxxm936H	SC_STAT25	xxxxmB36H
SC_STAT10	xxxxm956H	SC_STAT26	xxxxmB56H
SC_STAT11	xxxxm976H	SC_STAT27	xxxxmB76H
SC_STAT12	xxxxm996H	SC_STAT28	xxxxmB96H
SC_STAT13	xxxxm9B6H	SC_STAT29	xxxxmBB6H
SC_STAT14	xxxxm9D6H	SC_STAT30	xxxxmBD6H
SC_STAT15	xxxxm9F6H	SC_STAT31	xxxxmBF6H

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(10) CAN interrupt pending register (CCINTP)

The CCINTP register is used to confirm the pending status of various interrupts.

This register is read-only in 16-bit units.

Figure 11-34. CAN Interrupt Pending Register (CCINTP)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CCINTP	0	INTMAC	0	0	0	0	0	0	0	0	0	0	0	CAN1 ERR	CAN1 REC	CAN1 TRX	xxxxmC00H[Note]	0000H

Bit Position	Bit Name	Function
14	INTMAC	Indicates an MAC error interrupt (generated by bits GINT3 to GINT0 of the CGINTP register) is pending. 0: Not pending 1: Pending
2	CAN1ERR	Indicates a CAN error occurrance interrupt (generated by bits C1INT6 to C1INT2 of the C1INTP register) is pending. 0: Not pending 1: Pending
1	CAN1REC	Indicates a CAN receive completion interrupt (generated by bit C1INT0 of the C1INTP register) is pending. 0: Not pending 1: Pending
0	CAN1TRX	Indicates a CAN transmit completion interrupt (generated by bit C1INT1 of the C1INTP register) is pending. 0: Not pending 1: Pending

Note MAC (Message Access Control) errors are errors that are set only when an interrupt source has occurred for the CAN global interrupt pending register (CGINTP).

(11) CAN global interrupt pending register (CGINTP)

The CGINTP register is used to confirm the pending status of MAC access error interrupts.

This register can be read/written in 8-bit units.

Figure 11-35. CAN Global Interrupt Pending Register (CGINTP)

	7	6	5	4	3	2	1	0	Address	Initial value
CGINTP	0	0	0	0	GINT3	GINT2	GINT1	0	xxxxmC02H[Note]	00H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
3	GINT3	Indicates that a wake-up interrupt from CAN sleep mode with stopped clock supply to FCAN is pending. 0: Not pending 1: Pending
2	GINT2	Indicates that an invalid write access error interrupt is pending. 0: Not pending 1: Pending
1	GINT1	Indicates that an unavailable memory address access error interrupt is pending. 0: Not pending 1: Pending

Cautions 1. When "1" is written to a bit in the CGINTP register, that bit is cleared (to 0). When "0" is written to it, the bit's value does not change.

2. An interrupt is generated when the corresponding interrupt request is enabled and when no interrupt pending bit has been set (to 1) for a new interrupt.

The correct or incorrect timing of setting the interrupt pending bit (to 1) is controlled by an interrupt service routine. The earlier that the interrupt service routine clears the interrupt pending bit (to 0), the more quickly the interrupt is generated without losing any new interrupts of the same type.

The interrupt pending bit can be set (to 1) only when the interrupt enable bit has been set (to 1). However, the interrupt pending bit is not automatically cleared (to 0) just because the interrupt ready bit has been cleared (to 0).

Use software processing to clear the interrupt pending bit (to 0).

Remark For details of invalid write access error interrupts and unavailable memory address access error interrupts, see **11.15.2 Interrupts that are generated for global CAN interface**.

(12) CAN1 local interrupt pending register (C1INTP)

The C1INTP register is used to confirm the pending status of local interrupts issued to FCAN.

This register can be read/written in 8-bit units.

Figure 11-36. CAN1 Local Interrupt Pending Register (C1INTP)

	7	6	5	4	3	2	1	0	Address	Initial value
C1INTP	0	C1INT6	C1INT5	C1INT4	C1INT3	C1INT2	C1INT1	C1INT0	xxxxmC04H[Note]	00H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
6	C1INT6	Indicates pending status of the CAN error interrupt. 0: Not pending 1: Pending
5	C1INT5	Indicates pending status of the CAN bus error interrupt. 0: Not pending 1: Pending
4	C1INT4	Indicates pending status of the wake up from CAN sleep mode interrupt. 0: Not pending 1: Pending
3	C1INT3	Indicates pending status of the CAN receive error passive status interrupt. 0: Not pending 1: Pending
2	C1INT2	Indicates pending status of the CAN transmit error passive or bus-off status interrupt. 0: Not pending 1: Pending
1	C1INT1	Indicates pending status of the CAN receive completion interrupt. 0: Not pending 1: Pending
0	C1INT0	Indicates pending status of the CAN transmit completion interrupt. 0: Not pending 1: Pending

Cautions 1. When "1" is written to a bit in the C1INTP register, that bit is cleared (to 0). When "0" is written to it, the bit's value does not change.

2. An interrupt is generated when the corresponding interrupt request is enabled and when no interrupt pending bit has been set (to 1) for a new interrupt.

The correct or incorrect timing of setting the interrupt pending bit (to 1) is controlled by an interrupt service routine. The earlier that the interrupt service routine clears the interrupt pending bit (to 0), the more quickly the interrupt is generated without losing any new interrupts of the same type.

The interrupt pending bit can be set (to 1) only when the interrupt ready bit has been set (to 1). However, the interrupt pending bit is not automatically cleared (to 0) just because the interrupt enable bit has been cleared (to 0). Use software processing to clear the interrupt pending bit (to 0).

Remark n = 1, 2

(13) CAN stop register (CSTOP)

The CSTOP register controls clock supply to the entire CAN system.

This register can be read/written in 16-bit units.

Figure 11-37. CAN Stop Register (CSTOP)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CSTOP	CSTP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	xxxxmC0CH[Note]	0000H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
15	CSTP	Controls clock supply to FCAN. 0: FCAN is operating (supplies clock to FCAN) 1: FCAN is stopped (access to FCAN is disabled) **Cautions 1. Be sure to set the CSTP bit (to 1) if the FCAN function will not be used.** **2. When the CSTP bit has been set (to 1), access to FCAN registers other than the CSTOP register is prohibited. Access to FCAN (other than the CSTOP register) is possible only when the CSTP bit has not been set (to 1). When it has been set (to 1), read access is undefined and write access is not possible.** **3. When a change occurs on the CAN bus via a CSTP bit setting while the clock supply to the CPU or peripheral functions CPU can be woken up.**

(14) CAN global status register (CGST)

The CGST register indicates global status information.

This register can be accessed in 16-bit or 8-bit units when reading. If the CGST register is read, bit 8 is set (to1). This register also can be accessed in 16-bit units when writing.

Cautions 1. Both bitwise writing and direct writing to the CGST register are prohibited. Attempts to write directly to this register may result in operation faults, so be sure to follow the sequence described in 11.9 Caution Points on Bit Set/Clear Function.

2. When writing to the CGST register, set or clear bits according to the register configuration during a write operation.

Figure 11-38. CAN Global Status Register (CGST) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CGST (Read)	0	0	0	0	0	0	0	1	MERR	0	0	0	EFSD	TSM	0	GOM	xxxxmC10H[Note]	0100H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CGST (Write)	0	0	0	0	set EFSD	set TSM	0	set GOM	clear MERR	0	0	0	clear EFSD	clear TSM	0	clear GOM

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) Read (1/2)

Bit Position	Bit Name	Function
7	MERR	This is the status flag that indicates an MAC error. 0: Error has not occurred after the status flag has been cleared. 1: Error occurred at least once after the status flag was cleared. **Caution An MAC error occurs when access to an invalid RAM address is attempted.**
3	EFSD	Indicates shutdown request. 0: Shutdown disabled 1: Shutdown enabled The EFSD bit must be set (to 1) before clearing the GOM bit (to 0). **Caution Be sure to set the EFSD bit (to 1) before clearing the GOM bit (to 0)(needs to be accessed twice). The EFSD bit will be cleared (to 0) automatically when the CGST register is accessed again.**

Figure 11-38. CAN Global Status Register (CGST) (2/2)

(a) Read (2/2)

Bit Position	Bit Name	Function
2	TSM	Indicates the operation status of the time stamp counter[Note]. 0: Time stamp counter is stopped 1: Time stamp counter is operating **Note** See **11.10 (17) CAN time stamp count register (CGTSC)**
0	GOM	Indicates the status of the global operation mode. 0: Accesses to message buffers and CAN module is disabled 1: Access to message buffers and CAN module is enabled **Cautions 1. Access to the FCAN's internal register areas is enabled regardless of the GOM bit's status.** **If the GOM bit has not been set (to 1), the CPU has read/write access to the temporary buffer area, but an error will occur if any of the CAN module registers are accessed. If the GOM bit has been set (to 1), the CPU is able to read only from the temporary buffer area, and is able to access the CAN module** **2. Before clearing the GOM bit (to 0), set the CCTRL register's INT bit (to 1), then set the EFSD bit (to 1). The GOM bit and EFSD bit will both be automatically cleared (to 0) when the CGST register is next accessed.**

(b) Write

Bit Position	Bit Name	Function
11, 3	set EFSD, clear EFSD	Enables/clears the EFSD bit. set EFSD / clear EFSD / Enables EFSD Bit 0 / 1 / EFSD bit cleared (to 0) 1 / 0 / EFSD bit set (to 1) Other than above / No change in EFSD bit's value
10, 2	set TSM, clear TSM	Enables/clears the TSM bit. set TSM / clear TSM / Enables TSM Bit 0 / 1 / TSM bit cleared (to 0) 1 / 0 / TSM bit set (to 1) Other than above / No change in TSM bit's value
8, 0	set GOM, clear GOM	Enables/clears the GOM bit. set GOM / clear GOM / Enables GOM Bit 0 / 1 / GOM bit cleared (to 0) 1 / 0 / GOM bit set (to 1) Other than above / No change in GOM bit's value
7	clear MERR	Clears the MERR bit. 0: No change in the MERR bit 1: MERR bit cleared (to 0)

(15) CAN global interrupt enable register (CGIE)

The CGIE register is used to issue interrupt requests for global interrupts.

This register can be read in 16-bit or 8-bit units and written in 16-bit units.

Cautions 1. Both bitwise writing and direct writing to the CGIE register are prohibited. Attempts to write directly to this register may result in operation faults, so be sure to follow the sequence described in 11.9 Caution Points on Bit Set/Clear Function.

2. When writing to the CGIE register, set or clear bits according to the register configuration during a write operation.

Figure 11-39. CAN Global Interrupt Enable Register (CGIE)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CGIE (Read)	0	0	0	0	1	0	1	0	0	0	0	0	0	G_IE2	G_IE1	0	xxxxmC12H[Note]	0A00H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CGIE (Write)	0	0	0	0	0	set G_IE2	set G_IE1	0	0	0	0	0	0	clear G_IE2	clear G_IE1	0

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) Read

Bit position	Bit name	Function
2	G_IE2	This is the invalid write access (to temporary buffer, etc.) interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
1	G_IE1	This is the unavailable memory address access interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled

(b) Write

Bit position	Bit name	Function
10, 9, 2, 1	set G_IEn, clear G_IEn	Sets/clears the G_IEn bit.

set G_IEn	clear G_IEn	Setting of G_IEn Bit
0	1	G_IEn bit cleared
1	0	G_IEn bit set
Other than above		No change

Remark n = 1, 2

(16) CAN main clock selection register (CGCS)

The CGCS register is used to select the main clock.

This register can be read/written in 16-bit units.

Figure 11-40. CAN Main Clock Selection Register (CGCS) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CGCS	CGTS7	CGTS6	CGTS5	CGTS4	CGTS3	CGTS2	CGTS1	CGTS0	GTCS1	GTCS0	0	0	MCP3	MCP2	MCP1	MCP0	xxxxmC14H[Note]	7F05H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit position	Bit name	Function
15 to 8	CGTS7 to CGTS0	Indicates global time system clock (f_{GTS})(see **Figure 11-41**).

n	CGTS7	CGTS6	CGTS5	CGTS4	CGTS3	CGTS2	CGTS1	CGTS0	System Timer Prescaler Selection $f_{GTS} = f_{GTS1} / (n + 1)$
0	0	0	0	0	0	0	0	0	$f_{GTS} = f_{GTS1}/1$
1	0	0	0	0	0	0	0	1	$f_{GTS} = f_{GTS1}/2$
					:				$f_{GTS} = f_{GTS1}/(n + 1)$
127	0	1	1	1	1	1	1	1	$f_{GTS} = f_{GTS1}/128$ (after reset)
					:				$f_{GTS} = f_{GTS1}/(n + 1)$
254	1	1	1	1	1	1	1	0	$f_{GTS} = f_{GTS1}/255$
255	1	1	1	1	1	1	1	1	$f_{GTS} = f_{GTS1}/256$

The global time system clock (f_{GTS}) is the source clock for the time stamp counter[Note] that is used for the time stamp function.

7, 6	GTCS1, GTCS0	Specifies the timer clock (f_{GTS1})(see **Figure 11-41**).

GTCS1	GTCS0	Global Timer Clock Selection (f_{GTS})
0	0	$f_{MEM}/2$
0	1	$f_{MEM}/4$
1	0	$f_{MEM}/8$
1	1	$f_{MEM}/16$

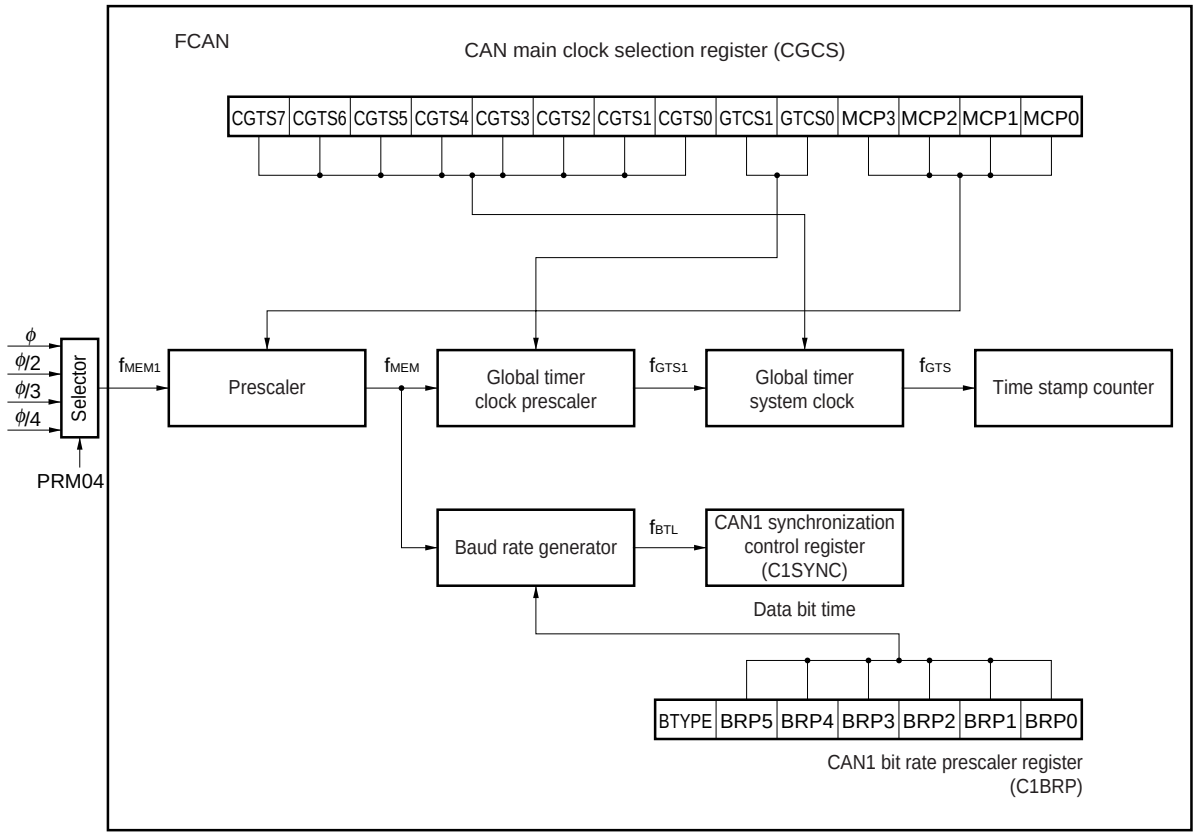
Note Refer to **11.10 (17) CAN time stamp count register (CGTSC).**

Figure 11-40. CAN Main Clock Selection Register (CGCS) (2/2)

Bit position	Bit name	Function
3 to 0	MCP3 to MCP0	Specifies the clock to memory access controller (f_{MEM})(see **Figure 11-41**).

n	MCP3	MCP2	MCP1	MCP0	Selection of Clock to Memory Access Controller (f_{MEM})
0	0	0	0	0	f_{MEM1}
1	0	0	0	1	$f_{MEM1}/2$
2	0	0	1	0	$f_{MEM1}/3$
			:		
14	1	1	1	0	$f_{MEM1}/15$
15	1	1	1	1	$f_{MEM1}/16$

Figure 11-41. FCAN Clocks



Caution When using a 1 Mbps transfer rate for the CPU, input f_{MEM1} as a 16 MHz clock signal. If input at another frequency, subsequent operation is not guaranteed.

(17) CAN time stamp count register (CGTSC)

The CGTSC register indicates the contents of the time stamp counter.

This register can be read at any time.

This register can be written to only when clearing bits. The clear function writes 0 to all bits in the CGTSC register.

This register is read-only in 16-bit units.

Figure 11-42. CAN Time Stamp Count Register (CGTSC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CGTSC	TSC15	TSC14	TSC13	TSC12	TSC11	TSC10	TSC9	TSC8	TSC7	TSC6	TSC5	TSC4	TSC3	TSC2	TSC1	TSC0	xxxxmC18H[Note]	0000H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(18) CAN message search start/result register (CGMSS (during write)/CGMSR (during read))

The CGMSS/CGMSR register indicates the message search start/result status. Messages in the message buffer that match the specified search criteria can be searched quickly (for example, a message for which the M_STATn register's DN bit is set (to 1) (n = 00 to 31)).

These registers can be read/written in 16-bit units.

Figure 11-43. CAN Message Search Start/Result Register (CGMSS (During Write)/CGMSR (During Read)) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
CGMSR (Read)	0	0	0	0	0	0	MM	AM	0	0	0	MFND4	MFND3	MFND2	MFND1	MFND0	xxxxmC1AH[Note]	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CGMSS (Write)	CIDE	0	CTRQ	CMSK	CDN	0	0	SMN0	0	0	0	STRT4	STRT3	STRT2	STRT1	STRT0

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed.

m = 2, 6, A, E

(a) Read

Bit Position	Bit Name	Function
9	MM	Confirms multiple hits from message search. 0: No messages or only one message meets the search criteria 1: Several messages meet the search criteria If several message buffers that meet search criteria are detected, the MM bit is set (to 1).
8	AM	Confirms hits from message search. 0: No messages meet the search criteria 1: At least one message meets the search criteria
4 to 0	MFND4 to MFND0	Indicates searched message number. 0 to 31: The number of the searched message

(b) Write

Bit Position	Bit Name	Function
15	CIDE	Checks message identifier (ID) format flag. 0: Message identifier format flag not checked 1: Message identifier format flag checked
13	CTRQ	Checks transmit request and message ready flag. 0: Transmit request and message ready flag not checked 1: Transmit request and message ready flag checked
12	CMSK	Checks masked messages. 0: Masked messages not checked 1: Masked messages checked

Figure 11-43. CAN Message Search Start/Result Register (CGMSS (During Write)/CGMSR (During Read)) (2/2)

(b) Write

Bit Position	Bit Name	Function
11	CDN	Checks status of the DN flag of M_STATn register. 0: Status not checked 1: Status checked
8	SMNO	Starts/stops search indicated by bits CIDE, CTRQ, CMSK, and CDN. 0: Search stopped 1: Search started
4 to 0	STRT4 to STRT0	Indicates message search start position. 0 to 31: Message number from which message search starts Search starts from the message number defined by bits STRT4 to STRT0. Search continues until it reaches the message buffer having the highest number among the usable message buffers. If the search results include several message buffer numbers among the matching messages, the message buffer with the lowest message buffer number is selected. To fetch the next message buffer number without changing the search criteria, “(MFND4 to MFND0) + 1” must be set as the values of bits STRT4 to STRT0.

(19) CAN1 address mask registers L0 to L3 and H0 to H3 (C1MASKL0 to C1MASKL3, SKH0 to C1MASKH3)

Registers C1MASKL0 to C1MASKL3 and C1MASKH0 to C1MASKH3 are used to extend the number of receivable messages by masking part of the messages' identifier (ID) and then ignoring the masked parts. These registers can be read/written in 16-bit units.

Figure 11-44. CAN1 Address Mask Registers L0 to L3 and H0 to H3 (C1MASKL0 to C1MASKL3 and C1MASKH0 to C1MASKH3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1MASKHn (n = 00-31)	CMIDE	0	0	CMID 28	CMID 27	CMID 26	CMID 25	CMID 24	CMID 23	CMID 22	CMID 21	CMID 20	CMID 19	CMID 18	CMID 17	CMID 16	See **Table 11-24**	Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1MASKLn (n = 00-31)	CMID 15	CMID 14	CMID 13	CMID 12	CMID 11	CMID 10	CMID 9	CMID 8	CMID 7	CMID 6	CMID 5	CMID 4	CMID 3	CMID 2	CMID 1	CMID 0	See **Table 11-23**	Undefined

Bit Position	Bit Name	Function
15 (C1MASKHn)	CMIDE	Sets mask for identifier (ID) bit. 0: ID format checked (standard or extended) 1: ID format not checked (standard or extended) When the CMID bit has been set (to 1), the high-order 11 bits of the ID are compared. There is no comparison between the received message's ID format and the ID format stored in the message buffer.
12 to 0 (C1MASKHn) 15 to 0 (C1MASKLn)	CMID28 to CMID16 (C1MASKHn) CMID15 to CMID0 (C1MASKLn)	Sets mask for identifier (ID) format. 0: ID bit in message buffer linked to bits CMID28 to CMID0 compared with received ID bit 1: ID bit in message buffer linked to bits CMID28 to CMID0 not compared (ID bit masked) with received ID bit Masks are always defined using an ID that is 29 bits in length. When a mask is assigned to a standard ID, the bits from CMID17 to CMID0 are ignored. Therefore, the received ID is masked only by bits CMID28 to CMID18. The same mask can be used for standard-format and extended-format IDs.

Remark n = 0 to 3

Table 11-23. Addresses of C1MASKLn (n = 00 to 31)

Register Name	Address[Note] (m = 2, 6, A, E)
C1MASKL0	xxxxmC40H
C1MASKL1	xxxxmC44H
C1MASKL2	xxxxmC48H
C1MASKL3	xxxxmC4CH

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

Table 11-24. Addresses of CIMASKHn (n = 00 to 3)

Register Name	Address (m = 3, 7, B)
C1MASKH0	xxxxmC42H
C1MASKH1	xxxxmC46H
C1MASKH2	xxxxmC4AH
C1MASKH3	xxxxmC4EH

Note CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

(20) CAN1 control register (C1CTRL)

The C1CTRL register is used to control the operation of the CAN module.

This register can be read/written in 16-bit units.

Cautions 1. Both bitwise writing and direct writing to the C1CTRL register are prohibited. Attempts to write directly to this register may result in operation faults, so be sure to follow the sequence described in 11.9 Caution Points on Bit Set/Clear Function.

2. When writing to the C1CTRL register, set or clear bits according to the register configuration during a write operation.

Figure 11-45. CAN1 Control Register (C1CTRL) (1/4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1CTRL (Read)	TECS1	TECS0	RECS1	RECS0	BOFF	TSTAT	RSTAT	ISTAT	0	DLEVR	DLEVT	OVM	TMR	STOP	SLEEP	INIT	xxxxmC50H[Note]	0101H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1CTRL (Write)	0	set DLEVR	set DLEVT	set OVM	set TMR	set STOP	set SLEEP	set INIT	0	clear DLEVR	clear DLEVT	clear OVM	clear TMR	clear STOP	clear SLEEP	clear INIT

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) Read (1/3)

Bit Position	Bit Name	Function
15, 14	TECS1, TECS0	This is the transmit error counter status flag.

TECS1	TECS0	Status of Transmit Error Counter
0	0	Transmit error counter value < 96
0	1	Transmit error counter value = 96 to 127 (warning level)
1	0	Not used
1	1	Transmit error counter value ≧ 128 (error passive)

Bit Position	Bit Name	Function
13, 12	ERCS1, RECS0	This is the receive error counter status flag.

RECS1	RECS0	Status of Receive Error Counter
0	0	Receive error counter value < 96
0	1	Receive error counter value = 96 to 127 (warning level)
1	0	Not used
1	1	Receive error counter value ≧ 128 (error passive)

Figure 11-45. CAN1 Control Register (C1CTRL) (2/4)

(a) Read (2/3)

Bit Position	Bit Name	Function
11	BOFF	This is the bus off status flag. 0: Transmit error counter < 256 (not bus off status) 1: Transmit error counter ≥ 256 (bus off status
10	TSTAT	This is the transmit status flag. 0: Transmission stopped status 1: Transmitting status
9	RSTT	This is the receive status flag. 0: Reception stopped status 1: Receiving status
8	ISTAT	This is the initialization status flag. 0: Normal operating status 1: FCAN is stopped and initialized **Cautions 1. The ISTAT bit is set (to 1) when the CAN protocol layer acknowledges the settings of the INIT and STOP bits. Also, this bit automatically cleared (to 0) when the INIT and STOP bits are cleared (to 0).** **2. In the initialization status, the error counter (see 11.10(23))is cleared and the error status (bits TECS1, TECS0, RECS0, RECS1) is reset.**
6	DLEVR	This is the dominant level control bit for receive pins. 0: Dominant = 0 (low level) 1: Dominant = 1 (high level)
5	DLEVT	This is the dominant level control bit for transmit pins. 0: Dominant = 0 (low level) 1: Dominant = 1 (high level)
4	OVM	This is the overwrite control bit. 0: New messages stored in message stored in which DN bit of M_STATn register (n = 00 to 31) is set 1: New messages in message buffer in which DN bit is set discarded.
3	TMR	This is the time stamp control bit for reception. 0: Captures time stamp counter value when SOF is sent via CAN bus 1: Captures time stamp counter value when EOF is sent via CAN bus (a valid message is confirmed)
2	STOP	This is the CAN stop mode control bit. 0: CAN sleep mode 1: CAN stop mode set The CAN stop mode can be selected only when the CAN module is set to CAN sleep mode (the SLEEP bit is set (to 1)). CAN stop mode can be released only by the CPU (STOP bit cleared (to 0)).

Caution Confirm that the ISTAT bit of the C1CTRL register has been set (to 1) before releasing the CAN stop mode. Also, be sure to release the CAN sleep mode at the same time.

Figure 11-45. CAN1 Control Register (C1CTRL) (3/4)

(a) Read (3/3)

Bit Position	Bit Name	Function
1	SLEEP	This is the CAN sleep mode control bit. 0: Normal operation 1: Switch to CAN sleep mode. Change in CAN bus performs wake-up. **Cautions 1. CAN sleep mode is c released under the following conditions.** **• When the CPU has cleared the SLEEP bit (to 0)** **• When the CAN bus changes (only when CAN stop mode has not been set)** **2. The WAKE bit (see 11.10 (21) CAN1 definition register (C1DEF)) can be set (to 1) only when CAN sleep mode is released by the change of the CAN bus.**
0	INIT	This is the initialization request bit used to initialize the CAN module. 0: Normal operation mode 1: Initialization mode **Cautions 1. Be sure to confirm that the CAN module has entered the initialization mode using the ISTAT bit (ISTAT bit (1) after setting the INIT bit (to 1). When the ISTAT bit = 0, set the INIT bit (to 1) again.** **2. "Recessive" is output via the CANTX pin in initialization mode.** **3. The C1SYNC and C1BRP registers can be written only in initialization mode.** **4. The error counter (see 11.10 (23) CAN1 error counter register (C1ERC))is cleared and the error status (TECS1, TECS0, RECS1, RECS0) is reset in initialization mode.** **5. If the INIT bit is set (to 1) in the bus off status (BOFF bit = 1), the ISTAT bit will not be 1.**

(b) Write (1/2)

Bit Position	Bit Name	Function
14, 6	Set DLEVR, clear DLEVR	Sets/clears the DLEVR bit.

set DLEVR	clear DLEVR	DLEVR Bit Setting
0	1	DLEVR bit cleared (to 0)
1	0	DLEVR bit set (to 1)
Other than above		DLEVR bit not changed

Bit Position	Bit Name	Function
13, 5	Set DLEVT, clear DLEVT	Sets/clears the DLEVT bit.

set DLEVT	clear DLEVT	DLEVT Bit Setting
0	1	DLEVT bit cleared (to 0)
1	0	DLEVT bit set (to 1)
Other than above		DLEVT bit not changed

Figure 11-45. CAN1 Control Register (C1CTRL) (4/4)

(b) Write (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>12, 4</td><td>OVM</td><td>Sets/clears the OVM bit.
<table>
<tr><th>set OVM</th><th>clear OVM</th><th>OVM Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>OVM bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>OVM bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>OVM bit not changed</td></tr>
</table></td></tr>
<tr><td>11, 3</td><td>set TMR,
clear TMR</td><td>Sets/clears the TMR bit.
<table>
<tr><th>set TMR</th><th>clear TMR</th><th>TMR Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>TMR bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>TMR bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>Stop bit not changed</td></tr>
</table></td></tr>
<tr><td>10, 2</td><td>set STOP,
clear STOP</td><td>Sets/clears the STOP bit.
<table>
<tr><th>set STOP</th><th>clear STOP</th><th>STOP Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>STOP bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>STOP bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>STOP bit not changed</td></tr>
</table></td></tr>
<tr><td>9, 1</td><td>set SLEEP,
clear SLEEP</td><td>Sets/clears the SLEEP bit.
<table>
<tr><th>set SLEEP</th><th>clear SLEEP</th><th>SLEEP Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>SLEEP bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>SLEEP bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>SLEEP bit not changed</td></tr>
</table></td></tr>
<tr><td>8, 0</td><td>set INIT,
clear INIT</td><td>/clears the INIT bit.
<table>
<tr><th>set INIT</th><th>clear INIT</th><th>INIT Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>INIT bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>INIT bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>INIT bit not changed</td></tr>
</table></td></tr>
</table>

(21) CAN1 definition register (C1DEF)

The C1DEF register is used to define the operation of the CAN module.

This register can be read in 16-bit or 8-bit units and written in 16-bit units.

Cautions 1. Both bitwise writing and direct writing to the C1DEF register are prohibited. Attempts to write directly to this register may result in operation faults, so be sure to follow the sequence described in 11.9 Caution Points on Bit Set/Clear Function.

2. When writing to the C1DEF register, set or clear bits according to the register configuration during a write operation.

Figure 11-46. CAN1 Definition Register (C1DEF) (1/4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1DEF (Read)	0	0	0	0	0	0	0	0	DGM	MOM	SSHT	PBB	BERR	VALID	WAKE	OVR	xxxxmC52H[Note]	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1DEF (Write)	set DGM	set MOM	set SSHT	set PBB	0	0	0	0	clear DGM	clear MOM	clear SSHT	clear PBB	clear BERR	clear VALID	clear WAKE	clear OVR

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) Read (1/3)

Bit Position	Bit Name	Function
7	DGM	Specifies diagnostic processing mode. 0: Valid messages received using diagnostic mode (Bits MT2 to MT0 of M_CONF register = 111) 1: Valid messages received using normal operation mode. The diagnostic processing mode (MOM bit = 1) is used for CAN baud rate detection and for diagnostic purposes. When this mode has been set, the following operations are performed. • When the VALID bit = 1, it indicates that the current receive operation is valid. • Setting the DGM bit confirms whether or not valid data has been stored in the message buffer used for diagnostics. The CAN protocol layer does not sent ACK, error frame, or transmit messages, nor does it operate an error counter.

Figure 11-46. CAN1 Definition Register (C1DEF) (2/4)

(a) Read (2/3)

Bit Position	Bit Name	Function
6	MOM	Specifies the CAN module operation mode. 0: Normal operating mode 1: Diagnostic processing mode **Cautions 1. The CAN bit rate prescaler register (C1BRP) can be accessed only when the CAN module is in initialization mode (C1CTRL register's ISTAT bit = INIT bit = 1) during normal operating mode (MOM bit = 0). Also, the CAN1 bus diagnostic information register (refer to 11. 10 (27) CAN1 bus diagnostic information register (C1DINF)) cannot be used in normal operating mode.** **2. When in diagnostic mode (MOM bit = 1), the C1BRP register can be accessed only when the CAN module has been set to initialization mode (i.e., when the C1CTRL register's ISTAT bit = INIT bit = 1). When the CAN module is operating (i.e., when the C1CTRL register's ISTAT bit = 0) the C1BRP register cannot be used, and the C1DINF register can be used instead.**
5	SSHT	Specifies single shot mode. 0: Normal operating mode 1: Single shot mode In single shot mode, the CAN module can transmit a message only one time. The M_STATa (a = 00 to 31) register's TRQ bit is then cleared (to 0) regardless of whether or not there are any pending normal transmit operations. Also, if a bus error has occurred due to a transmission, it is handled as an incomplete transmission. **Cautions 1. In single shot mode, even if the CAN bus is cut off and transmission is stopped during the arbitration phase, it is handled as a completed message transmission.** **When in this mode, the BERR bit is set (to 1) but the error counter value (refer to 11.10 (23) CAN1 bus error counter register (C1ERC) does not change since there are no CAN bus errors.** **2. During the time when the CAN module is active, the CPU switches between normal operation mode and single shot mode without causing any errors to occur on the CAN bus.**
4	PBB	Specifies priority control for transmission. 0: Identifier (ID) based priority control 1: Message number based priority control Ordinarily, priority for transmission is defined based on message IDs, but when the PBB bit has been set (to 1) priority becomes based instead on the position of messages, so that messages with lower message numbers have higher priority.
3	BERR	Indicates CAN bus error status. 0: CAN bus error was not detected 1: CAN bus error was detected at least once after bit was cleared
2	VALID	Indicates valid message detection status. 0: Valid message was not detected 1: Valid message was detected at least once after bit was cleared

Figure 11-46. CAN1 Definition Register (C1DEF) (3/4)

(a) Read (3/3)

Bit Position	Bit Name	Function
1	WAKE	Indicates CAN sleep mode release status. 0: Normal operation 1: CAN sleep mode released **Cautions 1. The WAKE bit is set (to 1) when the CAN bus active status is detected in CAN sleep mode and an error interrupt occurs.** **2. When the WAKE bit is set (to 1), the error interrupt signal remains active and must be cleared (to 0) by the CPU after the CPU becomes aware of this bit setting.**
0	OVR	Indicates overrun error status. 0: Normal operation 1: Overrun occurred during RAM access **Caution When an overrun error has occurred, the OVR bit is set (to 1) and an error interrupt occurs at the same time.** **The source of the overrun error may be that the RAM access clock is slower than the selected CAN baud rate.**

(b) Write (1/2)

Bit Position	Bit Name	Function
15, 7	set DGM, clear DGM	Sets/clears the DGM bit.
14, 6	set MOM, clear MOM	Sets/clears the MOM bit.
13, 5	set SSHT, clear SSHT	Sets/clears the SSHT bit.

set DGM	clear DGM	DGM Bit Setting
0	1	DGM bit cleared (to 0)
1	0	DGM bit set (to 1)
Other than above		DGM bit not changed

set MOM	clear MOM	MOM Bit Setting
0	1	MOM bit cleared (to 0)
1	0	MOM bit set (to 1)
Other than above		MOM bit not changed

set SSHT	clear SSHT	SSHT Bit Setting
0	1	SSHT bit cleared (to 0)
1	0	SSHT bit set (to 1)
Other than above		SSHT bit not changed

Figure 11-46. CAN1 Definition Register (C1DEF) (4/4)

(b) Write (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>12, 4</td><td>set PBB,
clear PBB</td><td>Sets/clears the PBB bit.
<table>
<tr><th>set PBB</th><th>clear PBB</th><th>PBB Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>PBB bit cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>PBB bit set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>PBB bit not changed</td></tr>
</table></td></tr>
<tr><td>3</td><td>clear
BERR</td><td>Clears the BERR bit.
0: No change in BERR bit
1: BERR bit cleared (to 0)</td></tr>
<tr><td>2</td><td>clear
VALID</td><td>Clears the VALID bit.
0: No change in VALID bit
1: VALID bit cleared (to 0)</td></tr>
<tr><td>1</td><td>clear
WAKE</td><td>Clears the WAKE bit.
0: No change in WAKE bit
1: WAKE bit cleared (to 0)</td></tr>
<tr><td>0</td><td>clear OVR</td><td>Clears the OVR bit.
0: No change in OVR bit
1: OVR bit cleared (to 0)</td></tr>
</table>

(22) CAN1 information register (C1LAST)

The C1LAST register indicates the CANn module's error information.

This register is read-only in 16-bit units.

Figure 11-47. CAN1 Information Register (C1LAST)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1LAST	0	0	0	0	LERR3	LERR2	LERR1	LERR0	LREC7	LREC6	LREC5	LREC4	LREC3	LREC2	LREC1	LREC0	xxxxmC54H[Note]	00FFH

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
11 to 8	LERR3 to LERR0	Indicates the last error information.
7 to 0	LREC7 to LREC0	Indicates the last received message number. 0 to 31: The number of the message buffer last received 32 to 255: Not used

LERR3	LERR2	LERR1	LERR0	Last Error Information
0	0	0	0	Error not detected
0	0	0	1	Bit error
0	0	1	0	Stuff error
0	0	1	1	CRC error
0	1	0	0	Form error
0	1	0	1	Acknowledge error
0	1	1	0	Arbitration lost (only in single shot mode) (C1DEF register's SSHT bit = 1)
0	1	1	1	CAN overrun error
1	0	0	0	Wake-up from CAN bus
Other than above				Undefined

Caution Since the LERR3 to LERR0 bits cannot be cleared, the current status is retained until the next error occurs.

(23) CAN1 error counter register (C1ERC)

The C1ERC register indicates the count values of the transmission/reception error counters.
This register is read-only in 16-bit units.

Figure 11-48. CAN1 Error Counter Register (C1ERC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1ERC	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0	xxxxmC56H[Note]	0000H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
15 to 8	REC7 to REC0	Indicates the reception error count. 0 to 255: The number of reception errors This reflects the current status of the reception error counter. The number of counts is defined by the CAN protocol.
7 to 0	TEC7 to TEC0	Indicates the transmission error count. 0 to 255: The number of transmission errors This reflects the current status of the transmission error counter. The number of counts is defined by the CAN protocol.

(24) CAN1 interrupt enable register (C1IE)

The C1IE register is used to enable/disable the CAN module's interrupts.

This register can be read in 16-bit or 8-bit units and written in 16-bit units.

Cautions 1. Both bitwise writing and direct writing to the C1IE register are prohibited. Attempts to write directly to this register may result in operation faults, so be sure to follow the sequence described in 11.9 Caution Points on Bit Set/Clear Function.

2. When writing to the CnIE register, set or clear bits according to the register configuration during a write operation.

Figure 11-49. CAN1 Interrupt Enable Register (C1IE) (1/3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1IE (Read)	0	0	0	0	1	0	0	1	0	E_INT6	E_INT5	E_INT4	E_INT3	E_INT2	E_INT1	E_INT0	xxxxmC58H[Note]	0900H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1IE (Write)	0	set E_INT6	set E_INT5	set E_INT4	set E_INT3	set E_INT2	set E_INT1	set E_INT0	0	clear E_INT6	clear E_INT5	clear E_INT4	clear E_INT3	clear E_INT2	clear E_INT1	clear E_INT0

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) Read

Bit Position	Bit Name	Function
6	E_INT6	This is the CAN error interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
5	E_INT5	This is the CAN bus error interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
4	E_INT4	This is the wake up from CAN sleep mode interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
3	E_INT3	This is the receive error passive interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
2	E_INT2	This is the transmit error passive or bus off interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
1	E_INT1	This is the receive completion interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled
0	E_INT0	This is the transmit completion interrupt enable flag. 0: Interrupt disabled 1: Interrupt enabled

Figure 11-49. CAN1 Interrupt Enable Register (C1IE) (2/3)

(b) Write (1/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>14, 6</td><td>set E_INT6, clear E_INT6</td><td>Sets/clears the E_INT6 bit.
<table>
<tr><th>set E_INT6</th><th>clear E_INT6</th><th>E_INT6 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT6 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT6 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT6 interrupt not changed</td></tr>
</table></td></tr>
<tr><td>13, 5</td><td>set E_INT5, clear E_INT5</td><td>Sets/clears the E_INT5 bit.
<table>
<tr><th>set E_INT5</th><th>clear E_INT5</th><th>E_INT5 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT5 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT5 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT5 interrupt not changed</td></tr>
</table></td></tr>
<tr><td>12, 4</td><td>set E_INT4, clear E_INT4</td><td>Sets/clears the E_INT4 bit.
<table>
<tr><th>set E_INT4</th><th>clear E_INT4</th><th>E_INT4 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT4 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT4 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT4 interrupt not changed</td></tr>
</table></td></tr>
<tr><td>11, 3</td><td>set E_INT3, clear E_INT3</td><td>Sets/clears the E_INT3 bit.
<table>
<tr><th>set E_INT3</th><th>clear E_INT3</th><th>E_INT3 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT3 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT3 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT3 interrupt not changed</td></tr>
</table></td></tr>
<tr><td>10, 2</td><td>set E_INT2, clear E_INT2</td><td>Sets/clears the E_INT2 bit.
<table>
<tr><th>set E_INT2</th><th>clear E_INT2</th><th>E_INT2 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT2 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT2 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT2 interrupt not changed</td></tr>
</table></td></tr>
<tr><td>9, 1</td><td>set E_INT1, clear E_INT1</td><td>Sets/clears the E_INT1 bit.
<table>
<tr><th>set E_INT1</th><th>clear E_INT1</th><th>E_INT1 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT1 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT1 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT1 interrupt not changed</td></tr>
</table></td></tr>
</table>

Figure 11-49. CANn Interrupt Enable Register (CnIE) (3/3)

(b) Write (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>8, 0</td><td>set E_INT0, clear E_INT0</td><td>Sets/clears the E_INT0 bit.
<table>
<tr><th>set E_INT0</th><th>clear E_INT0</th><th>E_INT0 Bit Setting</th></tr>
<tr><td>0</td><td>1</td><td>E_INT0 interrupt cleared (to 0)</td></tr>
<tr><td>1</td><td>0</td><td>E_INT0 interrupt set (to 1)</td></tr>
<tr><td colspan="2">Other than above</td><td>E_INT0 interrupt not changed</td></tr>
</table></td></tr>
</table>

(25) CAN1 bus active register (C1BA)

The C1BA register indicates frame information output via the CAN bus.

This register is read-only in 16-bit units.

Figure 11-50. CAN1 Bus Active Register (C1BA)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1BA	0	0	0	CACT4	CACT3	CACT2	CACT1	CACT0	TMNO7	TMNO6	TMNO5	TMNO4	TMNO3	TMNO2	TMNO1	TMNO0	xxxxmC5AH[Note]	00FFH

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
12 to 8	CACT4 to CACT0	Indicates CAN module status.
7 to 0	TMNO7 to TMNO0	Specifies transmit message counter. 0 to 31: Message number of message awaiting transmission or being transmitted 32 to 254: Not used 255: No messages awaiting transmission or being transmitted

CACT4	CACT3	CACT2	CACT1	CACT0	CAN Module Status
0	0	0	0	0	Reset state
0	0	0	0	1	Bus idle wait
0	0	0	1	0	Bus idle state
0	0	0	1	1	Start of frame
0	0	1	0	0	Standard identifier area
0	0	1	0	1	Data length code area
0	0	1	1	0	Data field area
0	0	1	1	1	CRC field area
0	1	0	0	0	CRC delimiter
0	1	0	0	1	ACK slot
0	1	0	1	0	ACK delimiter
0	1	0	1	1	End of frame area
0	1	1	0	0	Intermission state
0	1	1	0	1	Suspend transmission
0	1	1	1	0	Error frame
0	1	1	1	1	Error delimiter wait
1	0	0	0	0	Error delimiter
1	0	0	0	1	Bus off error
1	0	0	1	0	Extended identifier area
Other than above					Setting prohibited

(26) CAN1 bit rate prescaler register (C1BRP)

The C1BRP register is used to set the transmission baud rate for the CAN module.

Use the C1BRP register to select the CAN protocol layer main system clock (f_{BTL}). The baud rate is set by the C1BRP register and the C1SYNC register.

While in normal operation mode (C1DEF register's MOM bit = 0), writing to the C1BRP register is enabled only when initialization mode has been set (C1CTRL register's INIT bit = 1).

This register can be read/written in 16-bit units.

Caution While in diagnostic mode (C1DEF register's MOM bit = 1), the C1BRP register can only be accessed when the initialization mode has been set (C1CTRL register's INIT bit = 1) (refer to 11.10 (21) CAN1 definition register (C1DEF)).

Figure 11-51. CAN1 Bit Rate Prescaler Register (C1BRP) (1/2)

C1BRP (TLM = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
TLM	0	0	0	0	0	0	0	0	BTYPE	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	xxxxmC5CH[Note]	0000H

C1BRP (TLM = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLM	0	0	0	0	0	0	BTYPE	BRP7	BRP6	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

(a) When TLM = 0

Bit Position	Bit Name	Function
15	TLM	Specifies transfer layer mode. 0: 6-bit prescaler mode 1: 8-bit prescaler mode
8	BTYPE	Specifies CAN bus type. 0: Low speed (≤ 125 kbps) 1: High speed (> 125 kbps)
7 to 0	BRP7 to BRP0	Specifies CAN protocol layer main system clock (f_{BTL}) for CAN module

n	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	CAN Protocol Layer Main System Clock (f_{BTL})
0	0	0	0	0	0	0	$f_{MEM}/2$
1	0	0	0	0	0	1	$f_{MEM}/4$
2	0	0	0	0	1	0	$f_{MEM}/5$
3	0	0	0	0	1	1	$f_{MEM}/8$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
60	1	1	1	1	0	0	$f_{MEM}/122$
61	1	1	1	1	0	1	$f_{MEM}/124$
62	1	1	1	1	1	0	$f_{MEM}/126$
63	1	1	1	1	1	1	$f_{MEM}/128$

Remark $f_{BTL} = f_{MEM} / \{(n + 1) \times 2\}$: CAN protocol layer main system clock
n = 00 to 63 (set by bits BRP5 to BRP0)
f_{MEM} = CAN module clock

Figure 11-51. CAN1 Bit Rate Prescaler Register (C1BRP) (2/2)

(b) When TLM = 1

Bit Position	Bit Name	Function
15	TLM	Specifies transfer layer mode. 0: 6-bit prescaler mode 1: 8-bit prescaler mode
8	BTYPE	Specifies CAN bus type. 0: Low speed (≤ 125 kbps) 1: High speed (> 125 kbps)
7 to 0	BRP7 to BRP0	Specifies CAN protocol layer main system clock (f_{BTL}) for CAN module

n	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	CAN Protocol Layer Main System Clock (f_{BTL})
0	0	0	0	0	0	0	Setting Prohibited
1	0	0	0	0	0	1	$f_{MEM}/2$
2	0	0	0	0	1	0	$f_{MEM}/3$
3	0	0	0	0	1	1	$f_{MEM}/4$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
252	1	1	1	1	0	0	$f_{MEM}/253$
253	1	1	1	1	0	1	$f_{MEM}/254$
254	1	1	1	1	1	0	$f_{MEM}/255$
255	1	1	1	1	1	1	$f_{MEM}/256$

Remark $f_{BTL} = f_{MEM} / (n + 1)$: CAN protocol layer main system clock
n = 00 to 255 (set by bits BRP7 to BRP0)
f_{MEM} = CAN module clock

(27) CAN1 bus diagnostic information register (C1DINF)

The C1DINF register indicates diagnostic information (all CAN bus bits, including stuff bits, delimiters, etc.). This information is used only for diagnostic purposes.

This register is read-only in 16-bit units.

Cautions 1. While in diagnostic mode (C1DEF register's MOM bit = 1) and in normal operation mode (C1CTRL register's INIT bit = 0), the C1DINF register can only be accessed when the initialization mode has been set (C1DEF register's MOM bit = 0).

2. Storage of the last 8 bits is automatically stopped if an error or a normal message (Ack delimiter) is detected on the CAN bus. Storage is automatically started when the SOF is detected on the CAN bus.

Figure 11-52. CAN1 Bus Diagnostic Information Register (C1DINF)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1DINF	DINF15	DINF14	DINF13	DINF12	DINF11	DINF10	DINF9	DINF8	DINF7	DINF6	DINF5	DINF4	DINF3	DINF2	DINF1	DINF0	xxxxmC5CH[Note]	0000H

Note xxxx: CAN message buffer registers can be allocated to the xxxx addresses as programmable peripheral I/O registers. Note, however, that the xxxx addresses cannot be changed after being set.

m = 2, 6, A, E

Bit Position	Bit Name	Function
15 to 0	DINF15 to DINF0	Indicates CAN bus diagnostic information.

Bit Name	CAN Bus Diagnostic Information
DINF15 to DINF08	No. of bits starting from SOF
DINF7 to DINF0	Information from last 8 bits

(28) CAN1 synchronization control register (C1SYNC)

The C1SYNC register controls the data bit time for transmission speed.

This register can be read/written in 16-bit units.

Cautions 1. The CPU is able to read the C1SYNC register at any time.

2. Writing to the C1SYNC register is enabled when in initialization mode (when C1CTRL register's INIT bit = 1).

3. The limit values when setting the SPTn bit and DBTn bit are as follows.

2 ≦ SPT (sampling point) ≦ 16

7 ≦ DBT (data bit time) ≦ 24

SJW (reSynchronization Jump Width: baud rate shift tolerance period) < (DBT – SPT)

2 ≦ (DBT - SPT) ≦ 8

Also, make sure all settings are within the range shown below to ensure compliance with the CAN protocol specification.

1 ≦ (2 x SPT - DBT) ≦ 8

Figure 11-53. CAN1 Synchronization Control Register (C1SYNC) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
C1SYNC	0	0	0	SAMP	SJW1	SJW0	SPT4	SPT3	SPT2	SPT1	SPT0	DBT4	DBT3	DBT2	DBT1	DBT0	xxxxmC5EH[Note]	0218H

Bit Position	Bit Name	Function
12	SAMP	Specifies bit sampling. 0: Receive data sampled once at the sampling point. 1: Receive data sampled three times and the majority value used as the sampled value.
11, 10	SJW1, SJW0	Specifies syhcronization jump width stipulated in the CAN protocol specification, Ver. 2.0, part B.

SJW1	SJW0	Synchronization Jump Width
0	0	$f_{BTL} \times 1$
0	1	$f_{BTL} \times 2$
1	0	$f_{BTL} \times 3$
1	1	$f_{BTL} \times 4$

Remark f_{BTL}: CAN protocol layer main system clock

Figure 11-53. CAN1 Synchronization Control Register (C1SYNC) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>9 to 5</td><td>SPT4 to SPT0</td><td>Specifies position of sampling points.
<table>
<tr><th>SPT4</th><th>SPT3</th><th>SPT2</th><th>SPT1</th><th>SPT0</th><th>Position of Sampling Point</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>$f_{BTL} \times 3$</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>$f_{BTL} \times 4$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>$f_{BTL} \times 5$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>$f_{BTL} \times 6$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>$f_{BTL} \times 7$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>$f_{BTL} \times 8$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>$f_{BTL} \times 9$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>$f_{BTL} \times 10$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>$f_{BTL} \times 11$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>$f_{BTL} \times 12$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>$f_{BTL} \times 13$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>$f_{BTL} \times 14$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>$f_{BTL} \times 15$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>$f_{BTL} \times 16$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>$f_{BTL} \times 17$</td></tr>
<tr><td colspan="5">Other than above</td><td>Setting prohibited</td></tr>
</table>
Remark Sampling point within bit timing is selected.</td></tr>
<tr><td>4 to 0</td><td>DBT4 to DBT0</td><td>Sets data bit time.
<table>
<tr><th>DBT4</th><th>DBT3</th><th>DBT2</th><th>DBT1</th><th>DBT0</th><th>Data Bit Time</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>$f_{BTL} \times 8$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>$f_{BTL} \times 9$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>$f_{BTL} \times 10$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>$f_{BTL} \times 11$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>$f_{BTL} \times 12$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>$f_{BTL} \times 13$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>$f_{BTL} \times 14$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>$f_{BTL} \times 15$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>$f_{BTL} \times 16$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>$f_{BTL} \times 17$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>$f_{BTL} \times 18$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>$f_{BTL} \times 19$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>$f_{BTL} \times 20$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>$f_{BTL} \times 21$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>$f_{BTL} \times 22$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>$f_{BTL} \times 23$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>$f_{BTL} \times 24$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>$f_{BTL} \times 25$</td></tr>
<tr><td colspan="5">Other than above</td><td>Setting prohibited</td></tr>
</table>
Remark 1-bit length is set for CAN bus</td></tr>
</table>

Remark f_{BTL}: CAN protocol layer main system clock

11.11 Operations

11.11.1 Initialization processing

Figure 11-54 shows a flowchart of initialization processing. The register setting flow is shown in Figures 11-55 to 11-64.

Figure 11-54. Initialization Processing

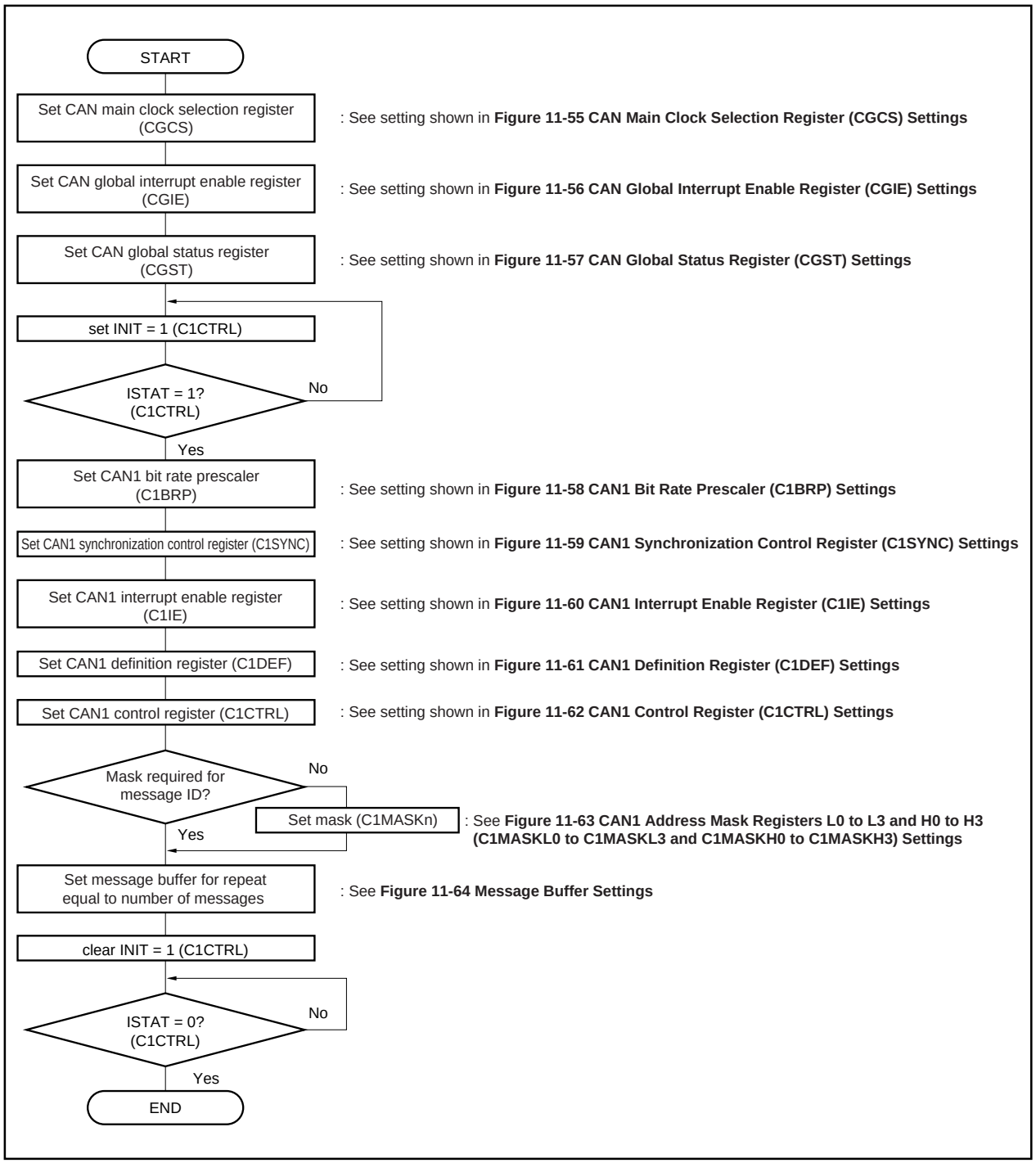
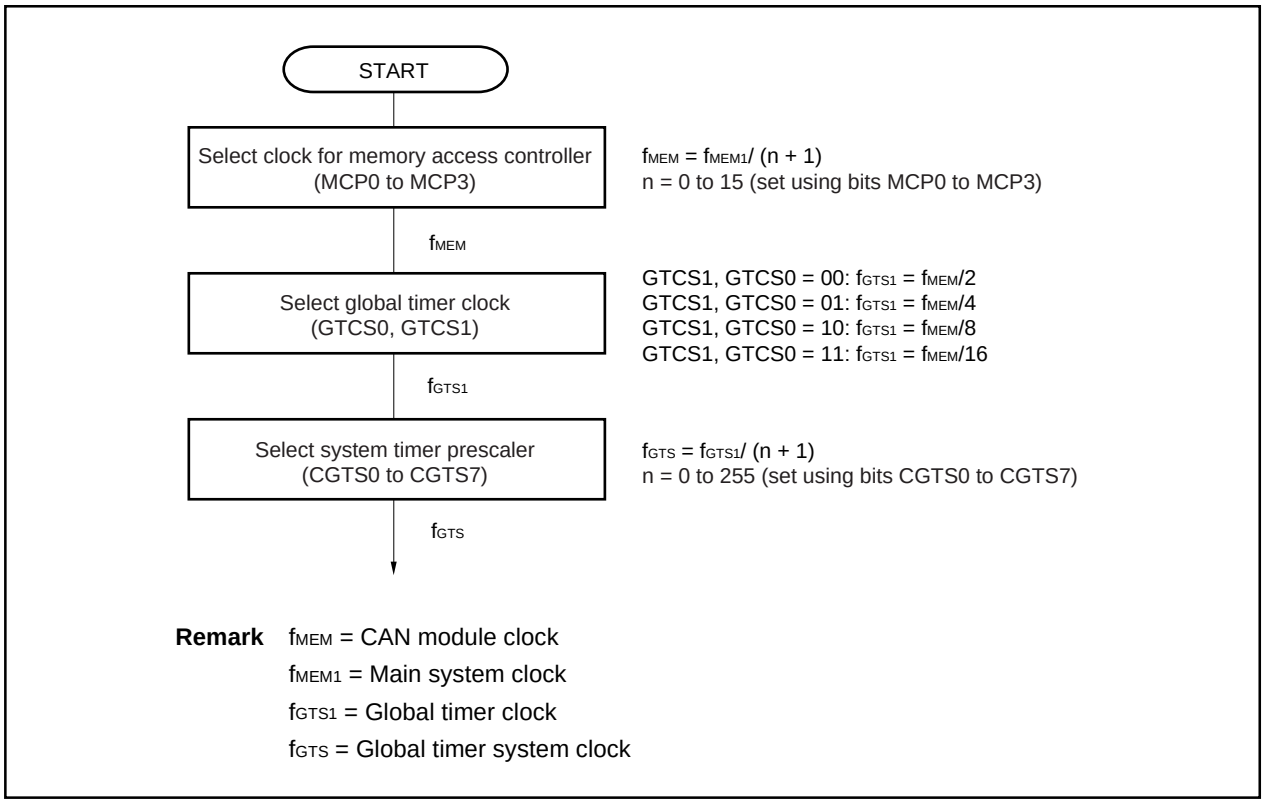


Figure 11-55. CAN Main Clock Selection Register (CGCS) Settings



Remark f_{MEM} = CAN module clock
f_{MEM1} = Main system clock
f_{GTS1} = Global timer clock
f_{GTS} = Global timer system clock

Figure 11-56. CAN Global Interrupt Enable Register (CGIE) Settings

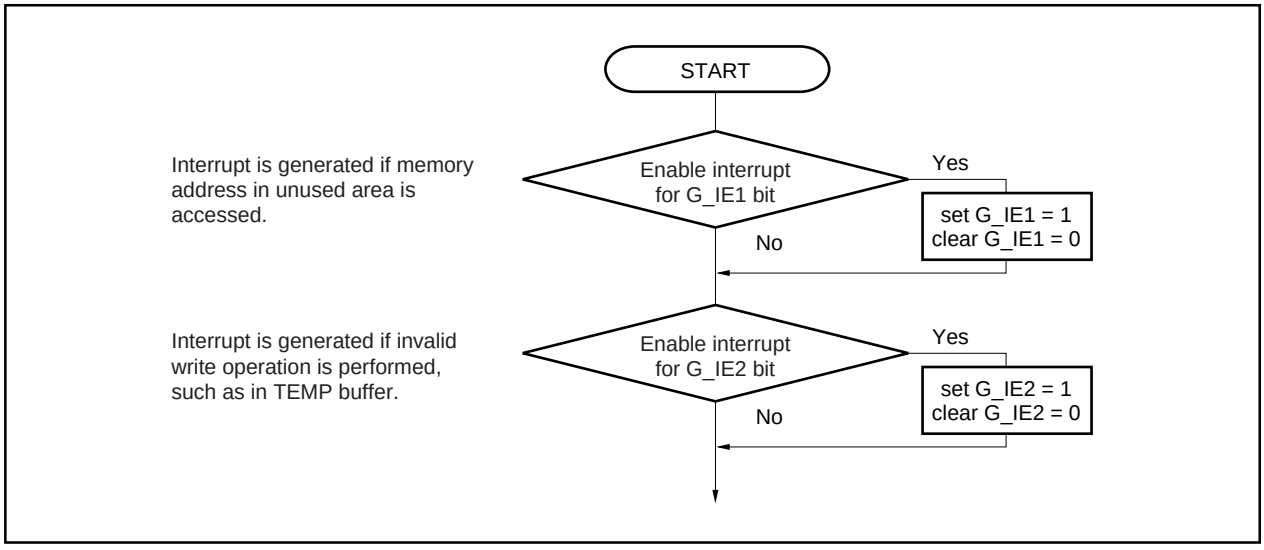


Figure 11-57. CAN Global Status Register (CGST) Settings

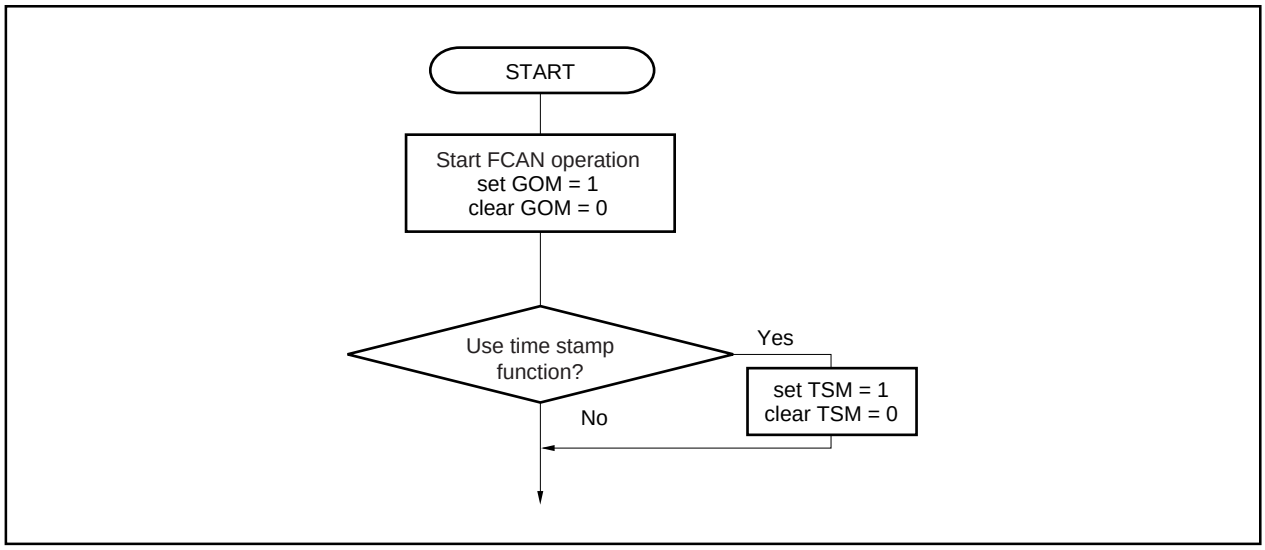
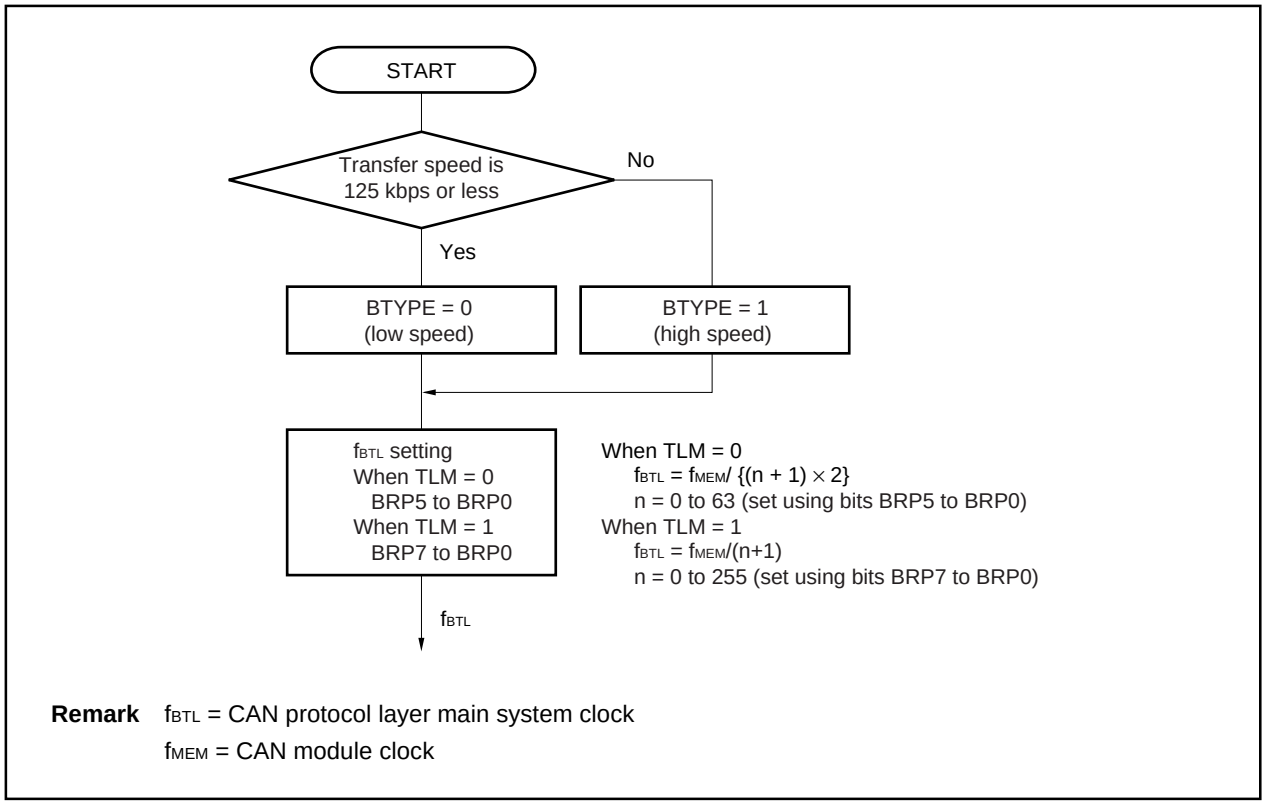
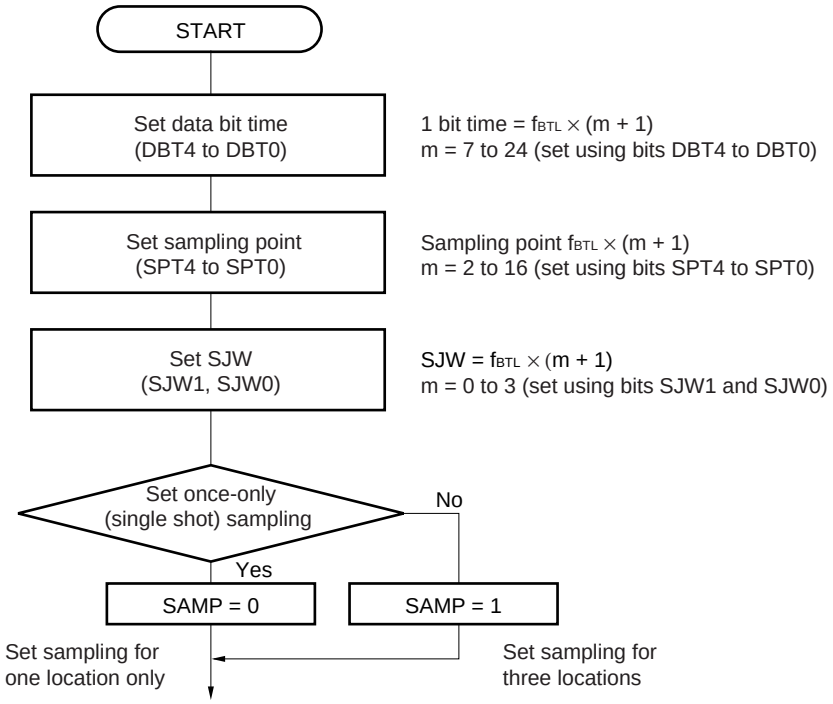


Figure 11-58. CAN1 Bit Rate Prescaler (C1BRP) Settings



Remark f_{BTL} = CAN protocol layer main system clock
f_{MEM} = CAN module clock

Figure 11-59. CAN1 Synchronization Control Register (C1SYNC) Settings



Remark f_{BTL} = CAN protocol layer main system clock

Figure 11-60. CAN1 Interrupt Enable Register (C1IE) Settings

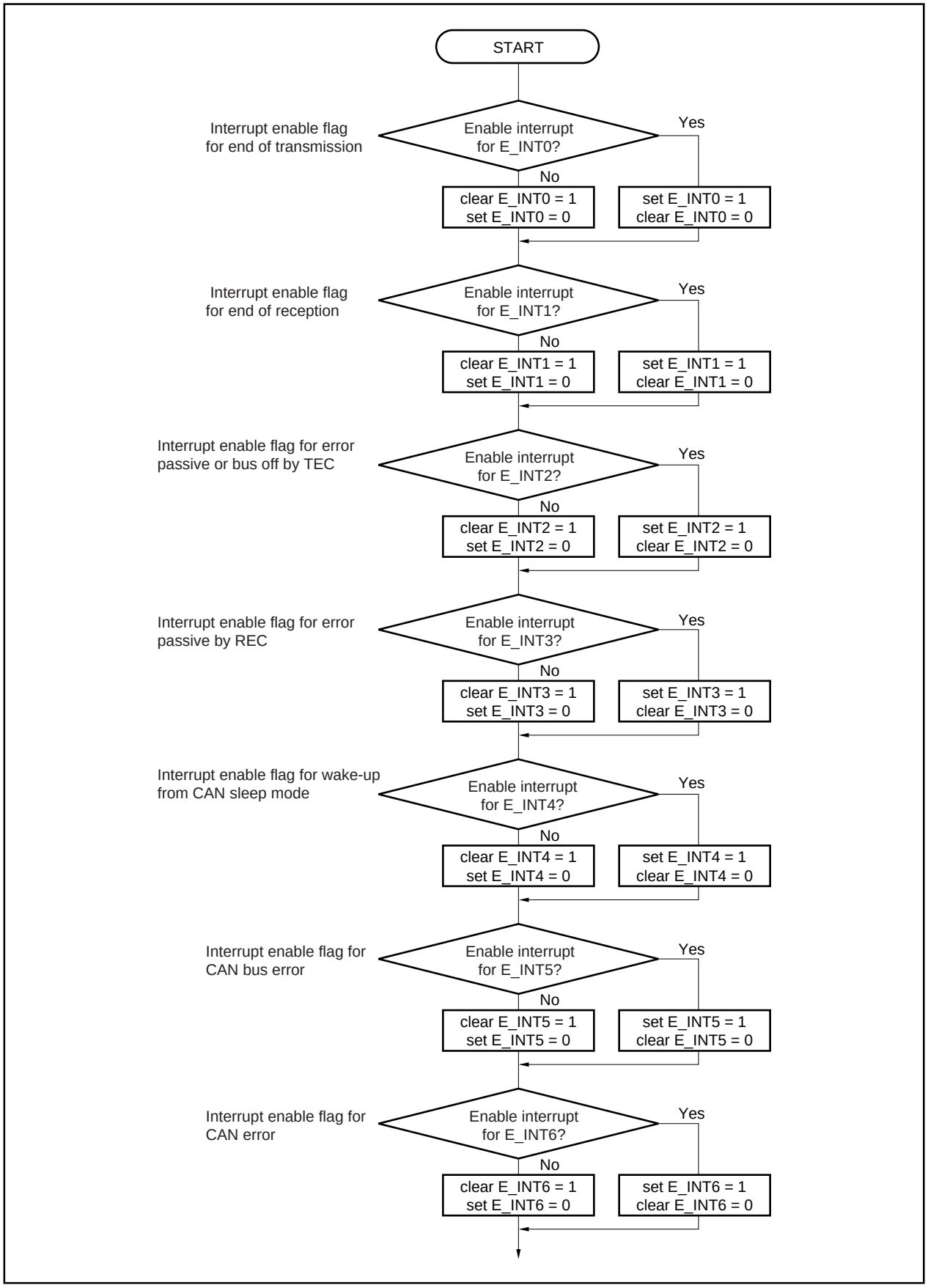
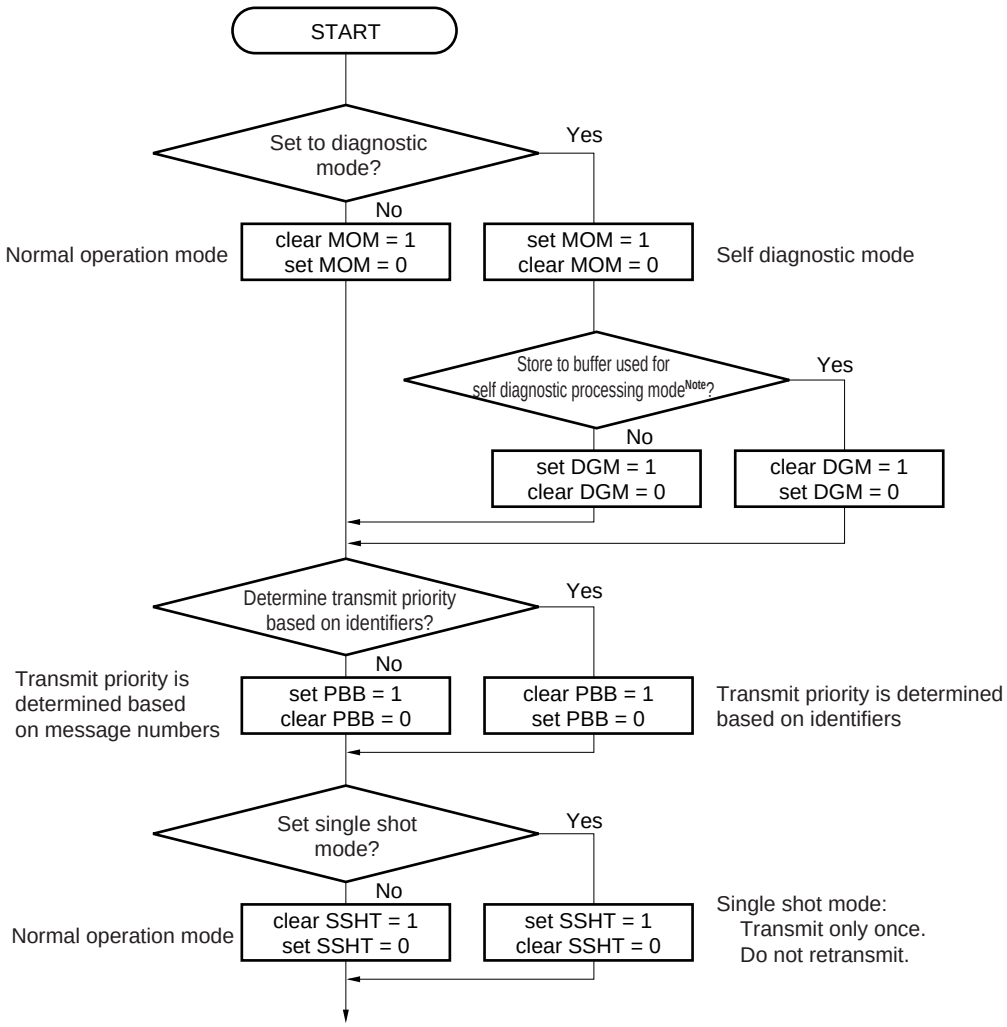


Figure 11-61. CAN1 Definition Register (C1DEF) Settings



Note Bits 5 to 3 (MT2 to MT0) in CAN message configuration register n (M_CONFn) (n = 00 to 31) are set as “111”

Figure 11-62. CAN1 Control Register (C1CTRL) Settings

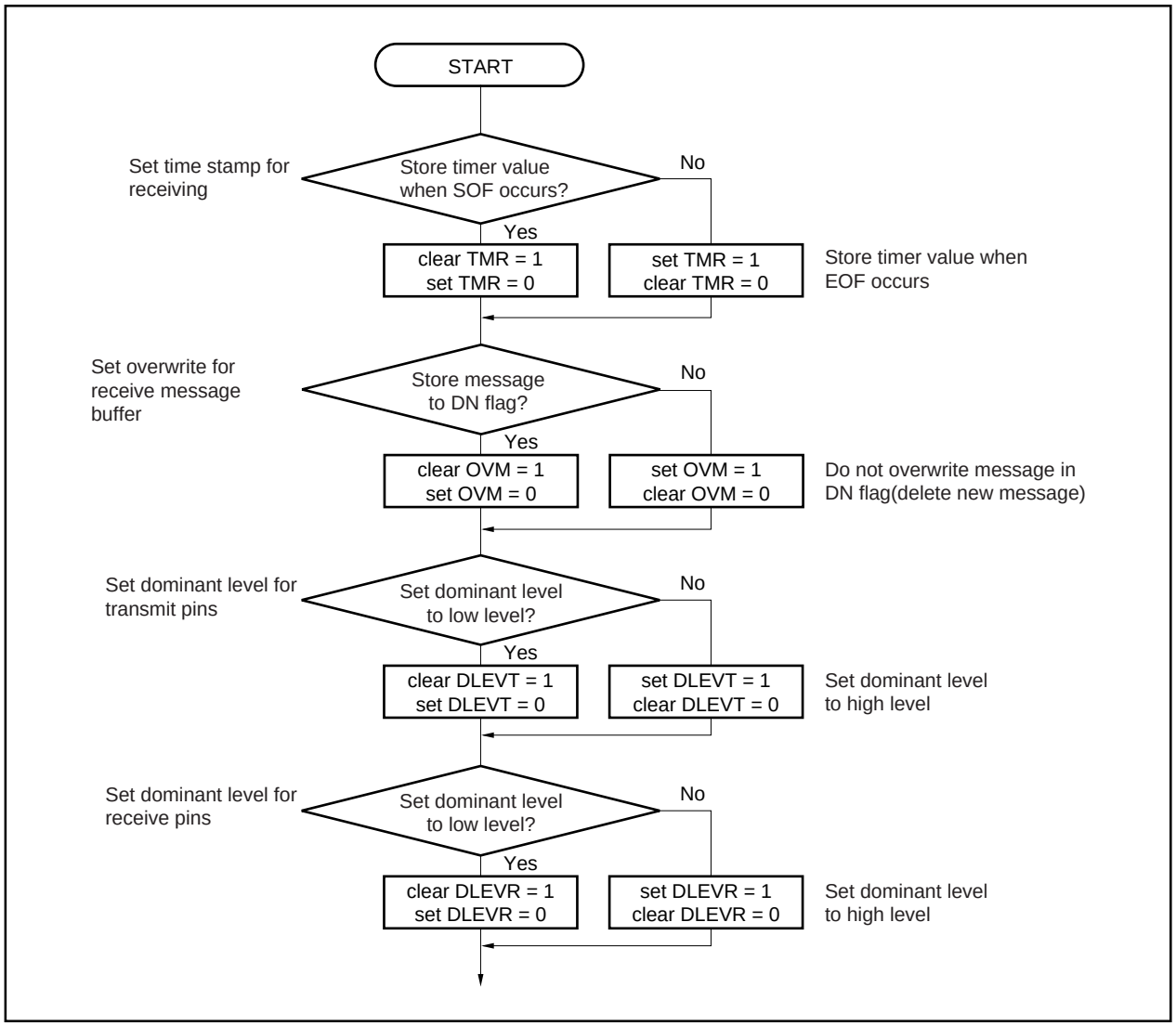


Figure 11-63. CAN1 Address Mask Registers L0 to L3 and H0 to H3 (C1MASKL0 to C1MASKL3 and C1MASKH0 to C1MASKH3) Settings

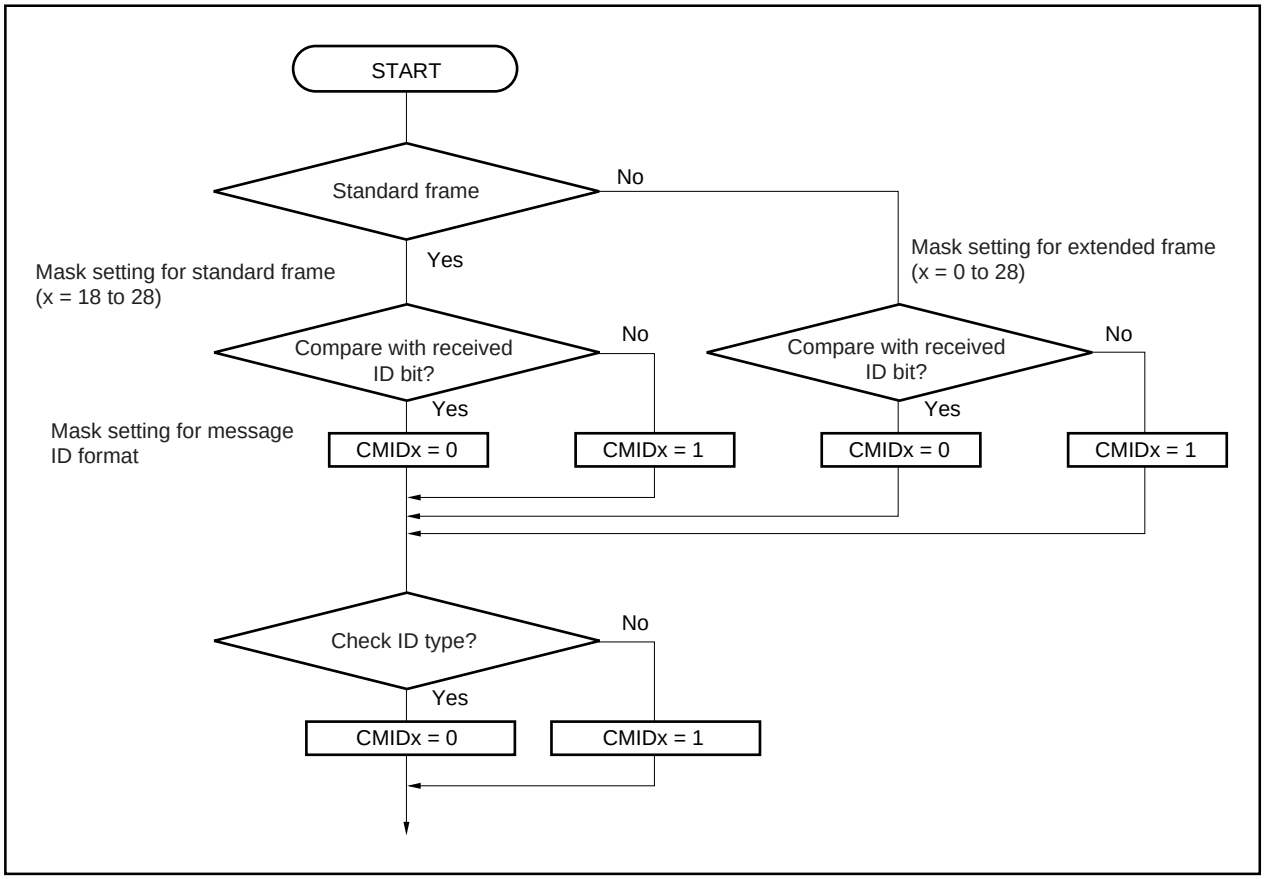
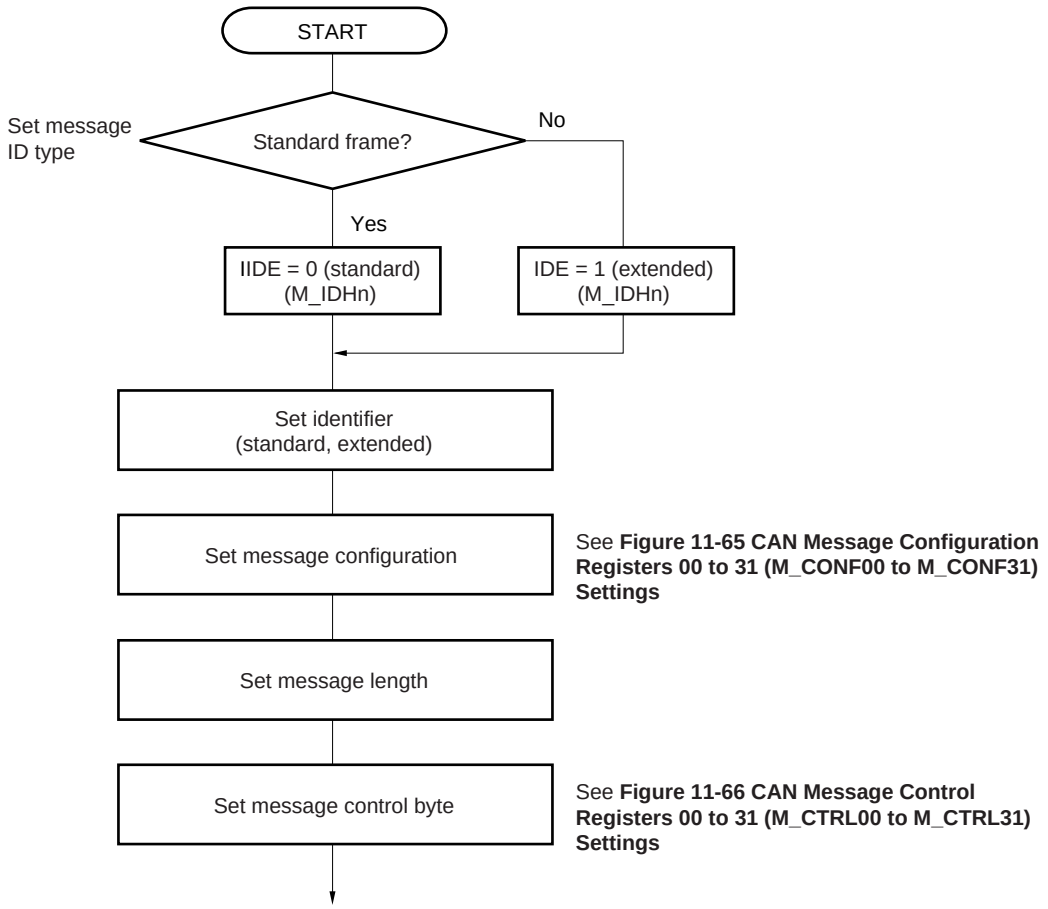
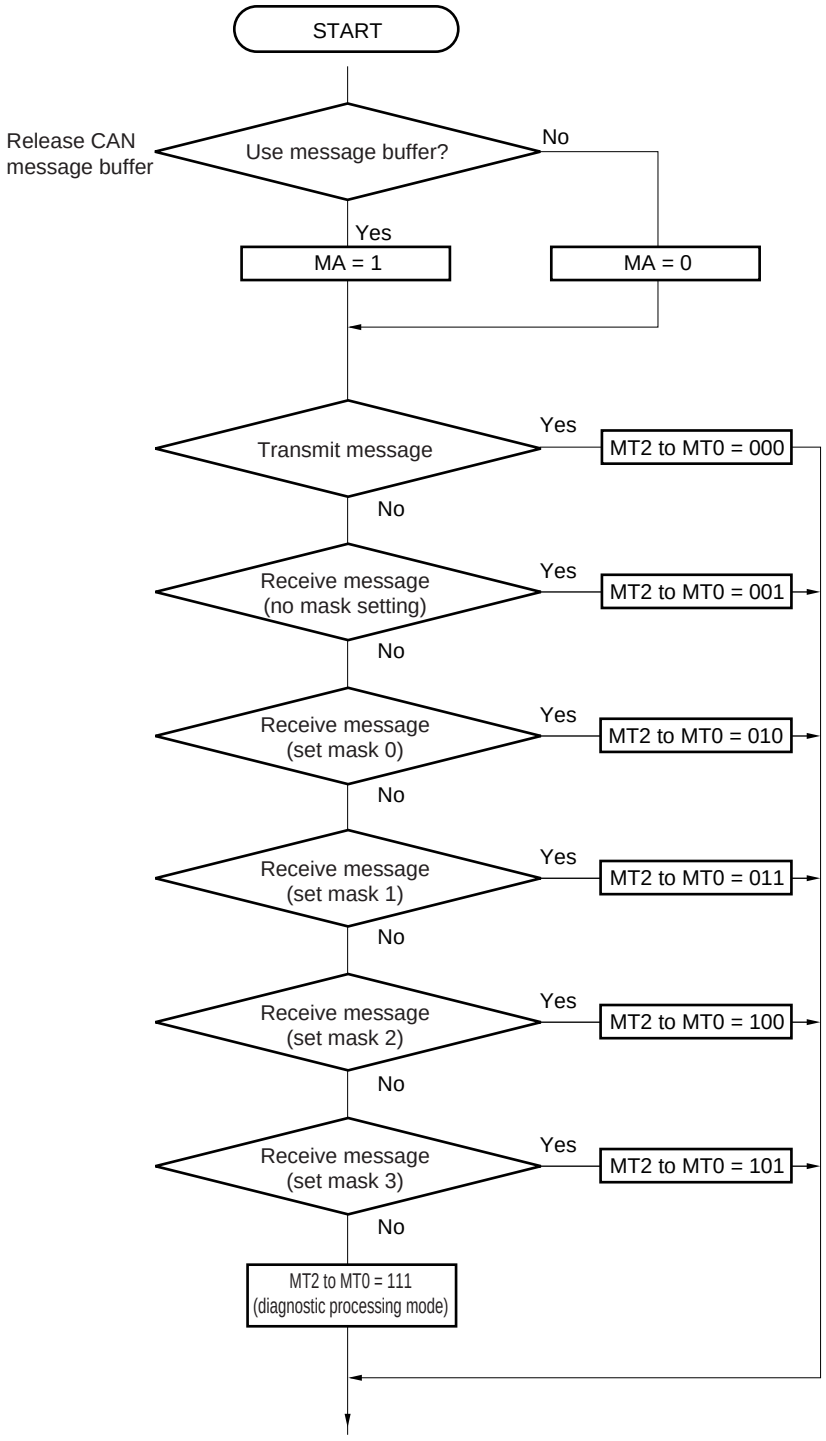


Figure 11-64. Message Buffer Settings



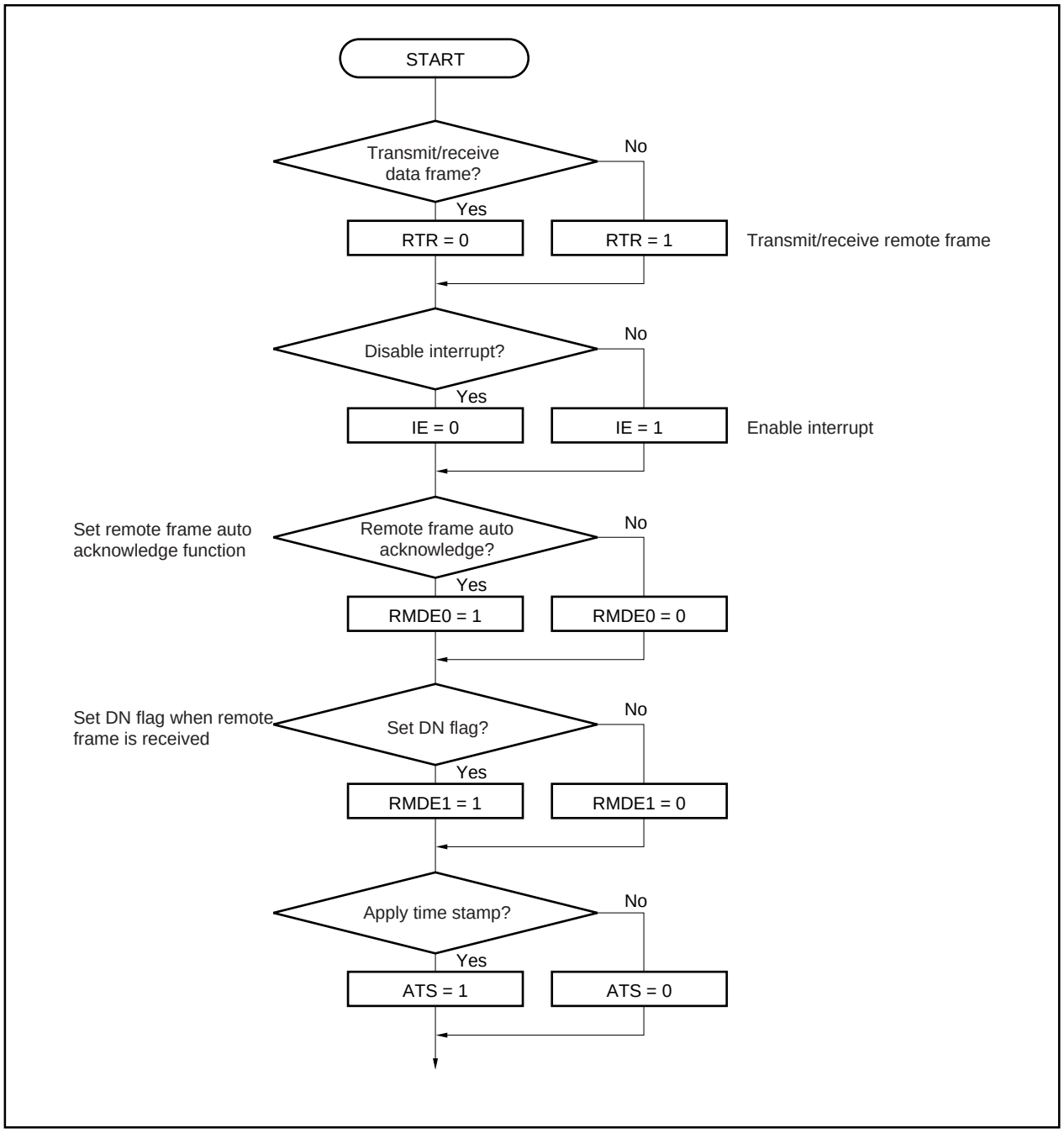
Remark n = 00 to 31

Figure 11-65. CAN Message Configuration Registers 00 to 31 (M_CONF00 to M_CONF31) Settings



Remark n = 00 to 31

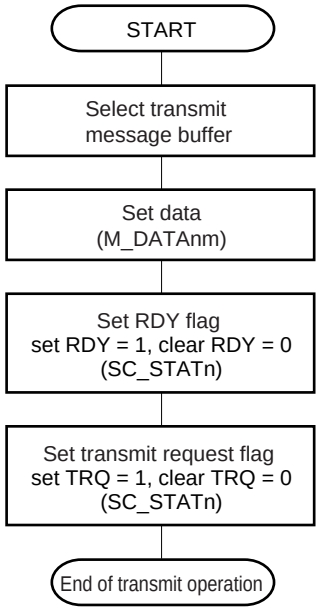
Figure 11-66. CAN Message Control Registers 00 to 31 (M_CTRL00 to M_CTRL31) Settings



11.11.2 Transmit operation mode

Transmit messages are output from the target message buffer.

Figure 11-67. Transmit Operation Mode

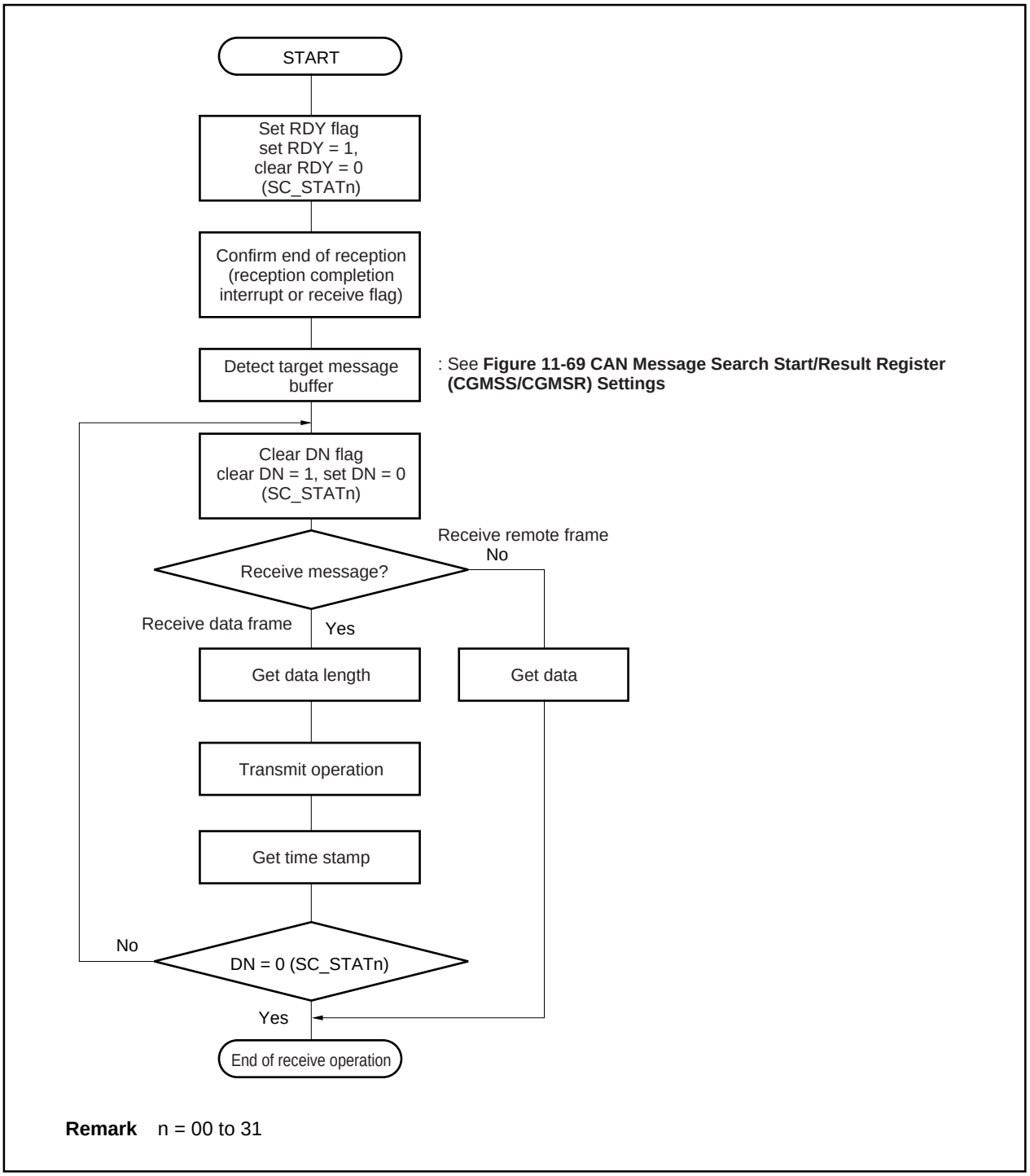


Remark n = 00 to 31, m = 0 to 7

11.11.3 Receive operation mode

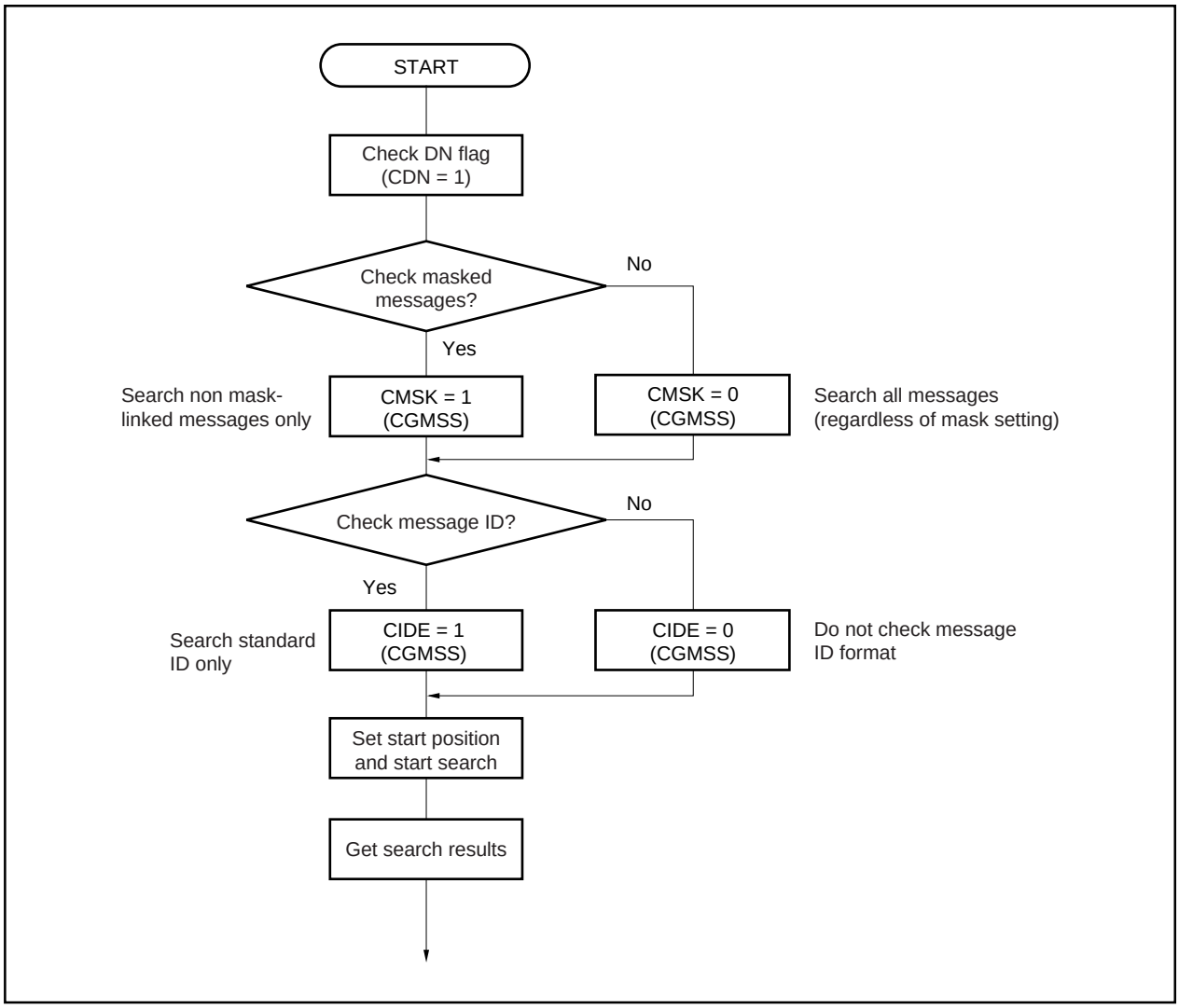
Receive messages are retrieved from the target message buffer.

Figure 11-68. Receive Operation Mode



Remark n = 00 to 31

Figure 11-69. CAN Message Search Start/Result Register (CGMSS/CGMSR) Settings



11.11.4 CAN sleep mode

In CAN sleep mode, the FCAN controller can be set to standby mode to reduce power consumption. A wake-up occurs when there is a bus operation.

Figure 11-70. CAN Sleep Mode Settings

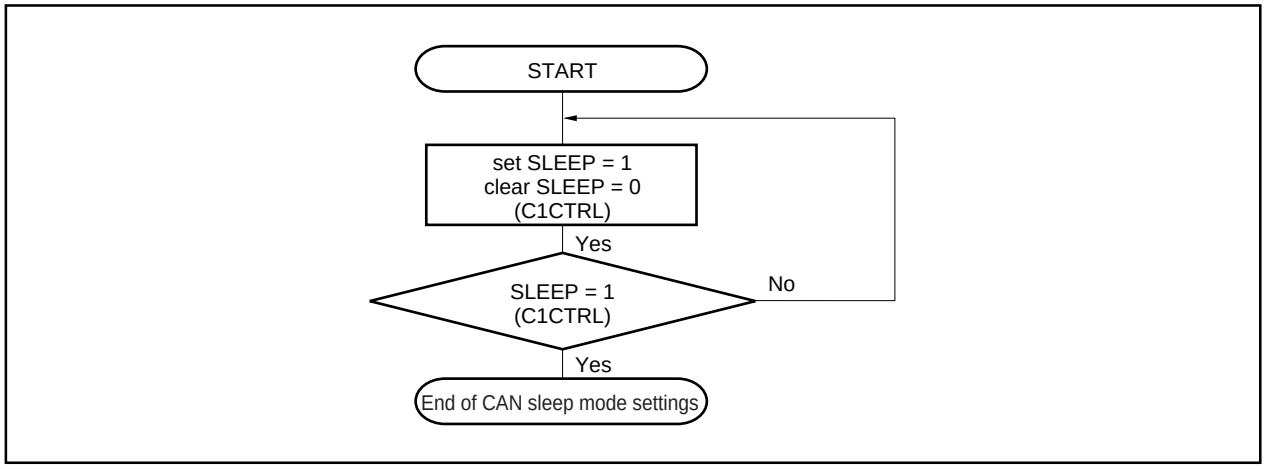


Figure 11-71. Clearing of CAN Sleep Mode by CAN Bus Active Status

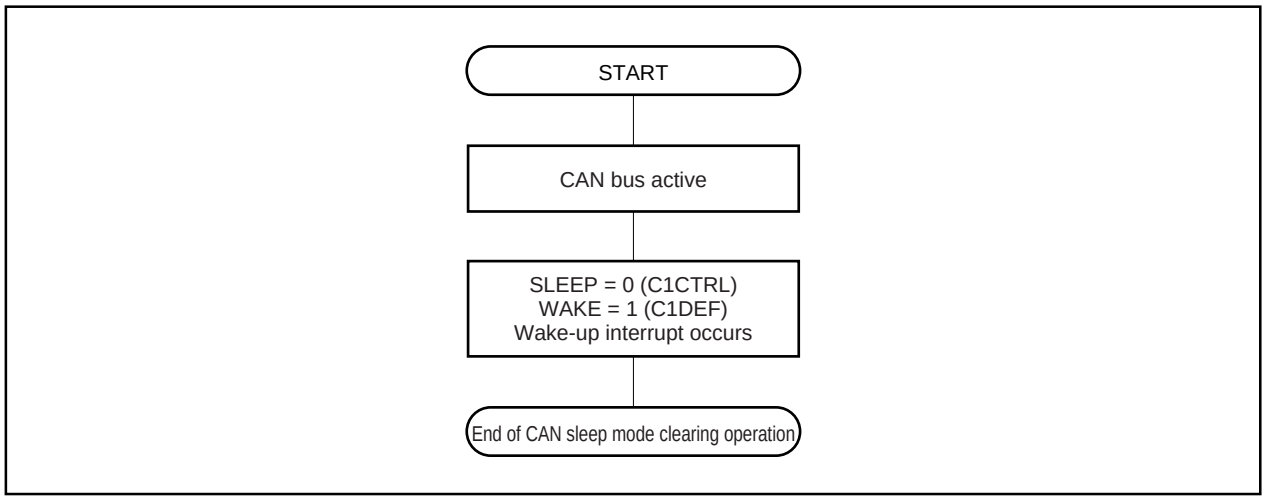
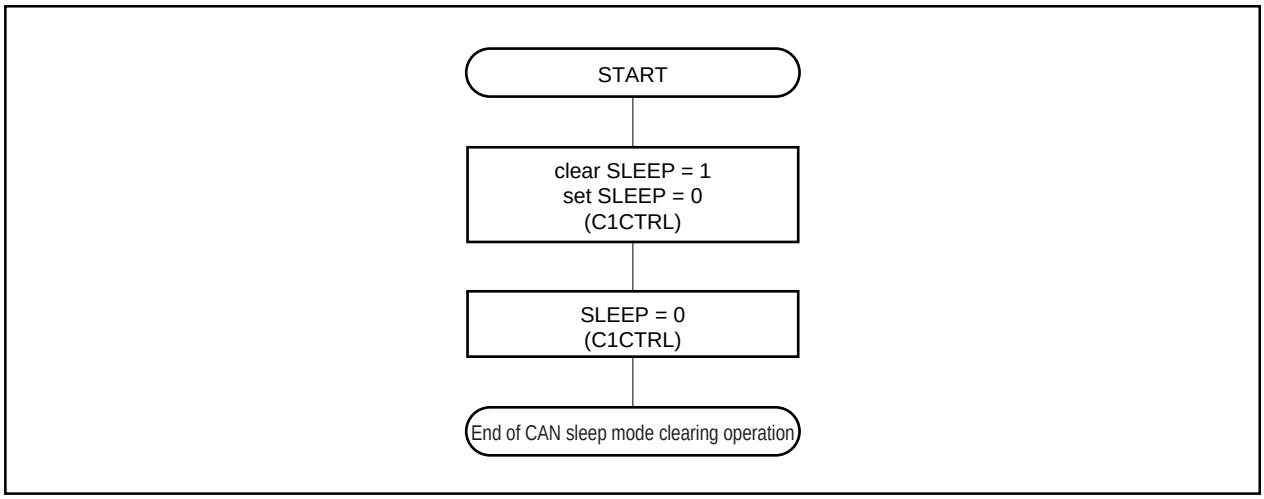


Figure 11-72. Clearing of CAN Sleep Mode by CPU



11.11.5 CAN stop mode

In CAN stop mode, the FCAN controller can be set to standby mode to reduce power consumption. No wake-up occurs when there is a bus operation (stop mode is controlled by CPU access only).

Figure 11-73. CAN Stop Mode Settings

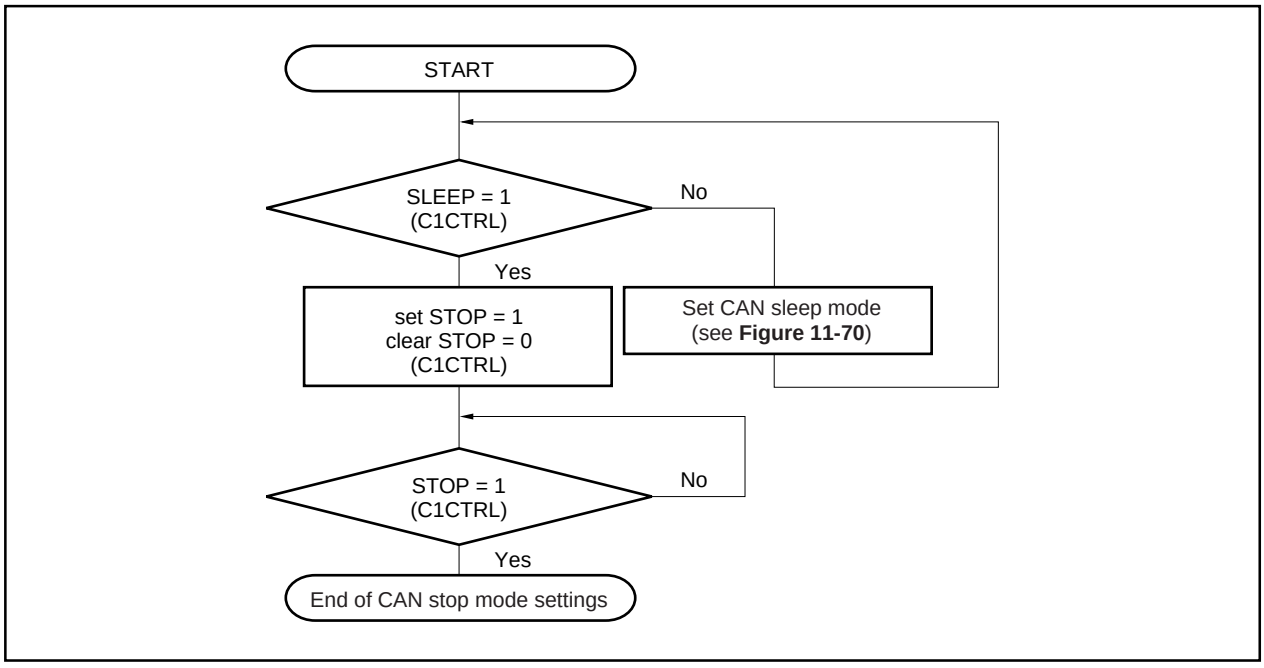
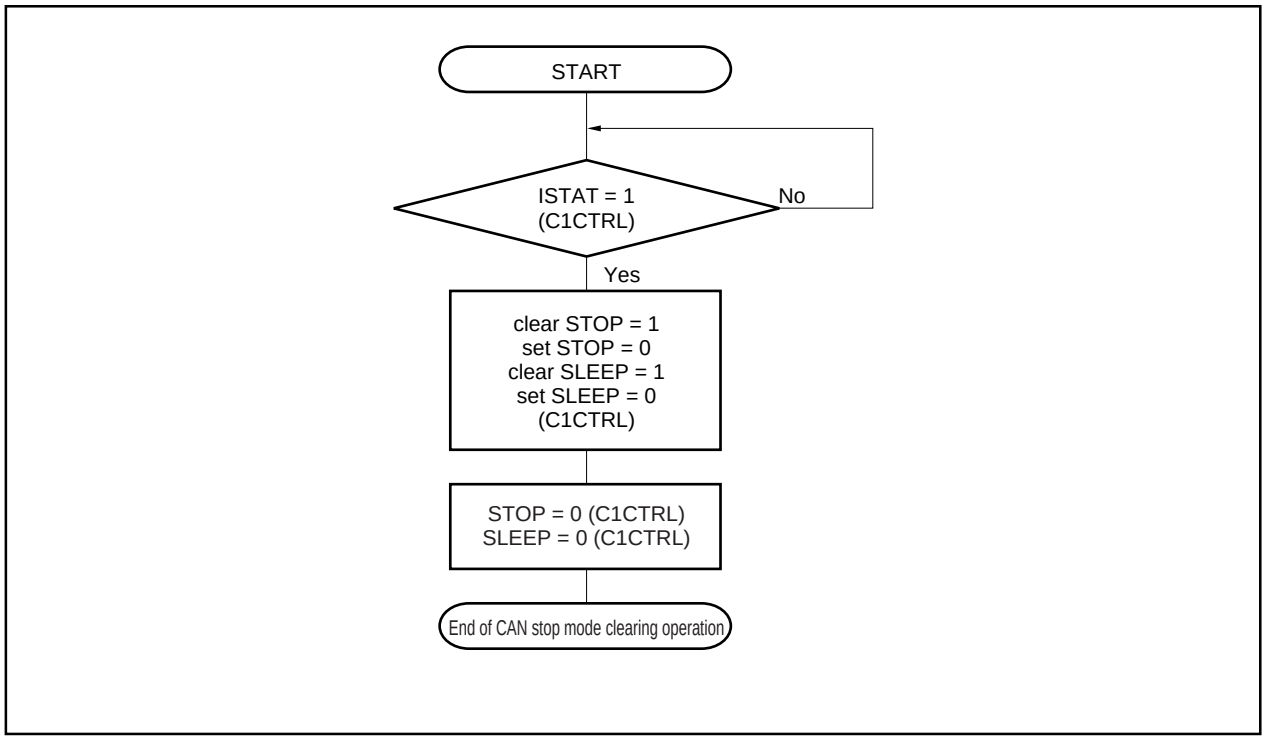


Figure 11-74. Clearing of CAN Stop Mode



11.12 Rules for Correct Setting of Baud Rate

The CAN protocol limit values for ensuring correct operation of FCAN are described below. If these limit values are exceeded, a CAN protocol violation may occur, which can result in operation faults. Always make sure that settings are within the range of limit values.

(a) $2 \leqq$ SPT (sampling point) $\leqq 16$
(b) $7 \leqq$ DBT (data bit time) $\leqq 24$
(c) SJW (reSynchronization Jump Width: baud rate shift tolerance period) < DBT – SPT
(d) $2 \leqq$ SPT (DBT – SPT) $\leqq 8$

Also, make sure all settings are within the range shown below to ensure compliance with the CAN protocol specification.

(e) $1 \leqq (2 \times \text{SPT} - \text{DBT}) \leqq 8$

(1) Example of FCAN baud rate setting

The following is an example of how correct settings for the C1BRP register and C1SYNC register can be calculated.

Conditions from CAN bus:

<1> CAN global frequency (f_{MEM}): 16 MHz
<2> CAN bus baud rate (f_{CAN}): 83 kbps
<3> Sampling point: 75% or more
<4> SJW: 3 BTL

First, calculate the ratio between the CAN global frequency and the CAN bus baud rate frequency as shown below.

f_{MEM} / f_{CAN} = 16 MHz / 83 kHz $\neq$ 192.77 $\neq 2^6 \times 3$

Set an even number between 2 and 128 to the C1BRP register's bits BRP5 to BRP0 as the setting for the prescaler (CAN protocol layer main system clock: f_{BTL}), then set a value between 8 and 25 to the C1SYNC register's bits DTB4 to DBT0 as the data bit time.
Since it is assumed that the SJW value is 3, the maximum setting for SPT (sampling point) is either 4 less than the data bit time setting or is less than 17.

(SPT $\leqq$ DBT – 4 or SPT $\leqq$ 17)

Given the above limit values, the following four settings are possible.

Prescaler	DBT	SPT (MAX.)	Calculated SPT
24	8	4	4/8 = 50%
16	12	8	8/12 = 67%
12	16	12	12/16 = 75%
8	24	17	17/24 = 71%

16 MHz 83 kbps $\cong$ 192 $= 64 \times 3$ <1>
$= 48 \times 4$ <2>
$= 32 \times 6$ <3>
$= 24 \times 8$ <4>
$= 16 \times 12$ <5>
$= 12 \times 16$ <6>
$= 8 \times 24$ <7>
$= 6 \times 32$ <8>
$= 4 \times 48$ <9>
$= 3 \times 64$ <10>

The settings that can actually be made for the V850E/IA1 are in the range from <4> to <7> above (the section enclosed in broken lines).
Among these options in the range from <4> to <7> above, the following register setting is made assuming option <4> is selected.

f_{BTL} = 16 MHz/24
= 16 MHz/((11 + 1) $\times$ 2)
= 11

Therefore, C1BRP register = 000BH

DBT = f_{BTL}/8
= 667 kHz
= 667 kHz/8
= 83 kbps

Therefore, C1SYNC register's bits DTB4 to DTB0 = f_{BTL}/(n + 1)
= 7

DBT4 to DBT0 = 00111B

Given SJW = 3:

SJW < DBT – SPT

3 < 8 – SPT

SPT < 5

Therefore, SPT is set as 4 (max.)

However, since SPT = 4/8 ≠ 75% is required, the above setting is not possible.
Instead, perform the following type of calculation to obtain a setting that meets the required specifications.

f_{BTL} = 16 MHz/12
= 16 MHz/((5 + 1) × 2)
= 5

Therefore, C1BRP register = 0005H

DBT = f_{BTL}/16
= f_{BTL}/(15 + 1)
= 15

Therefore, C1SYNC register's bits DTB4 to DTB0 = 01111B

SPT = f_{BTL}/12
= f_{BTL}/(11 + 1)
= 11

C1SYNC register's bits SJW1 and SJW0 = f_{BTL}/3
= f_{BTL}/(2 + 1)
= 2

The C1SYNC register settings based on these results are shown in Figure 11-75 below.

Figure 11-75. C1SYNC Register Settings

	15	14	13	12	11	10	9	8
C1SYNC	0	0	0	SAMP	SJW1	SJW0	SPT4	SPT3
Setting	0	0	0	0	1	0	0	1

	7	6	5	4	3	2	1	0
	SPT2	SPT1	SPT0	DBT4	DBT3	DBT2	DBT1	DBT0
Setting	0	1	1	0	1	1	1	1

11.13 Prioritization of Message Buffers During Receive Comparison

Several message buffers can be constructed for receiving messages. In such cases, a system of prioritization in receiving messages must be established for these message buffers.

11.13.1 Reception of data frames

Table 11-25. Prioritization of Message Buffers When Receiving Data Frames

Priority Ranking	Description
1 (High)	Receive messages can be stored in receive message buffers when the receive messages meet the following conditions. <1> Messages are not linked to masks <2> M_STATn register's DN bit has not been set (to 1) (n = 00 to 31) If several messages have met the above conditions, the message buffer having the lowest message number is selected.
2	Receive messages can be stored in receive message buffers when the receive messages meet the following conditions. <1> Messages are not linked to masks <2> M_STATn register's DN bit has been set (to 1) (n = 00 to 31) If several messages have met the above conditions, the message buffer having the lowest message number is selected.
3 (Low)	Receive messages can be stored in receive message buffers that are linked to masks. However, the following conditions must be met. <1> If several receive message buffers are linked to masks, the message buffer will be selected based on the mask number assigned to it. The lowest mask number takes the highest priority. <2> If several message buffers meet the conditions mentioned in “<1>“ above, the message buffer is selected based on its DN bit (in the M_STATn register). A message buffer in which this bit is not set (to 1) takes priority over a message buffer in which this bit is set (to 1). <3> If several message buffers meet the conditions mentioned in “<1>“ and “<2>“ above, the message buffer with the lowest message number is selected.

11.13.2 Reception of remote frames

Table 11-26. Prioritization of Message Buffers When Receiving Remote Frames

Priority Ranking	Description
1 (High)	Receive messages can be stored in transmit message buffers when the receive messages meet the following conditions. • Messages are not linked to masks If several transmit message buffers have met the above conditions, the message buffer having the lowest message number is selected.
2	Receive messages can be stored in receive message buffers when the receive messages meet the following conditions. • Messages are not linked to masks • M_STATn register's DN bit has not been set (to 1) (n = 00 to 31) If several receive message buffers have met the above conditions, the message buffer having the lowest message number is selected.
3	Receive messages can be stored in receive message buffers when the receive messages meet the following conditions. • Messages are not linked to masks • M_STATn register's DN bit has been set (to 1) (n = 00 to 31) If several receive message buffers have met the above conditions, the message buffer having the lowest message number is selected.
4 (Low)	Receive messages can be stored in receive message buffers that are linked to masks. However, the following conditions must be met. <1> If several receive message buffers are linked to masks, the message buffer will be selected based on the mask number assigned to it. The lowest mask number takes the highest priority. <2> If several message buffers meet the conditions mentioned in “<1>“ above, the message buffer is selected based on its DN bit (in the M_STATn register). (n = 00 to 31) A message buffer in which this bit is not set (to 1) takes priority over a message buffer in which this bit is set (to 1). <3> If several message buffers meet the conditions mentioned in “<1>“ and “<2>“ above, the message buffer with the lowest message number is selected.

11.14 Ensuring Data Consistency

When the CPU reads data from CAN message buffers, it must be guaranteed that the data will be read consistently.

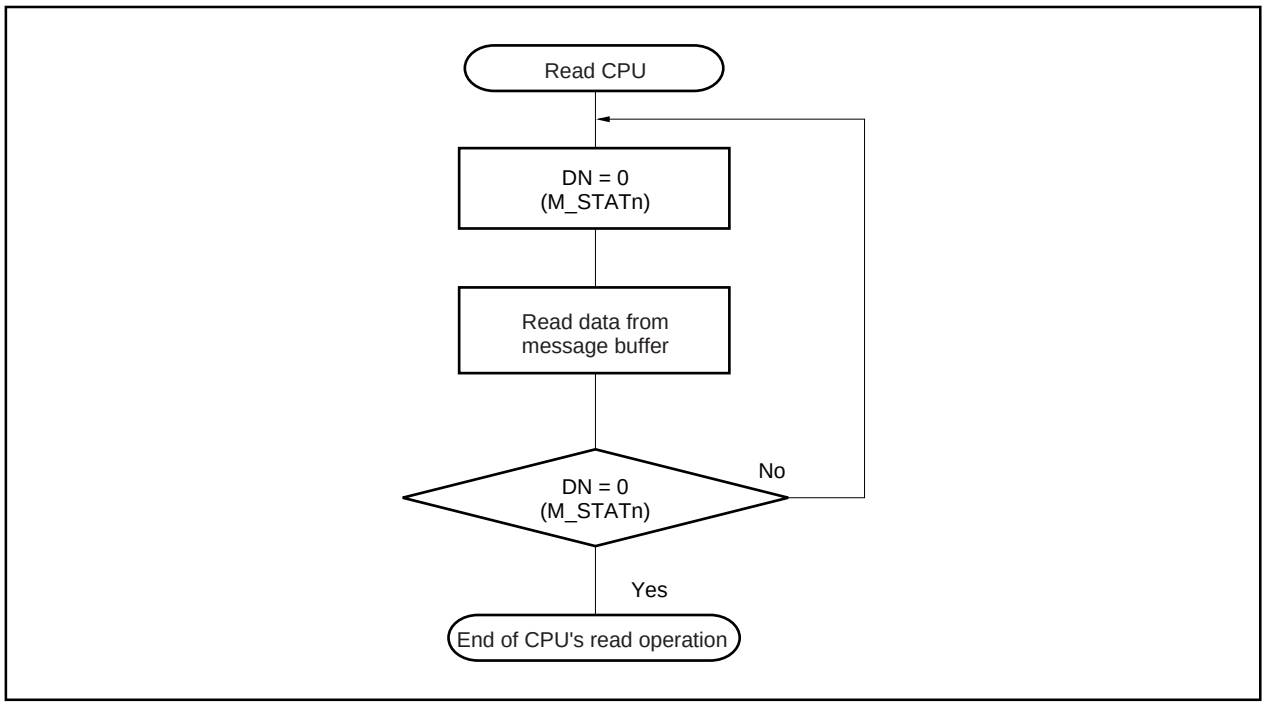
Two methods are used to ensure data consistency: sequential data read and burst mode data read.

11.14.1 Sequential data read

When the CPU performs sequential access of a message buffer, data is read from the buffer in the order shown in Figure 11-76 below.

Only the FCAN can set the M_STATn register's DN bit (to 1) and only the CPU can clear it (to 0), so during the read operation the CPU must be able to check whether or not any new data has been stored in the message buffer.

Figure 11-76. Sequential Data Read



Caution When the CPU reads data using only one read access operation, there is no problem as long as the data is consistent. Also, there is no need to check the M_STATn register's DN bit after the data has been read.

Remark n = 00 to 31

11.14.2 Burst mode data read

Burst mode data read is implemented in the FCAN to enable faster access to complete messages.

During the burst mode data read operation, complete messages are read from the message buffer area and are copied to temporary read buffers that are established as external to the CAN RAM area.

Consequently, the FCAN accesses the CAN RAM area when the CPU is about to read data, so as to enable read access without any wait time.

When messages are copied, such as from the message buffer 0 area, copying is started each time the CPU reads the M_DLC00 register and data is then copied from the message buffer 0 area to a temporary read buffer.

Data continues to be read from the temporary buffer as long as the CPU keeps directly incrementing (+ 1) the read address and reads more data. In other words, data is read in the following order: M_DLC00 register → M_CTRL00 register → M_TIME00 register → M_DATA000 to M_DATA007 registers → M_IDL00, M_IDH00 register.

If these linear access rules are not followed or if read access or write access is attempted at an address that is lower than the M_IDL00, M_IDH00 register's address (such as the M_CONF00 register or M_STAT00 register), burst read via the CAN interface read access may become invalid for the temporary buffer.

Caution 16-bit read access is required for the entire message buffer area when using the burst mode data read method. If 8-bit access (byte read operation) is attempted, burst read of the temporary buffer will be invalid even if the address is linearly incremented (+1) as described above.

11.15 Interrupt Conditions

11.15.1 Interrupts that are generated for FCAN controller

When interrupts are enabled (i.e., when the M_CTRLn register's IE bit = 1), interrupts will be generated under the following conditions (n = 00 to 31).

<1> Message-related operation has succeeded
- When a message has been received in the receive message buffer
- When a remote frame has been received in the transmit message buffer
  (only when auto acknowledge mode has not been set, i.e., when the M_CTRLn register's RMDE0 bit = 0)
- When a message has been transmitted from the transmit message buffer

<2> When a CAN bus error has been detected
- Bit error
- Bit stuff error
- Form error
- CRC error
- Ack error

<3> When the CAN bus mode has been changed
- Error passive status elapsed while FCAN was transmitting
- Bus off status was set while FCAN was transmitting
- Error passive status elapsed while FCAN was receiving

<4> Internal error
- Overrun error

11.15.2 Interrupts that are generated for global CAN interface

Interrupts are generated for the global CAN interface under the following conditions.

(1) An unusable memory address was accessed

(a) Access is attempted to an unused area (an area after the CGMSR/CGMSS register) that is within the common register area (for CAN global registers).

(2) When write access to a message buffer is disabled

(a) Write access is attempted to a CAN module (C1CRTL register, C1IE register, C1DEF register, etc.) in which the CGST register's GOM bit has been cleared.

(b) Write access is attempted to an unused area (an area after the C1SYNC register) that is within the CAN module

11.16 How To Shutdown FCAN Controller

The following procedure should be used to stop CAN bus operations in order to stop the clock supply to the CAN interface (to set low power mode).

<1> FCAN controller's initialization mode setting
- Set initialization mode (INIT bit = 1 in C1CTRL register (set INIT bit = 1, clear INIT bit = 0))

<2> Stop time stamp counter
- Set TSM bit = 0 in CGST register (set TSM = 0, clear TSM = 1)

<3> Stop CAN interface
- Set GOM bit = 0 in CGST register (set GOM = 0, clear GOM = 1)
- Stop CAN clock

Cautions 1. If the above procedure is not performed correctly, the CAN interface (in active status) can cause operation faults.

2. Perform only steps <1> and <2> above when setting the CPU itself to low power mode and operating the CAN interface using a CPU-supplied clock.
In this case, stopping the CAN interface clock (step <3> above) is automatically performed when the CPU clock is stopped, so there is no need to perform step <3>.

11.17 Cautions for Use

<1> Bit manipulation is prohibited for all FCAN controller registers.

<2> Release the CAN stop mode only after confirming that the ISTAT bit of the C1CTRL register is set (to 1). Operation cannot be guaranteed if the CAN stop mode is released while the ISTAT bit is cleared (to 0).

<3> Be sure to properly clear (to 0) all interrupt request flags[Note] in the interrupt routine. If these flags are not cleared (to 0), subsequent interrupt requests may not be generated. Note also that if an interrupt is generated at the same time as a CPU clear operation, that interrupt request flag will not be cleared (to 0). It is therefore important to confirm that interrupt request flags have been properly cleared (to 0).

Note See **11.10 (10) CAN interrupt pending register (CCINTP)**, **(11) CAN global interrupt pending register (CGINTP)**, and **(12) CAN1 local interrupt pending register (C1INTP)**.

<4> When a change occurs on the CAN bus via a setting of the CSTP in the CSTOP register while the clock supply to the CPU or peripheral functions is stopped, the CPU can be woken up.

CHAPTER 12 NBD FUNCTION (μPD70F3116)

The V850E/IA1 provides the Non Break Debug (NBD) function for on-chip data tuning.

12.1 Overview

The NBD function encompasses the following functions.

(1) RAM monitoring function

This function makes an arbitrary RAM area readable or writable from outside the chip via DMA.

[Corresponding RAM area]

XFFFC000H-XFFFE7FFH

If executed using an address outside the above, the function instantly returns "ready".
Output is undefined on a read, and the write operation is not performed on a write.

(2) Event detection function

By having a comparator (24-bit address setting) for match detection on-chip at a single point, this function outputs a match trigger (falling edge) when the address match detection shown below is performed.

- Execution PC address match detection
- On-chip RAM area address write timing match detection

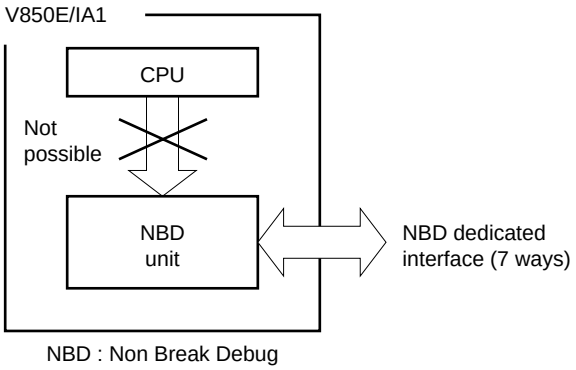
[Detection range]

ROM: X0000000H to X003FFFFH
RAM: XFFFC000H to XFFFE7FFH

Table 12-1. NBD Block Dedicated Pin Summary

Pin Name	I/O	Function Summary
CLK_DBG	Input	Serial clock input for debugging interface
SYNC	Input	Synchronization signal for debugging
AD0_DBG-AD3_DBG	I/O	Command data or RAM data input/output (4 bits)
TRIG_DBG	Output	Outputs trigger (falling edge) synchronized to timing of write to arbitrary specified RAM address or to timing of execution of instruction at specified address.

Figure 12-1. Image of NBD Space



NBD : Non Break Debug

Caution The debug function does not operate in software STOP mode, IDLE mode, or during oscillation stabilization (during TBC count). The debug function does operate in HALT mode.

12.2 NBD Function Register Map

Table 12-2 shows a map of the control registers of the NBD function. NBD space does not exist in the internal space of the CPU but exists independently as NBD space. Because of this, NBD space is space that cannot be read or written from within the CPU but can only be read or written from the NBD dedicated interface (refer to **Figure 12-1**).

Table 12-2. NBD Space Map

Address	Register Name	Symbol	R/W	After Reset
000H	Chip ID register 0	TID0	R	4EH
001H	Chip ID register 1	TID1		01H
002H	Chip ID register 2	TID2		01H
800H	User event address setting register	EVTU_A0-EVTU_A7	R/W	Undefined
801H		EVTU_A8-EVTU_A15		Undefined
802H		EVTU_A16-EVTU_A23		Undefined
803H		EVTU_A24-EVTU_A27		Undefined
820H	User event condition setting register	EVTU_C0		Undefined

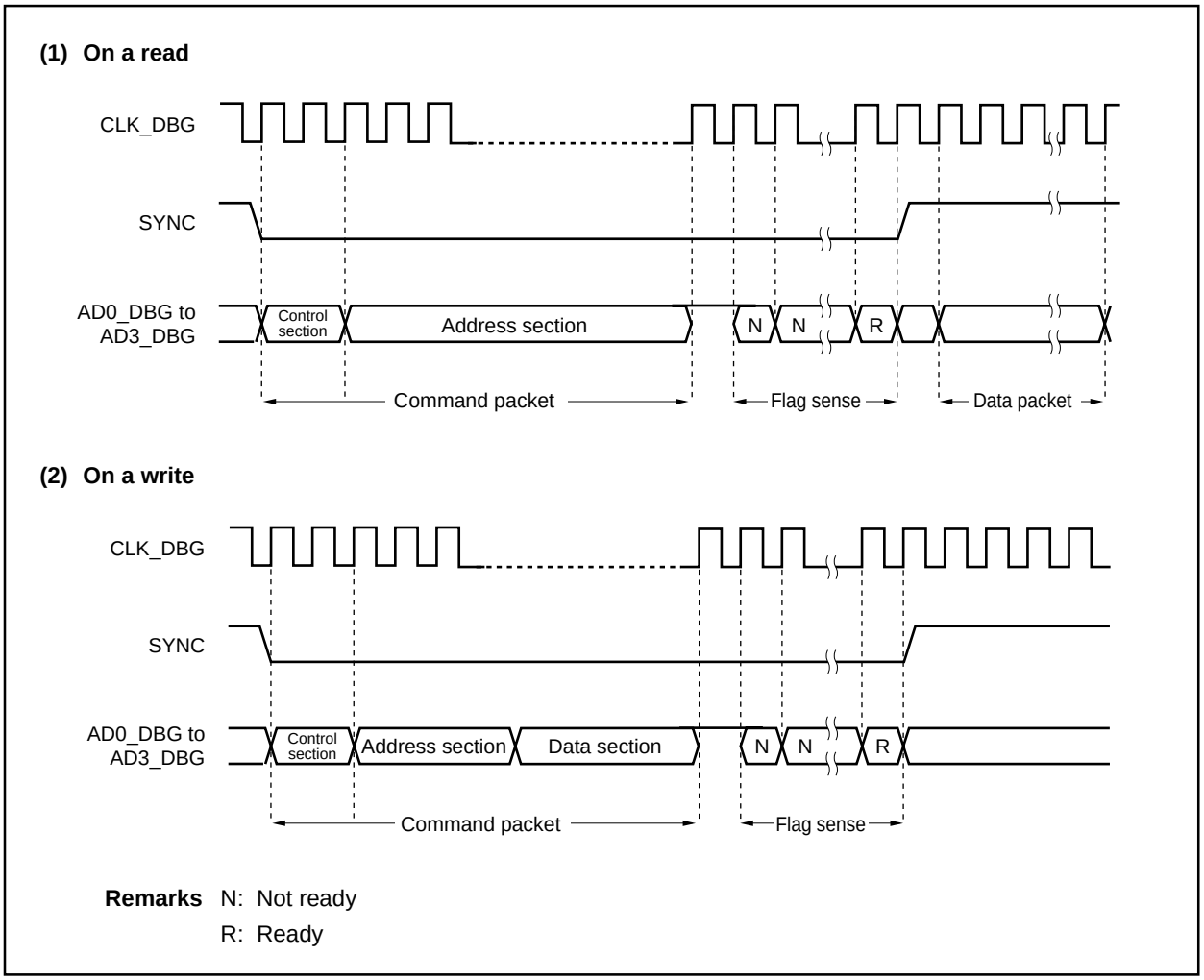
Caution Since the V850E/IA1 NBD uses DMA that is on-chip in the V850E1 (NB85E) CPU core, settings for DMA are initialized after reset.

12.3 NBD Function Protocol

The basic protocol of the NBD function is shown below.

(1) Basic protocol

Figure 12-2. Basic Protocol



Remarks N: Not ready
R: Ready

(2) Command packet

NBD Bus Line	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	aux3	aux2	aux1	aux0
2nd	SIZ1	SIZ0	R/W	I/T
3rd	A3	A2	A1	A0
4th	A7	A6	A5	A4
5th	A11	A10	A9	A8
6th	A15	A14	A13	A12
7th	A19	A18	A17	A16
8th	A23	A22	A21	A20
9th	D3	D2	D1	D0
10th	D7	D6	D5	D4
11th	D11	D10	D9	D8
12th	D15	D14	D13	D12
13th	D19	D18	D17	D16
14th	D23	D22	D21	D20
15th	D27	D26	D25	D24
16th	D31	D30	D29	D28

Caution Values are for command packet maximum setup.

- **Access to NDB space** **Address: 12 bits (A0 to A11) [Fixed]**
  Data: 8 bits (D0 to D7)
- **Access to target space** **Address: 24 bits (A0 to A23) [Fixed]**
  Data: 32 bits (D0 to D31)

(a) aux0 to aux3: Expansion bits

aux0	aux1	aux2	aux3	Remarks
0	0	0	0	Fixed
Other than 0000				For future expansion

(b) I/T: Access address space mode specification

I/T	Remarks
0	Specifies access to NBD space
1	Specifies access to target space

(c) R/W: External access mode specification

R/W	Remarks
0	External read mode
1	External write mode

(d) SIZ0, SIZ1: Access data size specification

SIZ1	SIZ0	Target Space Access	ICE Space Access
0	0	8-bit length[Note 1]	8-bit length
0	1	16-bit length[Note 1]	Setting disabled[Note 2]
1	0	32-bit length	
1	1	Setting disabled[Note 2]	

Notes 1. Can be set only on a read.
If set on a write, RAM data will be destroyed.

2. A write is ineffective and read data is undefined in cases where "Setting disabled" is specified.

(3) Flag sense packet

NBD Bus Line	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	0	0	0	RFLG

RFLG 0: Not Ready
1: Ready

(4) Data packet

The data packet data size is the data size specified by SIZ1 and SIZ0 in a command packet (8, 16, or 32 bits).

NBD Bus Line	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	D3	D2	D1	D0
2nd	D7	D6	D5	D4
3nd	D11	D10	D9	D8
4th	D15	D14	D13	D12
5th	D19	D18	D17	D16
6th	D23	D22	D21	D20
7th	D27	D26	D25	D24
8th	D31	D30	D29	D28

12.4 NBD Function

12.4.1 RAM monitoring, accessing NBD space

The NBD function performs read and write operations on on-chip RAM data via DMA (direct memory access) for addresses in internal RAM. It also performs reading or writing to RAM for data tuning and reading or writing to NBD space.

(1) RAM monitoring

The following are the commands for reading and writing to internal RAM areas and data tuning RAM from outside.

(a) Write command

The target address (real address of target: lower 24 bits) at which a write to internal RAM is to be made and the data are received from outside as a command packet. After receiving the command packet shown below from outside, a Ready command is output following write termination.

Command packets can be received from outside once more (after Ready command SYNC inactive confirmation).

Table 12-3. Command Packet (On a Write)

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	0	0	0	0
2nd	SIZ1	SIZ0	1	1
3rd to 8th	Target space write address specification (24 bits)			
9th to16th	Write data (data specified by SIZ0 and SIZ1)			

(b) Read command

The target address (target real address: lower 24 bits) at which a read of internal RAM is to be made is received from outside as a command packet. After receiving the command packet from outside, a Ready command is output, SYNC is made inactive, and the data at the address specified by the command packet is transmitted outside.

Table 12-4. Command Packet (On a Read)

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	0	0	0	0
2nd	SIZ1	SIZ0	0	1
3rd to 8th	Target space read address specification (24 bits)			

Caution In read mode, the output data section from outside is deleted.

Table 12-5. Data Packet (On a Read)

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st to 8th	Target space read data			

(2) Access to NBD space

The following are the commands for reading and writing to NBD space from outside. For NBD space, an access address is 12-bit fixed-length and the access data is 8-bit fixed-length.

(a) Write command

The address (NBD space address: 12 bits) at which a write to NBD space is to be made and the data are received from outside as a command packet. After receiving the command packet shown in Table 12-6 from outside, a Ready command is output following write termination.

Command packets can be received once more from outside (after Ready command SYNC inactive confirmation).

Table 12-6. Command Packet (On a Write to NBD Space)

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	0	0	0	0
2nd	0	0	1	0
3rd	A3	A2	A1	A0
4th	A7	A6	A5	A4
5th	A11	A10	A9	A8
6th	D3	D2	D1	D0
7th	D7	D6	D5	D4

Caution An NBD space write address is 12-bit fixed-length.
The write data is 8-bit fixed-length.

(b) Read command

The target address (real address of target: 12 bits) at which to read from internal RAM is received as a command packet from outside. After receiving the command packet from outside, a Ready command is output, SYNC is made inactive, and the data at the address specified by the command packet is transmitted outside.

Table 12-7. Command Packet (On a Read of NBD Space)

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	0	0	0	0
2nd	0	0	0	0
3rd	A3	A2	A1	A0
4th	A7	A6	A5	A4
5th	A11	A10	A9	A8

Caution An NBD space read address is 12-bit fixed-length.
In read mode, the output data section from outside is deleted.

Table 12-8. Data Packet

ADn_DBG	AD3_DBG	AD2_DBG	AD1_DBG	AD0_DBG
1st	D3	D2	D1	D0
2nd	D7	D6	D5	D4

Caution Read data is 8-bit fixed-length.

12.4.2 Event detection function

By having a comparator (24-bit address setting) for match detection on-chip at a single point, this function detects match of the address setting registers shown below and outputs a match trigger (falling edge). Event trigger output is low active and during the active period it is output synchronous with the system clock of the target CPU. The active width is one cycle of the internal system clock of the CPU.

(1) Event detection conditions

- Execution PC address match

  Match detection range for timing of a write to a set address in the on-chip RAM area

  XFFFC000H to XFFFE7FFH

(2) Event detection control register

(a) NBD event condition setting register (EVTU_C)

Figure 12-3. NBD Event Condition Setting Register (EVTU_C)

	7	6	5	4	3	2	1	0	NBD space address	Initial value
EVTU_C7 to EVTU_C0	0	0	0	0	0	0	0	PCU/DTU	820H	Undefined

Bit Position	Bit Name	Function
0	PCU/DTU	Selects an execution PC event or RAM access event. 0: On-chip RAM access event is in valid[Note] 1: Execution PC event is in valid **Note** If the EVTU_C register is set outside the on-chip RAM area, an event also is output when writing outside the RAM.

(b) NBD event address register (EVTU_A)

The EVTU_A register sets the value of the address that is the subject of the event.

Figure 12-4. NBD Event Address Register (EVTU_A)

	7	6	5	4	3	2	1	0	NBD space address	Initial value
EVTU_A7 to EVTU_A0	EVAU7	EVAU6	EVAU5	EVAU4	EVAU3	EVAU2	EVAU1	EVAU0	800H	Undefined

	15	14	13	12	11	10	9	8	NBD space address	Initial value
EVTU_A15 to EVTU_A8	EVAU15	EVAU14	EVAU13	EVAU12	EVAU11	EVAU10	EVAU9	EVAU8	801H	Undefined

	23	22	21	20	19	18	17	16	NBD space address	Initial value
EVTU_A23 to EVTU_A16	EVAU23	EVAU22	EVAU21	EVAU20	EVAU19	EVAU18	EVAU17	EVAU16	802H	Undefined

	31	30	29	28	27	26	25	24	NBD space address	Initial value
EVTU_A27 to EVTU_A24	Undefined	Undefined	Undefined	Undefined	EVAU27Note	EVAU26Note	EVAU25Note	EVAU24Note	803H	Undefined

Note Set bit 27 through bit 24 to 0.

Cautions 1. ROM address match functions only for internal ROM.

2. This cannot be used in single-chip mode 1.

12.4.3 Chip ID registers (TID0-TID2)

The chip ID registers are stored in NBD spaces 000H to 002H. By reading the ID codes in the chip ID registers from outside in NBD mode, the semiconductor manufacturer, CPU family code, and specific product type can be identified. The chip ID registers have fixed values for each product.

The chip ID registers (TID0 to TID2) are read-only registers.

Figure 12-5. Chip ID Registers (TID0 to TID2)

	7	6	5	4	3	2	1	0	NBD space address
TID0	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	000H

• MC7 to MC0 : Semiconductor manufacturer classification
NEC : 4EH

	7	6	5	4	3	2	1	0	NBD space address
TID1	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	001H

• FC7 to FC0 : CPU family classification code
V850E1 family : 01H

	7	6	5	4	3	2	1	0	NBD space address
TID2	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	002H

• SC7 to SC0 : Specific product classification code
V850E/IA1 : 01H

12.5 Control Registers

(1) Data buffer L for RAM access (NBDL) and data buffer LU for RAM access (NBDLU)

NBDL and NBDLU operate as buffers between DMA and outside when reading or writing RAM via DMA from outside.

NBDL can be used to read or write in 16-bit or 8-bit units and NBDLU to read or write in 8-bit units.

Figure 12-6. Data Buffer L (NBDL) for RAM Access and Data Buffer LU (NBDLU) for RAM Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDL	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FFFFFA60H	0000H

	15	14	13	12	11	10	9	8	Address	Initial value
NBDLU	D15	D14	D13	D12	D11	D10	D9	D8	FFFFFA61H	00H

Cautions 1. Although NBDL and NBDLU can be used to read or write, physically separate registers are used when reading and when writing and values written cannot be read.

2. Use both NBDL and NBDH (12.5 (2)) for 32-bit access of RAM.

Remarks 1. Register values written from outside can be read by DMA (CPU) and values written by DMA (CPU) can be read outside.

2. On an 8-bit access, NBDL is the lower 8 bits only.

3. On an 8-bit access, NBDLU is an odd-numbered address register that is paired with NBDL and is the upper 8 bits of NBDL.

(2) Data buffer H for RAM access (NBDH) and data buffer HU for RAM access (NBDHU)

NBDH and NBDHU operate as buffers between DMA and outside when reading or writing RAM via DMA from outside.

NBDH can be used to read or write in 16-bit or 8-bit units and NBDHU to read or write in 8-bit units.

Figure 12-7. Data Buffer H (NBDH) for RAM Access and Data Buffer HU (NBDHU) for RAM Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDH	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FFFFFA62H	0000H

	15	14	13	12	11	10	9	8	Address	Initial value
NBDHU	D31	D30	D29	D28	D27	D26	D25	D24	FFFFFA63H	00H

Cautions 1. Although NBDH and NBDHU can be used to read or write, physically separate registers are used when reading and when writing and values written cannot be read.

2. Use both NBDL (refer to 12.5 (1)) and NBDH for 32-bit access of RAM.

Remarks 1. Register values written from outside can be read by DMA (CPU) and values written by DMA (CPU) can be read outside.

2. On an 8-bit access, NBDH is the lower 8 bits only.

3. On an 8-bit access, NBDHU is an odd-numbered address register that is paired with NBDH and is the upper 8 bits of NBDH.

(3) DMA source address setting register SL (NBDMSL)

NBDMSL specifies a DMA source address.

It can be written from outside and read by DMA (CPU).

It can be read only in 16-bit units.

Figure 12-8. DMA Source Address Setting Register SL (NBDMSL)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDMSL	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFFFFA64H	Undefined

Remarks 1. When reading RAM, an address signal from outside is read by DMA (CPU).

2. When writing RAM, the NBDL register value is read by DMA (CPU).

(4) DMA source address setting register SH (NBDMSH)

NBDMSH specifies a DMA source address.

It can be written from outside and read by DMA (CPU).

It can be read only in 16-bit units.

Figure 12-9. DMA Source Address Setting Register SH (NBDMSH)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDMSH	IR	0	0	0	AD27	AD26	AD25	AD24	AD23	AD22	AD21	AD20	AD19	AD18	AD17	AD16	FFFFFA66H	Undefined

Bit Position	Bit Name	Function
15	IR	Shows read or write status when NBD accesses on-chip RAM of the V850E/IA1. 0: NBD is write accessing RAM 1: NBD is read accessing RAM

Remarks 1. When reading RAM, an address signal from outside is read by DMA (CPU).

2. When writing RAM, the NBDL register value is read by DMA (CPU).

(5) DMA destination address setting register DL (NBDMDL)

NBDMDL specifies a DMA destination address.

It can be written from outside and read by DMA (CPU).

It can be read only in 16-bit units.

Figure 12-10. DMA Destination Address Setting Register DL (NBDMDL)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDMDL	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFFFFA68H	Undefined

Remarks 1. When writing RAM, an address signal from outside is read by DMA (CPU).

2. When reading RAM, the NBDL register value is read by DMA (CPU).

(6) DMA destination address setting register DH (NBDMDH)

NBDMDH specifies a DMA destination address.

It can be written from outside and read by DMA (CPU).

It can be read only in 16-bit units.

Figure 12-11. DMA Destination Address Setting Register DH (NBDMDH)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
NBDMDH	IR	0	0	0	AD27	AD26	AD25	AD24	AD23	AD22	AD21	AD20	AD19	AD18	AD17	AD16	FFFFFA6AH	Undefined

Bit Position	Bit Name	Function
15	IR	Shows read or write status when NBD accesses on-chip RAM of the V850E/IA1. 0: NBD is read accessing RAM 1: NBD is write accessing RAM

Remarks 1. When writing RAM, an address signal from outside is read by DMA (CPU).

2. When reading RAM, the NBDL register value is read by DMA (CPU).

(7) RAM address alternate register L (ISL_RAML)

This register sets the trigger address (lower 16 bits) of RAM write address match.

It can be read or written in 16-bit units.

Figure 12-12. RAM Address Alternate Register L (ISL_RAML)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ISL_RAML	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	0	0	FFFFFA70H	0000H

(8) RAM address alternate register H (ISL_RAMH)

This register sets the trigger address (upper 16 bits) of RAM write address match.

It can be read or written in 16-bit units.

Figure 12-13. RAM Address Alternate Register H (ISL_RAMH)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ISL_RAMH	0	0	0	0	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	FFFFFA72H	0000H

(9) ROM address alternate register L (ISL_ROML)

This register sets the trigger address (lower 16 bits) of execution address match.

It can be read or written in 16-bit units.

Figure 12-14. ROM Address Alternate Register L (ISL_ROML)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ISL_ROML	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	0	0	FFFFFA74H	0000H

(10) ROM address alternate register H (ISL_ROMH)

This register sets the trigger address (upper 16 bits) of execution address match.

It can be read or written in 16-bit units.

Figure 12-15. ROM Address Alternate Register H (ISL_ROMH)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ISL_ROMH	0	0	0	0	0	0	0	0	0	0	0	0	A19	A18	A17	A16	FFFFFA76H	0000H

12.6 Restrictions on NBD

12.6.1 General restrictions

(1) CLK_DBG is 12.5 MHz maximum.

(2) If a command packet is sent during a reset period, "ready" is not returned afterwards. Reset again.

12.6.2 Restrictions related to read or write of RAM by NBD

(1) Initialize DMA in user software.

(2) Writes to RAM are 32-bit fixed-length only.
On a read-only, RAM can be accessed in 32-, 16-, or 8-bit units.
On a read/write, RAM can be accessed in 32-bit units.

(3) NBD does not function from during a reset until DMA initialization after the reset finishes.
If a read or write of RAM is performed in this interval, NBD does not return "ready" afterwards. Reset again.

12.6.3 Restrictions related to NBD event trigger function

(1) If a ROM execution address event trigger is set to the address after a branch instruction, an event is generated due to pipeline processing even if it is not executed. The trigger must be set to an address at least 32 bits x 3 words after a branch instruction.

(2) Since an event trigger is cleared by a reset, it must be set again after a reset.

(3) Unless there is a ROM fetch, a trigger occurs even on a read.

(4) ROM address match functions only for internal ROM.

12.6.4 How to detect termination of DMA initialization externally

Set an event trigger using a RAM write and send a write command from NDB to the relevant address. If an event trigger occurs at this time, DMA initialization has terminated.

12.7 Initialization Required for DMA (2 Channels)

(1) The DMA initialization in a setting change request must be performed by user software.

(2) Assign DMA two channels in NBD.
At this time, assign an NBDAD interrupt to a higher priority channel than an NBDREW interrupt.

(3) Initialize registers of the channel to which the NBDAD interrupt is assigned.
Set contents so that the contents of NBDMSL/NDBMSH and NBDMDL/NBDMDH (read-only SFR) transfer to DMA source address registers nL and nH (DSAnL, DSAnH)[Note] and DMA destination address registers nL and nH (DDAnL, DDAnH)[Note] (n=0 to 3) of the DMA channel assigned to the NBDREW interrupt in 16 bits × 4 blocks.

Note DMA registers are 16-bit access only.

(4) Set DMA addressing control register n (DADCn) of the DMA channel assigned to the NBDREW interrupt for 32-bit transfer (bit transfer settings 8 bits × 4, 16 bits × 2, and 32 bits × 1[Note]) (n=0 to 3). In addition, set the counter direction of the DMA transfer source address and DMA transfer destination address to increment mode (SADm bit of DADCn register = 0, DADm bit = 0 (m=0,1)) (since DMA judges data transfer terminated on reading or writing the uppermost 8 bits).

Note Bits that can be manipulated on 8 bits × 4, 16 bits × 2, and 32 bits × 1 bit transfer are shown below.
8 bits × 4: 32-, 16-, or 8-bit read is possible
16 bits × 2: 16- or 8-bit read is possible.
32 bits × 1: 32-bit read is possible. This is the highest read speed.
Settings other than the above are prohibited. Moreover, make the setting 32 bits × 1 when reading or writing RAM.

Caution In DMA initialization, set the DMA request selection last.

Examples of DMA initialization on 32-bit transfer, 16-bit transfer, and 8-bit transfer are shown below.

(a) Example of 32-bit transfer DMA initialization

```
-- DMA INITIAL  --
  mov       0x0000FA64 ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAH0[r0]
  mov       0x0000F088 ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAH0[r0]
  mov       0x0000400c ,       r24 -- DMACH0 Block MODE 16Bit MODE --
  st.h      r24 , DADC0[r0]
  mov       0x0000800c ,       r24 -- DMACH1 Block MODE 32Bit MODE --
  st.h      r24 , DADC1[r0]
  mov       0x00000003 ,       r24 -- DMACH0 Block MODE 16Bit*4 --
  st.h      r24 , DBC0[r0]
  mov       0x00000000 ,       r24 -- DMACH1 Block MODE 32Bit*1 --
  st.h      r24 , DBC1[r0]
  mov       0x00000009 ,       r24 -- DMACH0&1 DMA ready --
  st.b      r24 , DCHC0[r0]
  st.b      r24 , DCHC1[r0]
  mov       0x00000035 ,       r24 -- DMACH0 Trigger --
  st.b      r24 , DTFR0[r0]
  mov       0x00000036 ,       r24 -- DMACH1 Trigger --
  st.b      r24 , DTFR1[r0]
```

(b) Example of 16-bit transfer DMA initialization

```
-- DMA INITIAL  --
  mov       0x0000FA64 ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAH0[r0]
  mov       0x0000F088 ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAH0[r0]
  mov       0x0000400c ,       r24 -- DMACH0 Block MODE 16Bit MODE --
  st.h      r24 , DADC0[r0]
  mov       0x0000400c ,       r24 -- DMACH1 Block MODE 16Bit MODE -
  st.h      r24 , DADC1[r0]
  mov       0x00000003 ,       r24 -- DMACH0 Block MODE 16Bit*4 --
  st.h      r24 , DBC0[r0]
  mov       0x00000001 ,       r24 -- DMACH1 Block MODE 16Bit*2 --
  st.h      r24 , DBC1[r0]
  mov       0x00000009 ,       r24 -- DMACH0&1 DMA ready --
  st.b      r24 , DCHC0[r0]
  st.b      r24 , DCHC1[r0]
  mov       0x00000035 ,       r24 -- DMACH0 Trigger --
  st.b      r24 , DTFR0[r0]
  mov       0x00000036 ,       r24 -- DMACH1 Trigger --
  st.b      r24 , DTFR1[r0]
```

(c) Example of 8-bit transfer DMA initialization

```
-- DMA INITIAL  --
  mov       0x0000FA64 ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Source      Address --
  st.h      r24 , DSAH0[r0]
  mov       0x0000F088 ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAL0[r0]
  mov       0x00000FFF ,       r24 -- DMACH0 Destination Address --
  st.h      r24 , DDAH0[r0]
  mov       0x0000400c ,       r24 -- DMACH0 Block MODE 16Bit MODE --
  st.h      r24 , DADC0[r0]
  mov       0x0000000c ,       r24 -- DMACH1 Block MODE 8Bit MODE -
  st.h      r24 , DADC1[r0]
  mov       0x00000003 ,       r24 -- DMACH0 Block MODE 16Bit*4 --
  st.h      r24 , DBC0[r0]
  mov       0x00000003 ,       r24 -- DMACH1 Block MODE 8Bit*4 --
  st.h      r24 , DBC1[r0]
  mov       0x00000009 ,       r24 -- DMACH0&1 DMA ready --
  st.b      r24 , DCHC0[r0]
  st.b      r24 , DCHC1[r0]
  mov       0x00000035 ,       r24 -- DMACH0 Trigger --
  st.b      r24 , DTFR0[r0]
  mov       0x00000036 ,       r24 -- DMACH1 Trigger --
  st.b      r24 , DTFR1[r0]
```

CHAPTER 13 A/D CONVERTER

13.1 Features

- Two 10-bit resolution on-chip A/D converters (A/D converter 0 and 1)
  Simultaneous sampling by two circuits is possible.
- Analog input: 8 channels per circuit
- On-chip A/D conversion result registers 0n, 1n (ADCR0n, ADCR1n)
  10 bits × 8 registers × 2
- A/D conversion trigger mode
  A/D trigger mode
  A/D trigger polling mode
  Timer trigger mode
  External trigger mode
- Successive approximation technique
- Voltage detection mode

Remark n = 0 to 7

13.2 Configuration

A/D converters 0 and 1, which employ a successive approximation technique, perform A/D conversion operation using A/D scan mode registers 00, 01, 10, and 11 (ADSCM00, ADSCM01, ADSCM10, and ADSCM11) and registers ADCR0n and ADCR1n (n = 0 to 7).

(1) Input circuit

The input circuit selects an analog input (ANI0n or ANI1n) according to the mode set in the ADSCM00 or ADSCM10 register and sends it to the sample and hold circuit (n=0 to 7).

(2) Sample and hold circuit

The sample and hold circuit individually samples analog inputs sent sequentially from the input circuit and sends them to the comparator. It holds sampled analog inputs during A/D conversion.

(3) Voltage comparator

The voltage comparator compares the analog input voltage that was input with the output voltage of the D/A converter.

(4) D/A converter

The D/A converter is used to generate a voltage that matches an analog input.

The output voltage of the D/A converter is controlled by the successive approximation register (SAR).

(5) Successive approximation register (SAR)

The SAR is a 10-bit register that controls the output value of the D/A converter for comparing with an analog input voltage value. When an A/D conversion terminates, the current contents of the SAR (conversion result) are stored in an A/D conversion result register (ADCR0n, ADCR1n) (n = 0 to 7). When all specified A/D conversions terminate, there also is an A/D conversion termination interrupt (INTAD0, INTAD1).

(6) A/D conversion result registers 0n, 1n

ADCR0n and ADCR1n are 10-bit registers that hold A/D conversion results (n = 0 to 7). Whenever an A/D conversion terminates, the conversion result from the successive approximation register (SAR) is loaded.

$\overline{\text{RESET}}$ input sets this to 0000H.

(7) Controller

The controller selects an analog input, generates sample and hold circuit operation timing, controls conversion triggers, specifies the conversion operation time, and sets the low power consumption mode according to the mode set in the ADSCMn0 or ADSCMn1 register.

(8) ANI0n, ANI1n pins (n = 0 to 7)

The ANI0n and ANI1n pins are the 8-channel (total of 16 channels for two circuits) analog input pins to analog converters 0 and 1. They input analog signals to A/D convert.

Caution Use input voltages to ANI0n and ANI1n that are within the range of the ratings. In particular, if a voltage higher than AV_{DD} or lower than AV_{SS} (even one within the range of absolute maximum ratings) is input, the conversion value of that channel is undefined, and the conversion values of other channels also may be affected.

(9) AV_{REF0}, AV_{REF1} pins

The AV_{REF0} and AV_{REF1} pins are used to input reference voltages to A/D converters 0 and 1. A signal input to the ANI0n or ANI1n pin is converted to a digital signal based on the voltage applied between AV_{REF0} and AV_{SS} or between AV_{REF1} and AV_{SS} (n = 0 to 7).

Caution If not using the AV_{REF0} or AV_{REF1} pin, connect it to V_{SS5}.

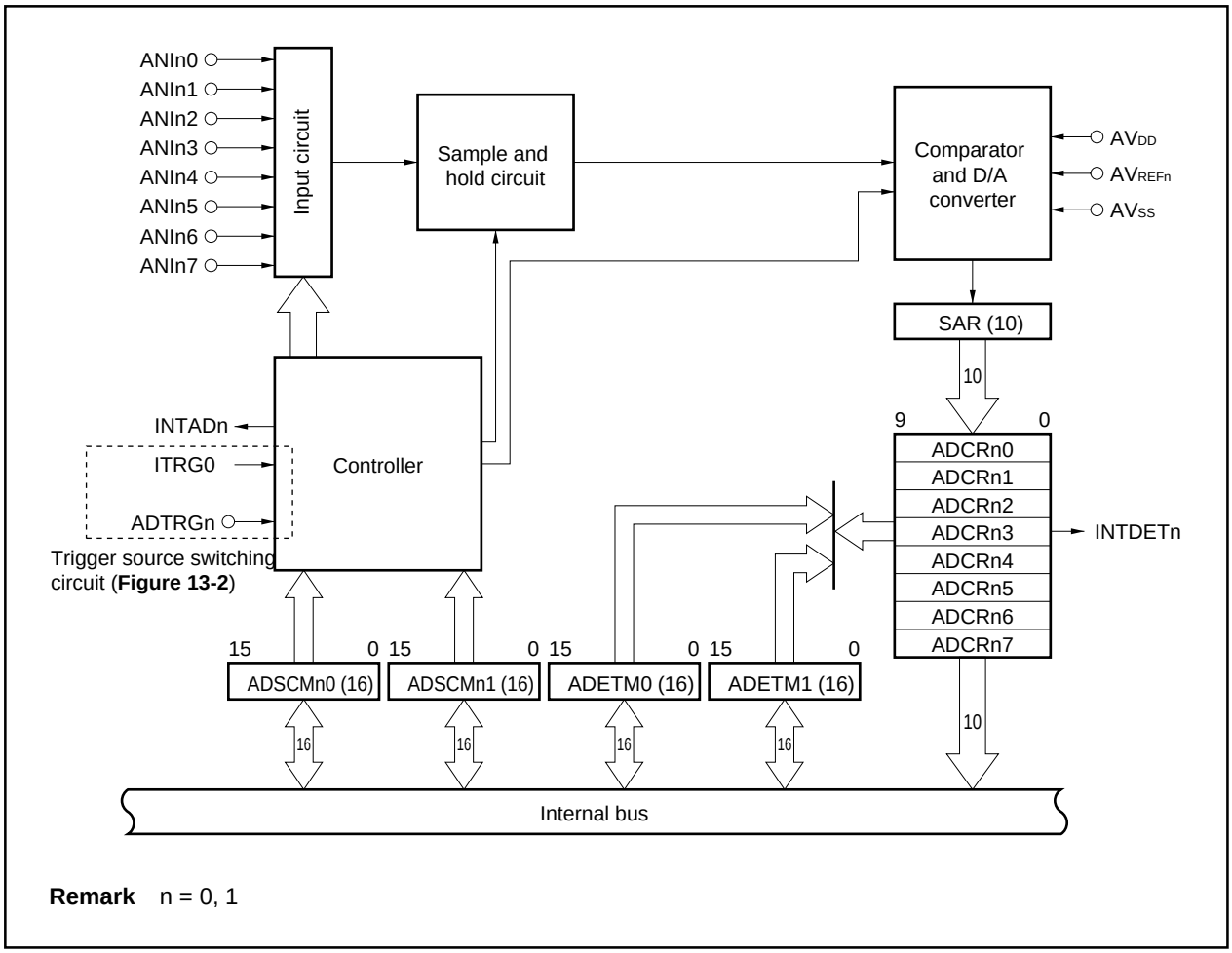
(10) AV_{SS} pin

The AVSS pin is the ground voltage pin of A/D converters 0 and 1. Even if not using A/D converters 0 and 1, always make this pin have the same potential as the V_{SS5} pin.

(11) AV_{DD} pin

The AV_{DD} pin is the analog power supply pin of A/D converters 0 and 1. Even if not using A/D converters 0 and 1, always make this pin have the same potential as the V_{DD5} pin.

Figure 13-1. Block Diagram of A/D Converter 0 or 1



Remark n = 0, 1

Caution 1. Noise at an analog input pin (ANI0n, ANI1n) or reference voltage input pin (AV_{REF0}, AV_{REF1}) may give rise to an invalid conversion result.

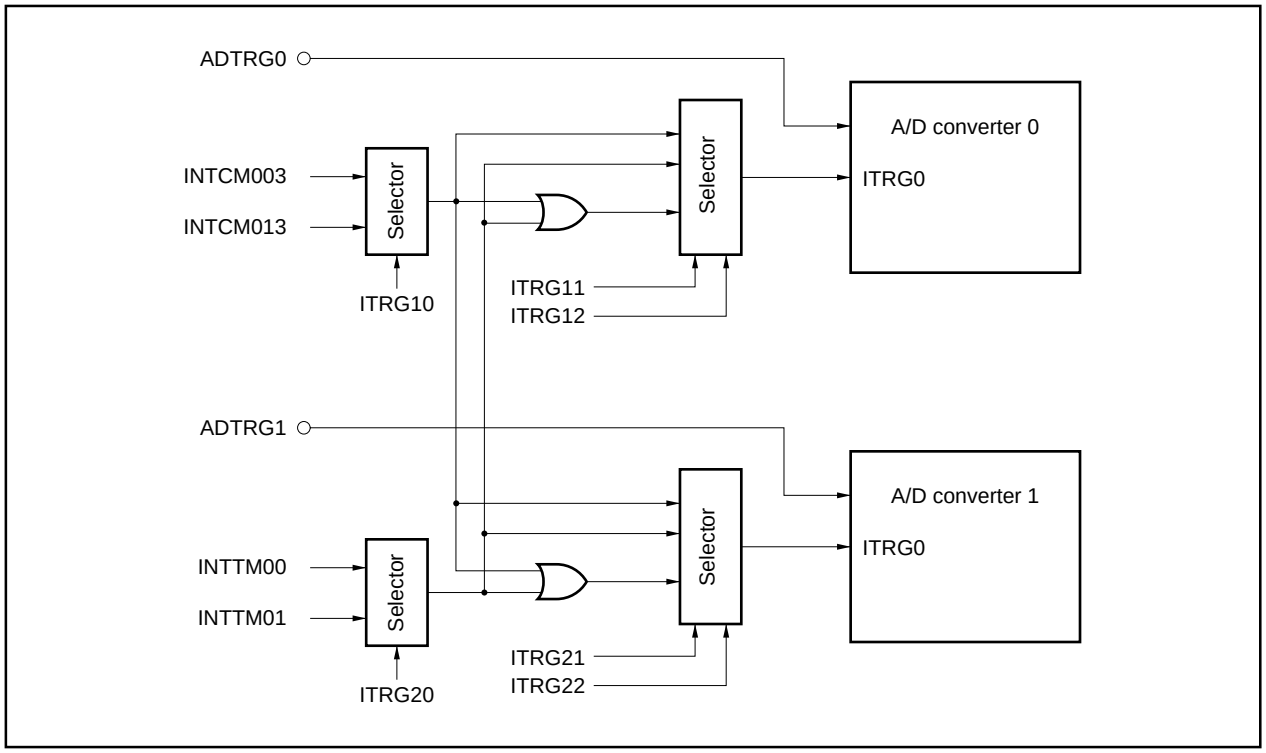
Software processing is needed in order to prevent this invalid conversion result from adversely affecting the system.

The following are examples of software processing.

- **Use the average value of the results of multiple A/D conversions as the A/D conversion result.**
- **Perform A/D conversion multiple consecutive times and use conversion results with the exception of any abnormal conversion results that are obtained.**
- **If an A/D conversion result from which it is judged that an abnormality occurred in the system is obtained, do not perform abnormality processing at once but perform it upon reconfirming the occurrence of an abnormality.**

2. Be sure that voltages outside the range [AV_{SS} to AV_{REF0}, AV_{SS} to AV_{REF1}] are not applied to pins being used as A/D converter 0 and 1 input pins.

Figure 13-2. Block Diagram of Trigger Source Switching Circuit



13.3 Control Registers

(1) A/D scan mode registers 00 and 10 (ADSCM00, ASDSCM10)

The ADSCMn0 registers are 16-bit registers that select analog input pins, specify operation modes, and control conversion operation.

They can be read or written in 16-, 8-, or 1-bit units. However, writing to an ADSCMn0 register during A/D conversion operation initializes conversion operation and starts the conversion over from the beginning.

Figure 13-3. A/D Scan Mode Registers 00 and 10 (ADSCM00 and ADSCM10) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADSCM00	CE	CS	0	MS	PLM	TRG2	TRG1	TRG0	SANI3	SANI2	SANI1	SANI0	ANIS3	ANIS2	ANIS1	ANIS0	FFFFF200H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADSCM10	CE	CS	0	MS	PLM	TRG2	TRG1	TRG0	SANI3	SANI2	SANI1	SANI0	ANIS3	ANIS2	ANIS1	ANIS0	FFFFF240H	0000H

Bit position	Bit name	Function
15	CE	Specifies enabling or disabling A/D conversion. 0: Disable 1: Enable
14	CS	Shows status of A/D converter 0 or 1. This bit is read-only. 0: Stopped 1: Operating
12	MS	Specifies operation mode of A/D converter 0 or 1. 0: Scan mode 1: Select mode
11 to 8	PLM, TRG2 to TRG0	PLM: Specifies polling mode. TRG2-TRG0: Specifies trigger mode.

PLM	TRG2	TRG1	TRG0	Trigger Mode
0	0	0	0	A/D trigger mode
0	0	0	1	Timer trigger mode
0	1	1	1	External trigger mode
1	0	0	0	A/D trigger polling mode
Other than above				Setting prohibited

Figure 13-3. A/D Scan Mode Registers 00 and 01 (ADSCM00 and ADSCM10) (2/2)

<table>
<tr><th>Bit position</th><th>Bit name</th><th>Function</th></tr>
<tr><td>7 to 4</td><td>SANI3 to SANI0</td><td>Specifies conversion start analog input pin in scan mode.
These bits are ignored in select mode.

<table>
<tr><th>SANI3</th><th>SANI2</th><th>SANI1</th><th>SANI0</th><th>Scan Start Analog Input Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>ANIn0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>ANIn1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>ANIn2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>ANIn3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ANIn4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>ANIn5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>ANIn6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>ANIn7</td></tr>
<tr><td colspan="4">Other than above</td><td>Setting prohibited</td></tr>
</table>

Caution Always set the conversion start analog input pin number that is set by bits SANI3-SANI0 to a smaller pin number than the conversion end analog input pin number that is set by bits ANIS3-ANIS0.</td></tr>
<tr><td>7 to 4</td><td>ANIS3 to ANIS0</td><td>Specifies analog input pin in select mode.
In scan mode, specifies conversion termination analog input pin and sets number of conversions.

<table>
<tr><th>ANIS3</th><th>ANIS2</th><th>ANIS1</th><th>ANIS0</th><th>In Select Mode</th><th>In Scan Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>ANIn0</td><td>ANIn0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>ANIn1</td><td>SANI → ANIn1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>ANIn2</td><td>SANI → ANIn2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>ANIn3</td><td>SANI → ANIn3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ANIn4</td><td>SANI → ANIn4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>ANIn5</td><td>SANI → ANIn5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>ANIn6</td><td>SANI → ANIn6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>ANIn7</td><td>SANI → ANIn7</td></tr>
<tr><td colspan="4">Other than above</td><td colspan="2">Setting prohibited</td></tr>
</table>

Remarks 1. n = 0, 1
2. SANI < ANInm
m = 1 to 7</td></tr>
</table>

(2) A/D scan mode registers 01 and 11 (ADSCM01, ADSCM11)

The ADSCMn1 registers are 16-bit registers that set the conversion time of the A/D converter.
They can be read or written in 16-, 8-, or 1-bit units.

Caution Do not write to the ADSCMn1 registers during A/D conversion operation. If a write is performed, conversion operation is suspended and subsequently terminates.

Figure 13-4. A/D Scan Mode Registers 01 and 11 (ADSCM01 and ADSCM11)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADSCM01	0	0	0	0	0	FR2	FR1	FR0	0	0	0	0	0	0	0	0	FFFFF202H	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADSCM11	0	0	0	0	0	FR2	FR1	FR0	0	0	0	0	0	0	0	0	FFFFF242H	0000H

Bit position	Bit name	Function
10 to 8	FR2 to FR0	Specifies conversion time.

FR2	FR1	FR0	Conversion Clocks	Conversion Time (μs)[Note]		
				ϕ = 50 MHz	ϕ = 40 MHz	ϕ = 33 MHz
0	0	0	336	6.72	8.40	10.2
0	0	1	240	–	6.00	7.27
0	1	0	168	–	–	5.09
0	1	1	120	–	–	–
1	0	0	96	–	–	–
1	0	1	72	–	–	–
1	1	0	48	–	–	–
1	1	1	Setting prohibited	–	–	

Note This is the time from sampling until conversion termination.

Caution Be sure the conversion time is at least 6 μs.
Conversion time = ϕ × Conversion clocks

Remark ϕ: Internal system clock

(3) A/D voltage detection mode registers 0 and 1 (ADETM0, ADETM1)

The ADETMn registers are 16-bit registers that set voltage detection mode. In voltage detection mode, the analog input pin for which voltage detection is being performed and a reference voltage value are compared and an interrupt is set in response to the comparison result.

These registers be read or written in 16-, 8-, or 1-bit units.

Caution Do not write to an ADETMn register during A/D conversion operation. If a write is performed, conversion is suspended and it subsequently terminates.

Figure 13-5. A/D Voltage Detection Mode Registers 0 and 1 (ADETM0 and ADETM1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADETM0	DETEN	DETLH	DETANI3	DETANI2	DETANI1	DETANI0	DETCMP9	DETCMP8	DETCMP7	DETCMP6	DETCMP5	DETCMP4	DETCMP3	DETCMP2	DETCMP1	DETCMP0	FFFFF204	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADETM1	DETEN	DETLH	DETANI3	DETANI2	DETANI1	DETANI0	DETCMP9	DETCMP8	DETCMP7	DETCMP6	DETCMP5	DETCMP4	DETCMP3	DETCMP2	DETCMP1	DETCMP0	FFFFF244	0000H

Bit position	Bit name	Function
15	DETEN	Specifies voltage detection mode. 0: Operate in normal mode 1: Operate in voltage detection mode
14	DETLH	Sets voltage comparison detection. 0: Generate INTDETn interrupt if reference voltage value > analog input pin voltage. 1: Generate INTDETn interrupt if reference voltage value < analog input pin voltage. **Remark** n = 0, 1
13 to 10	DETANI3 to DETANI0	Selects analog input pin to compare to reference voltage value set by DETCMP9-DETCMP0 when in voltage detection mode.
9 to 0	DETCMP9 to DETCMP0	Sets reference voltage value to compare with analog input pin selected in DETANI3-DETANI0.

DETANI3	DETANI2	DETANI1	DETANI0	Voltage Detection Analog Input Pin
0	0	0	0	ANIn0
0	0	0	1	ANIn1
0	0	1	0	ANIn2
0	0	1	1	ANIn3
0	1	0	0	ANIn4
0	1	0	1	ANIn5
0	1	1	0	ANIn6
0	1	1	1	ANIn7
1	×	×	×	Setting prohibited

Remark n = 0, 1
×: Arbitrary

(4) A/D conversion result registers 00 to 07 and 10 to 17 (ADCR00 to ADCR07, ADCR10 to ADCR17)

The ADCR0n and ADCR1n registers are 10-bit registers that hold the results of A/D conversions (n = 0 to 7). One A/D converter is equipped with eight 10-bit registers for 8 channels, and A/D converters 0 and 1 together have sixteen 10-bit registers.

These can only be read in 16-bit units.

When reading 10 bits of data of an A/D conversion result from an ADCR0n or ADCR1n register, only the lower 10 bits are valid and the upper 6 bits always read 0.

Figure 13-6. A/D Conversion Result Registers 00 to 07 and 10 to 17 (ADCR00 to ADCR07 and ADCR10 to ADCR17)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADCR0n	0	0	0	0	0	0	ADCRn9	ADCRn8	ADCRn7	ADCRn6	ADCRn5	ADCRn4	ADCRn3	ADCRn2	ADCRn1	ADCRn0	See **Table 13-1**	0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial value
ADCR1n	0	0	0	0	0	0	ADCRn9	ADCRn8	ADCRn7	ADCRn6	ADCRn5	ADCRn4	ADCRn3	ADCRn2	ADCRn1	ADCRn0	See **Table 13-2**	0000H

Table 13-1. Correspondence Between ADCR0n (n = 0 to 7) Register Names and Addresses

Register name	Address
ADCR00	FFFFF210
ADCR01	FFFFF212
ADCR02	FFFFF214
ADCR03	FFFFF216
ADCR04	FFFFF218
ADCR05	FFFFF21A
ADCR06	FFFFF21C
ADCR07	FFFFF21E

Table 13-2. Correspondence Between ADCR1n (n = 0 to 7) Register Names and Addresses

Register name	Address
ADCR10	FFFFF250
ADCR11	FFFFF252
ADCR12	FFFFF254
ADCR13	FFFFF256
ADCR14	FFFFF258
ADCR15	FFFFF25A
ADCR16	FFFFF25C
ADCR17	FFFFF25E

The correspondence between each analog input pin and the ADCR0n and ADCR1n registers is shown below.

Table 13-3. Correspondence Between Each Analog Input Pin and ADCR0n and ADCR1n Registers

A/D Converter	Analog Input Pin	A/D Conversion Result Register
A/D converter 0	ANI00	ADCR00
	ANI01	ADCR01
	ANI02	ADCR02
	ANI03	ADCR03
	ANI04	ADCR04
	ANI05	ADCR05
	ANI06	ADCR06
	ANI07	ADCR07
A/D converter 1	ANI10	ADCR10
	ANI11	ADCR11
	ANI12	ADCR12
	ANI13	ADCR13
	ANI14	ADCR14
	ANI15	ADCR15
	ANI16	ADCR16
	ANI17	ADCR17

(5) A/D internal trigger selection register (ITRG0)

The ITRG0 register is the register that switches the trigger source in timer trigger mode. The timer trigger source of A/D converters 0 and 1 can be set using the ITRG0 register.

This register can be read or written in 8- or 1-bit units.

Figure 13-7. A/D Internal Trigger Selection Register (ITRG0)

	7	6	5	4	3	2	1	0	Address	Initial value
ITRG0	0	ITRG22	ITRG21	ITRG20	0	ITRG12	ITRG11	ITRG10	FFFFF280H	00H

Bit position	Bit name	Function
6 to 4	ITRG22 to ITRG20	Sets timer trigger source of A/D converter 1.

ITRG22	ITRG21	ITRG20	ITRG10	Trigger Source
0	0	×	0	Select INTCM003
0	0	×	1	Select INTCM013
0	1	0	×	Select INTTM00
0	1	1	×	Select INTTM01
1	×	0	0	Select INTCM003 and INTTM00
1	×	0	1	Select INTCM013 and INTTM00
1	×	1	0	Select INTCM003 and INTTM01
1	×	1	1	Select INTCM013 and INTTM01

Remark ×: Arbitrary

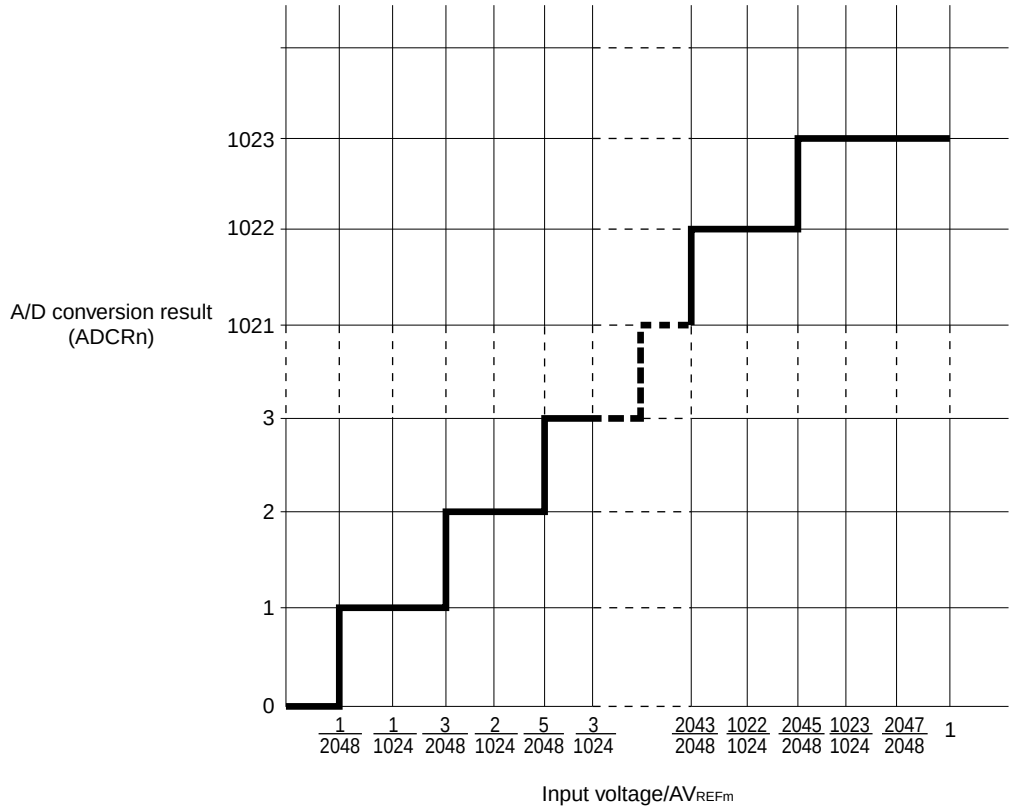
Bit position	Bit name	Function
2 to 0	ITRG12 to ITRG10	Specifies timer trigger source of A/D converter 0.

ITRG12	ITRG11	ITRG20	ITRG10	Trigger Source
0	0	×	0	Select INTCM003
0	0	×	1	Select INTCM013
0	1	0	×	Select INTTM000
0	1	1	×	Select INTTM001
1	×	0	0	Select INTCM003 and INTTM00
1	×	0	1	Select INTCM013 and INTTM00
1	×	1	0	Select INTCM003 and INTTM01
1	×	1	1	Select INTCM013 and INTTM01

Remark ×: Arbitrary

The following figure shows the relationship between analog input voltages and A/D conversion results.

Figure 13-8. Relationship Between Analog Input Voltages and A/D Conversion Results



Remark m = 0, 1

n = 00 to 07, 10 to 17

13.4 Interrupt Requests

A/D converters 0 and 1 generate two kinds of interrupts.

- A/D conversion termination interrupts (INTAD0, INTAD1)
- Voltage detection interrupts (INTDET0, INTDET1)

(1) A/D conversion termination interrupts (INTAD0, INTAD1)

In A/D conversion enabled status, an A/D conversion termination interrupt is generated when a specified number of A/D conversions have terminated.

A/D converter	A/D Conversion Termination Interrupt Signal
0	Generate INTAD0
1	Generate INTAD1

(2) Voltage detection interrupt (INTDET0, INTDET1)

In voltage detection mode (DETEN bit of ADETM0 or ADETM1 = 1), the value of the ADCR0n or ADCR1n register of the relevant analog input pin is compared to the reference voltage set in the DETCMP9-DETCMP0 bits of the ADETM0 or ADETM1 register and a voltage detection interrupt is generated in response to the value of the DETLH bit of the ADETM0 or ADETM1 register (n = 0 to 7).

A/D converter	A/D Conversion Termination Interrupt Signal
0	Generate INTDET0
1	Generate INTDET1

13.5 A/D Converter Operation

13.5.1 A/D converter basic operation

A/D conversion is performed using the following procedure.

(1) Set the analog input selection and the operation mode and trigger mode specifications using the ADSCM00 or ADSCM10 register[Note 1]. Setting (1) the CE bit of the ADSCM00 or ADSCM10 register when in A/D trigger mode or A/D trigger polling mode starts A/D conversion. In timer trigger mode or external trigger mode, the status becomes trigger standby[Note 2].

(2) When A/D conversion starts, compare the analog input to the voltage generated by the D/A converter.

(3) When 10-bit comparison terminates, store the conversion result in the ADCR0n or ADCR1n register. When the specified number of A/D conversions have terminated, generate an A/D conversion termination interrupt (INTAD0, INTAD1) (n = 0 to 7).

Notes 1. If the contents of the ADSCM00 or ADSCM10 register are changed during A/D conversion operation, the A/D conversion operation preceding the change stops and a conversion result is not stored in the ADSCR0n or ADSCR1n register. Conversion operation is initialized and conversion starts from the beginning.

2. In timer trigger mode or external trigger mode, there is a transition to trigger standby status when the CE0 or CE1 bit of the ADSCM00 or ADSCM10 register is set to 1. A/D conversion operation is activated by a trigger signal and there is a return to trigger standby status when A/D conversion operation terminates.

13.5.2 Operation modes and trigger modes

Diverse conversion operations can be specified for A/D converters 0 and 1 by specifying operation modes and trigger modes. Operation modes and trigger modes are set using the ADSCM00 or ADSCM10 register.

The relationship between operation modes and trigger modes is shown below.

Trigger Mode	Operation Mode	Setting	
		ADSCM00	ADSCM10
AD trigger	Select	XX010000XXXXXXXXB	XX010000XXXXXXXXB
	Scan	XX000000XXXXXXXXB	XX000000XXXXXXXXB
AD trigger polling	Select	XX011000XXXXXXXXB	XX011000XXXXXXXXB
	Scan	XX001000XXXXXXXXB	XX001000XXXXXXXXB
Timer trigger	Select	XX010001XXXXXXXXB	XX010001XXXXXXXXB
	Scan	XX000001XXXXXXXXB	XX000001XXXXXXXXB
External trigger	Select	XX010111XXXXXXXXB	XX010111XXXXXXXXB
	Scan	XX000111XXXXXXXXB	XX000111XXXXXXXXB

(1) Trigger modes

The four trigger modes that serve as the start timing of A/D conversion processing are available: A/D trigger mode, A/D trigger polling mode, timer trigger mode, and external trigger mode.

These trigger modes are set using the ADSCM00 and ADSCM10 registers.

(a) A/D trigger mode

A/D trigger mode, which starts the conversion timing for the analog input set for the ANI0n or ANI1n pin (n = 0 to 7), is a mode that starts A/D conversion by setting the CE bit of the ADSCM00 or ADSCM10 register to 1. In this mode, it is necessary to set the CE bit to 1 as an A/D conversion restart operation after an INTAD0 or INTAD1 interrupt (CS = 0).

(b) A/D trigger polling mode

A/D trigger polling mode, which starts the conversion timing of the analog input set for the ANI0n or ANI1n pin (n = 0 to 7), is a mode that starts A/D conversion by setting the CE bit of the ADSCM00 or ADSCM10 register to 1. In this mode, it is not necessary to set the CE bit to 1 as an A/D conversion restart operation after an INTAD0 or INTAD1 interrupt (CS = 1). The specified analog input is converted serially until the CE bit is set to 0. An INTAD0 or INTAD1 interrupt occurs each time a conversion terminates.

(c) Timer trigger mode

Timer trigger mode, which starts the conversion timing of the analog input set for the ANI0n or ANI1n pin (n=0-7), is a mode governed by a trigger specified in the trigger selection register (ITRG0).

(d) External trigger mode

External trigger mode, which starts the conversion timing of the analog input set using the ANI pins[Note], is a mode specified using the ADTRG0 or ADTRG1 pin.

Note External trigger select mode: ANI00 to ANI07, ANI10 to ANI17
External trigger scan mode: ANI00 to ANI03, ANI10 to ANI12

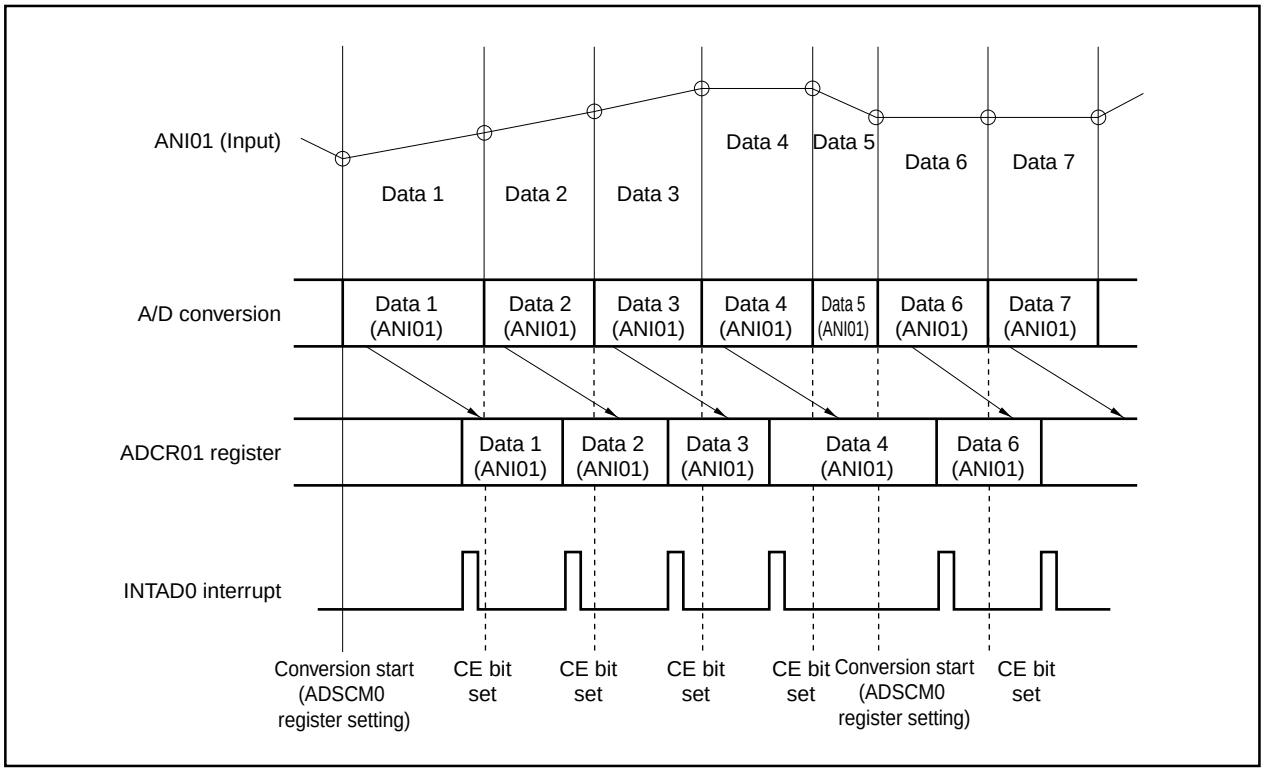
(2) Operation modes

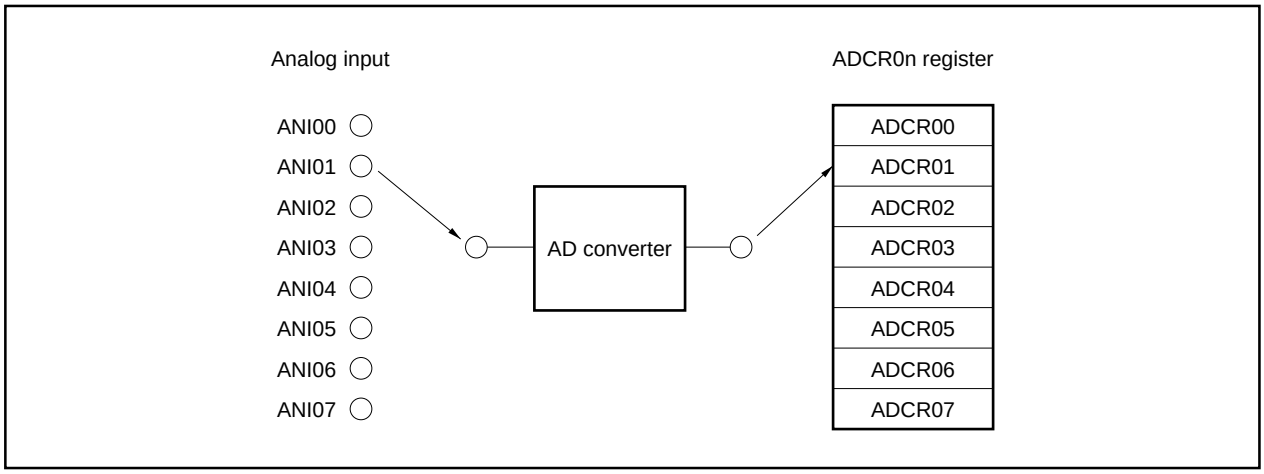
The two operation modes, which are the modes that set the ANI00 to ANI07 and ANI10 to ANI17 pins, are select mode and scan mode. These modes are set using the ADSCM00 and ADSCM10 registers.

(a) Select mode

Select mode A/D converts one analog input specified in the ADSCM00 or ADSCM10 register. It stores the conversion result in the ADCR0n or ADCR1n register corresponding to the analog input (ANI1n or ANI0n) (n = 0 to 7).

Figure 13-9. Example of Select Mode Operation Timing (ANI01): For A/D Converter 0





(b) Scan mode

Scan mode sequentially selects and A/D converts pins from the A/D conversion start analog input pin through the A/D conversion termination analog input pin specified in the ADSCM00 or ADSCM10 register. It stores the A/D conversion result in the ADCR0n or ADCR1n register corresponding to the analog input (n = 0 to 7). When the specified analog input conversion terminates, there is an A/D conversion termination interrupt (INTAD0 or INTAD1).

Figure 13-10. Example of Scan Mode Operation Timing: For A/D Converter 0 (4-Channel Scan (ANI00 to ANI03)) (1/2)

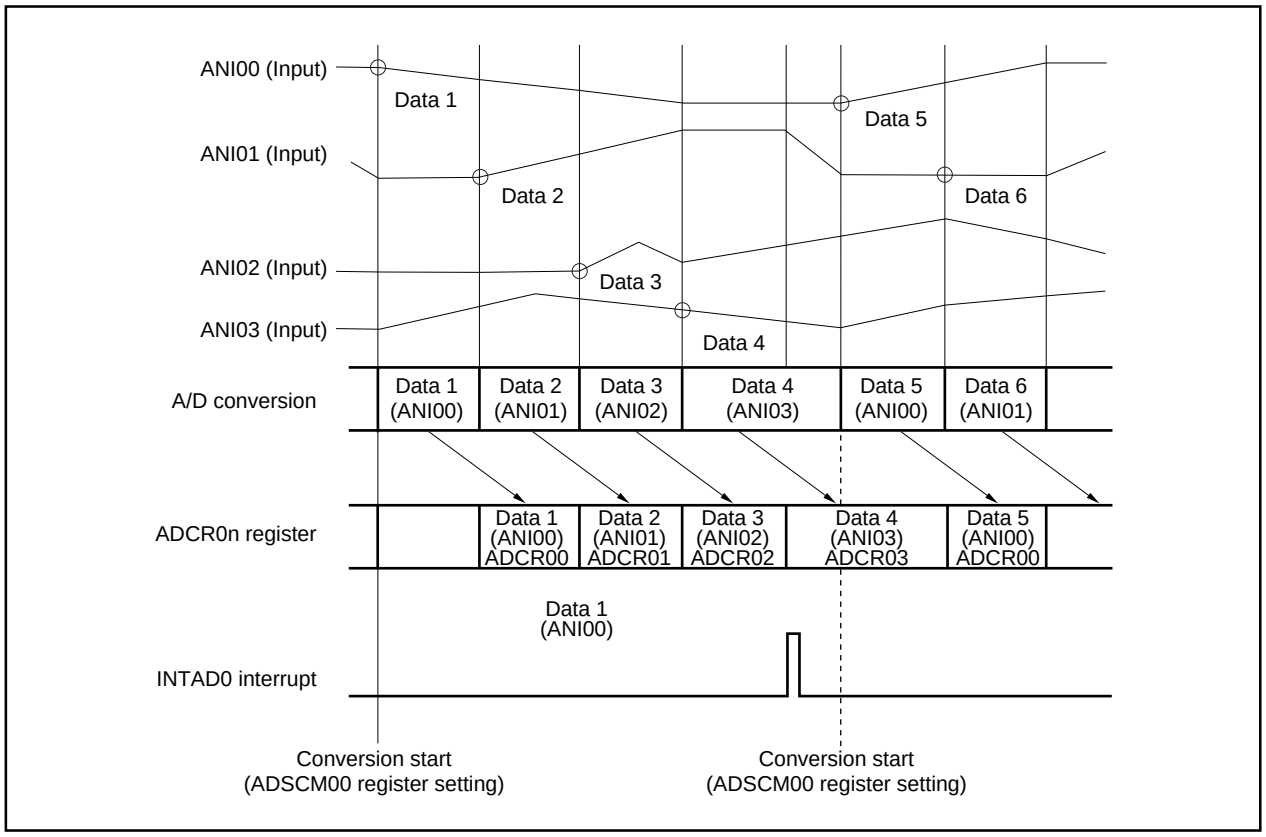
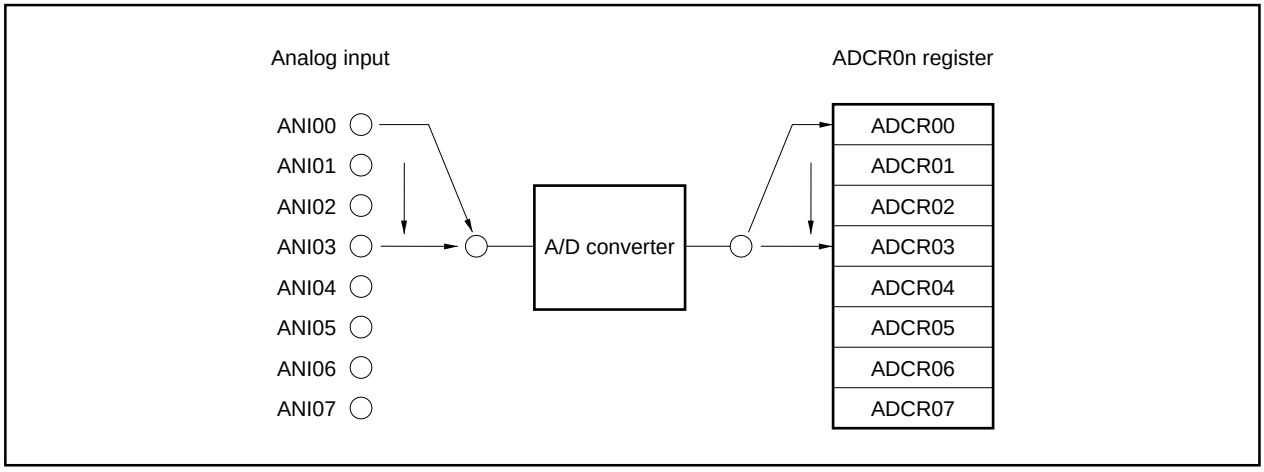


Figure 13-10. Example of Scan Mode Operation Timing: For A/D Converter 0 (4-Channel Scan (ANI00 to ANI03)) (2/2)



13.6 Operation in A/D Trigger Mode

Setting the CE bit of the ADSCM00 or ADSCM10 register to 1 starts A/D conversion.

13.6.1 Operation in select mode

One analog input specified in the ADSCM00 or ADSCM10 register is A/D converted at a time and the result is stored in an ADCR0n or ADCR1n register. Analog inputs correspond one-to-one with ADCR0n or ADCR1n registers (n = 0 to 7).

An A/D conversion termination interrupt (INTAD0, INTAD1) is generated for each A/D conversion termination, which terminates A/D conversion (CS bit = 0).

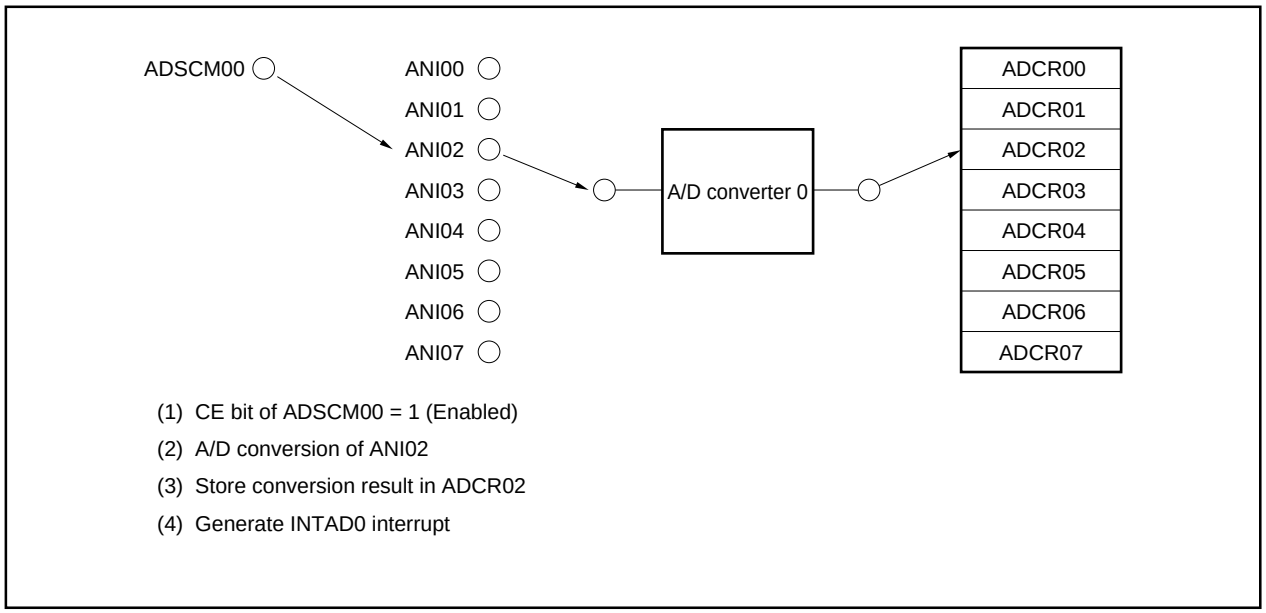
Analog input	A/D conversion result register
ANIn	ADCRn

RemarK n = 00 to 07, 10 to 17

To restart A/D conversion, write 1 in the CE bit of the ADSCM00 or ADSCM10 register.

This is optimal for an application that reads a result for each A/D conversion.

Figure 13-11. Example of Select Mode (A/D Trigger Select) Operation (ANI02): For A/D Converter 0



13.6.2 Operation in scan mode

Pins from the conversion start analog input pin through the conversion termination analog input pin specified in the ADSCM00 or ADSCM10 register are sequentially selected and A/D converted. An A/D conversion result is stored in the ADCR0n or ADCR1n register corresponding to the analog input (n = 0 to 7). When conversion terminates for all analog inputs through the conversion termination analog input pin, an A/D conversion termination interrupt (INTAD0, INTAD1) is generated, which terminates A/D conversion (CS bit of ADSCM0 or ADSCM1 register = 0).

Analog input	A/D conversion result register
ANIn[Note 1]	ADCRn
|	|
ANIn[Note 2]	ADCRn

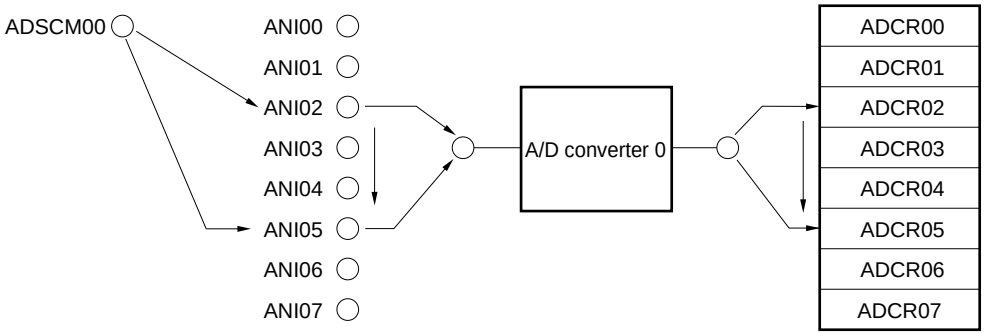
Notes 1. Set using SANI3 to SANI0 bits of ADSCM00 or ADSCM10 register.
Be sure to set a pin number that is smaller than the conversion termination analog input pin number set according to Note 2.

2. Set using ANIS3 to ANIS0 bits of ADSCM00 or ADSCM10 register.

Remark n = 00 to 07, 10 to 17

To restart A/D conversion, write 1 in the CE bit of the ADSCM00 or ADSCM10 register. This is optimal for an application that regularly monitors multiple analog inputs.

Figure 13-12. Example of Scan Mode (A/D Trigger Scan) Operation (ANI02-ANI05): For A/D Converter 0



(1) CE bit of ADSCM00 = 1 (Enabled)
(2) A/D conversion of ANI02
(3) Store conversion result in ADCR02
(4) A/D conversion of ANI03
(5) Store conversion result in ADCR03
(6) A/D conversion of ANI04
(7) Store conversion result in ADCR04
(8) A/D conversion of ANI05
(9) Store conversion result in ADCR05
(10) Generate INTAD0 interrupt

13.7 Operation in A/D Trigger Polling Mode

Setting the CE bit of the ADSCM00 or ADSCM10 register to 1 starts A/D conversion.

Both select mode and scan mode are available in A/D trigger polling mode. Since the CS bit of the ADSCM00 or ADSCM10 register remains 1 after an INTAD0 or INTAD1 interrupt in this mode, it is not necessary to write 1 in the CE bit as an A/D conversion restart operation.

13.7.1 Operation in select mode

The analog input specified in the ADSCM00 or ADSCM10 register is A/D converted. The conversion result is stored in the ADCR0n or ADCR1n register (n = 0 to 7).

One analog input is A/D converted at a time and the result is stored in one ADCR0n or ADCR1n register. Analog inputs correspond one-to-one with ADCR0n or ADCR1n registers.

An A/D conversion termination interrupt (INTAD0 or INTAD1) is generated for each A/D conversion termination. A/D conversion operation is repeated until the CE bit = 0 (CS bit = 1).

Analog input	A/D conversion result register
ANIn	ADCRn

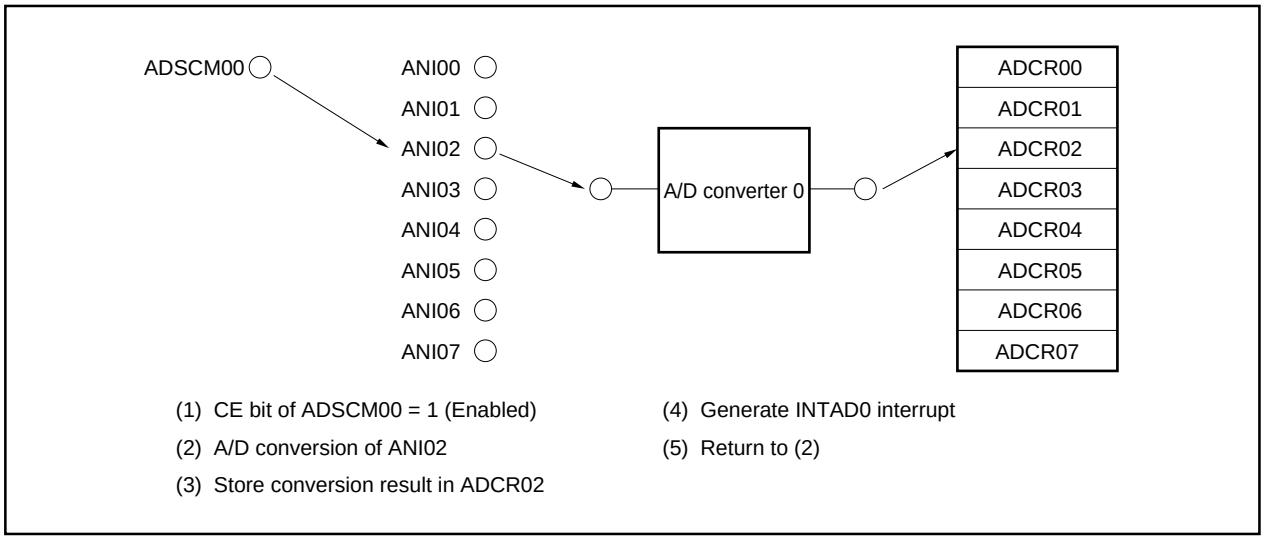
Remark n = 00 to 07, 10 to 17

In A/D trigger polling mode, it is not necessary to write 1 in the CE bit of the ADSCM00 or ADSCM10 register as an A/D conversion restart operation[Note].

This is optimal for applications that regularly read A/D conversion values.

Note In A/D trigger polling mode, the fact that the CE bit of the ADSCM00 or ADSCM10 register is 0 means that A/D conversion operation does not stop as long as the CS bit is not 0. Therefore, if the ADCR0n or ADCR1n register is not read before the next A/D conversion, it is overwritten.

Figure 13-13. Example of Select Mode (A/D Trigger Polling Select) Operation (ANI02): For A/D Converter 0



13.7.2 Operation in scan mode

Pins from the conversion start analog input pin through the conversion termination analog input pin specified in the ADSCM00 or ADSCM10 register are sequentially selected and A/D converted. An A/D conversion result is stored in the ADCR0n or ADCR1n register corresponding to the analog input (n = 0 to 7). When conversion terminates for all analog inputs through the conversion termination analog input pin, an A/D conversion termination interrupt (INTAD0, INTAD1) is generated. A/D conversion operation repeats until the CE bit = 0 (CS bit = 1).

Analog input	A/D conversion result register
ANIn[Note 1]	ADCRn
|	|
ANIn[Note 2]	ADCRn

Notes 1. Set using SANI3 to SANI0 bits of ADSCM00 or ADSCM10 register.
Be sure to set a pin number that is smaller than the conversion termination analog input pin number set according to Note 2.

2. Set using ANIS3 to ANIS0 of ADSCM00 or ADSCM10 register.

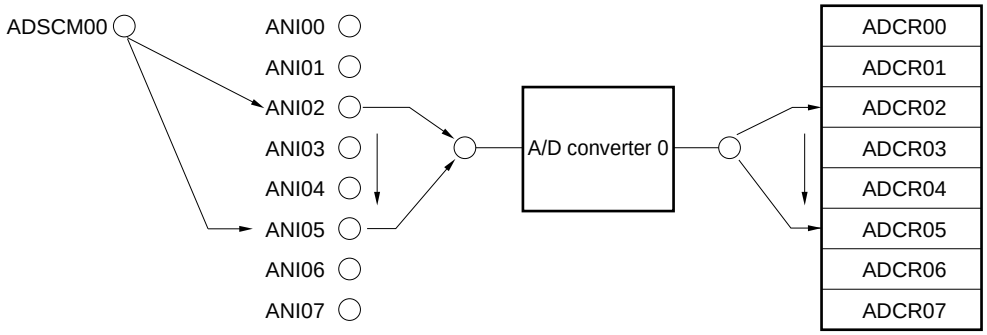
Remark n = 00 to 07, 10 to 17

It is not necessary to write 1 in the CE bit of the ADSCM00 or ADSCM10 register as an A/D conversion restart operation in A/D trigger polling mode[Note].

This is optimal for applications that regularly read A/D conversion values.

Note In A/D trigger polling mode, the fact that the CE bit of the ADSCM00 or ADSCM10 register is 0 means that A/D conversion operation does not stop as long as the CS bit is not 0. Therefore, if the ADCR0n or ADCR1n register is not read before the next A/D conversion, it is overwritten.

Figure 13-14. Example of Scan Mode (A/D Trigger Polling Scan) Operation (ANI02 to ANI05) : For A/D Converter 0



(1) CE bit of ADSCM00 = 1 (Enabled)
(2) A/D conversion of ANI02
(3) Store conversion result in ADCR02
(4) A/D conversion of ANI03
(5) Store conversion result in ADCR03
(6) A/D conversion of ANI04
(7) Store conversion result in ADCR04
(8) A/D conversion of ANI05
(9) Store conversion result in ADCR05
(10) Generate INTAD0 interrupt
(11) Return to (2)

13.8 Operation in Timer Trigger Mode

The A/D converter can set an interrupt signal specified by the trigger selection register (ITRG0) as a conversion trigger for up to 8 channels (a total of 16 channels in 2 circuits) of analog input (ANI00 to ANI07, ANI10 to ANI17).

The four interrupt signals that can be selected as triggers are the TM0n timer 0 register underflow interrupt signals (INTTM00 and INTTM01) and the CM003 and CM013 coincidence interrupt signals (INTCM003 and INTCM013) (n = 0,1).

13.8.1 Operation in select mode

One analog input (ANI00 to ANI07, ANI10 to ANI17) specified by the ADSCM00 or ADSCM10 register is A/D converted. The conversion result is stored in the ADCR0n or ADCR1n register corresponding to the analog input (n = 0 to 7).

This is optimal for applications that read A/D conversion values synchronized to a trigger.

(1) Timer trigger select mode

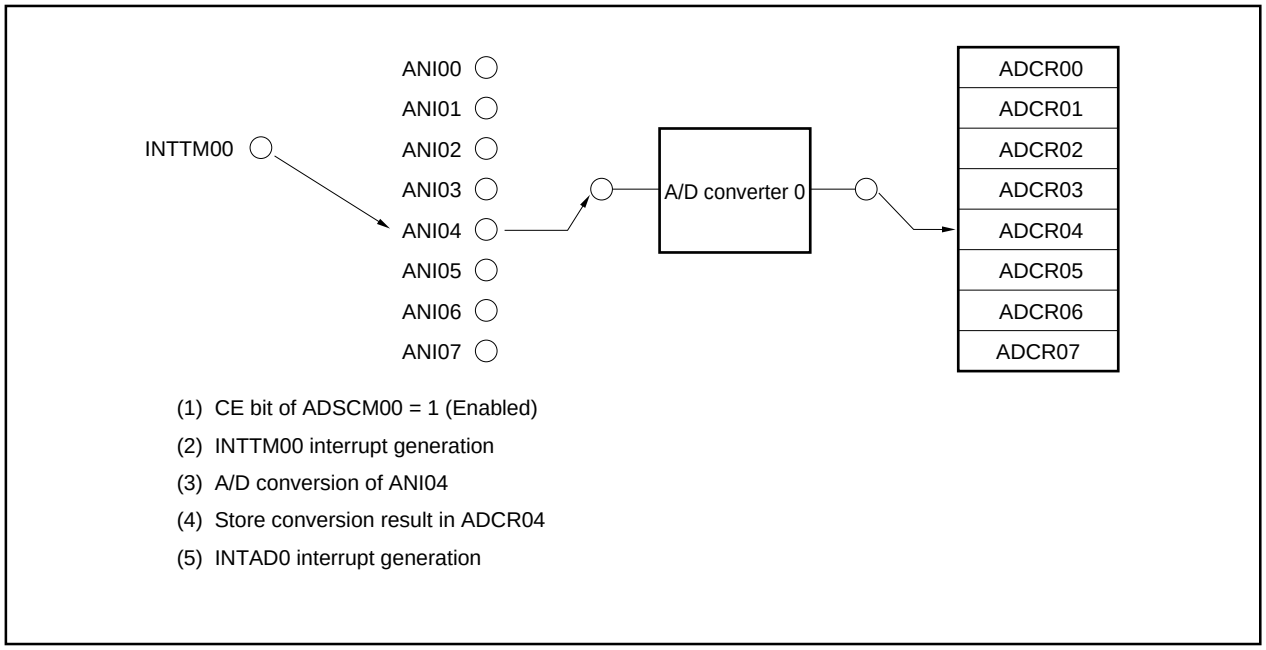
Taking the interrupt signal specified by the trigger selection register (ITRG0) as a trigger, one analog input at a time is A/D converted and the result is stored in one ADCR0n or ADCR1n register. An A/D conversion termination interrupt (INTAD0 or INTAD1) is generated for each A/D conversion, which terminates A/D conversion (CS = 0).

Trigger	Analog Input	A/D Conversion Result Register
Interrupt specified by ITRG0 register	ANIn	ADCRn

Remark n = 00 to 07, 10 to 17

After A/D conversion termination, A/D converter 0 or 1 changes to trigger wait status (CE = 1). It performs A/D conversion operation again when the interrupt signal specified in the ITRG0 register occurs.

Figure 13-15. Example of Timer Trigger Select Mode Operation (ANI04): For A/D Converter 0



13.8.2 Operation in scan mode

Analog input pins specified by register ADSCM00 or ADSCM10 are selected sequentially and the specified number of A/D conversions is performed using the interrupt specified by the ITRG0 register as a trigger. Conversion results are stored in the ADCR0n or ADCR1n registers corresponding to the analog inputs.

This is optimal for applications that regularly monitor multiple analog inputs.

(1) Timer trigger scan mode

Using the interrupt signal specified by the trigger selection register (ITRG0) as a trigger, the conversion start analog input pin through the conversion termination analog input pin specified by the ADSCM00 or ADSCM10 register are sequentially selected and A/D converted. Analog inputs correspond one-to-one with ADCR0n or ADCR1n registers. When all of the specified A/D conversions terminate, an A/D conversion termination interrupt (INTAD0 or INTAD1) is generated, which terminates A/D conversion (CS = 0).

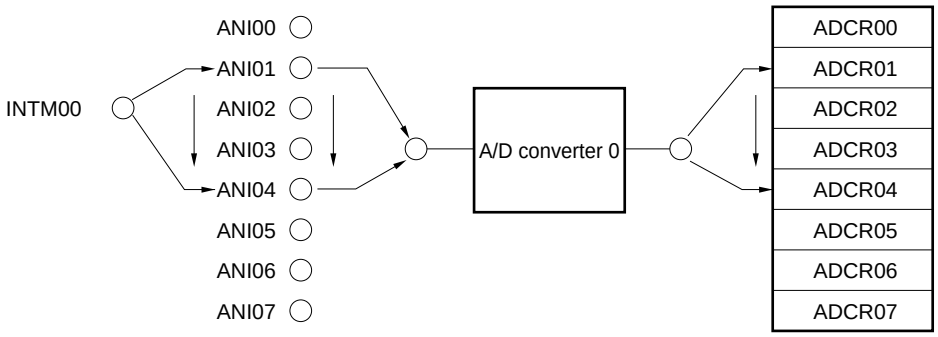
Trigger	Analog Input	A/D Conversion Result Register
Interrupt specified by ITRG0 register	ANIn0	ADCRn0
	ANIn1	ADCRn1
	ANIn2	ADCRn2
	ANIn3	ADCRn3
	ANIn4	ADCRn4
	ANIn5	ADCRn5
	ANIn6	ADCRn6
	ANIn7	ADCRn7

Remark n = 0, 1

After all of the specified A/D conversions terminate, the A/D converter changes to trigger wait status (CE=1). It performs A/D conversion operation again when the interrupt signal specified in the ITRG0 register occurs.

Figure 13-16. Example of Timer Trigger Scan Mode Operation (For A/D Converter 0) : INTTM00 Selected by ITRG0 Register

(a) Set to scan ANI01 to ANI04



(1) CE bit of ADSCM00 = 1 (Enabled)
(2) INTTM00 interrupt generation
(3) A/D conversion of ANI01
(4) Store conversion result in ADCR01
(5) A/D conversion of ANI02
(6) Store conversion result in ADCR02
(7) A/D conversion of ANI03
(8) Store conversion result in ADCR03
(9) A/D conversion of ANI04
(10) Store conversion result in ADCR04
(11) INTAD0 interrupt generation

13.9 Operation in External Trigger Mode

In external trigger mode, analog input[Note] is A/D converted on ADTRG0 or ADTRG1 pin input timing.

The valid edge of an external input signal in external trigger mode can be specified as a rising edge, a falling edge, or a rising or falling edge in the ES21 or ES20 bit of the INTM1 register for A/D converter 0 and in the ES31 or ES30 bit of the INTM1 register for A/D converter 1.

Note External trigger select: ANI00 to ANI07, ANI10 to ANI17
External trigger scan: ANI00 to ANI03, ANI10 to ANI13

13.9.1 Operation in select mode

One analog input (ANI00 to ANI07, ANI10 to ANI17) specified by the ADSCM00 or ADSCM10 register is A/D converted. The conversion result is stored in the ADCR0n or ADCR1n register (n = 0 to 7).

Using an ADTRG0 or ADTRG1 signal as a trigger, one analog input at a time is A/D converted and the result is stored in one ADCR0n or ADCR1n register. Analog inputs correspond one-to-one with A/D conversion result registers. For each A/D conversion, an A/D conversion termination interrupt (INTAD0 or INTAD1) is generated, which terminates A/D conversion (CS bit = 0).

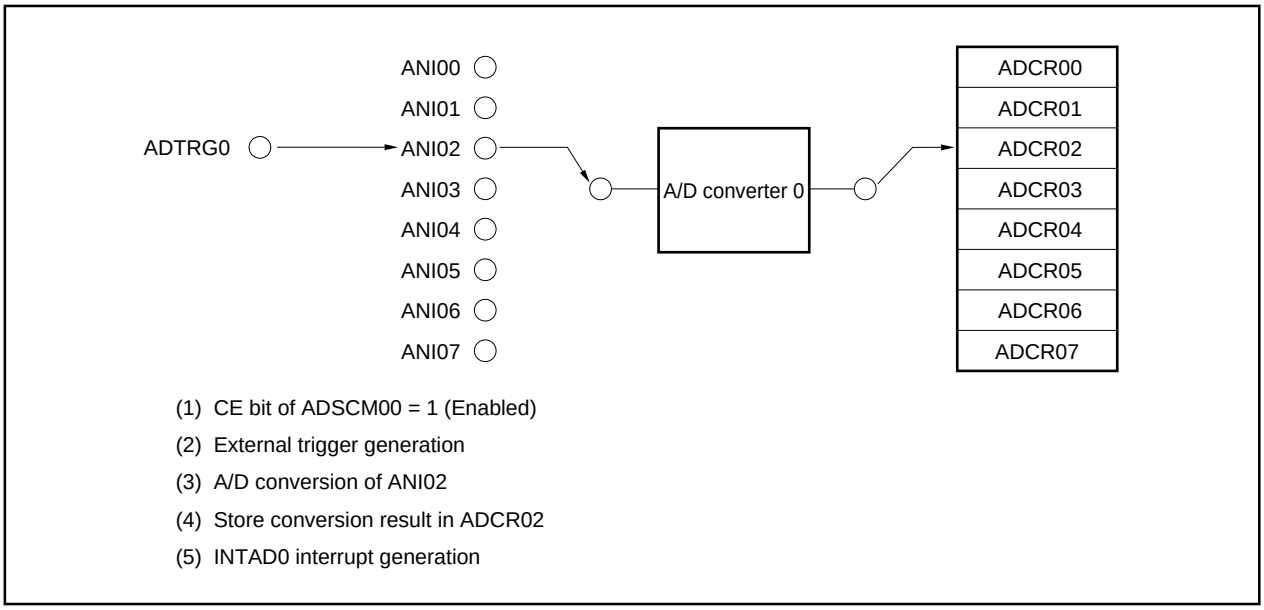
Trigger	Analog Input	A/D Conversion Result Register
ADTRGm signal	ANImn	ADCRmn

Remark m = 0, 1
n = 0 to 7

To restart A/D conversion, a trigger must be input again from the ADTRGn pin (n = 0, 1).

This is optimal for applications that read results each time there is an A/D conversion.

Figure 13-17. Example of Select Mode (External Trigger Select) Operation (ANI02): For A/D Converter 0



13.9.2 Operation in scan mode

Using an ADTRG0 or ADTRG1 signal as a trigger, pins from the conversion start analog input pin through the conversion termination analog input pin specified by the ADSCM00 or ADSCM10 register are sequentially selected and A/D converted. A/D conversion results are stored in the ADCR0n or ADCRN1n registers corresponding to the analog inputs (n = 0 to 7). When conversion terminates for all of the specified analog inputs, an INTAD0 or INTAD1 interrupt is generated, which terminates A/D conversion (CS = 0).

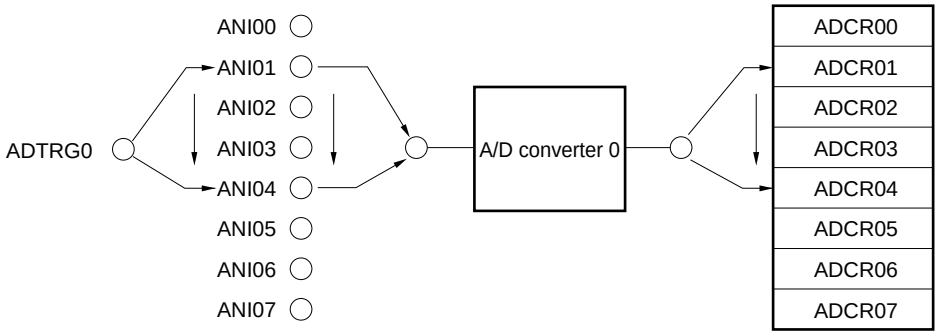
Trigger	Analog Input	A/D Conversion Result Register
ADTRGn signal	ANIn0	ADCRn0
	ANIn1	ADCRn1
	ANIn2	ADCRn2
	ANIn3	ADCRn3
	ANIn4	ADCRn4
	ANIn5	ADCRn5
	ANIn6	ADCRn6
	ANIn7	ADCRn7

Remark n = 0, 1

After all specified A/D conversions terminate, A/D conversion is restarted when an external trigger signal occurs. This is optimal for applications that regularly monitor multiple analog inputs.

Figure 13-18. Example of Scan Mode (External Trigger Scan) Operation: For A/D Converter 0

(a) When setting to scan ANI01 to ANI04



(1) CE bit of ADSCM00 or ADSCM10 = 1 (Enabled)
(2) External trigger generation
(3) A/D conversion of ANI01
(4) Store conversion result in ADCR01
(5) A/D conversion of ANI02
(6) Store conversion result in ADCR02
(7) A/D conversion of ANI03
(8) Store conversion result in ADCR03
(9) A/D conversion of ANI04
(10) Store conversion result in ADCR04
(11) INTAD0 interrupt generation

13.10 Precautions On Operation

13.10.1 Stopping conversion operation

If 0 is written in the CE bit of the ADSCM00 or ADSCM10 register during conversion operation, it stops conversion operation and a conversion result is not stored in the ADCR0n or ADCR1n register (n = 0 to 7).

13.10.2 Trigger input during conversion operation

If a trigger is input during conversion operation, that trigger input is ignored.

13.10.3 External or timer trigger interval

Make the trigger interval (input time interval) in external or timer trigger mode longer than the conversion time specified by the FR2-FR0 bits of the ADSCM01 or ADSCM11 register.

(1) When interval = 0

If multiple triggers are input simultaneously, the analog input whose ANI0n or ANI1n pin number is smallest is converted. The other trigger signals input at the same time are ignored (n = 0 to 7).

(2) When 0 < interval < conversion time

If an external or timer trigger is input during conversion operation, that trigger input is ignored.

If conversion operation is suspended, a conversion result is not stored in the ADCR0n or ADCR1n register (n = 0 to 7).

(3) When interval = conversion time

If an external or timer trigger is input at the same time as conversion termination (conversion termination signal and trigger contention), interrupt generation and ADCR0n or ADCR1n register storage of the value with which conversion terminated are performed correctly.

13.10.4 Operation in standby modes

(1) HALT mode

A/D conversion operation is suspended. If released by $\overline{\text{RESET}}$, NMI, or maskable interrupt input, the ADSCM00, ADSCM10, ADSCM01, or ADSCM11 register and ADCR0n or ADCR1n register maintain their values (n = 0 to 7).

(2) IDLE mode, software STOP mode

Since clock provision to A/D converter 0 or 1 stops, conversion operation is not performed.

If released by $\overline{\text{RESET}}$, NMI, or maskable interrupt input, the ADSCM00, ADSCM10, ADSCM01, or ADSCM11 register and ADCR0n or ADCR1n register maintain their values. However, if IDLE mode or software STOP mode is set during conversion operation, conversion operation stops. If released by NMI input, conversion resumes but the conversion result written in the ADCR0n or ADCR1n register becomes undefined (n = 0 to 7).

13.10.5 Compare coincidence interrupt in timer trigger mode

A TM0n timer 0 register underflow interrupt (INTTM00 or INTTM01) and CM003 or CM013 interrupt (INTCM003 or INTCM013) is an A/D conversion start trigger that starts conversion operation (n = 0,1). At this time, the CM003 or CM013 coincidence interrupt (INTCM003 or INTCM013) also functions as a compare register coincidence interrupt for the CPU. In order not to generate these match interrupts for the CPU, disable interrupts using the mask bits (TM0MK0, TM0MK1, CM03MK0, CM03MK1) of the interrupt control registers (TM0IC0, TM0IC1, CM03IC0, CM03IC1).

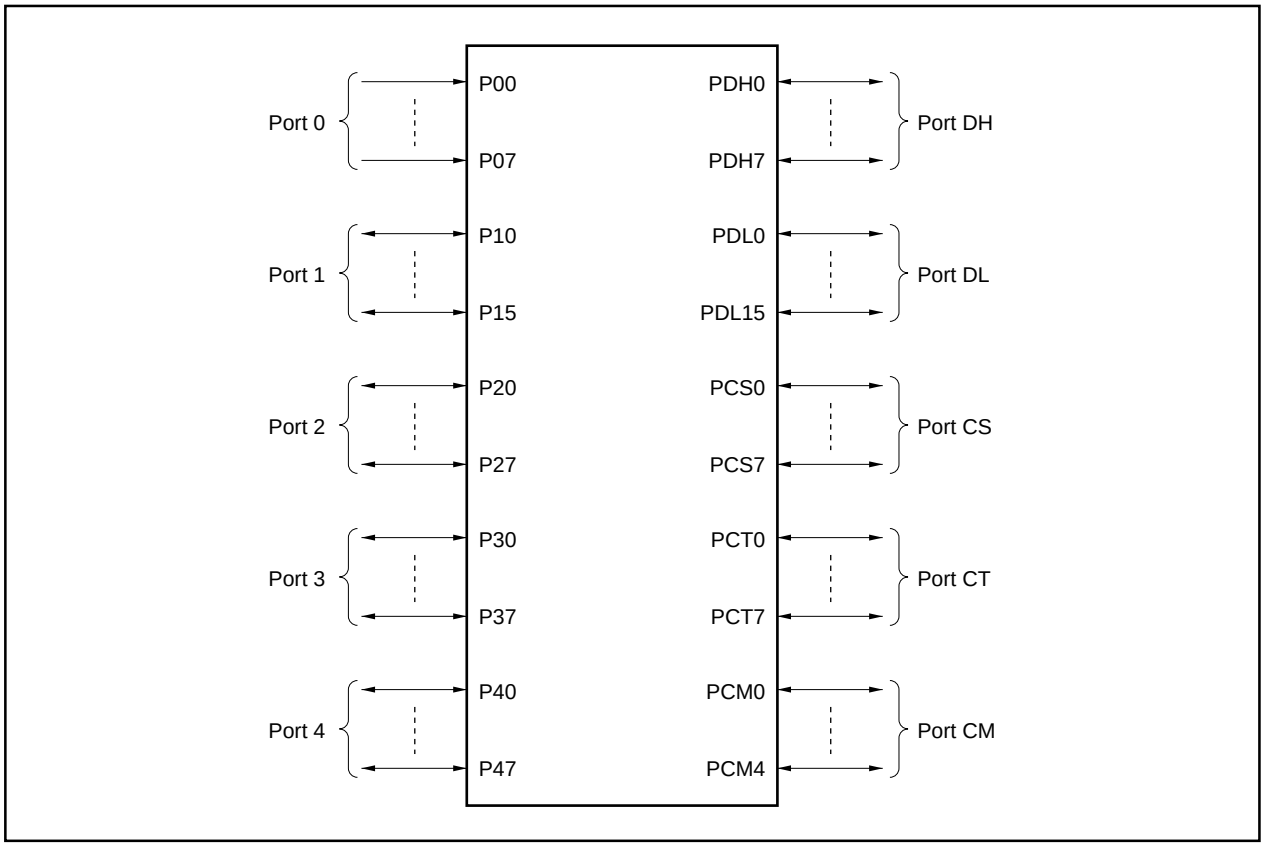
CHAPTER 14 PORT FUNCTIONS

14.1 Features

- Input dedicated ports: 8
  put/output ports : 75
- Ports alternate as input/output pins of other peripheral functions
- Input or output can be specified in bit units

14.2 Basic Configuration of Ports

The V850E/IA1 has a total of 83 on-chip input/output ports (ports 0 to 4, DH, DL, CS, CT, CM), of which 8 are input-only ports. The port configuration is shown below.



(1) Functions of each port

The V850E/IA1 has the ports shown below.

Any port can operate in 8- or 1-bit units and can provide a variety of controls.

Moreover, besides its function as a port, each has functions as the input/output pins of on-chip peripheral I/O in control mode.

Refer to **(3) Port block diagrams** for a block diagram of the block type of each port.

Port Name	Pin Name	Port Function	Function In Control Mode	Block Type
Port 0	P00 to P07	8-bit input	NMI input Real-time pulse unit (RPU) output stop signal input External interrupt input A/D converter (ADC) external trigger input	F
Port 1	P10 to P15	6-bit input/output	Real-time pulse unit (RPU) input/output External interrupt input	A, N
Port 2	P20 to P27	8-bit input/output	Real-time pulse unit (RPU) input/output External interrupt input	B, N
Port 3	P30 to P37	8-bit input/output	Serial interface input/output (UART0 to UART2)	A, C, G, H, M
Port 4	P40 to P47	8-bit input/output	Serial interface input/output (CSI0, CSI1, FCAN)	A, C, M
Port DH	PDH0 to PDH7	8-bit input/output	External address bus (A16 to A23)	O
Port DL	PDL0 to PDL15	16-bit input/output	External address data bus (AD0 to AD15)	O
Port CS	PCS0 to PCS7	16-bit input/output	External bus interface control signal output	J
Port CT	PCT0 to PCT7	16-bit input/output	External bus interface control signal output	A, J
Port CM	PCM0 to PCM4	5-bit input/output	Wait insertion signal input Internal system clock output External bus interface control signal input/output	A, D, J, K

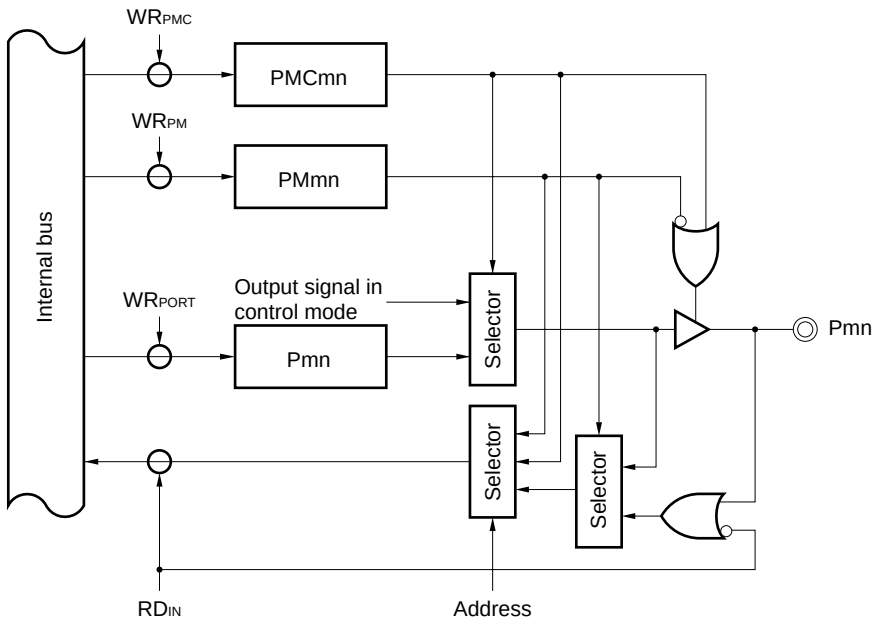
(2) Functions of each port pin on reset and registers that set port or control mode

Port Name	Pin Name	Pin Function after Reset				Mode-Setting Register
		Single-Chip Mode 0	Single-Chip Mode 1	ROM-less Mode 0	ROM-less Mode 1	
Port 0	P00/NMI	P00 (Input mode)				–
	P01/ESO0/INTP0	P01 (Input mode)				
	P02/ESO1/INTP1	P02 (Input mode)				
	P03/ADTRG0/INTP2	P03 (Input mode)				
	P04/ADTRG1/INTP3	P04 (Input mode)				
	P05/INTP4	P05 (Input mode)				
	P06/INTP5	P06 (Input mode)				
	P07/INTP6	P07 (Input mode)				
Port 1	P10/TIUD10/TO10	P10 (Input mode)				PMC1, PFC1
	P11/TCUD10/INTP100	P11 (Input mode)				PMC1
	P12/TCLR10/INTP101	P12 (Input mode)				
	P13/TIUD11/TO11	P13 (Input mode)				PMC1, PFC1
	P14/TCUD11/INTP110	P14 (Input mode)				PMC1
	P15/TCLR11/INTP111	P15 (Input mode)				
Port 2	P20/TI2/INTP20	P20 (Input mode)				PMC2
	P21/TO21/INTP21	P21 (Input mode)				PMC2, PFC2
	P22/TO22/INTP22	P22 (Input mode)				
	P23/TO23/INTP23	P23 (Input mode)				
	P24/TO24/INTP24	P24 (Input mode)				
	P25/TCLR2/INTP25	P25 (Input mode)				PMC2
	P26/TI3/TCLR3/INTP30	P26 (Input mode)				
	P27/TO3/INTP31	P27 (Input mode)				PMC2, PFC2
Port 3	P30/RXD0	P30 (Input mode)				PMC3
	P31/TXD0	P31 (Input mode)				
	P32/RXD1	P32 (Input mode)				
	P33/TXD1	P33 (Input mode)				
	P34/$\overline{\text{ASCK1}}$	P34 (Input mode)				
	P35/RXD2	P35 (Input mode)				
	P36/TXD2	P36 (Input mode)				
	P37/$\overline{\text{ASCK2}}$	P37 (Input mode)				

Port Name	Pin Name	Pin Function after Reset				Mode-Setting Register
		Single-Chip Mode 0	Single-Chip Mode 1	ROM-less Mode 0	ROM-less Mode 1	
Port 4	P40/SI0	P40 (Input mode)				PMC4
	P41/SO0	P41 (Input mode)				
	P42/$\overline{\text{SCK0}}$	P42 (Input mode)				
	P43/SI1	P43 (Input mode)				
	P44/SO1	P44 (Input mode)				
	P45/$\overline{\text{SCK1}}$	P45 (Input mode)				
	P46/CRXD	P46 (Input mode)				
	P47CTXD	P47 (Input mode)				
Port CM	PCM0/$\overline{\text{WAIT}}$	PCM0 (Input mode)	$\overline{\text{WAIT}}$			PMCCM
	PCM1/CLKOUT	PCM1 (Input mode)	CLKOUT			
	PCM2/$\overline{\text{HLDAK}}$	PCM2 (Input mode)	$\overline{\text{HLDAK}}$			
	PCM3/$\overline{\text{HLDRQ}}$	PCM3 (Input mode)	$\overline{\text{HLDRQ}}$			
	PCM4	PCM4 (Input mode)				–
Port CT	PCT0/$\overline{\text{LWR}}$	PCT0 (Input mode)	$\overline{\text{LWR}}$			PMCCT
	PCT1/$\overline{\text{UWR}}$	PCT1 (Input mode)	$\overline{\text{LWR}}$			
	PCT2	PCT2 (Input mode)				–
	PCT3	PCT3 (Input mode)				
	PCT4/$\overline{\text{RD}}$	PCT4 (Input mode)	$\overline{\text{RD}}$			PMCCT
	PCT5	PCT5 (Input mode)				–
	PCT6/ASTB	PCT6 (Input mode)	ASTB			PMCCT
	PCT7	PCT7 (Input mode)				–
Port CS	PCS0/$\overline{\text{CS0}}$ to PCS7/$\overline{\text{CS7}}$	PCS0 to PCS7 (Input mode)	$\overline{\text{CS0}}$ to $\overline{\text{CS7}}$			PMCCS
Port DH	PDH0/A16 to PDH7/A23	PDH0 to PDH7 (Input mode)	A16 to A23			PMCDH
Port DL	PDL0/AD0 to PDL15/AD15	PDL0 to PDL7 (Input mode)	AD0 to AD15			PMCDL

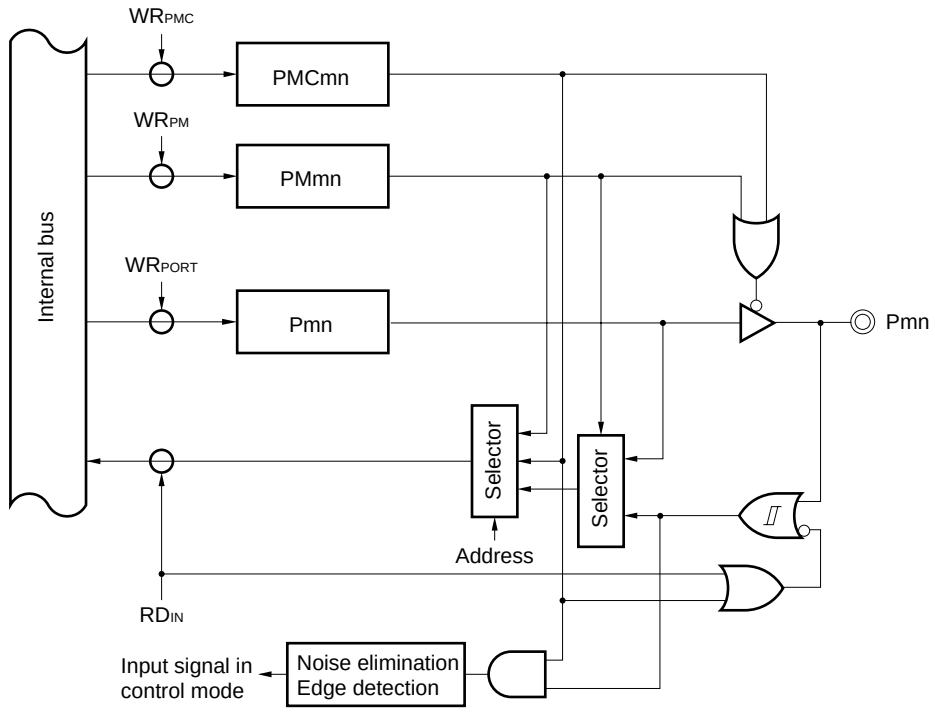
(3) Port block diagrams

Figure 14-1. Type A Block Diagram



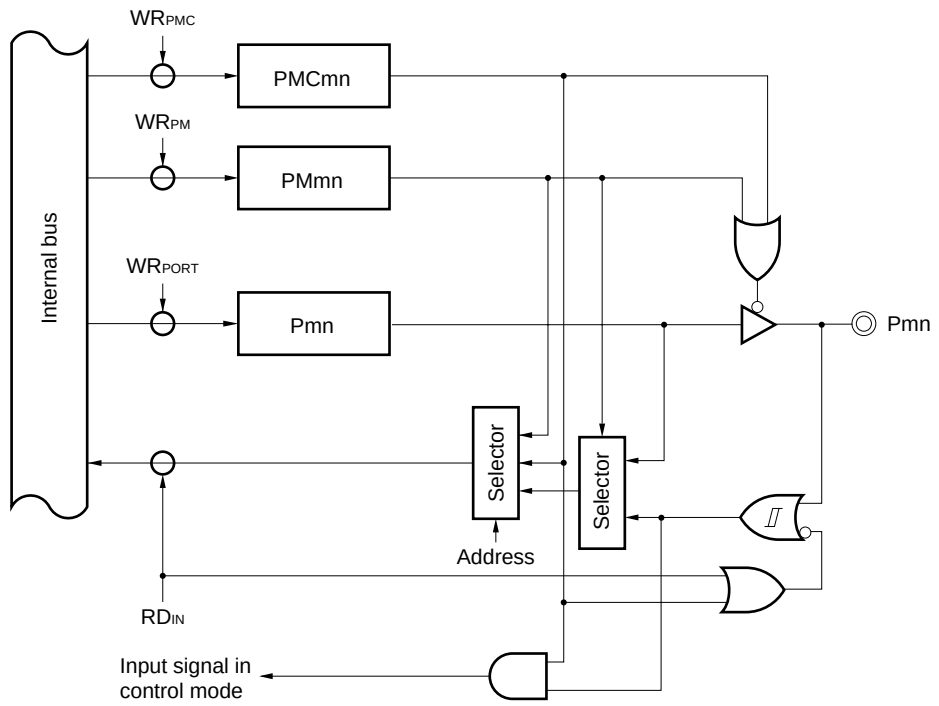
Remarks m: Port number
n : Bit number

Figure 14-2. Type B Block Diagram



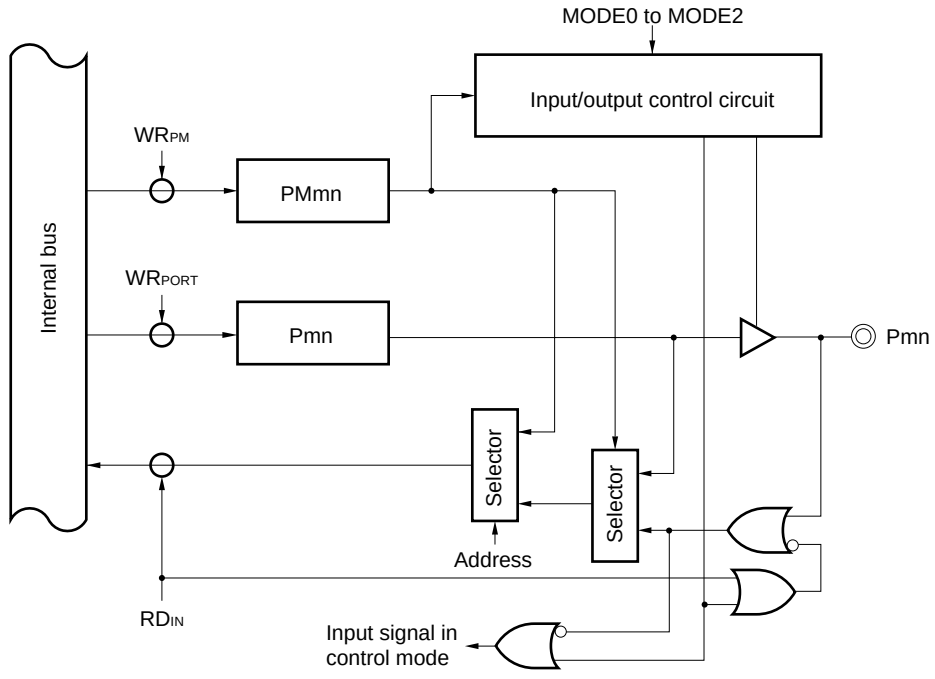
Remarks m : Port number
n : Bit number

Figure 14-3. Type C Block Diagram



Remarks m: Port number
n : Bit number

Figure 14-4. Type D Block Diagram



Remarks m: Port number
n : Bit number

Figure 14-5. Type F Block Diagram

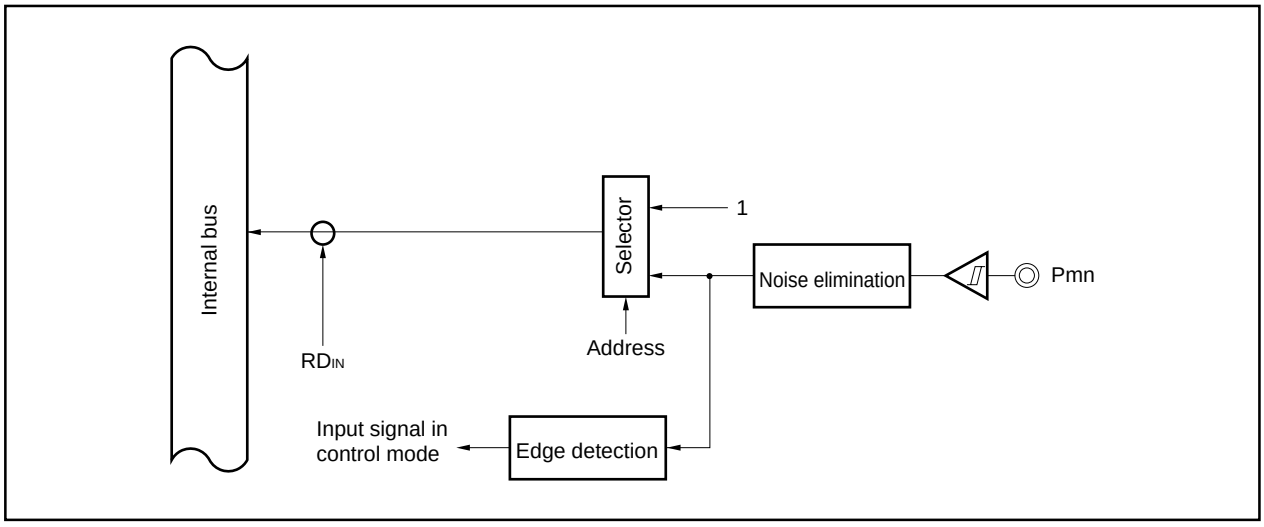
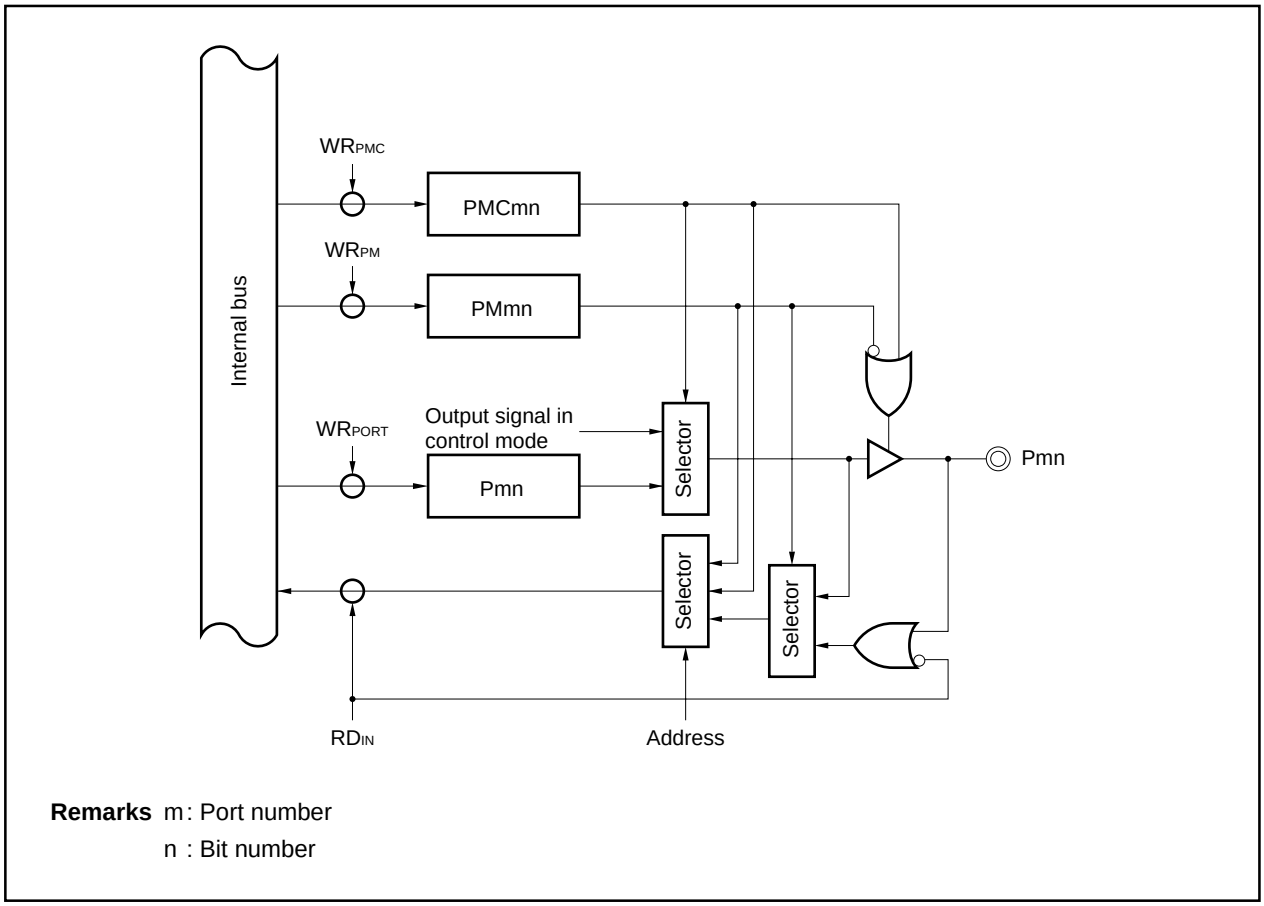
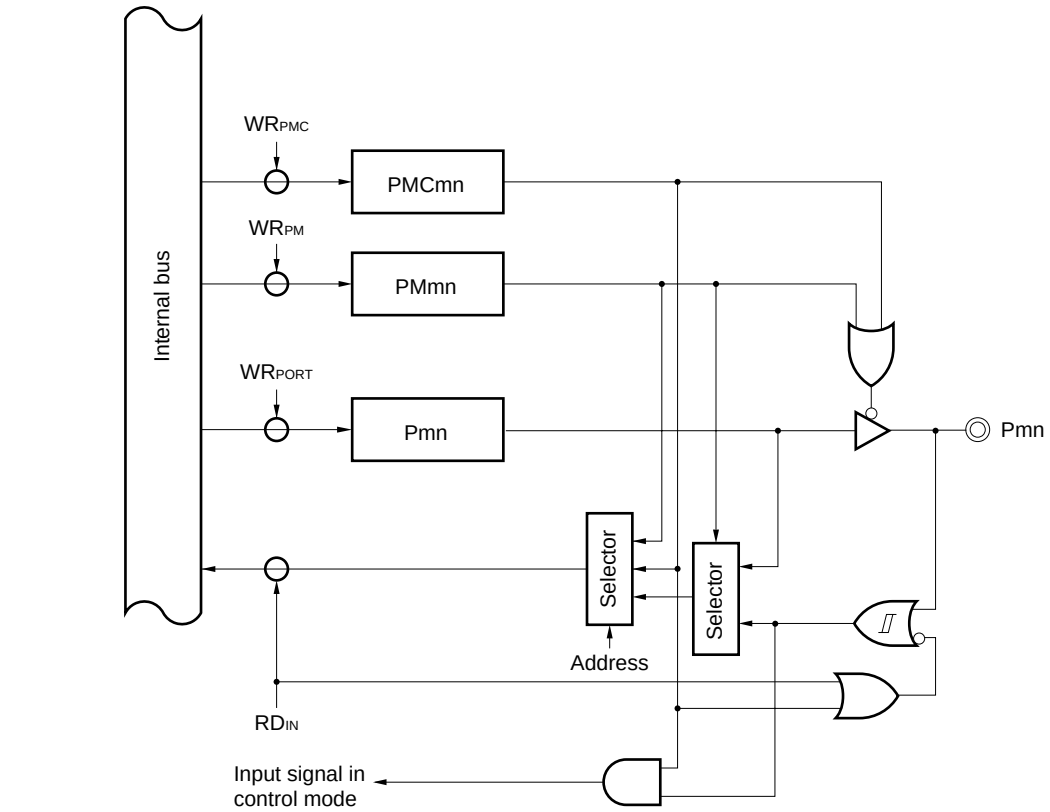


Figure 14-6. Type G Block Diagram



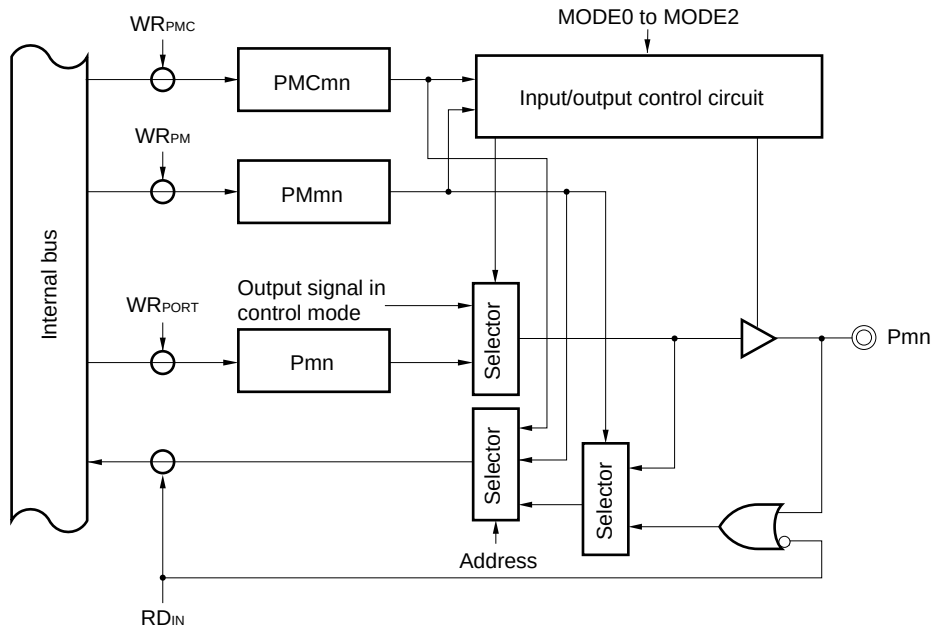
Remarks m: Port number
n : Bit number

Figure 14-7. Type H Block Diagram



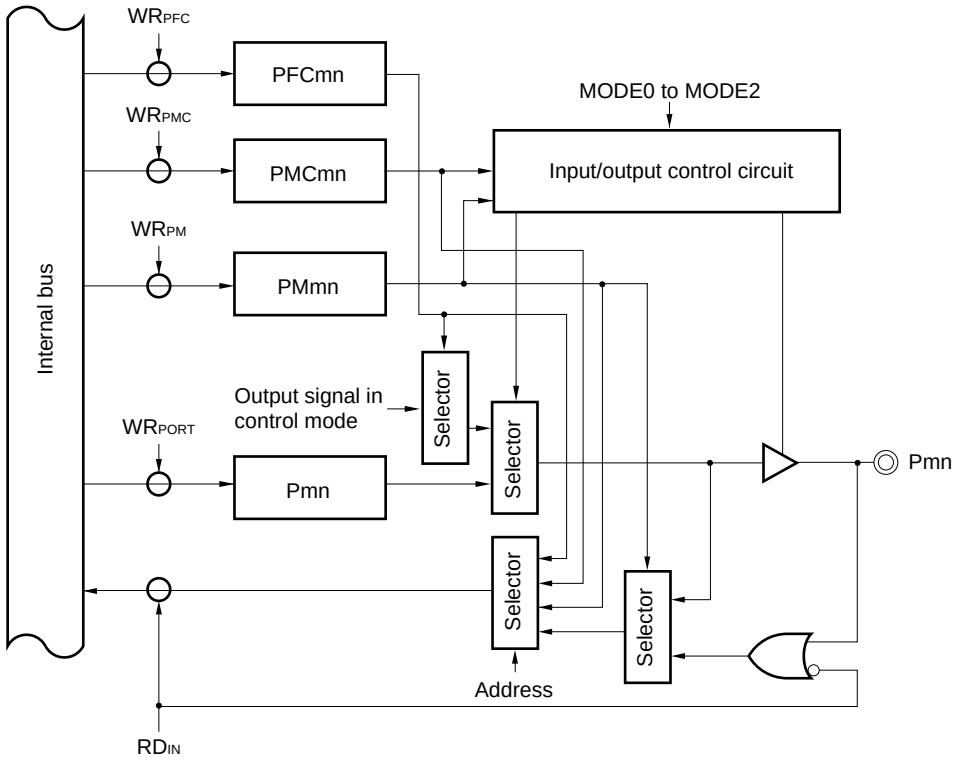
Remarks m: Port number
n : Bit number

Figure 14-8. Type J Block Diagram



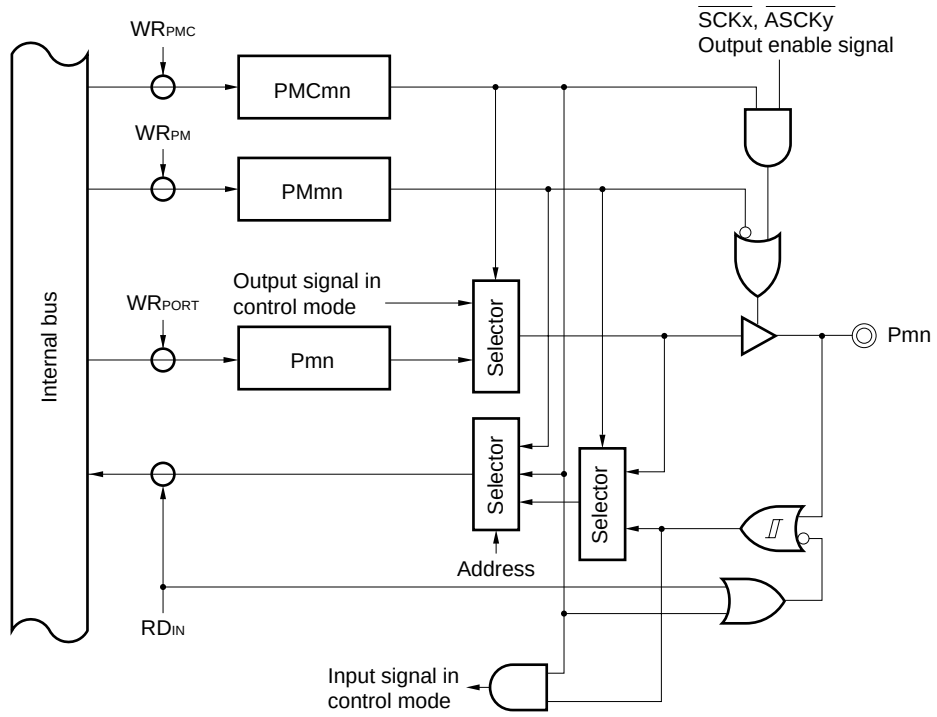
Remarks m: Port number
n : Bit number

Figure 14-9. Type K Block Diagram



Remarks m: Port number
n : Bit number

Figure 14-10. Type M Block Diagram



Remarks mn : 34, 37, 42, 45

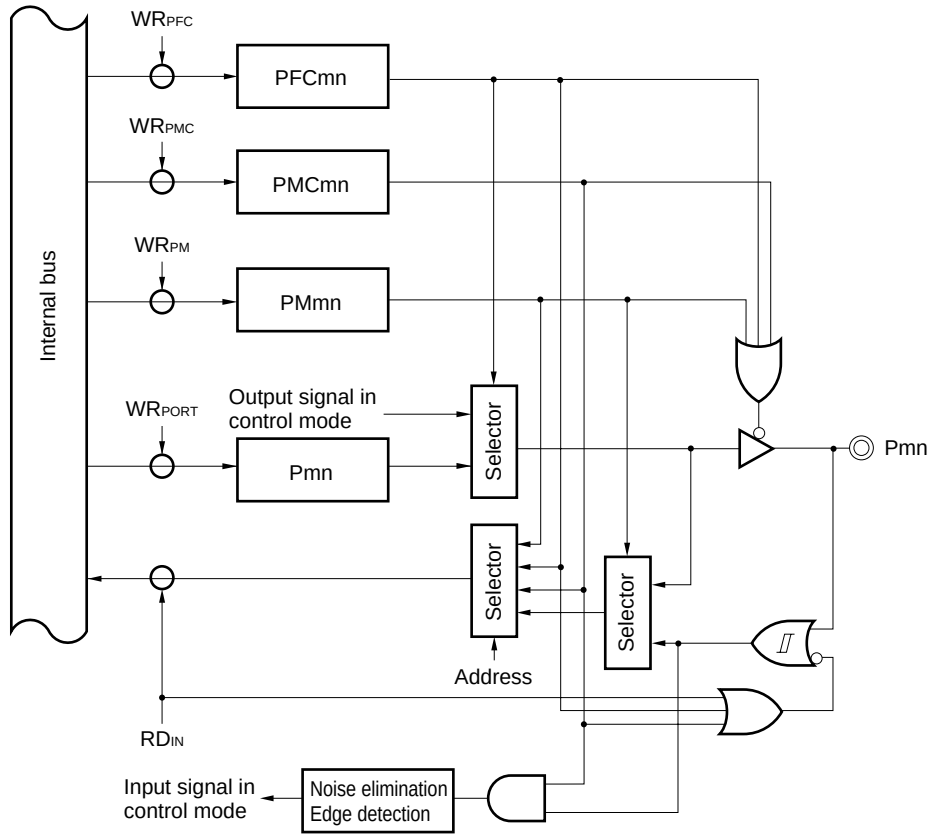
x : 0 (When mn = 42)

1 (When mn = 45)

y : 1 (When mn = 34)

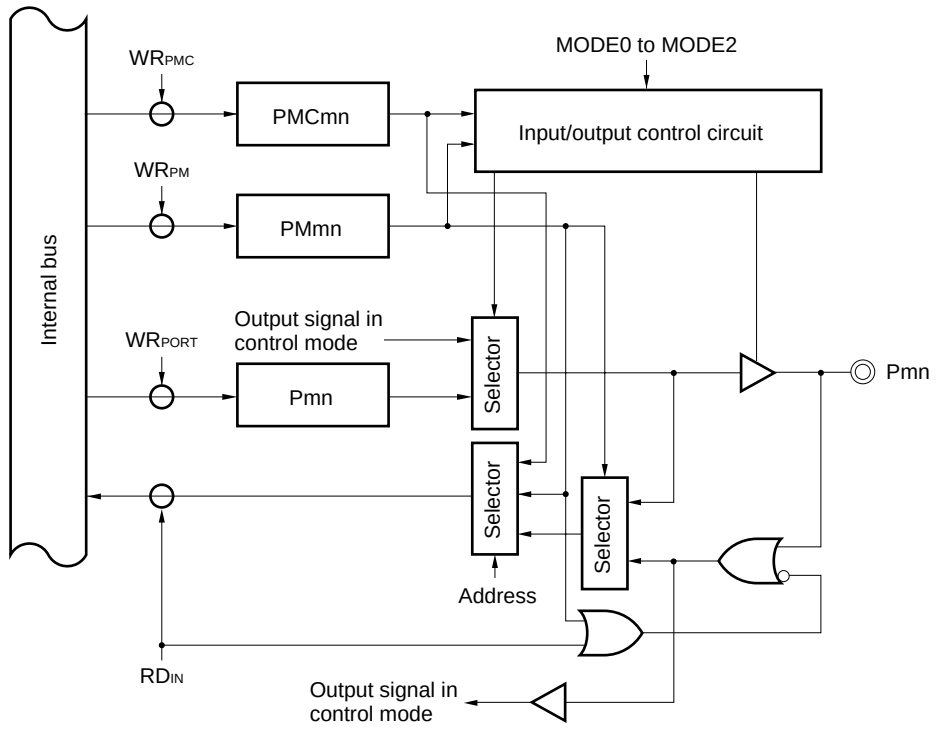
2 (When mn = 37)

Figure 14-11. Type N Block Diagram



Remarks m: Port number
n : Bit number

Figure 14-12. Type O Block Diagram



Remarks m: Port number
n : Bit number

14.3 Pin Functions of Each Port

14.3.1 Port 0

Port 0 is an 8-bit input dedicated port in which all pins are fixed for input.

Figure 14-13. Port 0 (P0)

	7	6	5	4	3	2	1	0	Address	Initial value
P0	P07	P06	P05	P04	P03	P02	P01	P00	FFFFF400H	Undefined

Besides functioning as an input port, in control mode, it also can operate as the real-time pulse unit (RPU) output stop signal input, external interrupt request input, and A/D converter (ADC) external trigger input.

Although this port also serves as NMI, ESO0/INTP0, ESO1/INTP1, ADTRG0/INTP2, ADTRG1/INTP3, and INTP4 to INTP6, NMI, ESO0/INTP0, ESO1/INTP1, ADTRG0/INTP2, ADTRG1/INTP3, and INTP4 to INTP6 cannot be switched with input port. The status of each pin is read by reading the port.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port 0	P00	NMI	Non-maskable interrupt request input	F
	P01	ESO0/INTP0	Real-time pulse unit (RPU) output stop signal input or external interrupt request input	
	P02	ESO1/INTP1		
	P03	ADTRG0/INTP2	A/D converter (ADC) external trigger input or external interrupt request input	
	P04	ADTRG1/INTP3		
	P05 to 07	INTP4 to INTP6	External interrupt request input	

14.3.2 Port 1

Port 1 is a 6-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-14. Port 1 (P1)

	7	6	5	4	3	2	1	0	Address	Initial value
P1	–	–	P15	P14	P13	P12	P11	P10	FFFFF402H	Undefined

Bit position	Bit name	Function
5 to 0	P1n (n = 5 to 0)	Input/output port

Besides functioning as a port, in control mode, it also can operate as the real-time pulse unit (RPU) input/output and external interrupt request input.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port 1	P10	TIUD10/TO10	Real-time pulse unit (RPU) input/output	A
	P11	TCUD10/INTP100	Real-time pulse unit (RPU) input or external interrupt request input	N
	P12	TCLR10/INTP101		
	P13	TIUD11/TO11	Real-time pulse unit (RPU) input/output	A
	P14	TCUD11/INTP110	Real-time pulse unit (RPU) input or external interrupt request input	N
	P15	TCLR11/INTP111		

(2) Setting in input/output mode and control mode

Port 1 is set in input/output mode using the port 1 mode register (PM1). In control mode, it is set using the port 1 mode control register (PMC1) and port function control register 1 (PFC1).

(a) Port 1 mode register (PM1)

This register can be read or written in 8- or 1-bit units. Write 1 in bits 6 and 7.

Figure 14-15. Port 1 Mode Register (PM1)

	7	6	5	4	3	2	1	0	Address	Initial value
PM1	1	1	PM15	PM14	PM13	PM12	PM11	PM10	FFFFF422H	FFH

Bit Position	Bit Name	Function
5 to 0	PM1n (n = 5 to 0)	Specifies input/output mode of P1n pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port 1 mode control register (PMC1)

This register can be read or written in 8- or 1-bit units. Write 0 in bits 6 and 7.

Figure 14-16. Port 1 Mode Control Register (PMC1)

	7	6	5	4	3	2	1	0	Address	Initial value
PMC1	0	0	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	FFFFF442H	00H

Bit Position	Bit Name	Function
5	PMC15	Specifies operation mode of P15 pin. 0: Input/output port mode 1: TCLR11 input mode or external interrupt request (INTP111) input mode
4	PMC14	Specifies operation mode of P14 pin. 0: Input/output port mode 1: TCUD11 input mode or external interrupt request (INTP110) input mode
3	PMC13	Specifies operation mode of P13 pin. 0: Input/output port mode 1: TIUD11 input mode or TO11 output mode
2	PMC12	Specifies operation mode of P12 pin. 0: Input/output port mode 1: TCLR10 input mode or external interrupt request (INTP101) input mode
1	PMC11	Specifies operation mode of P11 pin. 0: Input/output port mode 1: TCUD10 input mode or external interrupt request (INTP100) input mode
0	PMC10	Specifies operation mode of P10 pin. 0: Input/output port mode 1: TIUD10 input mode or TO10 output mode

Caution The PMC11, PMC12, PMC14, and PMC15 bits also serve as external interrupts (INTP100, INTP101, INTP110, and INTP111). When not using them as external interrupts, mask interrupt requests (refer to 7.3.4 Interrupt control registers (xxICn)).

(c) Port 1 function control register (PFC1)

This register can be read or written in 8- or 1-bit units. Write 0 in bits other than 0 and 3.

Figure 14-17. Port 1 Function Control Register (PFC1)

	7	6	5	4	3	2	1	0	Address	Initial value
PFC1	0	0	0	0	PFC13	0	0	PFC10	FFFFF462H	00H

Bit Position	Bit Name	Function
3	PFC13	Specifies operation mode of P13 pin in control mode. 0: TIUD11 input mode 1: TO11 output mode
0	PFC10	Specifies operation mode of P10 pin in control mode. 0: TIUD10 input mode 1: TO11 output mode

Caution When port mode is specified by the port 1 mode control register (PMC1), the setting of this register is invalid.

14.3.3 Port 2

Port 2 is an 8-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-18. Port 2 (P2)

	7	6	5	4	3	2	1	0	Address	Initial value
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFFFF404H	Undefined

Bit Position	Bit Name	Function
7 to 0	P2n (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, it also can operate as the real-time pulse unit (RPU) input/output and external interrupt request input.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port 2	P20	TI2/INTP20	Real-time pulse unit (RPU) input or external interrupt request input	B
	P21 to 24	TO21/INTP21 to TO24/INTP24	Real-time pulse unit (RPU) output or external interrupt request input	N
	P25	TCLR2/INTP25	Real-time pulse unit (RPU) input or external interrupt request input	B
	P26	TI3/TCLR3/INTP30		
	P27	TO3/INTP31	Real-time pulse unit (RPU) output or external interrupt request input	N

(2) Setting in input/output mode and control mode

Port 2 is set in input/output mode using the port 2 mode register (PM2). In control mode, it is set using the port 2 mode control register (PMC2) and port 2 function control register (PFC2).

(a) Port 2 mode register (PM2)

This register can be read or written in 8- or 1-bit units.

Figure 14-19. Port 2 Mode Register (PM2)

	7	6	5	4	3	2	1	0	Address	Initial value
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFFFF424H	FFH

Bit Position	Bit Name	Function
7 to 0	PM2n (n = 7 to 0)	Specifies input/output mode of P2n pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port 2 mode control register (PMC2)

This register can be read or written in 8- or 1-bit units.

Figure 14-20. Port 2 Mode Control Register (PMC2)

	7	6	5	4	3	2	1	0	Address	Initial value
PMC2	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	FFFFF444H	00H

Bit Position	Bit Name	Function
7	PMC27	Specifies operation mode of P27 pin 0: Input/output port mode 1: TO3 output mode or external interrupt request (INTP31) input mode
6	PMC26	Specifies operation mode of P26 pin 0: Input/output port mode 1: RPU (TI3, TCLR3) input mode or external interrupt request (INTP30) input mode
5	PMC25	Specifies operation mode of P25 pin 0: Input/output port mode 1: TCLR2 input mode or external interrupt request (INTP25) input mode
4 to 1	PMC24 to PMC21	Specify operation mode of P24 to P21 pins 0: Input/output port mode 1: TO24 to TO21 output mode or external interrupt request (INTP24 to INTP21) input mode
0	PMC20	Specifies operation mode of P20 pin 0: Input/output port mode 1: TI2 input mode or external interrupt request (INTP20) input mode

Caution The PMC20, PMC25, and PMC26 bits also serve as external interrupts (INTP20, INTP25, and INTP30). When not using them as external interrupts, mask interrupt requests (refer to 7.3.4 Interrupt control registers (xxICn)).

(c) Port 2 function control register (PFC2)

This register can be read or written in 8- or 1-bit units. Write 0 in bits 0, 5, and 6.

Figure 14-21. Port 2 Function Control Register (PFC2)

	7	6	5	4	3	2	1	0	Address	Initial value
PFC2	PFC27	0	0	PFC24	PFC23	PFC22	PFC21	0	FFFFF464H	00H

Bit Position	Bit Name	Function
7	PFC27	Specifies operation mode of P27 pin in control mode 0: External interrupt request (INTP31) input mode 1: TO3 output mode
4 to 1	PFC24 to PFC21	Specify operation mode of P24 to P21 pins in control mode 0: External interrupt request (INTP24 to INTP21) input mode 1: TO24 to TO21 output mode

Caution When port mode is specified by the port 2 mode control register (PMC2), the setting of this register is invalid.

14.3.4 Port 3

Port 3 is an 8-bit input/output port in which input or output can be specified in 1-bit units

Figure 14-22. Port 3 (P3)

	7	6	5	4	3	2	1	0	Address	Initial value
P3	P37	P36	P35	P34	P33	P32	P31	P30	FFFFF406H	Undefined

Bit Position	Bit Name	Function
7 to 0	P3n (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, it also can operate as the serial interface (UART0 to UART2) input/output.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port 3	P30	RXD0	Serial interface (UART0 to UART2) input/output	H
	P31	TXD0		G
	P32	RXD1		C
	P33	TXD1		A
	P34	$\overline{\text{ASCK1}}$		M
	P35	RXD2		C
	P36	TXD2		A
	P37	$\overline{\text{ASCK2}}$		M

(2) Setting in input/output mode and control mode

Port 3 is set in input/output mode using the port 3 mode register (PM3). In control mode, it is set using the port 3 mode control register (PMC3).

(a) Port 3 mode register (PM3)

This register can be read or written in 8- or 1-bit units.

Figure 14-23. Port 3 Mode Register (PM3)

	7	6	5	4	3	2	1	0	Address	Initial value
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FFFFF426H	FFH

Bit Position	Bit Name	Function
7 to 0	PM3n (n = 7 to 0)	Specifies input/output mode of P3n pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port 3 mode control register (PMC3)

This register can be read or written in 8- or 1-bit units.

Figure 14-24. Port 3 Mode Control Register (PMC3)

	7	6	5	4	3	2	1	0	Address	Initial value
PMC3	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	FFFFF446H	00H

Bit Position	Bit Name	Function
7	PMC37	Specifies operation mode of P37 pin 0: Input/output port mode 1: $\overline{\text{ASCK2}}$ input/output mode
6	PMC36	Specifies operation mode of P36 pin 0: Input/output port mode 1: TXD2 output mode
5	PMC35	Specifies operation mode of P35 pin 0: Input/output port mode 1: RXD2 input mode
4	PMC34	Specifies operation mode of P34 pin 0: Input/output port mode 1: $\overline{\text{ASCK1}}$ input/output mode
3	PMC33	Specifies operation mode of P33 pin 0: Input/output port mode 1: TXD1 output mode
2	PMC32	Specifies operation mode of P32 pin 0: Input/output port mode 1: RXD1 input mode
1	PMC31	Specifies operation mode of P31 pin 0: Input/output port mode 1: TXD0 output mode
0	PMC30	Specifies operation mode of P30 pin 0: Input/output port mode 1: RXD0 input mode

14.3.5 Port 4

Port 4 is an 8-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-25. Port 4 (P4)

	7	6	5	4	3	2	1	0	Address	Initial value
P4	P47	P46	P45	P44	P43	P42	P41	P40	FFFFF408H	Undefined

Bit Position	Bit Name	Function
7 to 0	P4n (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, it also can operate as the serial interface (CSI0, CSI1, FCAN) input/output.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port 4	P40	SI0	Serial interface (CSI0, CSI1, FCAN) input/output	C
	P41	SO0		A
	P42	$\overline{\text{SCK0}}$		M
	P43	SI1		C
	P44	SO1		A
	P45	$\overline{\text{SCK1}}$		M
	P46	CRXD		C
	P47	CTXD		A

(2) Setting in input/output mode and control mode

Port 4 is set in input/output mode using the port 4 mode register (PM4). In control mode, it is set using the port 4 mode control register (PMC4).

(a) Port 4 mode register (PM4)

This register can be read or written in 8- or 1-bit units.

Figure 14-26. Port 4 Mode Register (PM4)

	7	6	5	4	3	2	1	0	Address	Initial value
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FFFFF428H	FFH

Bit Position	Bit Name	Function
7 to 0	PM4n (n = 7 to 0)	Specifies input/output mode of P4n pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port 4 mode control register (PMC4)

This register can be read or written in 8- or 1-bit units.

Figure 14-27. Port 4 Mode Control Register (PMC4)

	7	6	5	4	3	2	1	0	Address	Initial value
PMC4	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	FFFFF448H	00H

Bit Position	Bit Name	Function
7	PMC47	Specifies operation mode of P47 pin 0: Input/output port mode 1: CTXD output mode
6	PMC46	Specifies operation mode of P46 pin 0: Input/output port mode 1: CRXD input mode
5	PMC45	Specifies operation mode of P45 pin 0: Input/output port mode 1: $\overline{\text{SCK1}}$ input/output mode
4	PMC44	Specifies operation mode of P44 pin 0: Input/output port mode 1: SO1 output mode
3	PMC43	Specifies operation mode of P43 pin 0: Input/output port mode 1: SI1 input mode
2	PMC42	Specifies operation mode of P42 pin 0: Input/output port mode 1: $\overline{\text{SCK0}}$ input/output mode
1	PMC41	Specifies operation mode of P41 pin 0: Input/output port mode 1: SO0 output mode
0	PMC40	Specifies operation mode of P40 pin 0: Input/output port mode 1: SI0 input mode

14.3.6 Port DH

Port DH is an 8-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-28. Port DH (PDH)

	7	6	5	4	3	2	1	0	Address	Initial value
PDH	PDH7	PDH6	PDH5	PDH4	PDH3	PDH2	PDH1	PDH0	FFFFF006H	Undefined

Bit Position	Bit Name	Function
7 to 0	PDHn (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, this can operate as an address bus when memory is expanded externally.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port DH	PDH7 to PDH0	A23 to A16	Memory expansion address bus	O

(2) Setting in input/output mode and control mode

Port DH is set in input/output mode using the port DH mode register (PMDH). In control mode, it is set using the port DH mode control register (PMCDH).

(a) Port DH mode register (PMDH)

This register can be read or written in 8- or 1-bit units.

Figure 14-29. Port DH Mode Register (PMDH)

	7	6	5	4	3	2	1	0	Address	Initial value
PMDH	PMDH7	PMDH6	PMDH5	PMDH4	PMDH3	PMDH2	PMDH1	PMDH0	FFFFF026	FFH

Bit Position	Bit Name	Function
7 to 0	PMDHn (n = 7 to 0)	Specifies input/output mode of PDHn pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port DH mode control register (PMCDH)

This register can be read or written in 8- or 1-bit units.

Figure 14-30. Port DH Mode Control Register (PMCDH)

	7	6	5	4	3	2	1	0	Address	Initial value[Note]
PMCDH	PMCDH7	PMCDH6	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0	FFFFF046	00H/FFH

Note 00H: Single-chip mode 0
FFH: Single-chip mode 1, ROMless mode 0 or 1

Bit Position	Bit Name	Function
7 to 0	PMCDHn (n = 7 to 0)	Specifies operation mode of PDHn pin 0: Input/output port mode 1: A23 to A16 output mode

14.3.7 Port DL

Port DL is a 16-bit input/output port in which input or output can be specified in 1-bit units.

When using the higher 8 bits of PDL as PDLH and the lower 8 bits as PDLL, it can be used as an 8-bit input/output port that can specify input/output in 1-bit units.

Figure 14-31. Port DL (PDL)

	15	14	13	12	11	10	9	8	Address	Initial value
PDL	PDL15	PDL14	PDL13	PDL12	PDL11	PDL10	PDL9	PDL8	FFFFF005H	Undefined

	7	6	5	4	3	2	1	0	Address
	PDL7	PDL6	PDL5	PDL4	PDL3	PDL2	PDL1	PDL0	FFFFF004H

Bit Position	Bit Name	Function
15 to 0	PDLn (n = 15 to 0)	Input/output port

Besides functioning as a port, in control mode, this can operate as an address and data bus when memory is expanded externally.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port DL	PDL15 to PDL0	AD15 to AD0	Memory expansion address and data bus	O

(2) Setting in input/output mode and control mode

Port DL is set in input/output mode using the port DL mode register (PMDL). In control mode, it is set using the port DL mode control register (PMCDL).

(a) Port DL mode register (PMDL)

The PMDL register can be read or written in 16-bit units.

When using the higher 8 bits of the PMDL register as the PMDLH register and the lower 8 bits as the PMDLL register, it can be read or written in 8- or 1-bit units.

Figure 14-32. Port DL Mode Register (PMDL)

	15	14	13	12	11	10	9	8	Address	Initial value
PMDL	PMDL15	PMDL14	PMDL13	PMDL12	PMDL11	PMDL10	PMDL9	PMDL8	FFFFF025H	FFFFH

7	6	5	4	3	2	1	0	Address
PMDL7	PMDL6	PMDL5	PMDL4	PMDL3	PMDL2	PMDL1	PMDL0	FFFFF024H

Bit Position	Bit Name	Function
15 to 0	PMDLn (n = 15 to 0)	Specifies input/output mode of PDLn pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port DL mode control register (PMCDL)

The PMCDL register can be read or written in 16-bit units.

When using the higher 8 bits of the PMCDL register as the PMCDLH register and the lower 8 bits as the PMCDLL register, it can be read or written in 8- or 1-bit units.

Figure 14-33. Port DL Mode Control Register (PMCDL)

	15	14	13	12	11	10	9	8	Address	Initial value[Note]
PMCDL	PMCDL15	PMCDL14	PMCDL13	PMCDL12	PMCDL11	PMCDL10	PMCDL9	PMCDL8	FFFFF045H	0000H/FFFFH

7	6	5	4	3	2	1	0	Address
PMCDL7	PMCDL6	PMCDL5	PMCDL4	PMCDL3	PMCDL2	PMCDL1	PMCDL0	FFFFF044H

Note 0000H : Single-chip mode 0

FFFFH: Single-chip mode 1, ROMless mode 0 or 1

Bit Position	Bit Name	Function
15 to 0	PMCDLn (n = 15 to 0)	Specifies operation mode of PDLn pin. 0: Input/output port mode 1: AD15 to AD0 input/output mode

14.3.8 Port CS

Port CS is an 8-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-34. Port CS (PCS)

	7	6	5	4	3	2	1	0	Address	Initial value
PCS	PCS7	PCS6	PCS5	PCS4	PCS3	PCS2	PCS1	PCS0	FFFFF008H	Undefined

Bit Position	Bit Name	Function
7 to 0	PCSn (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, this can operate as the chip select signal output when memory is expanded externally.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port CS	PCS7 to PCS0	$\overline{CS0}$ to $\overline{CS7}$	Chip select signal output	J

(2) Setting in input/output mode and control mode

Port CS is set in input/output mode using the port CS mode register (PMCS). In control mode, it is set using the port CS mode control register (PMCCS).

(a) Port CS mode register (PMCS)

This register can be read or written in 8- or 1-bit units.

Figure 14-35. Port CS Mode Register (PMCS)

	7	6	5	4	3	2	1	0	Address	Initial value
PMCS	PMCS7	PMCS6	PMCS5	PMCS4	PMCS3	PMCS2	PMCS1	PMCS0	FFFFF028H	FFH

Bit Position	Bit Name	Function
7 to 0	PMCSn (n = 7 to 0)	Specifies input/output mode of PCSn pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port CS mode control register (PMCCS)

This register can be read or written in 8- or 1-bit units.

Figure 14-36. Port CS Mode Control Register (PMCCS)

	7	6	5	4	3	2	1	0	Address	Initial value[Note]
PMCCS	PMCCS7	PMCCS6	PMCCS5	PMCCS4	PMCCS3	PMCCS2	PMCCS1	PMCCS0	FFFFF048H	00H/FFH

Note 00H: Single-chip mode 0
FFH: Single-chip mode 1, ROM-less mode 0 or 1

Bit Position	Bit Name	Function
7 to 0	PMCCSn (n = 7 to 0)	Specifies operation mode of PCSn pin 0: Input/output port mode 1: $\overline{CS7}$ to $\overline{CS0}$ output mode

14.3.9 Port CT

Port CT is an 8-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-37. Port CT (PCT)

	7	6	5	4	3	2	1	0	Address	Initial value
PCT	PCT7	PCT6	PCT5	PCT4	PCT3	PCT2	PCT1	PCT0	FFFFF00AH	Undefined

Bit Position	Bit Name	Function
7 to 0	PCTn (n = 7 to 0)	Input/output port

Besides functioning as a port, in control mode, this can operate as control signal outputs when memory is expanded externally.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block type
Port CT	PCT0	$\overline{\text{LWR}}$	Write strobe signal output	J
	PCT1	$\overline{\text{UWR}}$		
	PCT2 PCT3	–	Fixed in port mode	A
	PCT4	$\overline{\text{RD}}$	Read strobe signal output	J
	PCT5	–	Fixed in port mode	A
	PCT6	ASTB	Address strobe signal output	J
	PCT7	–	Fixed in port mode	A

(2) Setting in input/output mode and control mode

Port CT is set in input/output mode using the port CT mode register (PMCT). In control mode, it is set using the port CT mode control register (PMCCT).

(a) Port CT mode register (PMCT)

This register can be read or written in 8- or 1-bit units.

Figure 14-38. Port CT Mode Register (PMCT)

	7	6	5	4	3	2	1	0	Address	Initial value
PMCT	PMCT7	PMCT6	PMCT5	PMCT4	PMCT3	PMCT2	PMCT1	PMCT0	FFFFF02AH	FFH

Bit Position	Bit Name	Function
7 to 0	PMCTn (n = 7 to 0)	Specifies input/output mode of PCTn pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port CT mode control register (PMCCT)

This register can be read or written in 8- or 1-bit units.

Figure 14-39. Port CT Mode Control Register (PMCCT)

	7	6	5	4	3	2	1	0	Address	Initial value[Note]
PMCCT	0	PMCCT6	0	PMCCT4	0	0	PMCCT1	PMCCT0	FFFFF04AH	00H/53H

Note 00H: Single-chip mode 0
53H: Single-chip mode 1, ROM-less mode 0 or 1

Bit Position	Bit Name	Function
6	PMCCT6	Specifies operation mode of PCT6 pin 0: Input/output port mode 1: ASTB output mode
4	PMCCT4	Specifies operation mode of PCT4 pin 0: Input/output port mode 1: $\overline{RD}$ output mode
1	PMCCT1	Specifies operation mode of PCT1 pin 0: Input/output port mode 1: $\overline{UWR}$ output mode
0	PMCCT0	Specifies operation mode of PCT0 pin 0: Input/output port mode 1: $\overline{LWR}$ output mode

14.3.10 Port CM

Port CM is a 5-bit input/output port in which input or output can be specified in 1-bit units.

Figure 14-40. Port CM (PCM)

	7	6	5	4	3	2	1	0	Address	Initial value
PCM	–	–	–	PCM4	PCM3	PCM2	PCM1	PCM0	FFFFF00CH	Undefined

Bit Position	Bit Name	Function
4 to 0	PCMn (n = 4 to 0)	Input/output port

Besides functioning as a port, in control mode, this can operate as the wait insertion signal input, internal system clock output, and bus hold control signal output.

(1) Operation in control mode

Port		Alternate Pin Name	Remarks	Block Type
Port CM	PCM0	$\overline{\text{WAIT}}$	Wait insertion signal input	D
	PCM1	CLKOUT	Internal system clock output	K
	PCM2	$\overline{\text{HLDAK}}$	Bus hold acknowledge signal output	J
	PCM3	$\overline{\text{HLDAQ}}$	Bus hold request signal input	D
	PCM4	–	Fixed in port mode	A

(2) Setting in input/output mode and control mode

Port CM is set in input/output mode using the port CM mode register (PMCM). In control mode, it is set using the port CM mode control register (PMCCM).

(a) Port CM mode register (PMCM)

This register can be read or written in 8- or 1-bit units.

Figure 14-41. Port CM Mode Register (PMCM)

	7	6	5	4	3	2	1	0	Address	Initial value
PMCM	1	1	1	PMCM4	PMCM3	PMCM2	PMCM1	PMCM0	FFFFF02CH	FFH

Bit Position	Bit Name	Function
4 to 0	PMCMn (n = 4 to 0)	Specifies input/output mode of PCMn pin. 0: Output mode (Output buffer on) 1: Input mode (Output buffer off)

(b) Port CM mode control register (PMCCM)

This register can be read or written in 8- or 1-bit units.

Figure 14-42. Port CM Mode Control Register (PMCCM)

	7	6	5	4	3	2	1	0	Address	Initial value[Note]
PMCCM	0	0	0	0	PMCCM3	PMCCM2	PMCCM1	PMCCM0	FFFFF04CH	00H/0FH

Note 00H: Single-chip mode 0
0FH: Single-chip mode 1, ROM-less mode 0 or 1

Bit Position	Bit Name	Function
3	PMCCM3	Specifies operation mode of PCM3 pin 0: Input/output port mode 1: $\overline{\text{HLDRQ}}$ input mode
2	PMCCM2	Specifies operation mode of PCM2 pin 0: Input/output port mode 1: $\overline{\text{HLDAK}}$ output mode
1	PMCCM1	Specifies operation mode of PCM1 pin 0: Input/output port mode 1: CLKOUT output mode
0	PMCCM0	Specifies operation mode of PCM0 pin 0: Input/output port mode 1: $\overline{\text{WAIT}}$ input mode

14.4 Noise Elimination Circuit

14.4.1 Interrupt pins

A timing control circuit to guarantee the noise elimination times shown below is added to the pins that operate as NMI and valid edge inputs in port control mode. Signal input that changes in less than these elimination times is not accepted internally.

Pin	Noise Elimination Time
P00/NMI P01/ESO0/INTP0, P02/ESO1/INTP1 P03/ADTRG0/INTP2, P04/ADTRG1/INTP3 P05/INTP4 to P07/INTP6	Analog delay (Approx. 10 ns)

Cautions 1. The above non-maskable/maskable interrupt pins are used to release standby mode. A clock control timing circuit is not used since the internal system clock is stopped in standby mode.

2. The noise elimination circuit is valid only in control mode.

14.4.2 Timer 10, timer 11, timer 3 input pins

Noise filtering using the clock sampling shown below is added to the pins that operate as valid edge inputs to timer 10, timer 11, and timer 3. A signal input that changes in less than these elimination times is not accepted internally.

Pin		Noise Elimination Time	Sampling Clock
Timer 10	P10/TIUD10 P11/TCUD10/INTP100 P12/TCLR10/INTP101	4 to 5 clocks	Select from $\phi_{TM10,11,2}$ $\phi_{TM10,11,2}/2$ $\phi_{TM10,11,2}/4$ $\phi_{TM10,11,2}/8$
Timer 11	P13/TIUD11 P14/TCUD11/INTP110 P15/TCLR11/INTP111		
Timer 3	P26/TI3/INTP30/TCLR3		Select from $\phi_{TM3}/2$ $\phi_{TM3}/4$ $\phi_{TM3}/8$ $\phi_{TM3}/16$
	P27/TO3/INTP31		Select from $\phi_{TM3}/32$ $\phi_{TM3}/64$ $\phi_{TM3}/128$ $\phi_{TM3}/256$

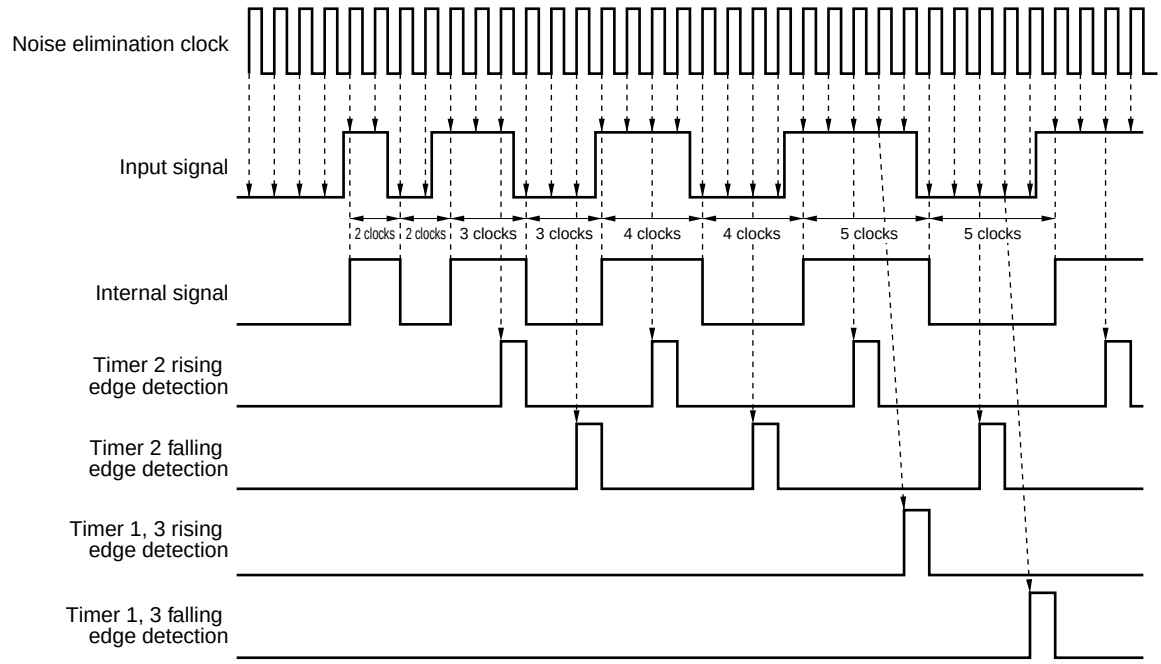
Cautions 1. Since the above pin noise filtering uses clock sampling, input signals are not received when the CPU clock is stopped.

2. The noise elimination circuit is valid only in control mode.

Remark $\phi_{TM10,11,2}$: Clock selected in PRM02 register

ϕ_{TM3} : Clock selected in PRM03 register

Figure 14-43. Example of Noise Elimination Timing



Cautions

1. **If there are two or less noise elimination clocks while the timer 2 input signal is high level (or low level), the input pulse is eliminated as noise. If it is sampled at least three times, the edge is detected as valid input.**
2. **If there are three or less noise elimination clocks while the timer 1 or 3 input signal is high level (or low level), the input pulse is eliminated as noise. If it is sampled at least four times, the edge is detected as valid input.**

(1) Timer 10 noise elimination time selection register (NRC10)

The NRC 10 register is used to set the clock source of timer 10 input pin noise elimination times.

It can be read or written in 8- or 1-bit units.

Figure 14-44. Timer 10 Noise Elimination Time Selection Register (NRC10)

	7	6	5	4	3	2	1	0	Address	Initial value
NRC10	0	0	0	0	0	0	NRC101	NRC100	FFFFF5F8H	00H

Bit Position	Bit Name	Function
1, 0	NRC101, NRC100	Selects the TIUD10, TCUD10/INTP100, and TCLR10/INTP101 pin noise elimination clocks.

NRC101	NRC100	Noise elimination clocks
0	0	$\phi_{TM10, 11, 2}/8$
0	1	$\phi_{TM10, 11, 2}/4$
1	0	$\phi_{TM10, 11, 2}/2$
1	1	$\phi_{TM10, 11, 2}$

Remark $\phi_{TM10,11,2}$: Clock selected in PRM02 register

(2) Timer 11 noise elimination time selection register (NRC11)

The NRC11 register is used to set the clock source of timer 11 input pin noise elimination times.

It can be read or written in 8- or 1-bit units.

Figure 14-45. Timer 11 Noise Elimination Time Selection Register (NRC11)

	7	6	5	4	3	2	1	0	Address	Initial value
NRC11	0	0	0	0	0	0	NRC111	NRC110	FFFFF618H	00H

Bit Position	Bit Name	Function
1, 0	NRC111, NRC110	Selects the TIUD11, TCUD11/INTP110, and TCLR11/INTP111 pin noise elimination clocks.

NRC111	NRC110	Noise elimination clocks
0	0	$\phi_{TM10, 11, 2}/8$
0	1	$\phi_{TM10, 11, 2}/4$
1	0	$\phi_{TM10, 11, 2}/2$
1	1	$\phi_{TM10, 11, 2}$

Remark $\phi_{TM10,11,2}$: Clock selected in PRM02 register

(3) Timer 3 noise elimination time selection register (NRC3)

The NRC3 register is used to set the clock source of timer 3 input pin noise elimination times.

It can be read or written in 8- or 1-bit units.

Figure 14-46. Timer 3 Noise Elimination Time Selection Register (NRC3)

	7	6	5	4	3	2	1	0	Address	Initial value
NRC3	0	0	0	0	NRC33	NRC32	NRC31	NRC30	FFFFF698H	00H

Bit Position	Bit Name	Function
3, 2	NRC33, NEC32	Selects the TO3/INTP31 pin noise elimination clock.

NRC33	NRC32	Noise elimination clock
0	0	ϕ_{TM3}/256
0	1	ϕ_{TM3}/128
1	0	ϕ_{TM3}/64
1	1	ϕ_{TM3}/32

Remark ϕ_{TM3}: Clock selected in PRM03 register

Bit Position	Bit Name	Function
1, 0	NEC31, NEC30	Selects the TI3/INTP30/TCLR3 pin noise elimination clock.

NRC31	NRC30	Noise elimination clocks
0	0	ϕ_{TM3}/16
0	1	ϕ_{TM3}/8
1	0	ϕ_{TM3}/4
1	1	ϕ_{TM3}/2

Remark ϕ_{TM3}: Clock selected in PRM03 register

14.4.3 Timer 2 input pins

A noise elimination circuit using analog filtering and digital filtering using clock sampling are added to the timer 2 input pins. A signal input that changes in less than these elimination times is not accepted internally.

Pin	Analog Filter Noise Elimination Time	Digital Filter	
		Noise Elimination Time	Sampling Clock
P20/TI2/INTP20 P21/TO21/INTP21 to P24/TO24/INTP24 P25/TCLR2/INTP25	10 to 100 ns	4 to 5 clocks	$\phi_{TM10, 11, 2}/4$

Cautions 1. Since digital filtering uses clock sampling, if it is selected, input signals are not received when the CPU clock is stopped.

2. The noise elimination circuit is valid only in control mode.

3. Refer to Figure 14-43 for an example of a noise elimination circuit.

Remarks $\phi_{TM10,11,2}$: Clock selected in PRM02 register

(1) Timer 2 input filter mode registers 0 to 5 (FEM0-FEM5)

The FEMn registers are used to specify timer 2 input pin filtering and to set the clock source of noise elimination times and the input valid edge.

It can be read or written in 8- or 1-bit units.

Figure 14-47. Timer 2 Input Filter Mode Registers 0 to 5 (FEM0 to FEM5) (1/2)

	7	6	5	4	3	2	1	0	Address	Initial value
FEM0	DFEN00	0	FSMP010	FSMP000	EDGE010	EDGE000	TMS010	TMS000	FFFFF630H	00H
					INTP20					
FEM1	DFEN01	0	FSMP011	FSMP001	EDGE011	EDGE001	TMS011	TMS001	FFFFF631H	00H
					INTP21					
FEM2	DFEN02	0	FSMP012	FSMP002	EDGE012	EDGE002	TMS012	TMS002	FFFFF632H	00H
					INTP22					
FEM3	DFEN03	0	FSMP013	FSMP003	EDGE013	EDGE003	TMS013	TMS003	FFFFF633H	00H
					INTP23					
FEM4	DFEN04	0	FSMP014	FSMP004	EDGE014	EDGE004	TMS014	TMS004	FFFFF634H	00H
					INTP24					
FEM5	DFEN05	0	FSMP015	FSMP005	EDGE015	EDGE005	TMS015	TMS005	FFFFF635H	00H
					INTP25					

Bit Position	Bit Name	Function
7	DFEN0n	Specifies the INTP2n pin filter. 0: Analog filter 1: Digital filter
5, 4	FSMP01n, FSMP00n	Selects the digital filter sampling clock.

FSMP01n	FSMP00n	Sampling Clock
0	0	ϕ_{TM2}
Other than above		Setting prohibited

Remark ϕ_{TM2}: Clock selected in PRM02 register

Remark n = 0 to 5

Figure 14-47. Timer 2 Input Filter Mode Registers 0 to 5 (FEM0 to FEM5) (2/2)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>3, 2</td><td>EDGE01n,
EDGE00n</td><td>Specifies the INTP2n pin valid edge.

<table>
<tr><th>EDGE01n</th><th>EGE00n</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>Interrupt due to INTCC2n^{Note}</td></tr>
<tr><td>0</td><td>1</td><td>Rising edge</td></tr>
<tr><td>1</td><td>0</td><td>Falling edge</td></tr>
<tr><td>1</td><td>1</td><td>Both rising and falling edges</td></tr>
</table>
Note Specify when selecting INTCC2n according to match of TM20, TM21 and subchannel compare registers (TMS01n, TMS00n bit settings) (n = 0 to 5).</td></tr>
<tr><td>1, 0</td><td>TMS01n,
TMS00n</td><td>Selects capture input^{Note}.

<table>
<tr><th>TMS01n</th><th>TMS00n</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>Use as pin</td></tr>
<tr><td>0</td><td>1</td><td>Digital filter (noise elimination circuit specification)</td></tr>
<tr><td>1</td><td>0</td><td>Capture to subchannel 1 according to timer</td></tr>
<tr><td>1</td><td>1</td><td>Capture to subchannel 2 according to timer</td></tr>
</table>
Note Capture input according to INTCM100 and INTCM101 can be selected only for the FEM1 and FEM2 registers. Set the values of the TMS01m and TMS00m bits in the FEMm register to 00B or 01B. Settings other than these are prohibited (m = 1, 3 to 5).
Capture according to INTP21, INTP22 and INTCM100, INTCM101 is possible for subchannel 1 and subchannel 2 of timer 2.
Examples are shown below.
(a) Capture subchannel 1 on INTCM101
FEM1 register = xxxxxx10B
TMIC0 register = 00000010B
(b) Capture subchannel 2 on INTCM101
FEM2 register = xxxxxx11B
TMIC0 register = 00001000B</td></tr>
</table>

Remark n = 0 to 5

CHAPTER 15 RESET FUNCTION

When a low level is input to the $\overline{\text{RESET}}$ pin, there is a system reset and each hardware item of the V850E/IA1 is initialized to its initial status.

When the $\overline{\text{RESET}}$ pin changes from low level to high level, reset status is released and the CPU starts program execution. Initialize the contents of various registers as needed within the program.

15.1 Features

- Noise elimination using analog delay (approx. 60 ns) in reset pin ($\overline{\text{RESET}}$)

15.2 Pin Functions

During a system reset period, most pin output is high impedance (all pins except CLKOUT[Note], $\overline{\text{RESET}}$, X2, V_{DD5}, V_{SS5}, V_{DD3}, V_{SS3}, CV_{DD}, CV_{SS}, AV_{DD}, AV_{REF}, and AV_{SS} pins).

Thus, if for example memory is extended externally, a pull-up (or pull-down) resistor must be attached to each pin of ports DH, DL, CS, CT, and CM. If there are no resistors, the external memory that is connected may be destroyed when these pins become high impedance.

Similarly, perform pin processing so that on-chip peripheral I/O function signal output and output ports are not affected.

Note In ROMless mode 0 or 1 and single-chip mode 1, CLKOUT signals also are output during a reset period. In single-chip mode 0, CLKOUT signals are not output until the PMCCM register is set.

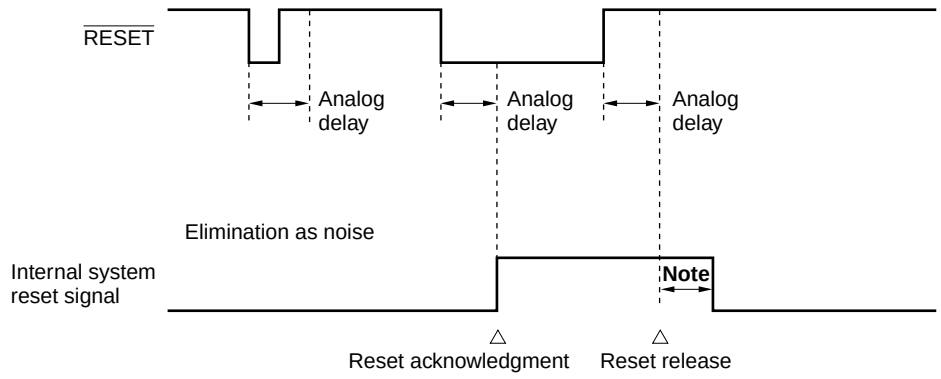
The V850E/IA1 has a total of 83 on-chip input/output ports (ports 0 to 4, DH, DL, CS, CT, CM), of which 8 are input-only ports. The port configuration is shown below.

Table 15-1 shows the operation status of each pin during a reset period.

Table 15-1. Operation Status of Each Pin During Reset Period

Pin Name		Pin Status			
		In Single-Chip Mode 0	In Single-Chip Mode 1	In ROM-Less Mode 0	In ROM-Less Mode 1
A16 to A23, AD0 to AD15, $\overline{CS0}$ to $\overline{CS7}$, $\overline{LWR}$, $\overline{UWR}$, $\overline{RD}$, ASTB, $\overline{WAIT}$, $\overline{HLDAK}$, $\overline{HLDRQ}$		(Port mode)	High impedance		
CLKOUT		(Port mode)	Operation		
Port pins	Ports 0 to 4	(Input)			
	Ports CM, CS, CT, DH, DL	(Input)	(Control mode)		

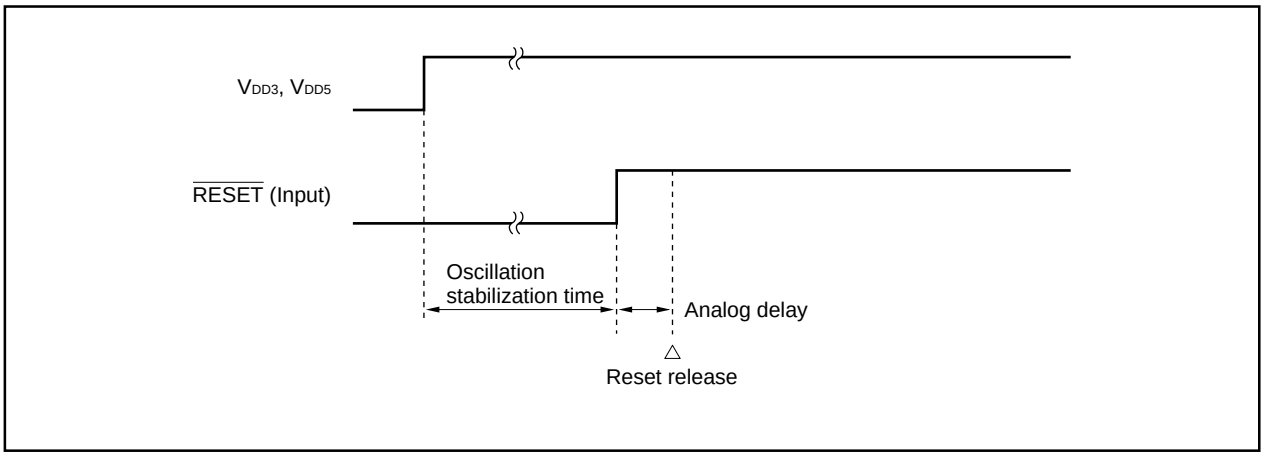
(1) Reset signal acknowledgment



Note The internal system reset signal continues in active status for a period of at least 4 system clocks after the timing of a reset release by the $\overline{RESET}$ signal.

(2) Reset at power-on

A reset operation at power-on (power supply application) must guarantee oscillation stabilization time from power-on until reset acknowledgment due to the low level width of the $\overline{\text{RESET}}$ signal.



15.3 Initialization

Initialize the contents of each register as needed within a program.

Table 15-2 shows the initial values of the CPU, internal RAM, and on-chip peripheral I/O after reset.

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (1/6)

On-Chip Hardware		Register Name	Initial Value After Reset
CPU	Program registers	General-purpose register (r0)	00000000H
		General-purpose registers (r1 to r31)	Undefined
		Program counter (PC)	00000000H
	System registers	Status save registers during interrupt (EIPC, EIPSW)	Undefined
		Status save registers during NMI (FEPC, FEPSW)	Undefined
		Interrupt cause register (ECR)	00000000H
		Program status word (PSW)	00000020H
		Status save registers during CALLT execution (CTPC, CTPSW)	Undefined
		Status save registers during exception/debug trap (DBPC, DBPSW)	Undefined
		CALLT base pointer (CTBP)	Undefined
Internal RAM		–	Undefined
On-chip peripheral I/O	Bus control function	Chip area selection control register n (CSCn) (n = 0,1)	2C11H
		Peripheral area selection control register (BPC)	0000H
		Bus size configuration register (BSC)	0000H/5555H
		System wait control register (VSWC)	77H
	Memory control function	Bus cycle type configuration register n (BCTn) (n = 0,1)	CCCCH
		Data wait control register n (DWCn) (n = 0,1)	3333H
		Address wait control register (AWC)	0000H
		Bus cycle control register (BCC)	AAAAH

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (2/6)

On-Chip Hardware		Register Name	Initial Value After Reset
On-chip peripheral I/O	DMA function	DMA source address register nL (DSAnL) (n = 0 to 3)	Undefined
		DMA source address register nH (DSAnH) (n = 0 to 3)	Undefined
		DMA destination address register nL (DDAnL) (n = 0 to 3)	Undefined
		DMA destination address register nH (DDAnH) (n = 0 to 3)	Undefined
		DMA transfer count register n (DBCn) (n = 0 to 3)	Undefined
		DMA addressing control register n (DADCn) (n = 0 to 3)	0000H
		DMA channel control register n (DCHCn) (n = 0 to 3)	00H
		DMA disable status register (DDIS)	00H
		DMA restart register (DRST)	00H
		DMA trigger source register n (DTFRn) (n = 0 to 3)	00H
	Interrupt/exception control function	In service priority register (ISPR)	00H
		External interrupt mode register n (INTMn) (n = 0 to 2)	00H
		Interrupt mask register n (IMRn) (n = 0 to 3)	FFFFH
		Signal edge selection register n (SESAn) (n = 10,11)	00H
		Valid edge selection register (SESC)	00H
		Timer 2 input filter mode register n (FEMn) (n = 0 to 5)	00H
		Interrupt control registers (P0IC0 to P0IC6, DETIC0, DETIC1, TM0IC0, CM03IC0, TM0IC1, CM03IC1, CC10IC0, CC10IC1, CM10IC0, CM10IC1, CC11IC0, CC11IC1, CM11IC0, CM11IC1, TM2IC0, TM2IC1, CC2IC0 to CC2IC5, TM3IC0, CC3IC0, CC3IC1, CM4IC0, DMAIC0 to DMAIC3, CANIC0 to CANIC3, CSIIC0, CSIIC1, SRIC0 to SRIC2, STIC0 to STIC2, SEIC0, ADIC0, ADIC1)	47H
	Power save control function	Command register (PRCMD)	Undefined
		Power save control register (PSC)	00H
		Clock control register (CKC)	00H
		Power save mode register (PSMR)	00H
		Lock register (LOCK)	Undefined
	System control	Peripheral command register (PHCMD)	Undefined
		Peripheral status register (PHS)	00H
	Timer 0	Dead time timer reload register n (DTRRn) (n = 0,1)	FFFH
		Buffer registers CM0n, CM1n (BFCM0n, BFCM1n) (n = 0 to 3)	FFFFH
		Timer control register 0n (TMC0n) (n = 0,1)	0508H
		Timer unit control register 0n (TUC0n) (n = 0,1)	01H
		Timer output mode register n (TOMRn) (n = 0,1)	00H
		PWM software timing output register n (PSTOn) (n = 0,1)	00H
		PWM output enable register n (POERn) (n = 0,1)	00H
		TOMR write enable register n (SPECn) (n = 0,1)	0000H
		Timer 0n clock selection register (PRM01)	00H

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (3/6)

On-Chip Hardware		Register Name	Initial Value After Reset
On-chip peripheral I/O	Timer 1	Timer 1n (TM1n) (n = 0,1)	0000H
		Compare register 1n (CM1n) (n = 00,01,10,11)	0000H
		Capture/compare register 1n (CC1n) (n = 00,01,10,11)	0000H
		Capture/compare control register n (CCRn) (n = 0,1)	00H
		Timer unit mode register n (TUMn) (n = 0,1)	00H
		Timer control register 1n (TMCn) (n = 0,1)	00H
		Signal edge selection register 1n (SESA1n) (n = 0.1)	00H
		Prescaler mode register 1n (PRM1n) (n = 0,1)	07H
		Status register n (STATUSn) (n = 0,1)	00H
		Timer connection selection register 0 (TMIC0)	00H
		Timer 1n/timer 2n clock selection register (PRM02)	00H
		CC1n1 capture input selection register (CSL1n) (n = 0,1)	00H
		Timer 1n noise elimination time selection register (NRC1n) (n = 0,1)	00H
	Timer 2	Timer 2 clock stop register (STOPTE0)	0000H
		Timer 2 count clock/control edge selection register (CSE0)	0000H
		Timer 2 subchannel input event edge selection register (SESE0)	0000H
		Timer 2 time base control register (TCRE0)	0000H
		Timer 2 output control register (OCTLE0)	0000H
		Timer 2 subchannels 0 and 5 capture/compare control register (CMSE050)	0000H
		Timer 2 subchannels 1 and 2 capture/compare control register (CMSE120)	0000H
		Timer 2 subchannels 3 and 4 capture/compare control register (CMSE340)	0000H
		Timer 2 subchannel n secondary capture/compare register (CVSEn0) (n = 0 to 4)	0000H
		Timer 2 subchannel n main capture/compare register (CVPEn0) (n = 0 to 4)	0000H
		Timer 2 subchannel n capture/compare register (CVSEn0) (n = 0,5)	0000H
		Timer 2 time base status register (TBSTATE0)	0000H
		Timer 2 capture/compare 1 to 4 status register (CCSTATE0)	0000H
		Timer 2 output delay register (ODELE0)	0000H
		Timer 2 software event capture register (OSCE0)	0000H
	Timer 3	Timer 3 (TM3)	0000H
		Capture/compare register 3n (CC3n) (n = 0,1)	0000H
		Timer control register 30 (TMC30)	00H
		Timer control register 31 (TMC31)	20H
		Valid edge selection register (SESC)	00H
		Timer 3 clock selection register (PRM03)	00H
		Timer 3 noise elimination time selection register (NRC3)	00H

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (4/6)

On-Chip Hardware		Register Name	Initial Value After Reset
	Timer 4	Timer 4 (TM4)	0000H
		Compare register 4 (CM4)	0000H
		Timer control register 4 (TMC4)	00H
On-chip peripheral I/O	Serial interface function (CSI0, CSI1)	Clocked serial interface mode register n (CSIMn) (n = 0,1)	00H
		Clocked serial interface clock selection register n (CSICn) (n = 0,1)	00H
		Clocked serial interface receive buffer register n (SIRBn) (n = 0,1)	0000H
		Clocked serial interface transmit buffer register n (SOTBn) (n = 0,1)	0000H
		Clocked serial interface read-only receive buffer register n (n = 0,1)	0000H
		Clocked serial interface first stage transmit buffer register n (SOTBFn) (n = 0,1)	0000H
		Serial I/O shift register n (SIOn) (n = 0,1)	0000H
		Prescaler mode register (PRSM3)	00H
		Prescaler compare register (PRSCM3)	00H
	Serial interface function (UART0)	Asynchronous serial interface mode register 0 (ASIM0)	01H
		Receive buffer register 0 (RXB0)	FFH
		Asynchronous serial interface status register 0 (ASIS0)	00H
		Transmit buffer register 0 (TXB0)	FFH
		Asynchronous serial interface transmit status register 0 (ASIF0)	00H
		Baud rate generator control register 0 (BRGC0)	FFH
		Clock selection register 0 (CKSR0)	00H
	Serial interface function (UART1, UART2)	Asynchronous serial interface mode register n0 (ASIMn0) (n=1,2)	81H
		Asynchronous serial interface mode register n1 (ASIMn1) (n=1,2)	00H
		Asynchronous serial interface status register n (ASISn) (n=1,2)	00H
		2-frame consecutive receive buffer register n (RXBn) (n=1,2)	Undefined
		Receive buffer register Ln (RXBLn) (n = 1,2)	Undefined
		2-frame consecutive transmit shift register n (TXSn) (n = 1,2)	Undefined
		Transmit shift register Ln (TXSLn) (n = 1,2)	Undefined
		Prescaler mode register n (PRSMn) (n = 1,2)	00H
		Prescaler compare register n (PRSCMn) (n = 1,2)	00H
	Serial interface function (FCAN)	CAN message data length register n (M_DLCn) (n = 00 to 31)	Undefined
		CAN message control register n (M_CTRLn) (n = 00 to 31)	Undefined
		CAN message time stamp register n (M_TIMEn) (n = 00 to 31)	Undefined
		CAN message data register nm (M_DATAnm) (n = 00 to 31, m = 0 to 7)	Undefined
		CAN message ID register Ln, Hn (M_IDLn, M_IDHn) (n = 00 to 31)	Undefined

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (5/6)

On-Chip Hardware		Register Name	Initial Value After Reset
On-chip peripheral I/O	Serial interface function (FCAN)	CAN message configuration register n (M_CONFn) (n = 00 to 31)	Undefined
		CAN message status register n (M_STATn) (n = 00 to 31)	Undefined
		CAN status set/cancel register n (SC_STATn) (n = 00 to 31)	0000H
		CAN interrupt hold register (CCINTP)	0000H
		CAN global interrupt hold register (CGINTP)	00H
		CAN1 local interrupt hold register (C1INTP)	00H
		CAN stop register (CSTOP)	0000H
		CAN global status register (CGST)	0100H
		CAN global interrupt enable register (CGIE)	0A00H
		CAN main clock selection register (CGCS)	7F05H
		CAN time stamp count register (CGTSC)	0000H
		CAN message retrieval start/result register (CGMSS on write; CGMSR on read)	0000H
		CAN1 address mask register Ln, Hn (C1MASKLn, C1MASKHn) (n = 0 to 3)	Undefined
		CAN1 control register (C1CTRL)	0101H
		CAN1 definition register (C1DEF)	0000H
		CAN1 information register (C1LAST)	00FFH
		CAN1 error counter register (C1ERC)	0000H
		CAN1 interrupt enable register (C1IE)	0900H
		CAN1 bus active register (C1BA)	00FFH
		CAN1 bit rate prescaler register (C1BRP)	0000H
		CAN1 bus diagnostic information register (C1DINF)	0000H
		CAN1 synchronization control register (C1SYNC)	0218H
		FCAN clock selection register (PRM04)	00H
	A/D converter	A/D scan mode register n0 (ADSCMn0) (n = 0,1)	0000H
		A/D scan mode register n1 (ADSCMn1) (n = 0,1)	0000H
		A/D voltage detection register n (ADETMn) (n = 0,1)	0000H
		A/D conversion result register 0n (ADCR0n) (n = 0 to 7)	0000H
		A/D conversion result register 1n (ADCR1n) (n = 0 to 7)	0000H
		A/D internal trigger selection register (ITRG0)	00H

Table 15-2. Initial Values of CPU, Internal RAM, and On-Chip Peripheral I/O After Reset (6/6)

On-Chip Hardware		Register Name	Initial Value After Reset
On-chip peripheral I/O	Port function	Ports (P0 to P4, PDH, PDL, PCS, PCT, PCM)	Undefined
		Mode registers (PM1 to PM4, PMDH, PMCS, PMCT, PMCM)	FFH
		Mode register (PMDL)	FFFFH
		Mode control registers (PMC1 to PMC4)	00H
		Mode control registers (PMCDH, PMCCS)	00H/FFH
		Mode control register (PMCDL)	0000H/FFFFH
		Mode control register (PMCCT)	00H/53H
		Mode control register (PMCCM)	00H/0FH
		Function control registers (PFC1, PFC2)	00H
	NBD function	RAM access data buffer L (NBDL)	0000H
		RAM access data buffer LU (NBDLU)	00H
		RAM access data buffer H (NBDH)	0000H
		RAM access data buffer HU (NBDHU)	00H
		DMA source address setting register SL (NBDMSL)	Undefined
		DMA source address setting register SH (NBDMSH)	Undefined
		DMA destination address setting register DL (NBDMDL)	Undefined
		DMA destination address setting register DH (NBDMDH)	Undefined
		RAM address alternate register L (ISL_RAML)	0000H
		RAM address alternate register H (ISL_RAMH)	0000H
		ROM address alternate register L (ISL_ROML)	0000H
		ROM address alternate register H (ISL_ROMH)	0000H
	Flash memory	Flash programming mode control register (FLPMC)	08H/0CH

Caution In the table above, "Undefined" means either undefined at the time of a power-on reset or undefined due to data destruction when $\overline{\text{RESET}}$ ↓ input and data write timing are synchronized. On a $\overline{\text{RESET}}$ ↓ other than this, data is maintained in its previous status.

CHAPTER 16 FLASH MEMORY (μPD70F3116)

The μPD70F3116 is the flash memory version of the V850E/IA1 and it has an on-chip 256 KB flash memory configured as two 128-Kbyte areas.

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

Writing to a flash memory can be performed with memory mounted on the target system (on board). The dedicated flash programmer is connected to the target system to perform writing.

The following can be considered as the development environment and the applications using a flash memory.

- Software can be changed after the V850E/IA1 is solder mounted on the target system.
- Small scale production of various models is made easier by differentiating software.
- Data adjustment in starting mass production is made easier.

16.1 Features

- All area batch erase, or erase in block units (128 KB)
- Communication through serial interface from the dedicated flash programmer
- Erase/write voltage: V_{PP} = 7.8 V
- On-board programming
- Flash memory programming is possible by the selfwrite in block units (128 KB)

16.2 Writing by Flash Programmer

Writing can be performed either on-board or off-board by the dedicated flash programmer.

(1) On-board programming

The contents of the flash memory is rewritten after the V850E/IA1 is mounted on the target system. Mount connectors, etc., on the target system to connect the dedicated flash programmer.

(2) Off-board programming

Writing to a flash memory is performed by the dedicated program adapter (FA Series), etc., before mounting the V850E/IA1 on the target system.

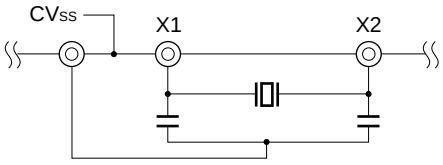
Remark The FA Series is a product of Naito Densei Machida Mfg. Co., Ltd.

When the flash programming adapter (FA-144GJ-8EU) is used for writing, connect the pins as follows.

Table 16-1. Connection of V850E/IA1 Flash Programming Adapter (FA-144GJ-8EU)

FA-144GJ-8EU Silk Name	V850E/IA1			
	UART0		CSI0	
	Pin Name	Pin No.	Pin Name	Pin No.
SI	TXD0/P31	38	SO0/P41	30
SO	RXD0/P30	37	SI0/P40	29
SCK	–		$\overline{SCK0}$/P42	31
X1	X1	23 Note 1	X1	23 Note 1
X2	X2	24 Note 1	X2	24 Note 1
/RESET	$\overline{RESET}$	20	$\overline{RESET}$	20
V_{PP}	V_{PP}/IC5	89	V_{PP}/IC5	89
RESERVE/HS	–		A16/PDH0 Note 1	73
LVDD	V_{DD3}	53, 128	V_{DD3}	53, 128
	CV_{DD}	21	CV_{DD}	21
VDD	V_{DD5}	56, 91, 125	V_{DD5}	56, 91, 125
	AV_{REF0}	137	AV_{REF0}	137
	AV_{REF1}	4	AV_{REF1}	4
	MODE1	27	MODE1	27
	AV_{DD}	2,135	AV_{DD}	2,135
GND	V_{SS3}	54, 127	V_{SS3}	54, 127
	V_{SS5}	55, 90, 126	V_{SS5}	55, 90, 126
	AV_{SS}	3,136	AV_{SS}	3,136
	CV_{SS}	22	CV_{SS}	22
	MODE0	26	MODE0	26
	MODE2	28	MODE2	28
	NMI/P00	111	NMI/P00	111
Note 3	CKSEL	25	CKSEL	25

Notes 1. Configure the oscillator on the FA-144GJ-8EJ board using a resonator and a capacitor. The following figure shows an example of the oscillator.



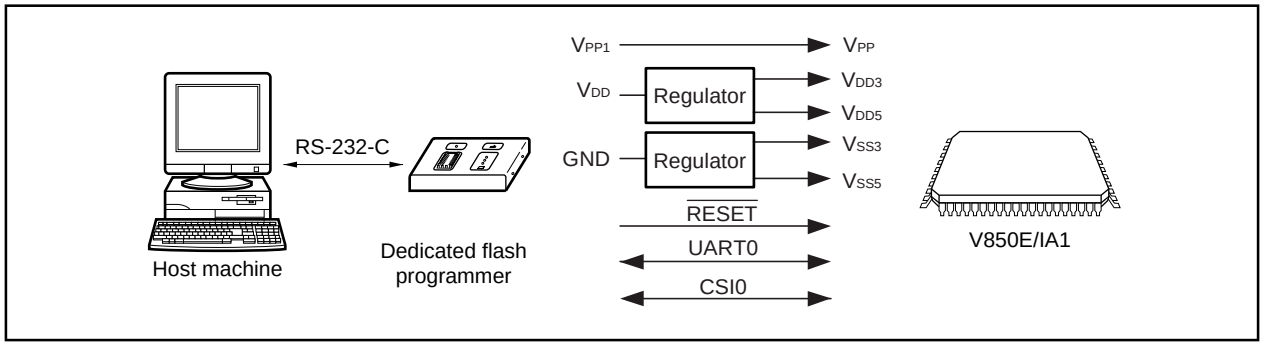
2. Connection is not required for this pin when not using handshakes.

3. In PLL mode: GND
In direct mode: V_{DD5}

Remark –: Leave open

16.3 Programming Environment

The following shows the environment required for writing programs to the flash memory of the V850E/IA1.



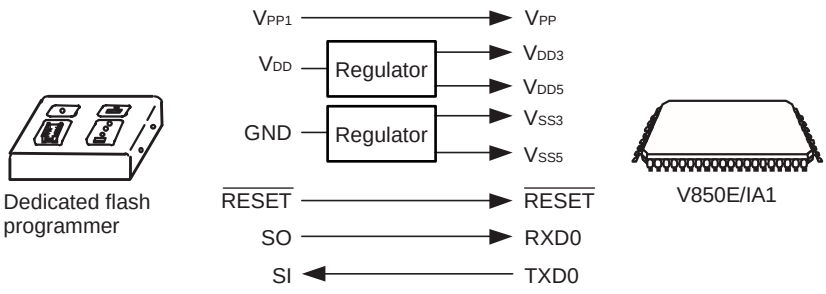
A host machine is required for controlling the dedicated flash programmer.

UART0 or CSI0 is used for the interface between the dedicated flash programmer and the V850E/IA1 to perform writing, erasing, etc. A dedicated program adapter (FA Series) is required for off-board writing. Supply the operating clock of the V850E/IA1 via the oscillator configured on the V850E/IA1 board using a resonator and a capacitor.

16.4 Communication Mode

(1) UART0

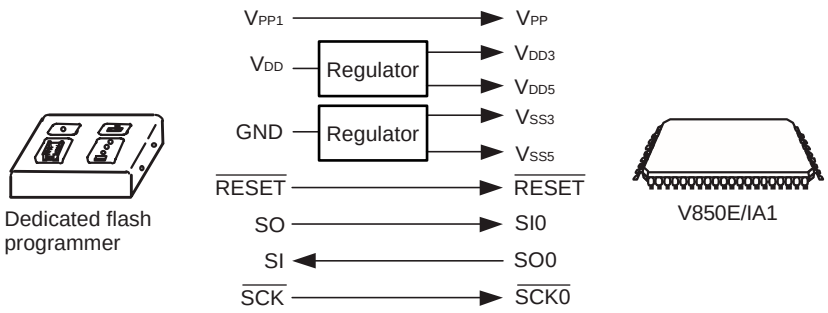
Transfer rate: 4,800 bps to 76,800 bps (LSB first)



Caution Supply the operating clock of the V850E/IA1 via the oscillator configured on the V850E/IA1 board using a resonator and a capacitor.

(2) CSI0

Transfer rate: up to 2 MHz (MSB first)

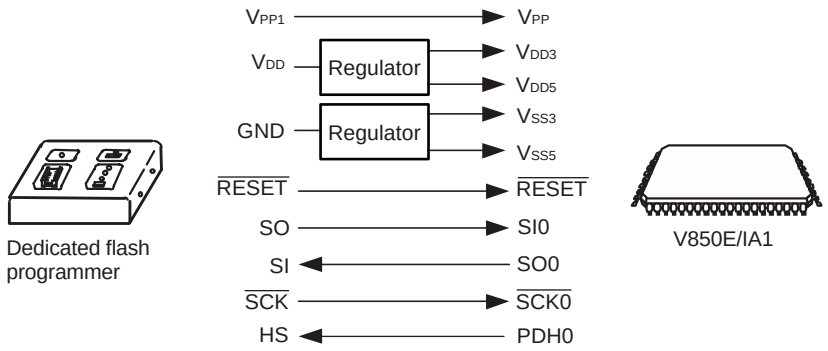


Caution Supply the operating clock of the V850E/IA1 via the oscillator configured on the V850E/IA1 board using a resonator and a capacitor.

The dedicated flash programmer outputs transfer clocks and the V850E/IA1 operates as a slave.

(3) Handshake-supported CSI communication

Transfer rate: up to 2 MHz (MSB first)



Caution Supply the operating clock of the V850E/IA1 via the oscillator configured on the V850E/IA1 board using a resonator and a capacitor.

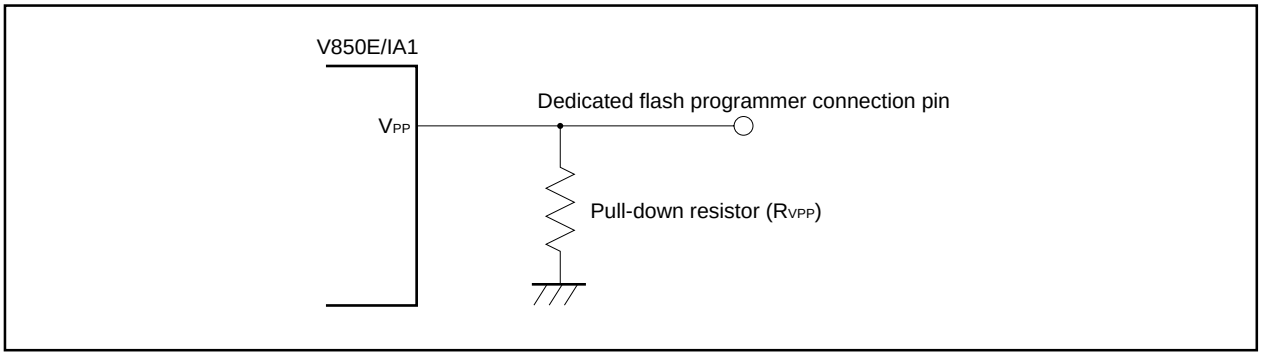
16.5 Pin Connection

When performing on-board writing, install a connector on the target system to connect to the dedicated flash programmer. Also, install a function on-board to switch from the normal operation mode (single-chip modes 0, 1 or ROM-less modes 0, 1) to the flash memory programming mode.

In the flash memory programming mode, all the pins not used for flash memory programming become the same status as they were immediately after reset in single-chip mode 0. Therefore, all the ports become output high-impedance status, so that pin connection is required when the external device does not acknowledge the output high-impedance status.

16.5.1 V_{PP} pin

In the normal operation mode, 0 V is input to the V_{PP} pin. In the flash memory programming mode, 7.8 V writing voltage is supplied to the V_{PP} pin. The following shows an example of the connection of the V_{PP} pin.



16.5.2 Serial interface pin

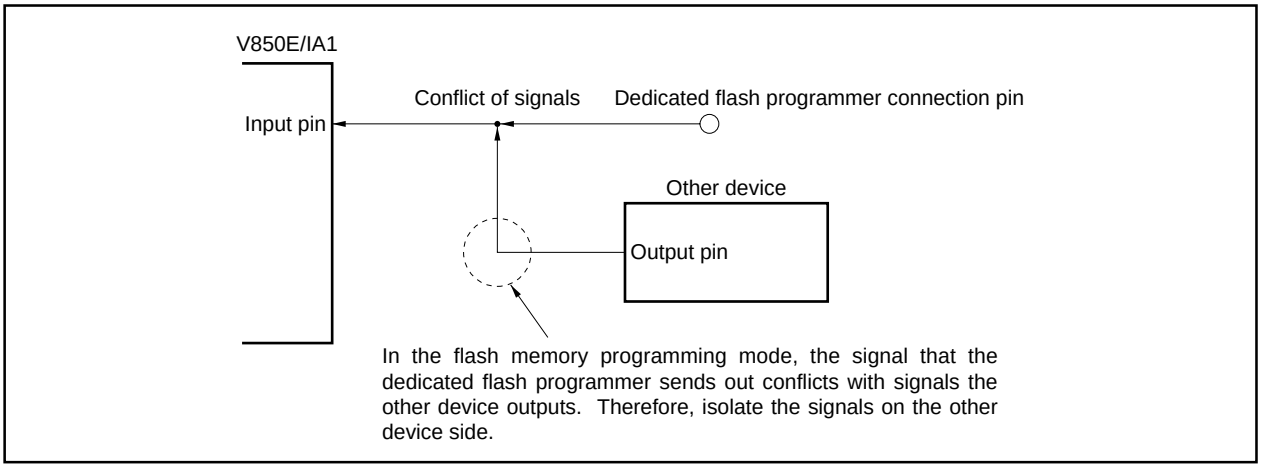
The following shows the pins used by each serial interface.

Serial Interface	Pins Used
CSI0	SO0, SI0, $\overline{SCK0}$
UART0	TXD0, RXD0

When connecting a dedicated flash programmer to a serial interface pin that is connected to other devices on-board, care should be taken to avoid the conflict of signals and the malfunction of other devices, etc.

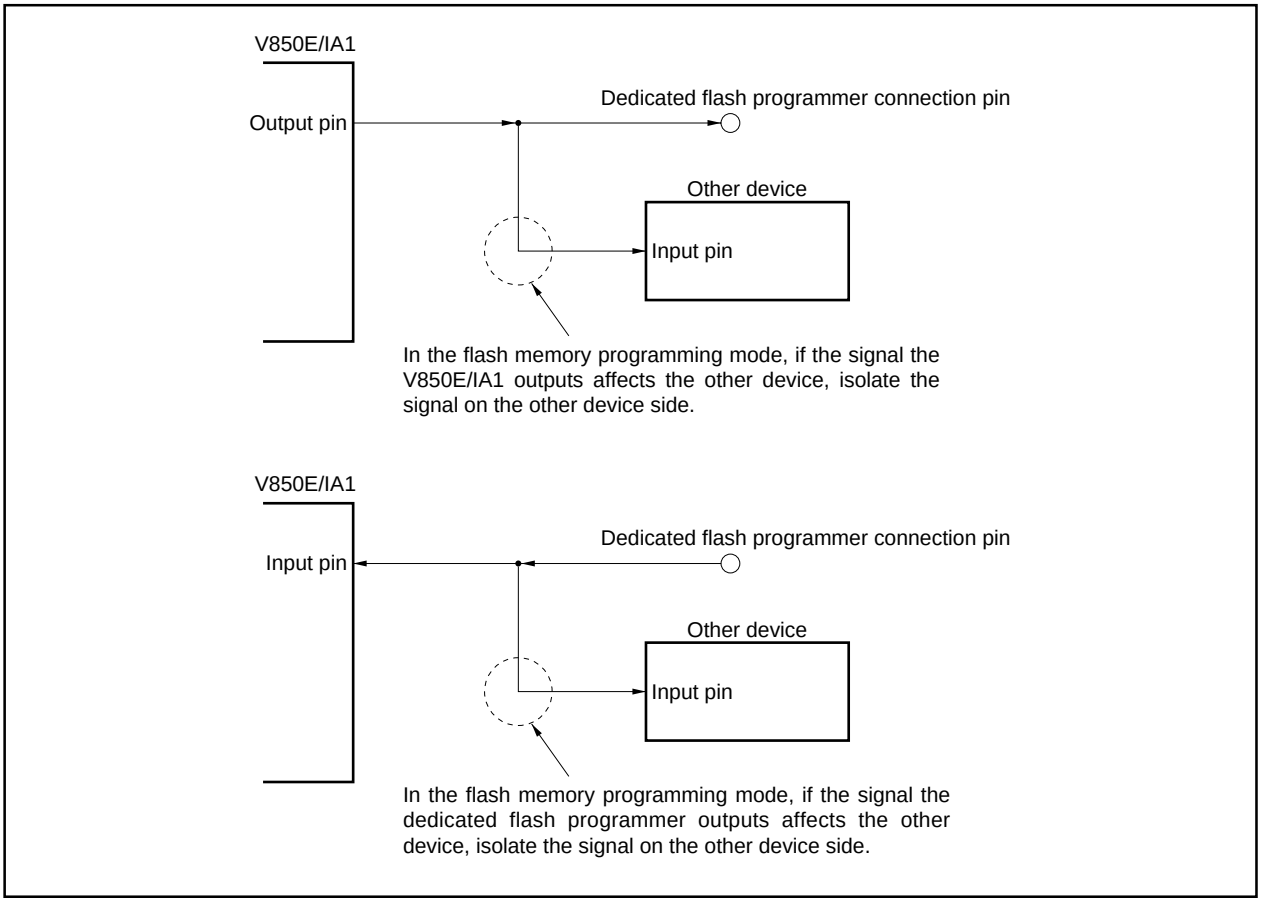
(1) Conflict of signals

When connecting a dedicated flash programmer (output) to a serial interface pin (input) which is connected to another device (output), a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the other device or set the other device to the output high-impedance status.



(2) Malfunction of the other device

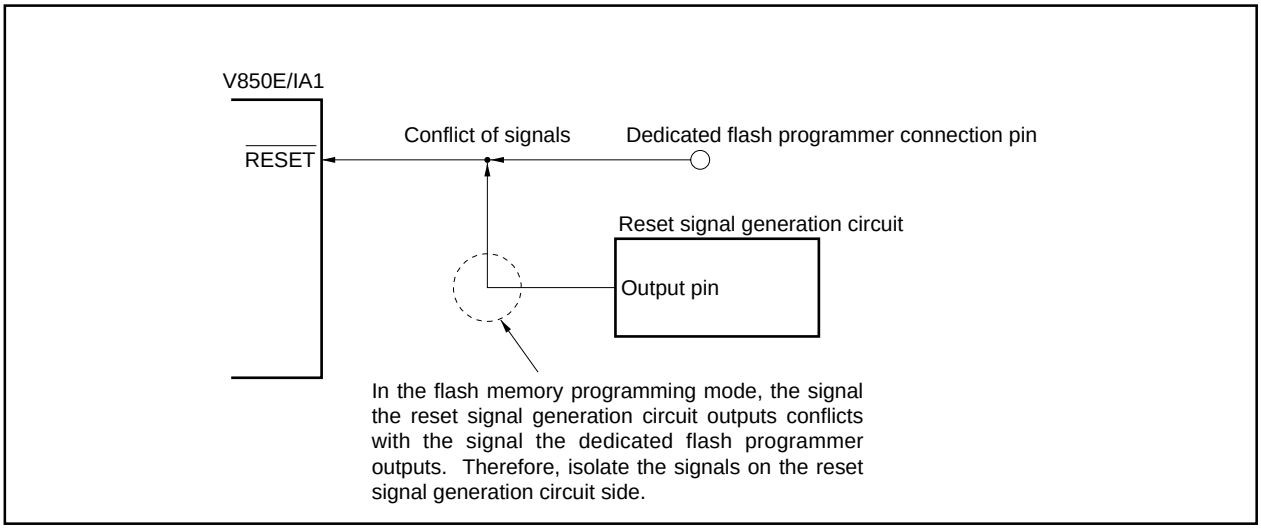
When connecting a dedicated flash programmer (output or input) to a serial interface pin (input or output) connected to another device (input), the signal output to the other device may cause the device to malfunction. To avoid this, isolate the connection to the other device or make the setting so that the input signal to the other device is ignored.



16.5.3 $\overline{\text{RESET}}$ pin

When connecting the reset signals of the dedicated flash programmer to the $\overline{\text{RESET}}$ pin, which is connected, to the reset signal generation circuit on-board, a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the reset signal generation circuit.

When the reset signal is input from the user system in flash memory programming mode, the programming operation will not be performed correctly. Therefore, do not input signals other than the reset signals from the dedicated flash programmer.



16.5.4 NMI pin

Do not change the input signal to the NMI pin in flash memory programming mode. If it is changed in flash memory programming mode, programming may not be performed correctly.

16.5.5 MODE0 to MODE2 pins

To shift to the flash memory programming mode, set MODE0 to high-level or low-level input, MODE1 to high-level input, and MODE2 to low-level input, apply the writing voltage (7.8 V) to the V_{PP} pin, and release reset.

16.5.6 Port pins

When the flash memory programming mode is set, all the port pins except the pins which communicate with the dedicated flash programmer become output high-impedance status. Nothing need be done to these port pins. If problems such as disabling output high-impedance status should occur to the external devices connected to the ports, connect them to V_{DD5} or V_{SS5} via resistors.

16.5.7 Other signal pins

Connect X1 and X2 to the same status as in the normal operation mode.

16.5.8 Power supply

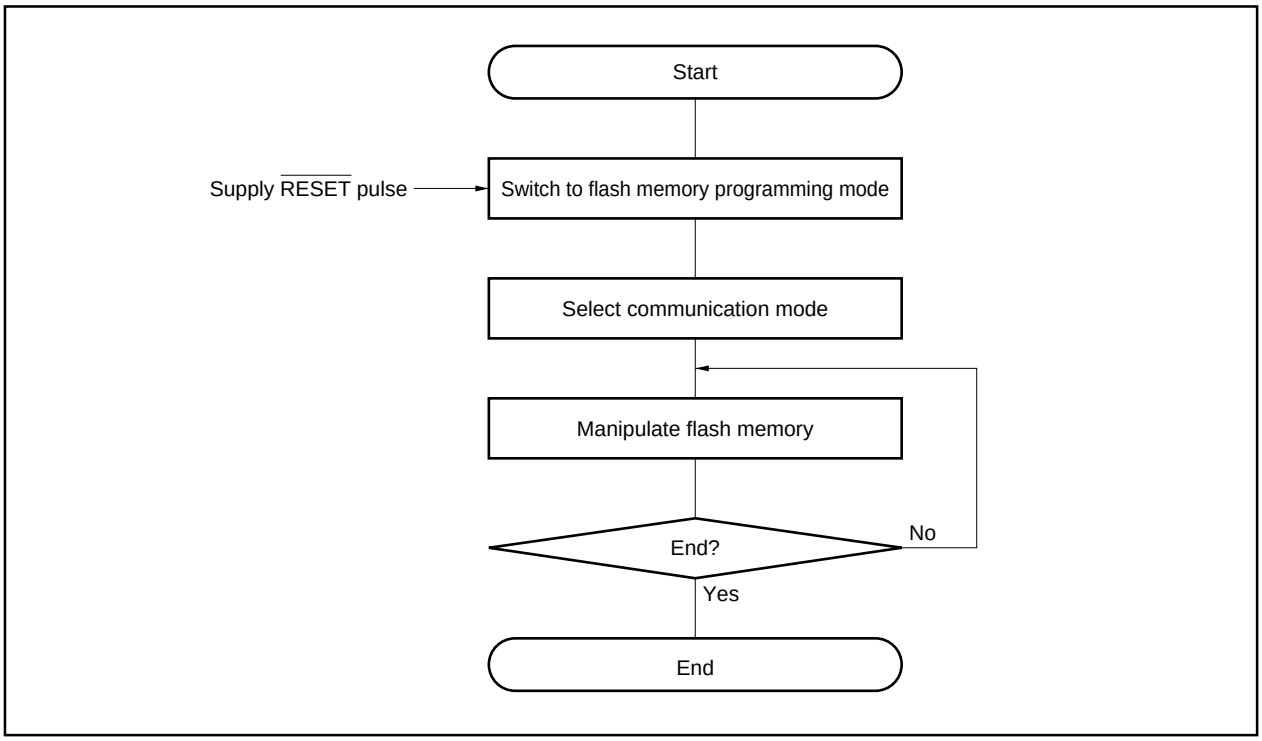
Supply the power supply (V_{DD3}, V_{SS3}, V_{DD5}, V_{SS5}, AV_{DD}, AV_{REF0}, AV_{REF1}, AV_{SS}, CV_{DD}, and CV_{SS}) the same as in normal operation mode. Connect V_{DD}[Note] and GND of the dedicated flash programmer to V_{DD3} , V_{SS3}, V_{DD5}, and V_{SS5}. (V_{DD} of the dedicated flash programmer is provided with a power supply monitoring function.)

Note Connect V_{DD} after converting the power supply to 3 V using a regulator.

16.6 Programming Method

16.6.1 Flash memory control

The following shows the procedure for manipulating the flash memory.

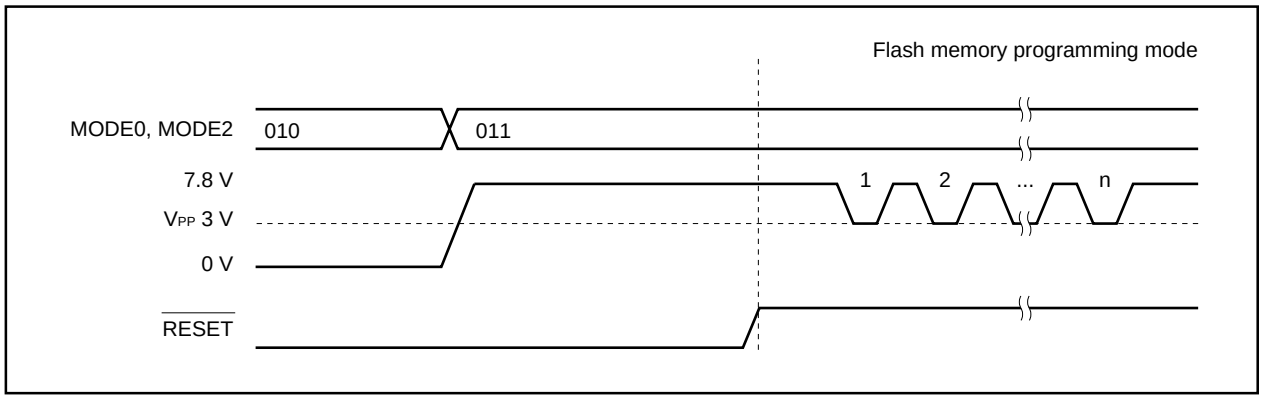


16.6.2 Flash memory programming mode

When rewriting the contents of flash memory using the dedicated flash programmer, set the V850E/MA1 in the flash memory programming mode. To switch to this mode, set the MODE0 to MODE1 and MODE2, V_{PP} pins before canceling reset.

When performing on-board writing, change modes using a jumper, etc.

- MODE0: High-level or low-level input
- MODE1: High-level input
- MODE2: Low-level input
- V_{PP}: 7.8 V



16.6.3 Selection of communication mode

In the V850E/IA1, a communication mode is selected by inputting pulses (16 pulses max.) to V_{PP} pin after switching to the flash memory programming mode. The V_{PP} pulse is generated by the dedicated flash programmer.

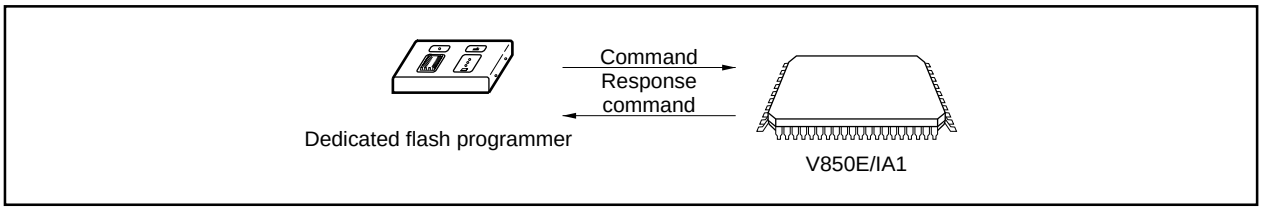
The following shows the relationship between the number of pulses and the communication mode.

Table 16-2. List of Communication Mode

V_{PP} Pulse	Communication Mode	Remarks
0	CSI0	V850E/IA1 performs slave operation, MSB first
3	CSI0 handshake mode	
8	UART0	Communication rate: 9600 bps (after reset), LSB first
Others	RFU (reserved)	Setting prohibited

16.6.4 Communication commands

The V850E/IA1 communicates with the dedicated flash programmer by means of commands. A command sent from the dedicated flash programmer to the V850E/IA1 is called a “command”. The response signal sent from the V850E/IA1 to the dedicated flash programmer is called the “response command”.



The following shows the commands for controlling flash memory of the V850E/IA1. All of these commands are issued from the dedicated flash programmer, and the V850E/IA1 performs the various processing corresponding to the commands.

Category	Command Name	Function
Verify	Batch verify command	Compares the contents of the entire memory and the input data.
	Block verify command	Compares the contents of the specified memory block and the input data.
Erase	Block erase command	Erases the contents of the specified memory block.
	Write back command	Writes back the contents which were erased.
Blank check	Batch blank check command	Checks the erase state of the entire memory.
	Block blank check command	Checks the erase state of the specified memory block.
Data write	High-speed write command	Writes data by the specification of the write address and the number of bytes to be written, and executes verify check.
	Continuous write command	Writes data from the address following the high-speed write command executed immediately before, and executes verify check.
System setting and control	Status read out command	Acquires the status of operations.
	Oscillating frequency setting command	Sets the oscillation frequency.
	Erasing time setting command	Sets the erasing time of batch erase.
	Writing time setting command	Sets the writing time of data write.
	Write back time setting command	Sets the write back time.
	Silicon signature command	Reads outs the silicon signature information.
	Reset command	Escapes from each state.

The V850E/IA1 sends back response commands for the commands issued from the dedicated flash programmer. The following shows the response commands the V850E/IA1 sends out.

Response Command Name	Function
ACK (acknowledge)	Acknowledges command/data, etc.
NAK (not acknowledge)	Acknowledges illegal command/data, etc.

16.7 Flash Memory Programming by Means of Self Writing

The contents of the flash memory in the μPD70F3116 can be rewritten by program.

To perform self writing, a flash memory self programming library[Note], which executes operations such as writing/deleting data to/from on-chip flash memory with an application program described in the C language, is provided.

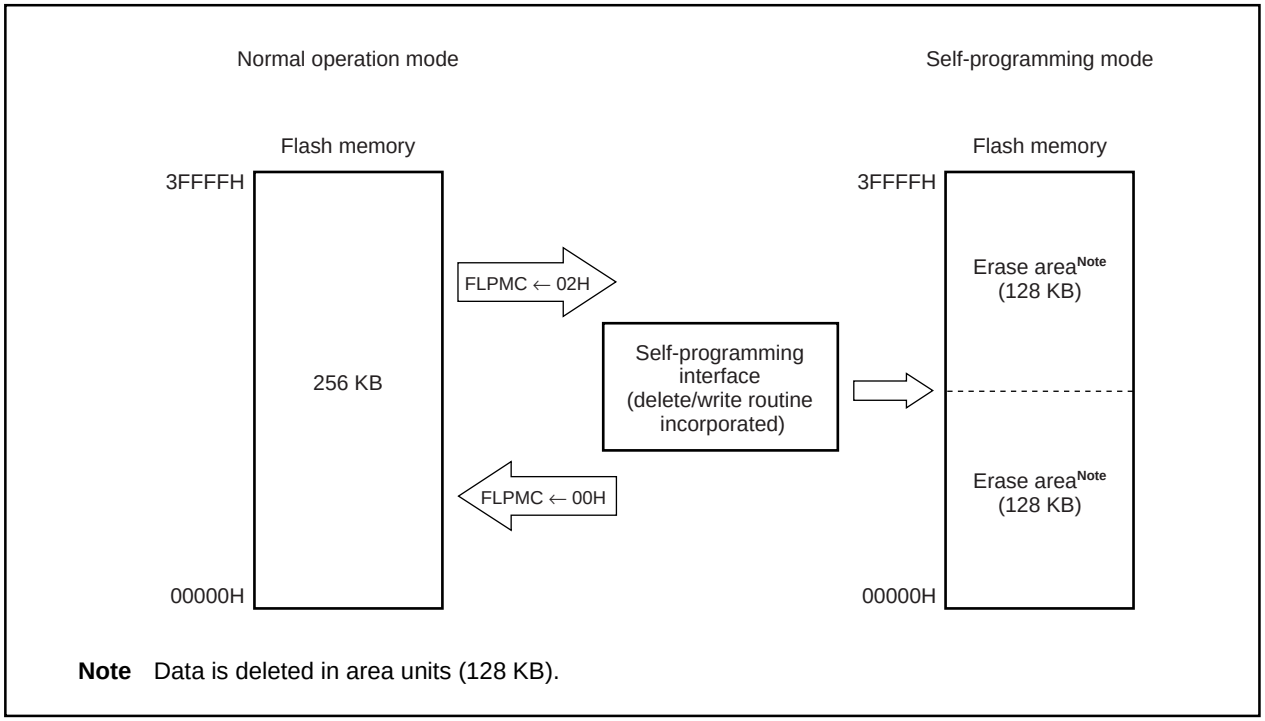
Note Under preparation

Caution Be sure to allocate the routine for self writing to an area other than the CS space and the internal ROM area.

16.7.1 Flash memory configuration

The figure below shows the configuration of flash memory.

Figure 16-1. Configuration of Flash Memory



Note Data is deleted in area units (128 KB).

16.7.2 Flash programming mode control register (FLPMC)

The flash memory mode control register (FLPMC) is a register used to enable/disable writing to flash memory and to specify the self programming mode.

This register can be read/written in 8-bit or 1-bit units (the VPP bit (bit 2) is read-only).

Figure 16-2. Flash Programming Mode Control Register (FLPMC)

	7	6	5	4	3	2	1	0	Address	Initial value[Note]
FLPMC	0	0	0	0	VPPDIS	VPP	FLSPM	0	FFFFF8D4H	08H/0CH

Note 08H: When writing voltage is not applied to the V_{PP} pin
0CH: When writing voltage is applied to the V_{PP} pin

Bit Position	Bit Name	Function
3	VPPDIS	Enables/Disables writing/deleting to/from on-chip flash memory. When this bit is 1, writing/deleting to/from on-chip flash memory is disabled even if high voltage is applied to the V_{PP} pin. 0: Enables writing/deleting to/from flash memory 1: Disables writing/deleting to/from flash memory
2	VPP	Indicates the voltage applied to the V_{PP} pin reaches the writing-enabled level. This bit is used to check whether writing is possible or not in the self-programming mode. 0: Indicates high-voltage application is not detected (the voltage does not reach the writing voltage enable level) 1: Indicates high-voltage appliance is detected (the voltage reaches the writing voltage enable level)
1	FLSPM	Controls switching between internal ROM and the self-programming interface. This bit can switch the mode between the normal mode set by the mode pin on the application system and the self-programming mode. The setting of this bit is valid only if the voltage applied to the V_{PP} pin reaches the writing voltage enable level. 0: Normal mode (for all addresses, instruction fetch is performed from on-chip flash memory) 1: Self-programming mode (accessing the self-programming interface part)

Cautions 1. The VPP bit indicates the status of the voltage applied to the V_{PP} pin. When this bit is 0, it indicates that voltage sufficient for writing/deleting has not been applied. Therefore, be sure to configure the hardware in which the voltage required for writing /deleting is always applied to the V_{PP} pin.

2. Do not change the initial value of bits 0 and 4 to 7.

Setting data to the flash programming mode control register (FLPMC) is performed in the following sequence.

<1> Disable interrupts (set the NP bit of the PSW to 1)
<2> Prepare the data to be set in the specific register in a general-purpose register
<3> Write data to the peripheral command register (PHCMD)
<4> Set the flash memory programming mode control register (FLPMC) by executing the following instructions
- Store instruction (ST/SST instructions)
- Bit manipulation instruction (SET1/CLR1/NOT1 instructions)

<5> Insert NOP instructions (5 instructions <5> to <9>)
<10> Cancel the interrupt disabled state (reset the NP bit of the PSW to 0)

[Description example]

```
<1>  LDSR  rX, 5
<2>  MOV  0x04, r10
<3>  ST.B  r10, PHCMD [r0]
<4>  ST.B  r10, FLPMC [r0]
<5>  NOP
<6>  NOP
<7>  NOP
<8>  NOP
<9>  NOP
<10> LDSR  rY, 5
```

Remark rX: Value written to the PSW
rY: Value returned to the PSW

No special sequence is required for reading a specific register.

Cautions 1. If an interrupt is acknowledged between when PHCMD is issued (<3>) and writing to a specific register (the following operation <4>), writing to the specific register may not be performed and a protection error may occur (the PRERR bit of the PHS register = 1). Therefore, set the NP bit of the PSW to 1 (<1>) to disable interrupt acknowledgment. Similarly, disable acknowledgement of interrupts when a bit manipulation instruction is used to set a specific register.

2. Use the same general-purpose register used to set a specific register (<3>) for writing to the PHCMD register (<4>) even though the data written to the PHCMD register is dummy data. This is the same as when a general-purpose register is used for addressing.

3. Do not use DMA transfer for writing to the PHCMD register and a specific register.

16.7.3 Self-programming function

The V850E/IA1 provides self-programming functions, as shown below. By combining these functions, deleting/writing flash memory becomes possible.

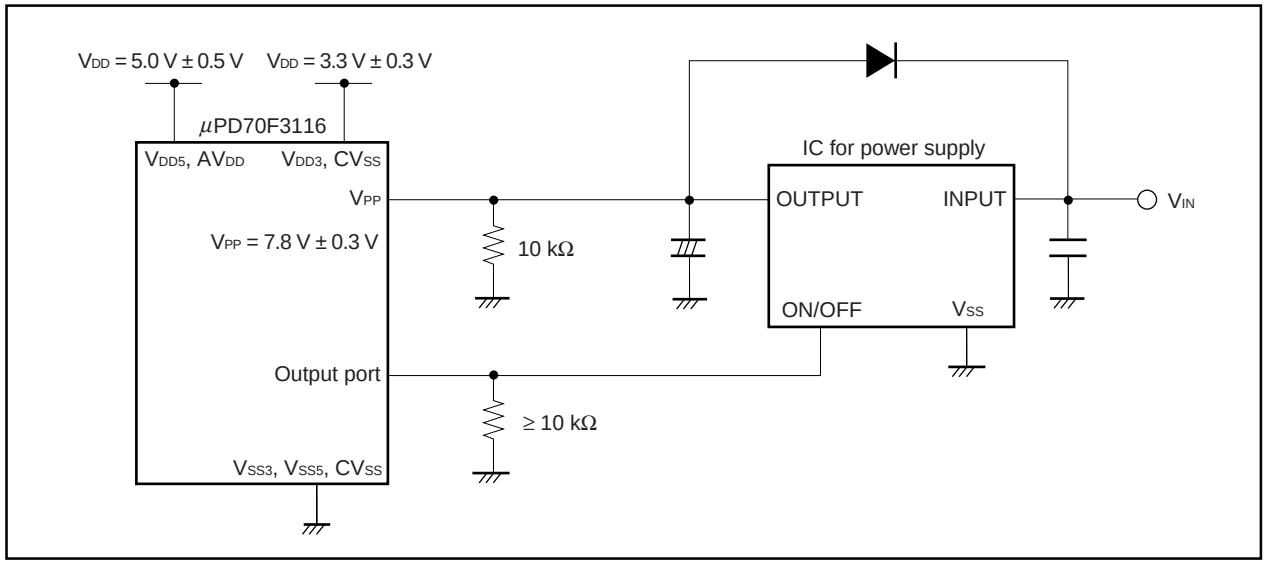
Table 16-3. Function List

Type	Function Name	Function
Erase	Area erase	Erases the specified area.
Write	Continuous write in word units	Continuously writes the specified memory contents from the specified flash memory address, for the number of words specified in 4-byte units.
	Prewrite	Writes 0 to flash memory before erasure.
Check	Erase verify	Checks whether an over erase occurred after erasure.
	Erase byte verify	Checks whether erasure is complete.
	Internal verify	Checks whether the signal level of the post-write data in flash memory is appropriate.
Write back	Area write back	Writes back the flash memory area in which an over erase occurred.
Acquire information	Flash memory information read	Reads out information about flash memory.

16.7.4 Configuration of self-writing circuit

An example of a self-writing circuit configuration is shown below.

Figure 16-3. Example of Self-Writing Circuit Configuration



16.7.5 How to distinguish flash memory and mask ROM versions

It is possible to distinguish a flash memory version (μPD70F3116) and a mask ROM version (μPD703117) by means of software, using the methods shown below.

<1> Disable an interrupt (set the NP bit of PSW to 1).
<2> Write arbitrary data to the peripheral command register (PHCMD).
<3> Set the VPPDIS bit of the flash programming mode control register (FLPMC) to 1.
<4> Insert NOP instructions (5 instructions (<4> to <8>)).
<9> Cancel the interrupt disabled state (reset the NP bit of the PSW to 0).
<10> Read the VPPDIS bit of the flash programming mode control register (FLPMC).
If the value read is 0: Mask ROM version (μPD703117)
If the value read is 1: Flash memory version (μPD70F3116)

[Description example]

```
<1>  LDSR  rX, 5
<2>  ST.B  r10, PHCMD [r0]
<3>  SET1  4, FLPMC [r0]
<4>  NOP
<5>  NOP
<6>  NOP
<7>  NOP
<8>  NOP
<9>  LDSR  rY, 5
<10> TST1  4, FLPMC [r0]
     BNZ        <start address of self-programming routine>
     BR         <routine when writing is not performed>
```

Remark rX: Value written to the PSW
rY: Value returned to the PSW

Cautions 1. If an interrupt is acknowledged between when PHCMD is issued (<2>) and writing to a specific register (the following operation <3>), writing to a specific register may not be performed and a protection error may occur (the PRERR bit of the PHS register = 1). Therefore, set the NP bit of the PSW to 1 (<1>) to disable interrupt acknowledgment. Similarly, disable acknowledgement of interrupts when a bit manipulation instruction is used to set a specific register.

2. When a store instruction is used for setting a specific register, be sure to use the same general-purpose register used to set the specific register for writing to the PHCMD register even though the data written to the PHCMD register is dummy data. This is the same as when a general-purpose register is used for addressing.

3. Do not use DMA transfer for writing to the PHCMD register and a specific register.

[MEMO]

APPENDIX A REGISTER INDEX

(1/10)

Symbol	Register Name	Unit	Page
ADCR00	A/D conversion result register 00	ADC	654
ADCR01	A/D conversion result register 01	ADC	654
ADCR02	A/D conversion result register 01	ADC	654
ADCR03	A/D conversion result register 01	ADC	654
ADCR04	A/D conversion result register 01	ADC	654
ADCR05	A/D conversion result register 01	ADC	654
ADCR06	A/D conversion result register 01	ADC	654
ADCR07	A/D conversion result register 01	ADC	654
ADCR10	A/D conversion result register 01	ADC	654
ADCR11	A/D conversion result register 01	ADC	654
ADCR12	A/D conversion result register 01	ADC	654
ADCR13	A/D conversion result register 01	ADC	654
ADCR14	A/D conversion result register 01	ADC	654
ADCR15	A/D conversion result register 01	ADC	654
ADCR16	A/D conversion result register 01	ADC	654
ADCR17	A/D conversion result register 01	ADC	654
ADETM0	A/D voltage detection mode register 0	ADC	653
ADETM1	A/D voltage detection mode register 1	ADC	653
ADIC0	Interrupt control register	INTC	184
ADIC1	Interrupt control register	INTC	184
ADSCM00	A/D scan mode register 00	ADC	650
ADSCM01	A/D scan mode register 01	ADC	655
ADSCM10	A/D scan mode register 10	ADC	650
ADSCM11	A/D scan mode register 11	ADC	652
ASIF0	Asynchronous serial interface mode transmission status register 0	UART0	423
ASIM0	Asynchronous serial interface mode register 0	UART0	419
ASIM10	Asynchronous serial interface mode register 10	UART1	449
ASIM11	Asynchronous serial interface mode register 11	UART1	451
ASIM20	Asynchronous serial interface mode register 20	UART2	449
ASIM21	Asynchronous serial interface mode register 21	UART2	451
ASIS0	Asynchronous serial interface status register 0	UART0	422
ASIS1	Asynchronous serial interface status register 1	UART1	452
ASIS2	Asynchronous serial interface status register 2	UART2	452
AWC	Address wait control register	BCU	132
BCC	Bus cycle control register	BCU	134

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Symbol	Register Name	Unit	Page
BCT0	Bus cycle type configuration register 0	BCU	121
BCT1	Bus cycle type configuration register 1	BCU	121
BFCM00	Buffer register CM00	RPU	238
BFCM01	Buffer register CM01	RPU	238
BFCM02	Buffer register CM02	RPU	238
BFCM03	Buffer register CM03	RPU	239
BFCM10	Buffer register CM10	RPU	238
BFCM11	Buffer register CM11	RPU	238
BFCM12	Buffer register CM12	RPU	238
BFCM13	Buffer register CM13	RPU	239
BPC	Peripheral area selection control register	CPU	96
BRGC0	Baud rate generator control register 0	UART0	439
BSC	Bus size configuration register	BCU	123
C1BA	CAN1 bus active register	FCAN	590
C1BRP	CAN1 bit rate prescaler register	FCAN	591
C1CTRL	CAN1 control register	FCAN	577
C1DEF	CAN1 definition register	FCAN	581
C1DINF	CAN1 bus diagnostic information register	FCAN	594
C1ERC	CAN1 error counter register	FCAN	586
C1IE	CAN1 interrupt enable register	FCAN	587
C1INTP	CAN1 local interrupt pending register	FCAN	565
C1LAST	CAN1 information register	FCAN	585
C1MASKH0	CAN1 address mask register H0	FCAN	575
C1MASKH1	CAN1 address mask register H1	FCAN	575
C1MASKH2	CAN1 address mask register H2	FCAN	575
C1MASKH3	CAN1 address mask register H3	FCAN	575
C1MASKL0	CAN1 address mask register L0	FCAN	575
C1MASKL1	CAN1 address mask register L1	FCAN	575
C1MASKL2	CAN1 address mask register L2	FCAN	575
C1MASKL3	CAN1 address mask register L3	FCAN	575
C1SYNC	CAN1 synchronization control register	FCAN	595
CANIC0	Interrupt control register	INTC	184
CANIC1	Interrupt control register	INTC	184
CANIC2	Interrupt control register	INTC	184
CANIC3	Interrupt control register	INTC	184
CC100	Capture/compare register 100	RPU	304
CC101	Capture/compare register 101	RPU	305
CC10IC0	Interrupt control register	INTC	184
CC10IC1	Interrupt control register	INTC	184
CC110	Capture/compare register 110	RPU	304

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Symbol	Register Name	Unit	Page
CC111	Capture/compare register 111	RPU	305
CC11IC0	Interrupt control register	INTC	184
CC11IC1	Interrupt control register	INTC	184
CC2IC0	Interrupt control register	INTC	184
CC2IC1	Interrupt control register	INTC	184
CC2IC2	Interrupt control register	INTC	184
CC2IC3	Interrupt control register	INTC	184
CC2IC4	Interrupt control register	INTC	184
CC2IC5	Interrupt control register	INTC	184
CC30	Capture/compare register 30	RPU	381
CC31	Capture/compare register 31	RPU	381
CC3IC0	Interrupt control register	INTC	184
CC3IC1	Interrupt control register	INTC	184
CCINTP	CAN interrupt pending register	FCAN	563
CCR0	Capture/compare control register 0	RPU	311
CCR1	Capture/compare control register 1	RPU	311
CCSTATE0	Timer 2 capture/compare 1 to 4 status register	RPU	356
CGCS	CAN main clock selection register	FCAN	570
CGIE	CAN global interrupt enable register	FCAN	569
CGINTP	CAN global interrupt pending register	FCAN	564
CGMSR	CAN message search result register	FCAN	573
CGMSS	CAN message search start register	FCAN	573
CGST	CAN global status register	FCAN	567
CGTSC	CAN time stamp count register	FCAN	572
CKC	Clock control register	CG	212
CKSR0	Clock selection register 0	UART0	438
CM000	Compare register 000	RPU	236
CM001	Compare register 001	RPU	236
CM002	Compare register 002	RPU	236
CM003	Compare register 003	RPU	237
CM010	Compare register 010	RPU	236
CM011	Compare register 011	RPU	236
CM012	Compare register 012	RPU	236
CM013	Compare register 013	RPU	237
CM03IC0	Interrupt control register	INTC	184
CM03IC1	Interrupt control register	INTC	184
CM100	Compare register 100	RPU	302
CM101	Compare register 101	RPU	303
CM10IC0	Interrupt control register	INTC	184
CM10IC1	Interrupt control register	INTC	184

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Symbol	Register Name	Unit	Page
CM110	Compare register 110	RPU	302
CM111	Compare register 111	RPU	303
CM11IC0	Interrupt control register	INTC	184
CM11IC1	Interrupt control register	INTC	184
CM4	Compare register 4	RPU	406
CM4IC0	Interrupt control register	INTC	184
CMSE050	Timer 2 sub-channel 0, 5 capture/compare control register	RPU	350
CMSE120	Timer 2 sub-channel 1, 2 capture/compare control register	RPU	351
CMSE340	Timer 2 sub-channel 3, 4 capture/compare control register	RPU	353
CSC0	Chip area selection control register 0	BCU	117
CSC1	Chip area selection control register 1	BCU	117
CSCE0	Timer 2 software event capture register	RPU	358
CSE0	Timer 2 count clock/control edge selection register	RPU	344
CSIC0	Clocked serial interface clock selection register 0	CSI0	484
CSIC1	Clocked serial interface clock selection register 1	CSI1	484
CSIIC0	Interrupt control register	INTC	184
CSIIC1	Interrupt control register	INTC	184
CSIM0	Clocked serial interface mode register 0	CSI0	482
CSIM1	Clocked serial interface mode register 1	CSI1	482
CSL10	CC101 capture input selection register	RPU	317
CSL11	CC111 capture input selection register	RPU	317
CSTOP	CAN stop register	FCAN	566
CVPE10	Timer 2 sub-channel 1 main capture/compare register	RPU	340
CVPE20	Timer 2 sub-channel 2 main capture/compare register	RPU	340
CVPE30	Timer 2 sub-channel 3 main capture/compare register	RPU	340
CVPE40	Timer 2 sub-channel 4 main capture/compare register	RPU	340
CVSE00	Timer 2 sub-channel 0 capture/compare register	RPU	339
CVSE10	Timer 2 sub-channel 1 sub capture/compare register	RPU	341
CVSE20	Timer 2 sub-channel 2 sub capture/compare register	RPU	341
CVSE30	Timer 2 sub-channel 3 sub capture/compare register	RPU	341
CVSE40	Timer 2 sub-channel 4 sub capture/compare register	RPU	341
CVSE50	Timer 2 sub-channel 5 capture/compare register	RPU	341
DADC0	DMA addressing control register 0	DMAC	154
DADC1	DMA addressing control register 1	DMAC	154
DADC2	DMA addressing control register 2	DMAC	154
DADC3	DMA addressing control register 3	DMAC	154
DBC0	DMA transfer count register 0	DMAC	153
DBC1	DMA transfer count register 1	DMAC	153
DBC2	DMA transfer count register 2	DMAC	153
DBC3	DMA transfer count register 3	DMAC	153

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Symbol	Register Name	Unit	Page
DCHC0	DMA channel control register 0	DMAC	156
DCHC1	DMA channel control register 1	DMAC	156
DCHC2	DMA channel control register 2	DMAC	156
DCHC3	DMA channel control register 3	DMAC	156
DDA0H	DMA destination address register 0H	DMAC	151
DDA0L	DMA destination address register 0L	DMAC	152
DDA1H	DMA destination address register 1H	DMAC	151
DDA1L	DMA destination address register 1L	DMAC	152
DDA2H	DMA destination address register 2H	DMAC	151
DDA2L	DMA destination address register 2L	DMAC	152
DDA3H	DMA destination address register 3H	DMAC	151
DDA3L	DMA destination address register 3L	DMAC	152
DDIS	DMA disable status register	DMAC	157
DETIC0	Interrupt control register	INTC	184
DETIC1	Interrupt control register	INTC	184
DMAIC0	Interrupt control register	INTC	184
DMAIC1	Interrupt control register	INTC	184
DMAIC2	Interrupt control register	INTC	184
DMAIC3	Interrupt control register	INTC	184
DRST	DMA restart register	DMAC	157
DSA0H	DMA source address register 0H	DMAC	149
DSA0L	DMA source address register 0L	DMAC	150
DSA1H	DMA source address register 1H	DMAC	149
DSA1L	DMA source address register 1L	DMAC	150
DSA2H	DMA source address register 2H	DMAC	149
DSA2L	DMA source address register 2L	DMAC	150
DSA3H	DMA source address register 3H	DMAC	149
DSA3L	DMA source address register 3L	DMAC	150
DTFR0	DMA trigger factor register 0	DMAC	158
DTFR1	DMA trigger factor register 1	DMAC	158
DTFR2	DMA trigger factor register 2	DMAC	158
DTFR3	DMA trigger factor register 3	DMAC	158
DTM00	Dead time timer 00	RPU	236
DTM01	Dead time timer 01	RPU	236
DTM02	Dead time timer 02	RPU	236
DTM10	Dead time timer 10	RPU	236
DTM11	Dead time timer 11	RPU	236
DTM12	Dead time timer 12	RPU	236
DTRR0	Dead time timer reload register 0	RPU	236
DTRR1	Dead time timer reload register 1	RPU	236

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Symbol	Register Name	Unit	Page
DWC0	Data wait control register 0	BCU	130
DWC1	Data wait control register 1	BCU	130
FEM0	Timer 2 input filter mode register 0	RPU	194, 727
FEM1	Timer 2 input filter mode register 1	RPU	194, 727
FEM2	Timer 2 input filter mode register 2	RPU	194, 727
FEM3	Timer 2 input filter mode register 3	RPU	194, 727
FEM4	Timer 2 input filter mode register 4	RPU	194, 727
FEM5	Timer 2 input filter mode register 5	RPU	194, 727
FLPMC	Flash programming mode control register	CPU	748
IMR0	Interrupt mask register 0	INTC	187
IMR1	Interrupt mask register 1	INTC	187
IMR2	Interrupt mask register 2	INTC	187
IMR3	Interrupt mask register 3	INTC	187
INTM0	External interrupt mode register 0	INTC	176
INTM1	External interrupt mode register 1	INTC	190
INTM2	External interrupt mode register 2	INTC	190
ISL_RAMH	RAM address alternate register H	NBD	639
ISL_RAML	RAM address alternate register L	NBD	638
ISL_ROMH	RAM address alternate register H	NBD	639
ISL_ROML	RAM address alternate register L	NBD	639
ISPR	In-service priority register	INTC	188
ITRG0	/D internal trigger selection register	ADC	656
LOCK	Lock register	CPU	215
M_CONF00 to M_CONF31	CAN message configuration registers 00 to 31	FCAN	557
M_CTRL00 to M_CTRL31	CAN message control registers 00 to 31	FCAN	549
M_DATAn0 to M_DATAn7	CAN message data registers n0 to n7 (n = 00 to 31)	FCAN	553
M_DLC00 to M_DLC31	CAN message data length registers 00 to 31	FCAN	547
M_IDH00 to M_IDH31	CAN message ID registers H00 to H31	FCAN	555
M_IDL00 to M_IDL31	CAN message ID registers L00 to L31	FCAN	555
M_STAT00 to M_STAT31	CAN message status registers 00 to 31	FCAN	559
M_TIME00 to M_TIME31	CAN message time stamp registers 00 to 31	FCAN	552
NBDH	Data buffer H for RAM access	NBD	636
NBDHU	Data buffer HU for RAM access	NBD	636

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Symbol	Register Name	Unit	Page
NBDL	Data buffer L for RAM access	NBD	635
NBDLU	Data buffer LU for RAM access	NBD	635
NBDMDH	DMA destination address setting register DH	NBD	638
NBDMDL	DMA destination address setting register DL	NBD	638
NBDMSH	DMA source address setting register SH	NBD	637
NBDMSL	DMA source address setting register SL	NBD	637
NRC10	Timer 10 noise elimination time selection register	RPU	724
NRC11	Timer 11 noise elimination time selection register	RPU	724
NRC3	Timer 3 noise elimination time selection register	RPU	725
OCTLE0	Timer 2 output control register	RPU	349
ODELE0	Timer 2 output delay register	RPU	357
P0	Port 0	Port	695
P0IC0	Interrupt control register	INTC	184
P0IC1	Interrupt control register	INTC	184
P0IC2	Interrupt control register	INTC	184
P0IC3	Interrupt control register	INTC	184
P0IC4	Interrupt control register	INTC	184
P0IC5	Interrupt control register	INTC	184
P0IC6	Interrupt control register	INTC	184
P1	Port 1	Port	696
P2	Port 2	Port	700
P3	Port 3	Port	703
P4	Port 4	Port	706
PCM	Port CM	Port	718
PCS	Port CS	Port	713
PCT	Port CT	Port	715
PDH	Port DH	Port	709
PDL	Port DL	Port	711
PFC1	Port 1 function control register	Port	699
PFC2	Port 2 function control register	Port	702
PHCMD	Peripheral command register	CPU	211
PHS	Peripheral status register	CPU	214
PM1	Port 1 mode register	Port	697
PM2	Port 2 mode register	Port	701
PM3	Port 3 mode register	Port	704
PM4	Port 4 mode register	Port	707
PMC1	Port 1 mode control register	Port	698
PMC2	Port 2 mode control register	Port	701
PMC3	Port 3 mode control register	Port	705
PMC4	Port 4 mode control register	Port	708

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Symbol	Register Name	Unit	Page
PMCCM	Port CM mode control register	Port	720
PMCCS	Port CS mode control register	Port	714
PMCCT	Port CT mode control register	Port	717
PMCDH	Port DH mode control register	Port	710
PMCDL	Port DL mode control register	Port	712
PMCM	Port CM mode register	Port	719
PMCS	Port CS mode register	Port	714
PMCT	Port CT mode register	Port	716
PMDH	Port DH mode register	Port	709
PMDL	Port DL mode register	Port	712
POER0	PWM output enable register 0	RPU	251
POER1	PWM output enable register 1	RPU	251
PRCMD	Command register	CPU	219
PRM01	Timer 0n clock selection register	RPU	240
PRM02	Timer 1n/ Timer 2n clock selection register	RPU	306, 342
PRM03	Timer 3 clock selection register	RPU	383
PRM04	FCAN clock selection register	FCAN	546
PRM10	Prescaler mode register 10	RPU	314
PRM11	Prescaler mode register 11	RPU	314
PRSCM1	Prescaler compare register 1	UART1	474
PRSCM2	Prescaler compare register 2	UART2	474
PRSCM3	Prescaler compare register 3	CSI0, CSI1	515
PRSM1	Prescaler mode register 1	UART1	473
PRSM2	Prescaler mode register 2	UART2	473
PRSM3	Prescaler mode register 3	CSI0, CSI1	514
PSC	Power save control register	CPU	220
PSMR	Power save mode register	CPU	219
PSTO0	PWM software timing output register 0	RPU	252
PSTO1	PWM software timing output register 1	RPU	252
RXB0	Reception buffer register	UART0	424
RXB1	2-frame continuous reception buffer registers 1	UART1	453
RXB2	2-frame continuous reception buffer registers 2	UART2	453
RXBL1	Reception buffer register L1	UART1	453
RXBL2	Reception buffer register L2	UART2	453
SC_STAT00 to SC_STAT31	CAN status set/clear registers 00 to 31	FCAN	561
SEIC0	Interrupt control register	INTC	184
SESA10	Signal edge selection register 10	INTC, RPU	191, 312
SESA11	Signal edge selection register 11	INTC, RPU	191, 312
SESC	Valid edge selection register	INTC, RPU	193, 388

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Symbol	Register Name	Unit	Page
SESE0	Timer 2 sub-channel input event edge selection register	RPU	345
SIO0	Serial I/O shift register 0	CSI0	494
SIO1	Serial I/O shift register 1	CSI1	494
SIOL0	Serial I/O shift register L0	CSI0	495
SIOL1	Serial I/O shift register L1	CSI1	495
SIRB0	Clocked serial interface reception buffer register 0	CSI0	486
SIRB1	Clocked serial interface reception buffer register 1	CSI1	486
SIRBE0	Clocked serial interface read-only reception buffer register 0	CSI0	488
SIRBE1	Clocked serial interface read-only reception buffer register 1	CSI1	488
SIRBEL0	Clocked serial interface read-only reception buffer register L0	CSI0	489
SIRBEL1	Clocked serial interface read-only reception buffer register L1	CSI1	489
SIRBL0	Clocked serial interface reception buffer register L0	CSI0	487
SIRBL1	Clocked serial interface reception buffer register L1	CSI1	487
SOTB0	Clocked serial interface transmission buffer register 0	CSI0	490
SOTB1	Clocked serial interface transmission buffer register 1	CSI1	490
SOTBF0	Clocked serial interface initial transmission buffer register 0	CSI0	492
SOTBF1	Clocked serial interface initial transmission buffer register 1	CSI1	492
SOTBFL0	Clocked serial interface initial transmission buffer register L0	CSI0	493
SOTBFL1	Clocked serial interface initial transmission buffer register L1	CSI1	493
SOTBL0	Clocked serial interface initial transmission buffer register L0	CSI0	491
SOTBL1	Clocked serial interface initial transmission buffer register L1	CSI1	491
SPEC0	TOMR write enable register 0	RPU	253
SPEC1	TOMR write enable register 1	RPU	253
SRIC0	Interrupt control register	INTC	184
SRIC1	Interrupt control register	INTC	184
SRIC2	Interrupt control register	INTC	184
STATUS0	Status register 0	RPU	316
STATUS1	Status register 1	RPU	316
STIC0	Interrupt control register	INTC	184
STIC1	Interrupt control register	INTC	184
STIC2	Interrupt control register	INTC	184
STOPTE0	Timer 2 clock stop register	RPU	343
TBSTATE0	Timer 2 timer base status register	RPU	355
TCRE0	Timer 2 time base control register	RPU	346
TM00	Timer 00	RPU	235
TM01	Timer 01	RPU	235
TM0IC0	Interrupt control register	INTC	184
TM0IC1	Interrupt control register	INTC	184
TM10	Timer 10	RPU	300
TM11	Timer 11	RPU	300

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Symbol	Register Name	Unit	Page
TM20	Timer 20	RPU	339
TM21	Timer 21	RPU	339
TM2IC0	Interrupt control register	INTC	184
TM2IC1	Interrupt control register	INTC	184
TM3	Timer 3	RPU	379
TM3IC0	Interrupt control register	INTC	184
TM4	Timer 4	RPU	405
TMC00	Timer control register 00	RPU	241
TMC01	Timer control register 01	RPU	241
TMC10	Timer control register 10	RPU	309
TMC11	Timer control register 11	RPU	309
TMC30	Timer control register 30	RPU	384
TMC31	Timer control register 31	RPU	386
TMC4	Timer control register 4	RPU	408
TMIC0	Timer connection selection register 0	RPU	413
TOMR0	Timer output mode register 0	RPU	248
TOMR1	Timer output mode register 1	RPU	248
TUC00	Timer unit control register 00	RPU	247
TUC01	Timer unit control register 01	RPU	247
TUM0	Timer unit mode register 0	RPU	307
TUM1	Timer unit mode register 1	RPU	307
TXB0	Transmission buffer register 00	UART0	425
TXS1	2-frame continuous transmission shift register 1	UART1	456
TXS2	2-frame continuous transmission shift register 2	UART2	456
TXSL1	Transmission shift register L1	UART1	456
TXSL2	Transmission shift register L2	UART2	456
VSWC	System wait control register	BCU	112

APPENDIX B INSTRUCTION SET LIST

B.1 Functions

(1) Symbols used in operand descriptions

Symbol	Explanation
reg1	General-purpose register (Used as source register)
reg2	General-purpose register (Usually used as destination register. Used as source register in some instructions.)
reg3	General-purpose register (Usually stores remainder of division result or higher 32 bits of multiplication result.)
bit#3	3-bit data for bit number specification
immX	X-bit immediate data
dispX	X-bit displacement data
regID	System register number
vector	5-bit data that specifies a trap vector (00H to 1FH)
cccc	4-bit data that shows a condition code
sp	Stack pointer (r3)
ep	Element pointer (r30)
list×	X-item register list

(2) Symbols used in operands

Symbol	Explanation
R	1 bit of data of code that specifies reg1 or regID
r	1 bit of data of code that specifies reg2
w	1 bit of data of code that specifies reg3
d	1 bit of data of a displacement
I	1 bit of immediate data (Shows higher bit of immediate data)
i	1 bit of immediate data
cccc	4-bit data that shows a condition code
CCCC	4-bit data that shows condition code of Bcond instruction
bbb	3-bit data for bit number specification
L	1 bit of data that specifies a program register in a register list
S	1 bit of data that specifies a system register in a register list

(3) Symbols used in operations

Symbol	Explanation
←	Assignment
GR [ ]	General-purpose register
SR [ ]	System register
zero-extend (n)	Zero-extend n to word length.
sign-extend (n)	Sign-extend n to word length.
load-memory (a, b)	Read data of size “b” from address “a”.
store-memory (a, b, c)	Write data “b” of size “c” to address “a”.
load-memory-bit (a, b)	Read bit “b” of address “a”.
store-memory-bit (a, b, c)	Write “c” in bit “b” of address “a”.
saturated (n)	Perform saturation processing of n (n is 2’s complement). If n is a computation result and n > 7FFFFFFFH, make n = 7FFFFFFFH. If n is a computation result and n < 80000000H, make n = 80000000H.
result	Reflect result in flag.
Byte	Byte (8 bits)
Half-word	Halfword (16 bits)
Word	Word (32 bits)
+	Addition
–	Subtraction
||	Bit concatenation
×	Multiplication
÷	Division
%	Remainder of division result
AND	Logical product
OR	Logical sum
XOR	Exclusive logical sum
NOT	Logical negation
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

(4) Symbols used in execution clock

Symbol	Explanation
i	When executing another instruction immediately after instruction execution (issue).
r	When repeating same instruction immediately after instruction execution (repeat)
|	When using instruction execution result in instruction immediately after instruction execution (latency)

(5) Symbols used in flag operations

Symbol	Explanation
(Blank)	No change
0	Clear to 0.
×	Set or cleared according to result.
R	Previously saved value is restored.

(6) Condition codes

Condition Name (cond)	Condition Code (CCCC)	Condition Expression	Explanation
V	0000	OV = 1	Overflow
NV	1000	OV = 0	No overflow
C/L	0001	CY = 1	Carry Lower (Less than)
NC/NL	1001	CY = 0	No carry No lower (Greater than or equal)
Z/E	0010	Z = 1	Zero Equal
NZ/NE	1010	Z = 0	Not zero Not equal
NH	0011	(CY or Z) = 1	Not higher (Less than equal)
H	1011	(CY or Z) = 0	Higher (Greater than)
N	0100	S = 1	Negative
P	1100	S = 0	Positive
T	0101	–	Always (Unconditional)
SA	1101	SAT = 1	Saturated
LT	0110	(S xor OV) = 1	Less then signed
GE	1110	(S xor OV) = 0	Greater than or equal signed
LE	0111	((S xor OV) or Z) = 1	Less than or equal signed
GT	1111	((S xor OV) or Z) = 0	Greater than signed

B.2 Instruction Set (Alphabetical Order)

Mnemonic	Operands	Opcode	Operation		Execution Clock			Flags				
					i	r	I	CY	OV	S	Z	SAT
ADD	reg1, reg2	r r r r r 0 0 1 1 1 0 R R R R R	GR[reg2] ← GR[reg2] + GR[reg1]		1	1	1	×	×	×	×	
	imm5, reg2	r r r r r 0 1 0 0 1 0 i i i i i	GR[reg2] ← GR[reg2] + sign-extend (imm5)		1	1	1	×	×	×	×	
ADDI	imm16, reg1, reg2	r r r r r 1 1 0 0 0 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + sign-extend (imm16)		1	1	1	×	×	×	×	
AND	reg1, reg2	r r r r r 0 0 1 0 1 0 R R R R R	GR[reg2] ← GR[reg2] AND GR[reg1]		1	1	1		0	×	×	
ANDI	imm16, reg1, reg2	r r r r r 1 1 0 1 1 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] AND zero-extend (imm 16)		1	1	1		0	0	×	
Bcond	disp9	d d d d d 1 0 1 1 d d d c c c c **Note 1**	if conditions are satisfied then PC ← PC + sign extend (disp9)	Conditions satisfied	**2** Note 2	**2** Note 2	**2** Note 2					
				Conditions not satisfied	1	1	1					
BSH	reg2, reg3	r r r r r 1 1 1 1 1 1 0 0 0 0 0 w w w w w 0 1 1 0 1 0 0 0 0 1 0	GR[reg3] ← GR[reg2] (23:16) || GR[reg2] (31:24)||GR[reg2] (7:0)||GR[reg2] (15:8)		1	1	1	×	0	×	×	
BSW	reg2, reg3	r r r r r 1 1 1 1 1 1 0 0 0 0 0 w w w w w 0 1 1 0 1 0 0 0 0 0 0	GR[reg3] ← GR[reg2] (7:0) || GR[reg2] (15:8)||GR[reg2] (23:16)||GR[reg2] (31:24)		1	1	1	×	0	×	×	
CALLT	imm6	0 0 0 0 0 0 1 0 0 0 i i i i i i	CTPC ← PC + 2 (return PC) CTPSW ← PSW adr ← CTBP + zero-extend (imm6 logically shift left by 1) PC ← CTBP + zero-extend (Load-memory (adr, Halfword)		4	4	4					
CLR1	bit#3, disp16[reg1]	1 0 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp 16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, 0)		**3** Note 3	**3** Note 3	**3** Note 3				×	
	reg2, [reg1]	1 0 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] Z flag ← Not (Load-memory-bit (adr, reg2)) Store-memory-bit (adr, reg2, 0)		**3** Note 3	**3** Note 3	**3** Note 3				×	
CMOV	cccc, imm5, reg2, reg3	r r r r r 1 1 1 1 1 1 i i i i i w w w w w 0 1 1 0 0 0 c c c c 0	if conditions are satisfied then GR[reg3] ← sign-extend (imm5) else GR[reg3] ← GR[reg2]		1	1	1					
	cccc, reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 1 0 0 1 c c c c 0	if conditions are satisfied then GR[reg3] ← GR[reg1] else GR[reg3] ← GR[reg2]		1	1	1					
CMP	reg1, reg2	r r r r r 0 0 1 1 1 1 R R R R R	result ← GR[reg2] – GR[reg1]		1	1	1	×	×	×	×	
	imm5, reg2	r r r r r 0 1 0 0 1 1 i i i i i	result ← GR[reg2] – sign-extend (imm5)		1	1	1	×	×	×	×	
CTRET		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 1 0 0	PC ← CTPC PSW ← CTPSW		3	3	3	R	R	R	R	R
DBRET		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 1 1 0	PC ← DBPC PSW ← DBPSW		3	3	3	R	R	R	R	R
DBTRAP		1 1 1 1 1 0 0 0 0 1 0 0 0 0 0 0	DBPC ← PC + 2 (return PC) DBPSW ← PSW PSW.NP ← 1 PSW.EP ← 1 PSW.ID ← 1 PC ← 00000060H		3	3	3					
DI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID ← 1		1	1	1					

Mnemonic	Operands	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DISPOSE	imm5, list12	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L 0 0 0 0 0	sp ← sp + zero-extend (imm5 logically shift left by 2) GR[reg in list12] ← Load-memory (sp, Word) sp ← sp + 4 repeat 2 steps above until regs in list 12 is loaded	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	imm5, list12[reg1]	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L R R R R R **Note 5**	sp ← sp + zero-extend (imm5 logically shift left by 2) GR[reg in list12] ← Load-memory (sp, Word) sp ← sp + 4 repeat 2 steps above until regs in list12 is loaded PC ← GR[reg1]	n+3 Note 4	n+3 Note 4	n+3 Note 4					
DIV	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 1 0 0 0 0 0 0	GR[reg2] ← GR[reg2] ÷ GR[reg1] GR[reg3] ← GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVH	reg1, reg2	r r r r r 0 0 0 0 1 0 R R R R R	GR[reg2] ← GR[reg2] ÷ GR[reg1]**Note 6**	35	35	35		×	×	×	
	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 0 0 0 0 0 0 0	GR[reg2] ← GR[reg2] ÷ GR[reg1]**Note 6** GR[reg3] ← GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVHU	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 0 0 0 0 1 0	GR[reg2] ← GR[reg2] ÷ GR[reg1]**Note 6** GR[reg3] ← GR[reg2]%GR[reg1]	34	34	34		×	×	×	
DIVU	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 1 0 0 0 0 1 0	GR[reg2] ← GR[reg2] ÷ GR[reg1] GR[reg3] ← GR[reg2]%GR[reg1]	34	34	34		×	×	×	
EI		1 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID ← 0	1	1	1					
HALT		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0	Stop	1	1	1					
HSW	reg2, reg3	r r r r r 1 1 1 1 1 1 0 0 0 0 0 w w w w w 0 1 1 0 1 0 0 0 1 0 0	GR[reg3] ← GR[reg2] (15:0)||GR[reg2] (31:16)	1	1	1	×	0	×	×	
JARL	disp22, reg2	r r r r r 1 1 1 1 0 d d d d d d d d d d d d d d d d d d d 0	GR[reg2] ← PC + 4 PC ← PC + sign-extend (disp22)	2	2	2					
JMP	[reg1]	0 0 0 0 0 0 0 0 0 0 1 1 R R R R R	PC ← GR[reg1]	3	3	3					
JR	disp22	0 0 0 0 0 1 1 1 1 0 d d d d d d d d d d d d d d d d d d d 0 **Note 7**	PC ← PC + sign-extend (disp22)	2	2	2					
LD.B	disp16[reg1], reg2	r r r r r 1 1 1 0 0 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← sign-extend (Load-memory (adr, Byte))	1	1	Note 11					
LD.BU	disp16[reg1], reg2	r r r r r 1 1 1 1 0 b R R R R R d d d d d d d d d d d d d d d 1 **Notes8, 10**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← zero (Load-memory (adr, Byte))	1	1	Note 11					
LD.H	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d d 0 **Note 8**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← sign-extend (Load-memory (adr, Halfword))	1	1	Note 11					
LDSR	reg2, regID	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 **Note 12**	SR[regID] ← GR[reg2] — Other than regID = PSW	1	1	1					
			SR[regID] ← GR[reg2] — regID = PSW	1	1	1	×	×	×	×	×
LD.HU	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d d 1 **Note 8**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← zero-extend (Load-memory (adr, Halfword))	1	1	Note 11					

Mnemonic	Operands	Opcode	Operation	Execution Clock			Flags				
				i	r	I	CY	OV	S	Z	SAT
LD.W	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d d 1 **Note 8**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← Load-memory (adr, Word)	1	1	Note 11					
MOV	reg1, reg2	r r r r r 0 0 0 0 0 0 R R R R R	GR[reg2] ← GR[reg1]	1	1	1					
	imm5, reg2	r r r r r 0 1 0 0 0 0 i i i i i	GR[reg2] ← sign-extend (imm5)	1	1	1					
	imm32, reg1	0 0 0 0 0 1 1 0 0 0 1 R R R R R i i i i i i i i i i i i i i i i 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	GR[reg1] ← imm32	2	2	2					
MOVEA	imm16, reg1, reg2	r r r r r 1 1 0 0 0 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + sign-extend (imm16)	1	1	1					
MOVHI	imm16, reg1, reg2	r r r r r 1 1 0 0 1 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + (imm16 || 0^{16})	1	1	1					
MUL	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 0 0 1 0 0 0 0 0	GR[reg3] || GR[reg2] ← GR[reg2] × GR[reg1]	1	2 Note 14	2					
	imm9, reg2, reg3	r r r r r 1 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 I I I I 0 0 **Note 13**	GR[reg3] || GR[reg2] ← GR[reg2] × sign-extend (imm9)	1	2 Note 14	2					
MULH	reg1, reg2	r r r r r 0 0 0 1 1 1 R R R R R	GR[reg2] ← GR[reg2] **Note 6** × GR[reg1] **Note 6**	1	1	2					
	imm5, reg2	r r r r r 0 1 0 1 1 1 i i i i i	GR[reg2] ← GR[reg2] **Note 6** × sign-extend (imm5)	1	1	2					
MULHI	imm16, reg1, reg2	r r r r r 1 1 0 1 1 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] **Note 6** × imm16	1	1	2					
MULU	reg1, reg2, reg3	r r r r r 1 1 1 1 1 1 R R R R R w w w w w 0 1 0 0 0 1 0 0 0 1 0	GR[reg3] || GR[reg2] ← GR[reg2] × GR [reg1]	1	2 Note 14	2					
	imm9, reg2, reg3	r r r r r 1 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 I I I I 1 0 **Note 13**	GR[reg3]||GR[reg2] ← GR[reg2] × zero-extend (imm9)	1	2 Note 14	2					
NOP		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Passes at least 1 cycle doing nothing.	1	1	1					
NOT	reg1, reg2	r r r r r 0 0 0 0 0 1 R R R R R	GR[reg2] ← NOT (GR[reg1])	1	1	1		0	×	×	
NOT1	bit#3, disp16[reg1]	0 1 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, Z flag)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 1 1 0 0 0 1 0	adr ← GR[reg1] Z flag ← Not (Load-memory-bit (adr, reg2)) Store-memory-bit (adr, reg2, Z flag)	3 Note 3	3 Note 3	3 Note 3				×	
OR	reg1, reg2	r r r r r 0 0 1 0 0 0 R R R R R	GR[reg2] ← GR[reg2] OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16, reg1, reg2	r r r r r 1 1 0 1 0 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] OR zero-extend (imm16)	1	1	1		0	×	×	
PREPARE	list12, imm5	0 0 0 0 0 1 1 1 1 0 i i i i i L L L L L L L L L L L 0 0 0 0 1	Store-memory (sp-4, GR[reg in list12], Word) sp ← sp−4 repeat 1 steps above until regs in list12 is stored sp ← sp-zero-extend (imm5)	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	list12, imm5, sp/imm[Note15]	0 0 0 0 0 1 1 1 1 0 i i i i i L L L L L L L L L L L f f 0 1 1 imm16/imm32 **Note 16**	Store-memory (sp-4, GR[reg in list12], Word) GR[reg in list12] ← Load-memory (sp, Word) sp ← sp + 4 repeat 2 steps above until regs in list12 is loaded PC ← GR[reg1]	n+2 Note 4 Note 17	n+2 Note 4 Note 17	n+2 Note 4 Note 17					

Mnemonic	Operands	Opcode	Operation	Execution Clock			Flags				
				i	r	I	CY	OV	S	Z	SAT
RETI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0	if PSW.EP = 1 then PC ← EIPC PSW ← EIPSW else if PSW.NP = 1 then PC ← FEPC PSW ← FEPSW else PC ← EIPC PSW ← EIPSW	3	3	3	R	R	R	R	R
SAR	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0	GR[reg2] ← GR[reg2] arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5, reg2	r r r r r 0 1 0 1 0 1 i i i i i	GR[reg2] ← GR[reg2] arithmetically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SASF	cccc, reg2	r r r r r 1 1 1 1 1 1 1 0 c c c c 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	if conditions are satisfied then GR[reg2] ← (GR[reg2] Logically shift left by 1) OR 00000001H else GR[reg2] ← (GR[reg2] Logically shift left by 1) OR 00000000H	1	1	1					
SATADD	reg1, reg2	r r r r r 0 0 0 1 1 0 R R R R R	GR[reg2] ← saturated (GR[reg2] + GR[reg1])	1	1	1	×	×	×	×	×
	imm5, reg2	r r r r r 0 1 0 0 0 1 i i i i i	GR[reg2] ← saturated (GR[reg2] sign-extend (imm5))	1	1	1	×	×	×	×	×
SATSUB	reg1, reg2	r r r r r 0 0 0 1 0 1 R R R R R	GR[reg2] ← saturated (GR[reg2] – GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16, reg1, reg2	r r r r r 1 1 0 0 1 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← saturated (GR[reg1] – sign-extend (imm16)	1	1	1	×	×	×	×	×
SATSUBR	reg1, reg2	r r r r r 0 0 0 1 0 0 R R R R R	GR[reg2] ← saturated (GR[reg1] – GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc, reg2	r r r r r 1 1 1 1 1 1 0 c c c c 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	if conditions are satisfied then GR[reg2] ← 00000001H else GR[reg2] ← 00000000H	1	1	1					
SET1	bit#3, disp16 [reg1]	0 0 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, 1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0	adr ← GR[reg1] Z flag ← Not (Load-memory-bit (adr, reg2)) Store-memory-bit (adr, reg2, 1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	GR[reg2] ← GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5, reg2	r r r r r 0 1 0 1 1 0 i i i i i	GR[reg2] ← GR[reg2] logically shift left by zero-extend (imm5)	1	1	1	×	0	×	×	
SHR	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	GR[reg2] ← GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5, reg2	r r r r r 0 1 0 1 0 0 i i i i i	GR[reg2] ← GR[reg2] logically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep], reg2	r r r r r 0 1 1 0 d d d d d d d	adr ← ep + zero-extend (disp7) GR[reg2] ← sign-extend (Load-memory (adr, Byte))	1	1	Note 9					
SLD.BU	disp4[ep], reg2	r r r r r 0 0 0 0 1 1 0 d d d d **Note 18**	adr ← ep + zero-extend (disp4) GR[reg2] ← zero-extend (Load-memory (adr, Byte))	1	1	Note 9					
SLD.H	disp8[ep], reg2	r r r r r 1 0 0 0 d d d d d d d **Note 19**	adr ← ep + zero-extend (disp8) GR[reg2] ← sign-extend (Load-memory (adr, Halfword))	1	1	Note 9					

Mnemonic	Operands	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SLD.HU	disp5[ep], reg2	r r r r r 0 0 0 0 1 1 1 d d d d **Notes 18, 20**	adr ← ep + zero-extend (disp5) GR[reg2] ← zero-extend (Load-memory (adr, Halfword)	1	1	Note 9					
SLD.W	disp8[ep], reg2	r r r r r 1 0 1 0 d d d d d d 0 **Note 21**	adr ← ep + zero-extend (disp8) GR[reg2] ← Load-memory (adr, Word)	1	1	Note 9					
SST.B	reg2, disp7[ep]	r r r r r 0 1 1 1 d d d d d d d	adr ← ep + zero-extend (disp7) Store-memory (adr, GR[reg2], Byte)	1	1	1					
SST.H	reg2, disp8[ep]	r r r r r 1 0 0 1 d d d d d d d **Note 19**	adr ← ep + zero-extend (disp8) Store-memory (adr, GR[reg2], Halfword)	1	1	1					
SST.W	reg2, disp8[ep]	r r r r r 1 0 1 0 d d d d d d 1 **Note 21**	adr ← ep + zero-extend (disp8) Store-memory (adr, GR[reg2], Word)	1	1	1					
ST.B	reg2, disp16 [reg1]	r r r r r 1 1 1 0 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Byte)	1	1	1					
ST.H	reg2, disp16 [reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d d 0 **Note 8**	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Halfword)	1	1	1					
ST.W	reg2, disp16 [reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d d 1 **Note 8**	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Word)	1	1	1					
STSR	regID, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	GR[reg2] ← SR[regID]	1	1	1					
SUB	reg1, reg2	r r r r r 0 0 1 1 0 1 R R R R R	GR[reg2] ← GR[reg2] – GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1, reg2	r r r r r 0 0 1 1 0 0 R R R R R	GR[reg2] ← GR[reg1] – GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	0 0 0 0 0 0 0 0 0 0 1 0 R R R R R	adr ← (PC + 2) + GR[reg1] logically shift left by 1) PC ← (PC + 2) + (sign-extend (Load-memory (adr, Halfward)) logically shift left by 1	5	5	5					
SXB	reg1	0 0 0 0 0 0 0 0 1 0 1 R R R R R	GR[reg1] ← sign-extend (GR[reg1] (7:0))	1	1	1					
SXH	reg1	0 0 0 0 0 0 0 0 1 1 1 R R R R R	GR[reg1] ← sign-extend (GR[reg1] (15:0))	1	1	1					
TRAP	vector	0 0 0 0 0 1 1 1 1 1 1 i i i i i 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	EIPC ← PC + 4 (return PC) EIPSW ← PSW ECR.EICC ← interrupt code PSW.EP ← 1 PSW.ID ← 1 PC ← 00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1, reg2	r r r r r 0 0 1 0 1 1 R R R R R	result ← GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3, disp16 [reg1]	1 1 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not(Load-memory-bit(adr,bit#3))	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 1 1 0 0 1 1 0	adr ← GR[reg1] Z flag ← Not(Load-memory-bit(adr,reg2))	3 Note 3	3 Note 3	3 Note 3					
XOR	reg1, reg2	r r r r r 0 0 1 0 0 1 R R R R R	GR[reg2] ← GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16, reg1, reg2	r r r r r 1 1 0 1 0 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	0 0 0 0 0 0 0 0 1 0 0 R R R R R	GR[reg1] ← zero-extend (GR[reg1] (7:0))	1	1	1					
ZXH	reg1	0 0 0 0 0 0 0 0 1 1 0 R R R R R	GR[reg1] ← zero-extend (GR[reg1] (15:0))	1	1	1					

Notes 1. dddddddd is the higher 8 bits of disp9.

2. 3 clocks if last instruction includes PSW write access

3. If there is no wait state (3 + number of read access wait states)

4. n is the total number of load registers in listX. (According to the number of wait states. If there are no wait states, n is the number of registers in listX.)

5. RRRRR: Other than 00000

6. Only the lower halfword of data is valid.

7. ddddddddddddddddddddd is the higher 21 bits of disp22.

8. ddddddddddddddd is the higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states)

10. b: Bit 0 of disp16

11. According to the number of wait states (2 if there are no wait states)

12. In this instruction, although the source register is regarded as reg2 for convenience of the mnemonic description, the reg1 field is used in the opcode. Therefore, the meanings of register specifications assigned in the mnemonic description and in the opcode differ from those in other instructions.
rrrrr = regID specification
RRRRR = reg2 specification

13. iiiii: Lower 5 bits of imm9
IIII: Lower 4 bits of imm9

14. Shortened by 1 clock if reg2 = reg3 (lower 32 bits of result are not written to register) or reg3 = r0 (higher 32 bits of result are not written to register).

15. sp/imm: Specify in bits 19 and 20 of sub-opcode.

16. ff = 00: Load sp in ep.
01: Load sign-extended 16-bit immediate data (bits 47 to 32) in ep.
10: Load 16-bit immediate data (bits 47 to 32) logically shifted 16 bits to the right in ep.
11: Load 32-bit immediate data (bits 63 to 32) in ep.

17. n + 3 clocks when imm = imm32

18. rrrrr: Other then 00000

19. ddddddd is the higher 7 bits of disp8.

20. dddd is the higher 4 bits of disp5.

21. dddddd is the higher 6 bits of disp8.

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