ARX-3400 SERIES CURRENT SOURCE TRANSCEIVERS to MIL-STD-1553

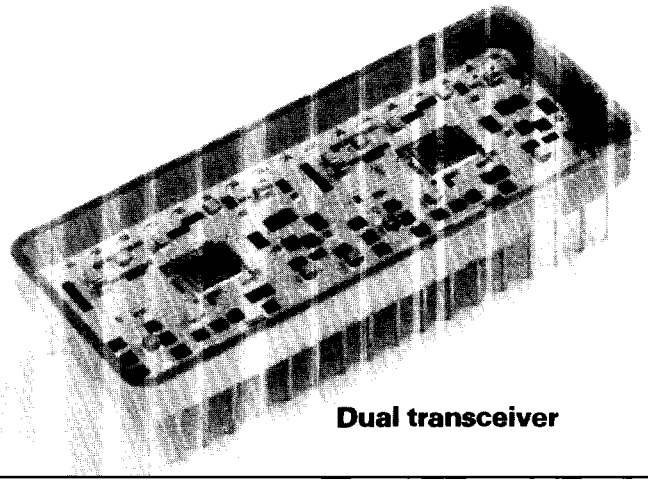
AEROFLEX
An ARX Company

Features

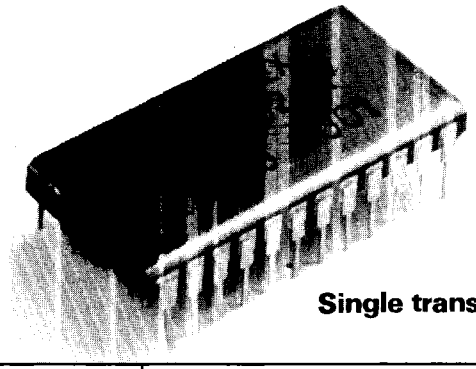
- **Monolithic construction for low parts count**
- **Very low standby power consumption**
- **Single and dual models**
- **Optional small footprint single model**
- **Outstanding MIL-STD-1553 electrical performance**
- **Full interchangeability with existing transceivers**
- **± 15 volt or ± 12 volt power supply operation**
- **Plug in and flat pack versions**
- **MIL-STD-883 Screened**

General Description:

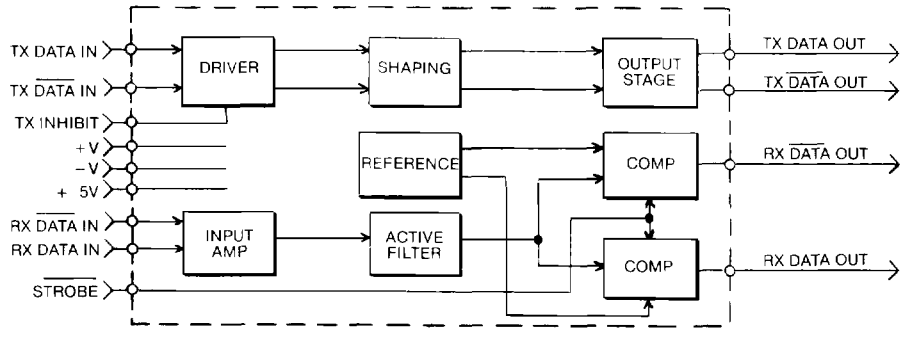
The Aeroflex Laboratories Incorporated Series 3400 Transceivers are a second generation design which utilize an Application Specific Integrated Circuit (ASIC) with Large Scale Integration (LSI) fabricated in Bipolar technology as its main element. The only parts external to the LSI device in the hybrid are the precision resistors and capacitors required in the filter and other portions of the circuit, and the components which make up the power driving stage of the transmitter. All units provide full compliance with MIL-STD-1553 A and B requirements and exhibit outstanding electrical performance.



Dual transceiver



Single transceiver



Block diagram (without transformer)

Design of these transceivers reflect particular attention to dynamic characteristics such as output offset, low bit and word error rate, waveform purity and absence of zero crossover distortion. Efficient overall electrical design provides very low internal power dissipation and thermal design keeps heat rise to a minimum.

Each channel of the dual transceiver is completely separate from the other and fully independent. This includes all power leads as well as signal lines and grounds. Hence each channel may be connected to a different data bus with no interaction between them.

The single transceiver is available in a 24 pin ceramic housing which has a footprint 21% smaller than metal counterparts, yet is pin interchangeable.

AROFS010

The single device is also available in 18 pin dual in line package.

Transmitter

The transmitter section accepts bi-phase TTL level data signals at the input and when coupled to the data bus with a transformer of appropriate turns ratio, isolated on the data bus side with two 52.5 ohm fault isolation resistors, and loaded by two 70 ohm terminations plus additional receivers, the data bus signal produced is 7.5 volts nominal peak-to-peak at A-A'. (See Figure 5).

When both "DATA" and "$\overline{\text{DATA}}$" inputs are held low or high the transmitter output becomes a high impedance and is "removed" from the line. Alternately, an overriding "INHIBIT" input provides for removal of the transmitter output as well. Logic high applied to the "INHIBIT" disables the transmitter. (See Transmitter Logic Waveform, Figure 1.) The transmitter may be safely operated for an indefinite period with output short circuited at 100% duty cycle.

Receiver

The Receiver section accepts bi-phase differential data at the input and produces two TTL level signals at the output. The outputs are "DATA" and "$\overline{\text{DATA}}$", and represent positive and negative excursions (respectively) of the input above a predetermined threshold. (See Receiver Logic Waveform, Figure 2.)

The pre-set internal threshold will detect data bus signals exceeding 1.15 volts p-p and reject signals less than 0.6 volts p-p when used with appropriate transformers. (See Figure 5 and ordering information table for transformer data and typical connections.)

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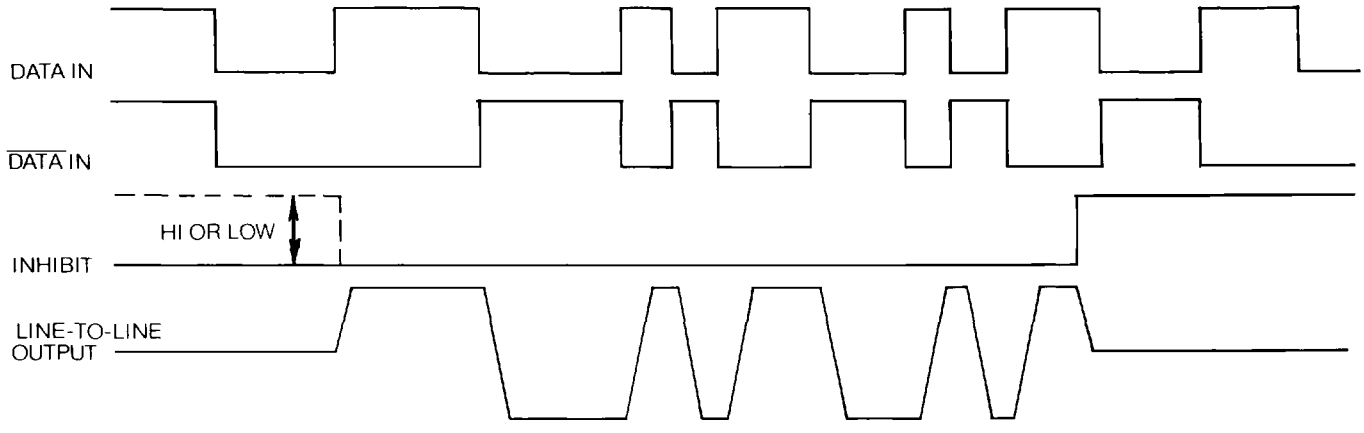
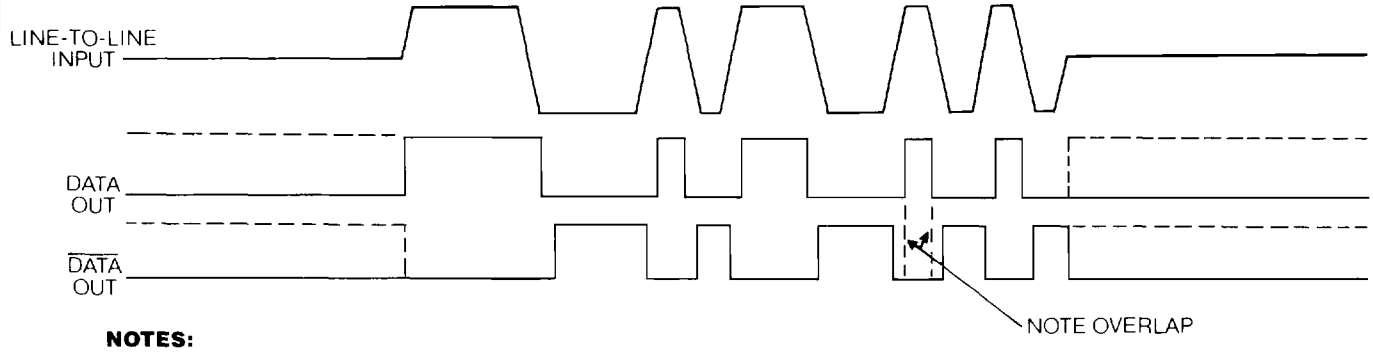
Figure 1. Transmitter Logic Waveform



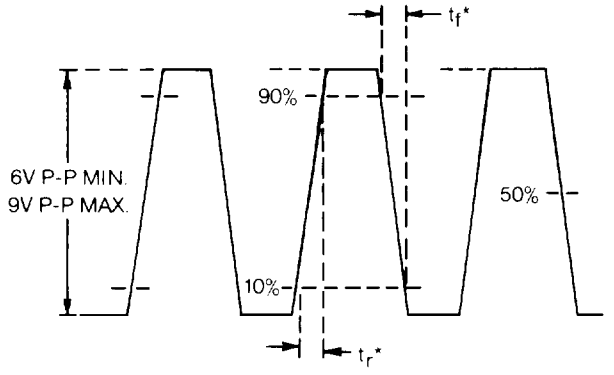
NOTES:
1: DATA and $\overline{\text{DATA}}$ inputs must be complementary waveforms, or 50% duty cycle average, with no delays between them.
2: DATA and $\overline{\text{DATA}}$ must be in the same state during off time. (both high or both low)

Figure 2. Receiver Logic Waveform



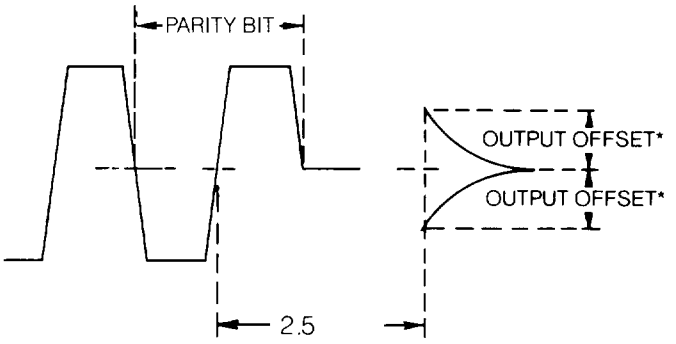
NOTES:
1: Receiver output waveforms shown are for normally low devices. For normally high devices the two outputs are inverted and swapped, as shown by the dashed lines.

Figure 3. Transmitter (TX) Data Differential Output Waveforms



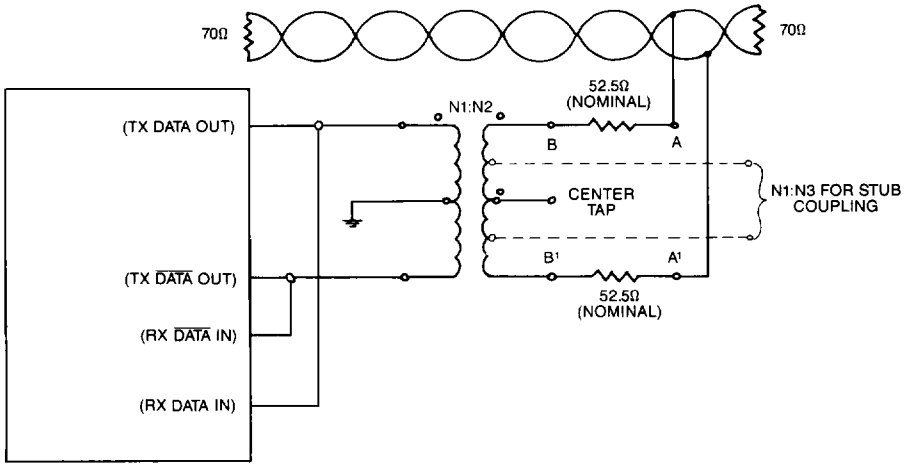
*Rise & Fall Times—
measured at point A-A′ in figure 5.

Figure 4. Transmitter (TX) Output Offset



*Offset measure at
point A-A′ in figure 5.

Figure 5. Typical Transformer Connection



Strobe Characteristics (Logic "0" inhibits Output) If not used, a 1K ohm pullup to 5V is recommended.

"0" Input Current	$V_S = 0.4V$	I_{IL}	−0.5		−0.4	mA
"1" Input Current	$V_S = 2.7V$	I_{IH}			40	μA
"0" Input Voltage		V_{IL}			0.7	V
"1" Input Voltage		V_{IH}	2.0			V
Strobe Delay (turn-on or turn-off)	**Note 1**	t_{SD}		125	250	nS

Output Characteristics, RX DATA & DATA

"1" State	$I_{OH} = -0.4mA$	V_{OH}	2.5	3.4		V
"0" State	$I_{OL} = 4mA$	V_{OL}			0.5	V
Delay (average) from differential input zero crossings to RX DATA and RX DATA output 50% points	**Note 1**	t_{DRX}		350	400	nS

Power Data

Voltage

15 volt versions	+14.25 to +15.75 −14.25 to −15.75
12 volt versions	+11.40 to +12.60 −11.40 to −12.60
Logic (all versions)	4.50 to 5.50

Currents, maximums per channel

Duty cycle	+12V	−12V	5V	+15V	−15V	5V
0%	1 mA	16.5 mA	30 mA	1 mA	16.5 mA	30 mA
50%	160 mA	25 mA	30 mA	110 mA	25 mA	30 mA
100% **Note 1**	320 mA	30 mA	30 mA	220 mA	30 mA	30 mA

General

Temperature Range
Operating (Case) ..... −55° to +125°C
Storage (Ambient) ..... −55° to +150°C
Weight Single ..... 0.4 oz. typ.
Dual ..... 0.51 oz. typ.

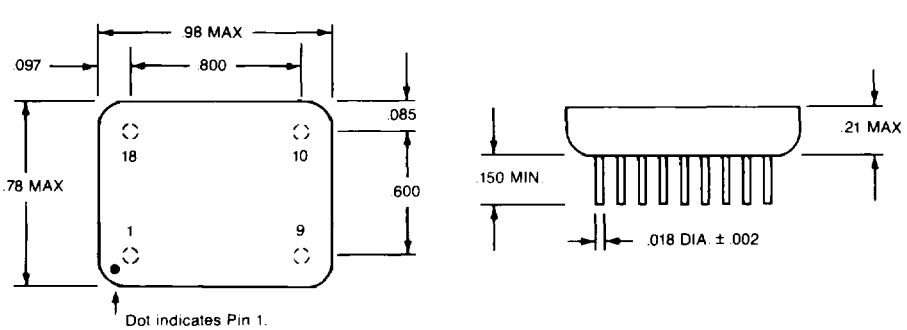
Maximum transmitting duty cycle
when case is held to 125°C maximum 100%

Configurations and Ordering Information

Model No.	Power Supply	Transformer Turns Ratio N1 : N2	N1 : N3	Receiver Data Outputs (Bus Inactive)	Configuration
ARX 3402	± 15V	1.4 : 1	2 : 1	Normally low	Single
ARX 3411	± 15V	1.4 : 1	2 : 1	Normally low	Dual
ARX 3415	± 15V	1.4 : 1	2 : 1	Normally high	Single
ARX 3416	± 15V	1.4 : 1	2 : 1	Normally high	Dual
ARX 3419	± 12V	1 : 1	1:.707	Normally low	Dual
ARX 3420	± 12V	1 : 1	1:.707	Normally low	Single
ARX 3424	± 12V	1 : 1	1:.707	Normally high	Single
ARX 3425	± 12V	1 : 1	1:.707	Normally high	Dual

Add suffix "FP" for Flat Pack Models (Dual only)
Add suffix "CP" for Ceramic Package Models (Singles only)

18 Pin Dual In Line



Pin Connection Table

P/N	FUNCTION
1	TX DATA OUT
2	TX $\overline{\text{DATA}}$ OUT
3	ANALOG GROUND
4	NC
5	RX DATA OUT
6	STROBE
7	GROUND
8	RX $\overline{\text{DATA}}$ OUT
9	NC
10	+V
11	RX DATA IN
12	RX $\overline{\text{DATA}}$ IN
13	GROUND
14	−V
15	+5V
16	INHIBIT
17	TX DATA IN
18	TX $\overline{\text{DATA}}$ IN

Absolute Maximum Ratings

Supply voltage, V+	−0.3 to +18.0V	
Supply voltage, V−	+0.3 to −18.0V	
Supply voltage, V_L	−0.3 to +7.0V	
Logic Input Voltage	−0.3 to +5.5V	
Receiver Differential Input	±20V (40V p-p)	
Receiver Input Voltage (Common Mode)	±15V	
Driver Peak Output Current	300mA	
Max. power dissipation (Max. Power Supplies Voltages) (Total hybrid at 100% duty cycle)* (Total hybrid standby mode)	Single 1591 mW 440 mW	Dual* 2031 mW 880 mW
Maximum power dissipation in hottest die @ 100% duty cycle (Derates to zero in standby mode)	477mW	
Θ_{JC}(junction to case) for hottest die	88°C/W	
Θ_{CA}(case in air) typical	Dual 20°C/W; Single 30°C/W	
Max. junction to case temperature rise for the hottest device (@ 100% duty cycle)	42° C	

* One channel transmitting at 100% duty cycle and the second channel at standby.

Electrical Characteristics, Driver Section

Input Characteristics, TX DATA in or TX $\overline{\text{DATA}}$ in

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
"0" Input Current	V_{IN} = 0.4V	I_{ILD}			−0.4	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHD}			40	μA
"0" Input Voltage		V_{ILD}			0.7	V
"1" Input Voltage		V_{IHD}	2.0			V

Inhibit Characteristic

"0" Input Current	V_{IN} = 0.4V	I_{ILI}			−0.4	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHI}			40	μA
"0" Input Voltage		V_{ILI}			0.7	V
"1" Input Voltage		V_{IHI}	2.0			V
Delay from TX Inhibit (0→1) to inhibited output	**Note 1**	t_{DXOFF}		150	350	nS
Delay from TX Inhibit (1→0) to active output	**Note 1**	t_{DXON}		120	200	nS
Differential output noise, inhibit mode		V_{NOI}			10	mVp-p
Differential output impedance (inhibited)	**Note 1**	Z_{OI}	10K			ohms

Output Characteristics

Differential output level	R_L = 35 ohms	V_O	6	7.5	9	Vp-p
Rise and Fall times (10% to 90% of p-p output)		t_r	100		300	nS
Output offset at point A-A′ in Fig. 5, 2.5 μS after mid-bit crossing of the parity bit of the last word of a 660 μs message	R_L = 35 ohms	V_{OS}			±90	mV peak
Delay from 50% point of TX DATA or TX DATA input to zero crossing of differential output	**Note 1**	t_{DTX}		150	350	nS

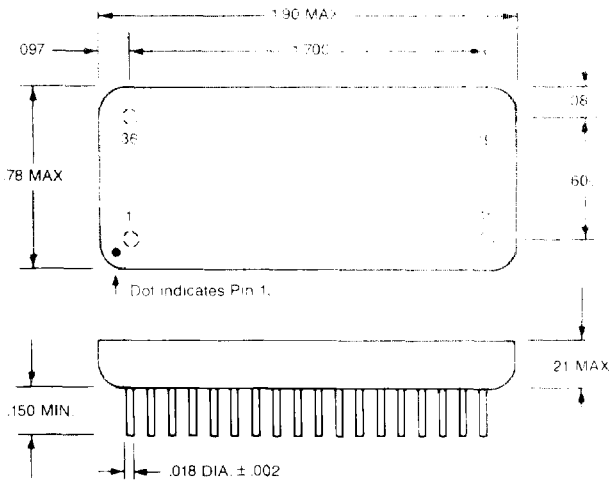
Note 1. Characteristic guaranteed by design; not production tested.

Note 2. Measured at bus side of transformer, including contribution from transformer.

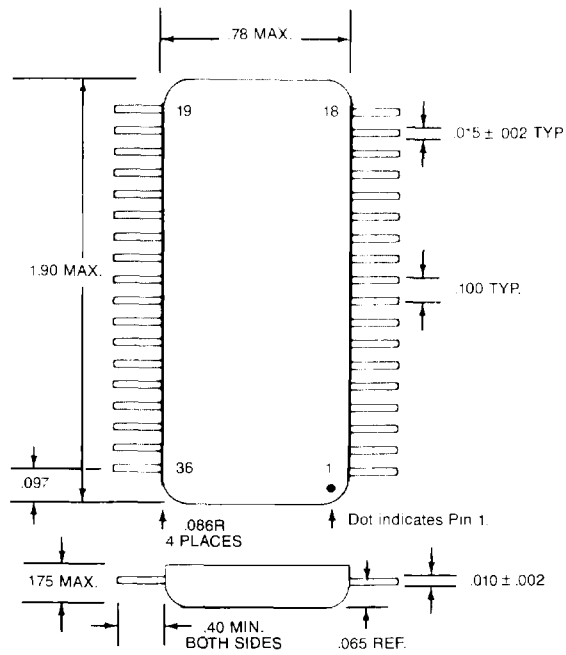
Electrical Characteristics, Receiver Section

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Differential Input Impedance	f = 1MHz	Z_{IN}	10K			ohms
Differential Voltage Range		V_{IDR}			±20	V peak
Input Common Mode Voltage Range	**Note 1**	V_{ICR}	±10			V peak
Common Mode Rejection Ratio **Note 2**	**Note 1**	CMRR	40			dB
Threshold Characteristics (Sinewave input.) *Note: Threshold voltages are referred to the bus.*	100KHz to 1MHz	V_{TH}	.60		1.15	Vp-p

Dual Transceiver Dual In Line



Dual Transceiver Flat Pack

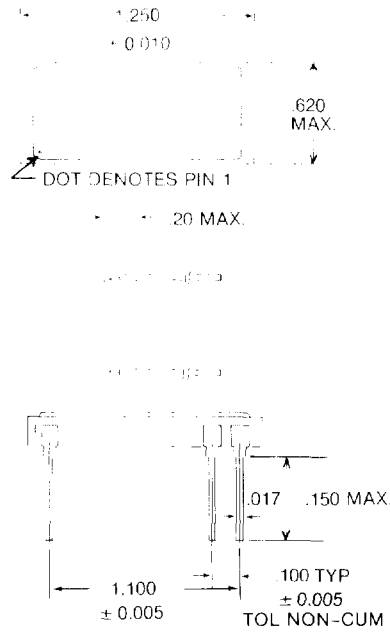


Pin Connection Table

P/N	FUNCTION
	TX DATA OUT A
	TX $\overline{\text{DATA}}$ OUT A
	ANALOG GROUND
	NC
	RX DATA OUT A
	STROBE A
	GROUND
	RX $\overline{\text{DATA}}$ OUT
9	CASE GROUND
10	TX DATA OUT B
11	TX $\overline{\text{DATA}}$ OUT B
12	ANALOG GROUND
13	NC
14	RX DATA OUT B
15	STROBE B
16	ANALOG GROUND
17	RX $\overline{\text{DATA}}$ OUT B
18	NC
19	+ V B
20	RX DATA IN B
21	RX $\overline{\text{DATA}}$ IN B
22	GROUND
23	V B
24	+ 5V B
25	INHIBIT B
26	TX DATA IN B
27	TX $\overline{\text{DATA}}$ IN B
28	+ V A
29	RX DATA IN A
30	RX $\overline{\text{DATA}}$ IN A
31	GROUND
32	V A
33	+ 5V A
34	INHIBIT A
35	TX DATA IN A
36	TX $\overline{\text{DATA}}$ IN A

Note: A and B denotes separate channels.

Single Transceiver Ceramic Package



Pin Connection Table

P/N	FUNCTION
1	TX $\overline{\text{DATA}}$ OUT
2	TX $\overline{\text{DATA}}$ OUT
3	GROUND
4	NC
5	NC
6	NC
7	RX DATA OUT
8	STROBE
9	GROUND
10	RX $\overline{\text{DATA}}$ OUT
11	NC
12	NC
13	+ V
14	NC
15	RX $\overline{\text{DATA}}$ IN
16	RX $\overline{\text{DATA}}$ IN
17	NC
18	GROUND
19	V
20	+ 5V DC
21	TX INHIBIT
22	TX $\overline{\text{DATA}}$ IN
23	TX $\overline{\text{DATA}}$ IN
24	NC

Notes:
1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Pins are equally spaced at .100 ± .002 tolerance, non-cumulative, each row.

Specifications subject to change without notice.

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