IA82510
Data Sheet

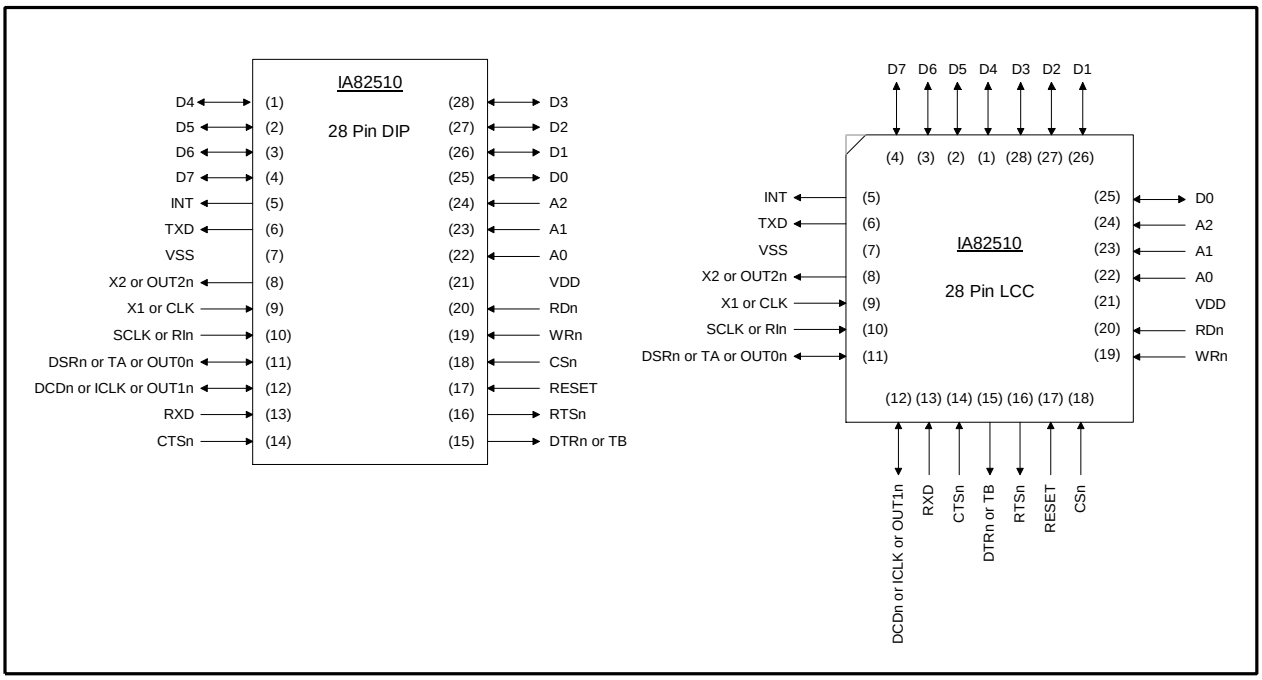
ASYNCHRONOUS SERIAL CONTROLLER

FEATURES

- **Form, Fit, and Function Compatible with the Intel® 82510**
- **Packaging options available: 28 Pin Plastic or Ceramic DIP, 28 Pin Plastic Leaded Chip Carrier, 28 Pin Ceramic Leadless Chip Carrier**
- **Asynchronous Serial Channel Operation**
- **Separate Transmit and Receive FIFOs with Programmable Threshold**
- **Programmable Baud Rate Generators up to 288K Baud**
- **Special Protocol Features**
  - **Control Character Recognition**
  - **Auto Echo and Loopback Modes**
  - **9-Bit Protocol Support**
  - **5 to 9 Bit Character Format**

The IA82510 uses **innovASIC**'s innovative new ***f*³ Program** to provide industry with parts that other vendors have declared obsolete. By specifying parts through this program a customer is assured of never having a component become obsolete again. This data sheet assumes the original part has been designed in, and so provides a summary of capabilities only. For new designs contact **innovASIC** for more detailed information.

Package Pinout

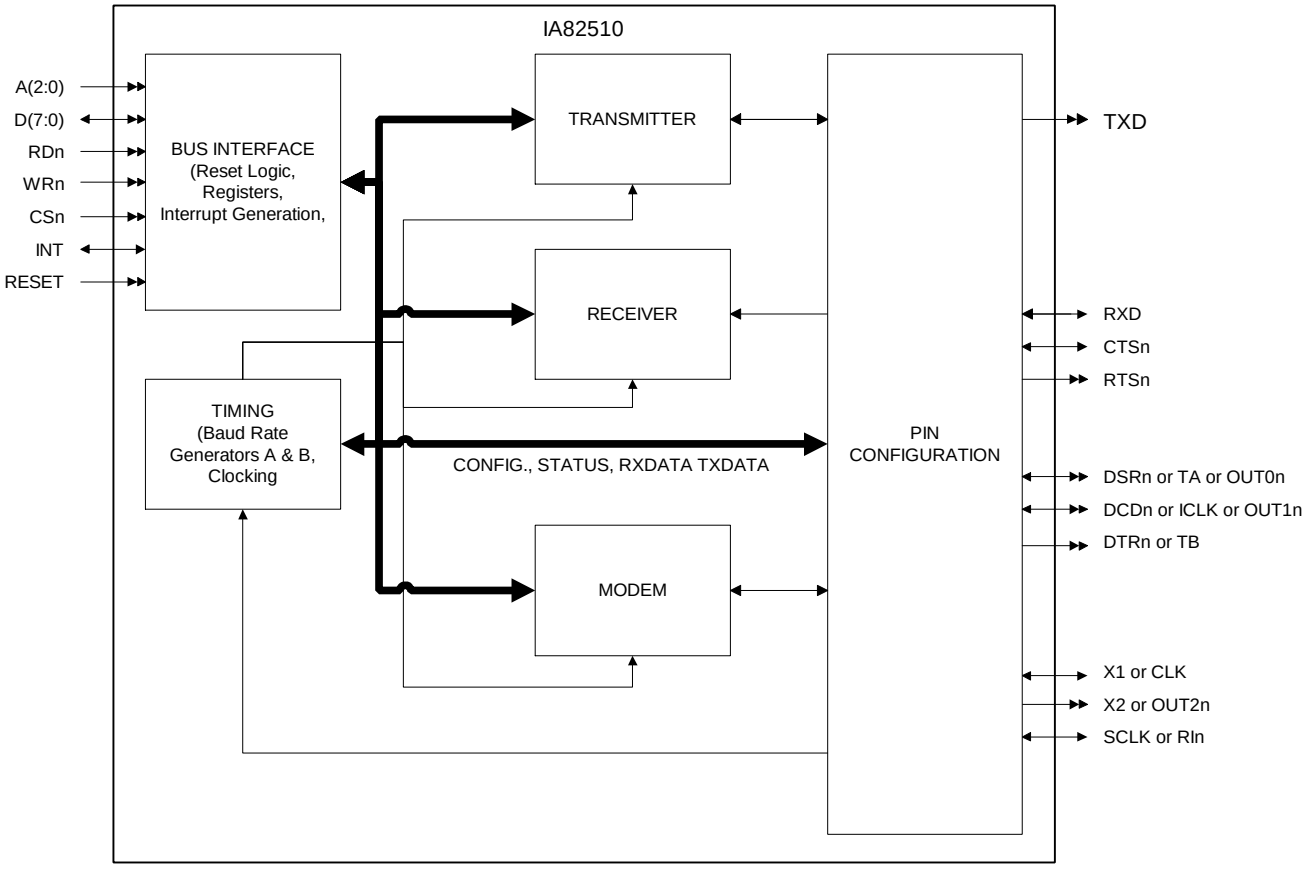


IA82510 Data Sheet
ASYNCHRONOUS SERIAL CONTROLLER

DESCRIPTION

The IA82510 is an asynchronous serial controller that provides a CPU interface to one transmit and one receive channel. It is Form, Fit, and Function compatible with the Intel 82510. Configuration registers are used to control the serial channel, interrupts, and modes of operation. The CPU controls this device via address and data lines with read/write control. The CPU also uses this interface to read and write data to receive and transmit data through the serial channel. FIFOs and various serial modes can be used to help off-load the CPU from transmitting and receiving data. An interrupt line provides an indication to the CPU that the device requires servicing. The device can be configured for 8250A/16450 compatibility.

functional block diagram



Functional Overview

Transmitter

The Transmit function consists of a 4 × 11 bit FIFO, and a Transmit Engine. The 4 × 11 FIFO is configurable as any depth between one and four words inclusive. The transmit engine is responsible for reading the data out of the FIFO and placing it in the proper order on the TXD pin. The transmit engine is highly configurable to be compatible with numerous formats, including 16450 and 8250 modes of communication. Transmit Communication parameters that can be programmed include:

- Parity modes
- Stop Bits
- Character Length
- FIFO Depth
- Clocking Options
- RTS and CTS modes

See the Register Description for more details.

Receiver

The Receiver function consists of a 4 × 11 configurable FIFO and a Receive Engine. The receive engine is responsible for sampling the data on the RXD input pin, formatting the data, and placing the data in the FIFO. The receive engine is highly configurable with parameters that include:

- Parity modes
- Stop Bits
- Character Length
- FIFO Depth
- Clocking Options
- Address Matching Options
- Control Character Detection
- RTS and CTS modes

See the Register Description for more details.

Bus Interface

The Bus Interface is a simple interface that allows a micro-processor or micro-controller to read and write the IA82510 Registers. It consists of the following I/O lines:

- A0, A1, A2 : 3 Bit Address
- D0-D7 : 8 Bit Data
- RDn: Active Low Read Enable
- WRn: Active Low Write Enable
- CSn: Active Low Chip Select
- INT: Interrupt Output
- RESET: Chip Reset

Register Description

Table 1 – IA82510 Register Summary					
Register	ADDR	Bank	DLAB	Mode	Default
ACR0	111	00	X	R/W	00000000
ACR1	101	10	X	R/W	00000000
BACF	001	11	0	R/W	00000100
BAH	001	00	1	R/W	00000000
BAL	000	00	1	R/W	00000010
BANK	010	X	X	W	00000000
BBCF	011	11	X	R/W	10000100
BBH	001	11	1	R/W	00000000
BBL	000	11	1	R/W	00000101
CLCF	000	11	0	R/W	00000000
FLR	100	01	X	R	00000000
FMD	001	10	X	R/W	00000000
GER	001	00	0	R/W	00000000
GIR_BANK	010	X	X	R	00000001
GSR	111	01	X	R	00010010
ICM	111	01	X	W	N/A
IMD	100	10	X	R/W	00001100
LCR	011	00	X	R/W	00000000
LSR	101	00	X	R/W	01100000
MCR	100 100	00 01	X X	R/W W	00000000
MIE	101	11	X	R/W	00001111
MSR	110 110	00 01	X X	R/W R	00000000
PMD	100	11	X	R/W	11111100
RCM	101	01	X	W	N/A
RIE	110	10	X	R/W	00011110
RMD	111	10	X	R/W	00000000
RST	101	01	X	R	00000000
RXDATA	000	00 01	0 X	R	Unknown
RXF	001	01	X	R	Unknown
TCM	110	01	X	W	N/A
TMCR	011	01	X	W	N/A
TMD	011	10	X	R/W	00000000
TMIE	110	11	X	R/W	00000000
TMST	011	01	X	R	00110000
TXDATA	000	00 01	0 X	W	N/A
TXF	001	01	X	W	N/A

Absolute Maximum Ratings

PARAMETER	Min	Max	UNITS	Notes
Supply voltage, V_{DD}	-0.3	6.0	V	
Input voltage, V_{IN}	-0.3	V_{DD} + 0.3	V	
Input Pin Current I_{IN}	-10.0	10.0	mA	25° C
Operating temperature range	-40	+85	°C	
Storage temperature range	-55	150	°C	
Ambient Temperature, T_a	-40	85	°C	(2)
Lead Temperature		300	°C	10 sec
Power Dissipation		155	mW	125°C, 25MHz, 15% Toggle

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Operating the device beyond the conditions indicated in the “recommended operating conditions” section is not recommended. Operation at the “absolute maximum ratings” may adversely affect device reliability.

DC Characteristics

PARAMETER	Min	Max	UNITS	Notes
DC Supply voltage, V_{DD}	4.5	5.5	V	(2)
Static Supply Current, I_{DD}		100	µA	(1)
Power Supply Current, I_{DD}		1.12	mA/MHz	
Standby Supply Current, I_{stby}		100	µA	
Input Capacitance, C_{IN}		5	pF	
I/O Capacitance, $C_{I/O}$		6	pF	
Circuit Ground, V_{SS}	0.0	0.0	V	25° C

Notes:

(1) Static I_{DD} current is exclusive of input/output drive requirements and is measured with the clocks stopped and all inputs tied to V_{DD} or V_{SS}, configured to draw minimum current.

(2) The input and output parametric values in section VII-B, parts 1, 2, and 3, are directly related to ambient temperature and DC supply voltage. A temperature or supply voltage range other than those specified in the Operating Conditions above will affect these values and part performance is not guaranteed by innovASIC.

Parametric Voltage and Current Levels (Ambient Temperature = -40 to 85 C)

Input Pin	V_{IL}	V_{IH}	Hysteresis	Note
X1, CLK (pin 9)	0.3 * V_{DD}	0.7 * V_{DD}	NA	Oscillator In (3)
D0-D7 SCLK DSRn, TA, OUT0n (Pin 11) DCDn, ICLK, OUT1n (Pin 12) RXD CTSn A0-A2 RDn WRn CSn RESET	0.7 V	2.1 V	0.38 V	TTL-SCHMITT (3)

Output Pin	V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OZ}		Note
					Min	Max	
X2 or OUT2n	0.4 V	2.4 V	1.92 mA	1.92 mA	NA	NA	(4), (6)
D0-D7 DSRn, TA, OUT0n (Pin 11) DCDn,ICLK,OUT1n (Pin 12)	0.4 V	2.4 V	1.92 mA	1.92 mA	-10 µA	10 µA	(4),(5),(7)
RTSn DTRn or TB (Pin 15)	0.4 V	2.4 V	1.92 mA	1.92 mA	NA	NA	(4), TTL

Pullup Pin	IPU		Note
	Min	Max	
DTRn or TB (Pin 15) RTSn (Pin 16)	-28.3 A	-137 A	(8), Strapping Pull Up Resistor

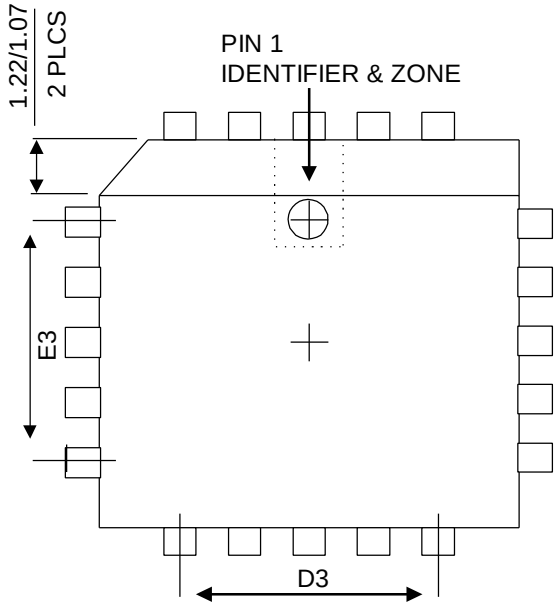
Notes:

(3) Input leakage is +-1µA
(4) V_{OL}, V_{OH}, I_{OL}, and I_{OH} are tested at V_{DD} = 4.5 Volts.
(5) I_{OZ} is tested with V_{DD} = 5.5 Volts.
(6) Oscillator Out
(7) Tri-states are tested using loads connected to predetermined voltage levels.
(8) Inputs with pullups are tested at V_{IN} = 0 Volts, V_{DD} = 5.5 Volts.

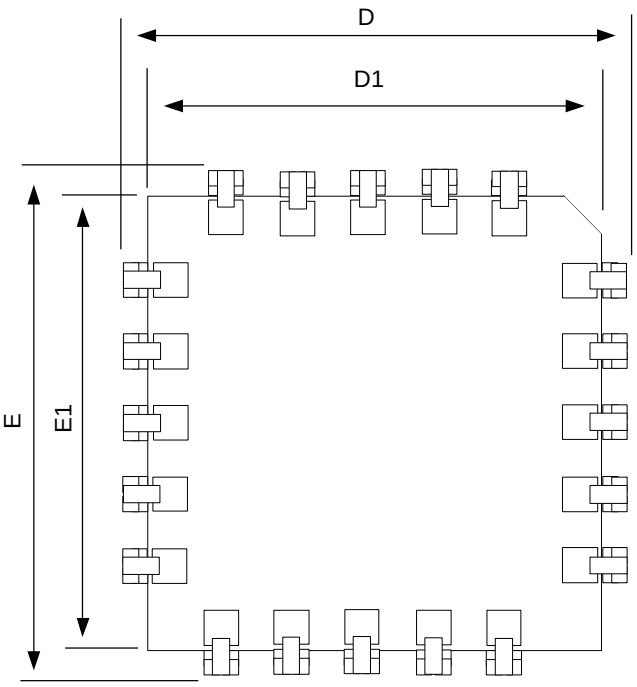
AC Specifications

Parameter	Min	Max	Notes
CLK period	54 ns	250 ns	Divide by Two
CLK period	54 ns	108 ns	No Divide by
CLK Low Time	25 ns		
CLK High Time	25 ns		
CLK Rise Time		10 ns	Divide by Two Measured between 0.3 * VDD and 0.7 * VDD
CLK Fall Time		10 ns	Divide by Two Measured between 0.3 * VDD and 0.7 * VDD
CLK Rise Time		15 ns	No Divide by
CLK Fall Time		15 ns	No Divide by
Crystal Frequency	1 Mhz	20 Mhz	
Reset Width	8 * Clock Period		
RTS/DTR Low Setup to Reset inactive	6 * Clock Period		
RTS/DTR Low Hold after Reset inactive		Clock Period – 20 ns	
RDn Active Width	2* clock period + 65 ns		
Address/CSn Setup Time to RDn Active	7 ns		
Address/CSn Hold after RDn Inactive	0 ns		
RDn or WRn Inactive to Active Delay	Clock Period + 15 ns		
Data Out Float Delay after RDn Inactive		40 ns	
WRn Active Width	2 * Clock Period + 15 ns		
Address CSn Setup Time to WRn Active	7 ns		
Address and CSn hold Time after WRn	0 ns		
Data in Setup Time to WRn Inactive	90 ns		
Data In Hold Time after WRn Inactive	12 ns		
SCLK Period	216 ns		16x Clocking Mode
SCLK Period	3500 ns		1x Clocking Mode
RXD Setup Time to SCLK High	250 ns		
RXD Hold Time after SCLK High	250 ns		
TXD Valid after SCLK Low		170 ns	
TXD Delay after RXD		170 ns	Remote Loopback

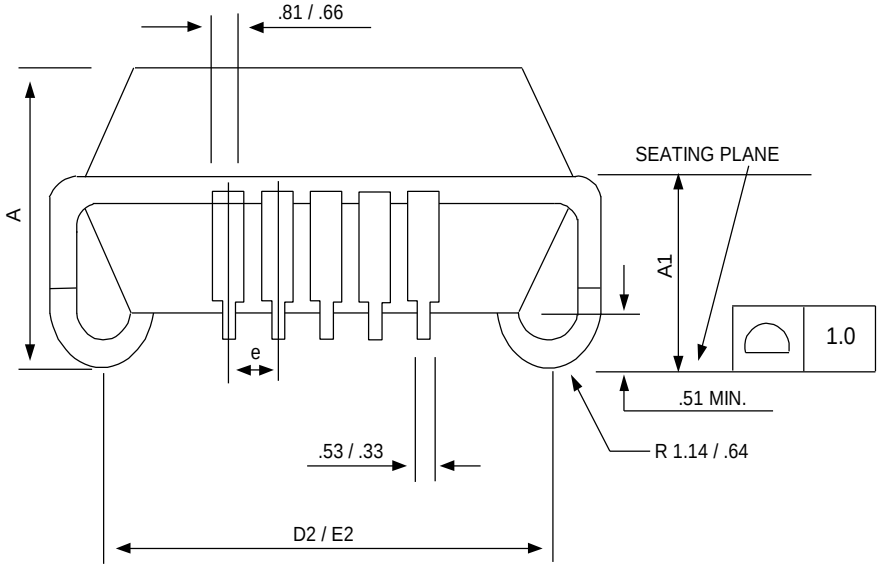
PLCC Packaging Dimensions (Theta J = 53)



TOP VIEW



BOTTOM VIEW

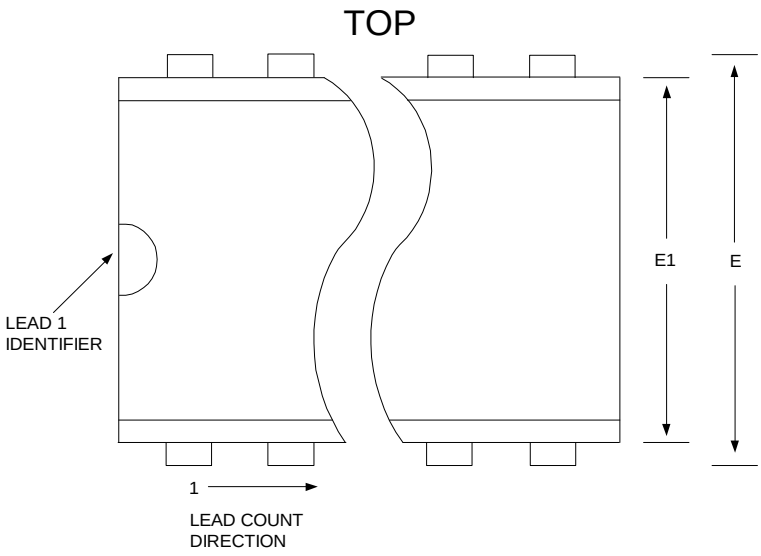


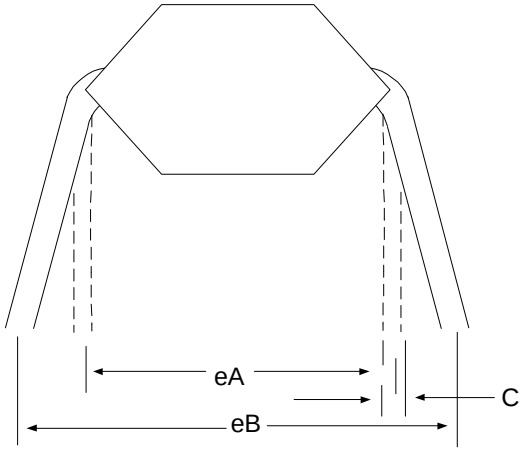
SIDE VIEW

LEAD COUNT

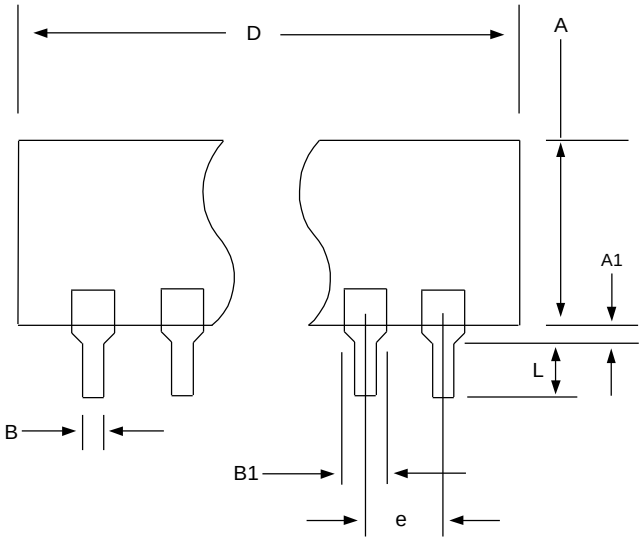
Symbol	28 (in Millimeters)	
	MIN	MAX
A	4.20	4.57
A1	2.29	3.04
D1	11.43	11.58
D2	9.91	10.92
D3	7.62 BSC	
E1	11.43	11.58
E2	9.91	10.92
E3	7.62 BSC	
e	1.27 BSC	
D	12.32	12.57
E	12.32	12.57

PDIP Packaging Dimensions (Theta J = 51)





SIDE VIEW (WIDTH)



SIDE VIEW (LENGTH)

Lead Count

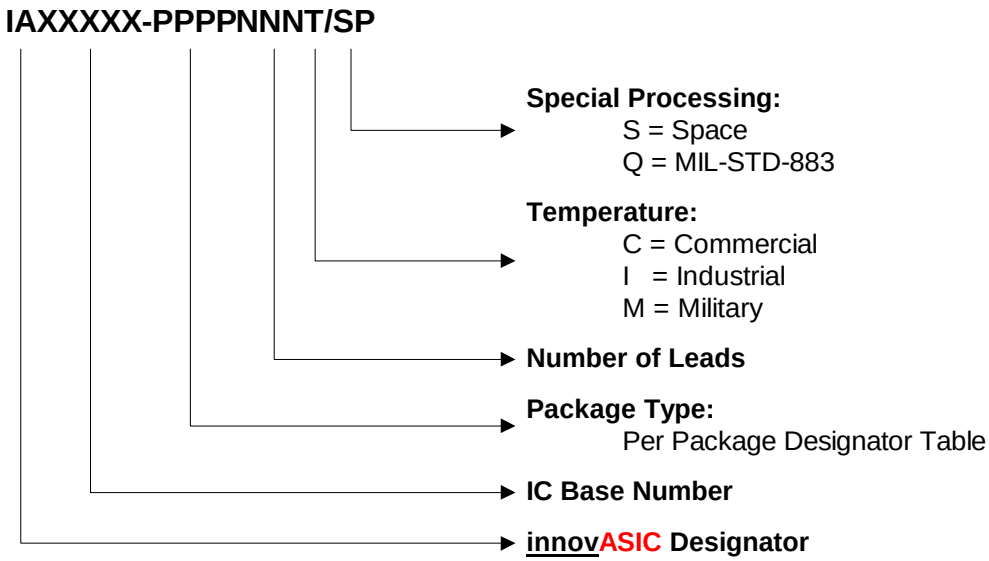
Symbol	28 (in Inches)	
	MIN	MAX
A	-	.200
A1	.015	-
B	.015	.020
B1	.050	.070
C	.008	.012
D	1.380	1.470
E	.580	.610
E1	.520	.560
e	.100 TYP	
eA	.580	-
eB	-	.686
L	.100 MIN	
B2	-	-
S	-	-

Package Options

The IA82510 is available in two package styles as shown in the table below.

Package Type	Environment	Order Number
28 Lead Ceramic DIP, 600 mil wide	Military	IA82510-CD28M
28 Lead Plastic DIP, 600 mil wide	Industrial	IA82510-PDW28I
	Commercial	IA82510-PDW28C
28 Lead Ceramic Leaded Chip Carrier	Military	IA82510-CLC28M
28 Lead Ceramic Leadless Chip Carrier	Military	IA82510-CLL28M
28 Lead Plastic Leaded Chip Carrier	Industrial	IA82510-PLC28I
	Commercial	IA82510-PLC28C

The following diagram depicts the **innov**ASIC Product Identification Number.



Package Designator Table

Package Type	innovASIC Designator
Ceramic side brazed Dual In-line	CDB
Cerdip with window	CDW
Ceramic leaded chip carrier	CLC
Cerdip without window	CD
Ceramic leadless chip carrier	CLL
PLCC	PLC
Plastic DIP standard (300 mil)	PD
Plastic DIP standard (600 mil)	PDW
Plastic metric quad flat pack	PQF
Plastic thin quad flat pack	PTQ
Skinny Cerdip	CDS
Small outline plastic gull-wing(150 mil body)	PSO
Small outline medium plastic gull-wing (207 mil body)	PSM
Small outline narrow plastic gull wing (150 mil body)	PSN
Small outline wide plastic gull wing (300 mil body)	PSW
Skinny Plastic Dip	PDS
Shrink small outline plastic (5.3mm .208 body)	PS
Thin shrink small outline plastic	PTS
Small outline large plastic gull wing (330 mil body)	PSL
Thin small outline plastic gull-wing (8 x 20mm) [TSOP]	PST
PGA	CPGA
BGA	CBGA

Contact **innovASIC** for other package and processing options.

ERRATA

1. *Issue*: RX FIFO Unlock command (RCM x04) generally does not work, because it always increments the RX FIFO write pointer after a LOCK command without transferring data. This command does work when LOCK command, transfer data, UNLOCK commands are executed. This command also, works correctly for the manual or semi-automatic uLAN mode if RX data has been received.

   Workaround: Execute a "Flush RX FIFO" command (via RCM register) after initial configuration in conjunction with the use of RX FIFO Lock/Unlock commands.

2. *Issue*: RX FIFO read pointer inadvertently increments on a read from an empty RX FIFO.

   Workaround: Execute a "Flush RX FIFO" command (via RCM register) after such RX FIFO reads, avoiding reads from RX FIFO when empty.

3. *Issue*: Device does not operate above 8 MHz in divide-by-one mode and strapped to an external clock source (non-crystal). Under normal conditions the system clock is divided by two; however, the user may disable divide by two via a hardware strapping option on the DTRn pin.

   Workaround: Switch to divide-by-two mode using 2X clock input. The hardware strapping option is similar to the one used on the RTSn pin. It is forbidden to strap both DTRn and RTSn.

4. *Issue*: Setting CLCF to x30, which effectively generates the TX clock from the incoming SCLK signal, in conjunction with PMD RI/SCLK set to RI, kills all transmits.

   Workaround: Set correct configuration for PMD allows TX clock generation.

5. *Issue*: Device does not operate using an external Crystal Oscillator.

   Workaround: Add 1 M Ω resistor across X1 and X2 pins.

6. *Issue*: Receiving streamed data appears to have corrupt data, no interrupt when first stop bit is complete, but random interrupts in message data when connected to some modems.

   Workaround: Configure external modem to transmit two stop bits.

7. *Issue*: Transmission of streamed data does not return interrupt.

   Workaround: : Reset logic with write to TX data or avoid stray reads of GIR

8. *Issue*: Transmission of streamed data does not return interrupt.

   Workaround: : Reset logic with write to TX data or avoid stray reads of GIR