

G E SOLID STATE

## Dual J-K Flip-Flop w/RESET

**CD54HC107/3A**  
**CD54HCT107/3A**

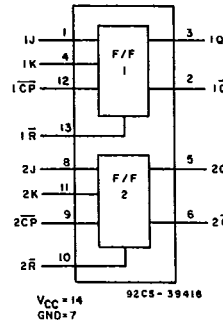
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The RCA-CD54HC107 and CD54HCT107 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and  $\bar{Q}$  outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low-level input.

This device is functionally identical to the HC/HCT73 but differs in terminal assignment and in some parametric limits.

The 54HCT logic family is functionally as well as pin-compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

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### Package Specifications

See Section 11, Fig. 10

### Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS	TEST CONDITIONS								UNITS	
	HC/HCT				$V_{IN}$		LIMITS			
	$V_{DD}$	$V_O$	$I_O$	$V_{CC}$ or GND	$V_{IL}$ or $V_{IH}$	$V_{IL}$ or $V_{IH}$	MIN.	MAX.		
Quiescent Device Current $I_{CC}$	25°C	6	—	—	6, 0	—	—	—	4•	$\mu A$
	-55°C	6	—	—	6, 0	—	—	—	80•	
	+125°C	6	—	—	6, 0	—	—	—	80•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

### HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.3

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 360  $\mu A$  max. @ 25°C.

### Switching Speed (Limits with black dots (•) are tested 100%)

SWITCHING CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r, t_f = 6$  ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_{CC}$ V	LIMITS								UNITS
			25°C				-55°C to +125°C				
			HC		HCT		54HC		54HCT		
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.				
Propagation Delay Time $\overline{CP}$ to Q	$t_{PLH}$ $t_{PHL}$	2	—	170	—	—	—	255	—	—	ns
		4.5	—	34•	—	43•	—	51•	—	65•	
		6	—	29	—	—	—	43	—	—	
$\overline{CP}$ to Q	$t_{PLH}$ $t_{PHL}$	2	—	170	—	—	—	255	—	—	
		4.5	—	34	—	40	—	51	—	60	
		6	—	29	—	—	—	43	—	—	
$\bar{R}$ to Q, $\bar{Q}$	$t_{TLH}$ $t_{THL}$	2	—	155	—	—	—	235	—	—	
		4.5	—	31•	—	38•	—	47•	—	57•	
		6	—	26	—	—	—	40	—	—	
Output Transition Time	$t_{TLH}$ $t_{THL}$	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—	10	pF

**CD54HC107/3A**  
**CD54HCT107/3A**

T-46-07-07

**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>CC</sub> (6V)	OPEN	GROUND	V <sub>CC</sub> (6V)
CD54HC/HCT107	2,3,5,6	1,4,7-13	14	2,3,5,6	7	1,4,8-14
Dynamic	OPEN	GROUND	1/2 V <sub>CC</sub> (3V)	V <sub>CC</sub> (6V)	OSCILLATOR	
CD54HC/HCT107	—	7	2,3,5,6	1,4,8,10,11,13,14	50 kHz	25 kHz

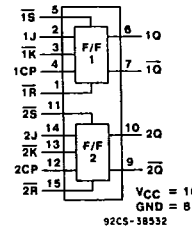
NOTE: Each pin except V<sub>CC</sub> and Gnd will have a resistor of 2k-47k ohms.

**CD54HC109/3A**  
**CD54HCT109/3A**

**Dual J-K̄ Flip-Flop w/SET and RESET**

The RCA-CD54HC109 and CD54HCT109 are dual J-K̄ flip-flops with set and reset. The flip-flop changes state with the positive transition of Clock (1CP and 2CP).

The flip-flop is set and reset by active-low  $\bar{S}$  and  $\bar{R}$ , respectively. A low on both the set and reset inputs simultaneously will force both Q and  $\bar{Q}$  outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.



FUNCTIONAL DIAGRAM

**Package Specifications**

See Section 11, Fig. 11

**Static Electrical Characteristics** (Limits with black dots (•) are tested 100%)

CHARACTERISTICS	TEST CONDITIONS								UNITS	
	V <sub>DD</sub>	HC/HCT			V <sub>IN</sub>		LIMITS			
		V <sub>O</sub>	I <sub>O</sub>	V <sub>CC</sub> or GND	HC V <sub>IL</sub> or V <sub>IH</sub>	HCT V <sub>IL</sub> or V <sub>IH</sub>	MIN.	MAX.		
Quiescent Device Current I <sub>CC</sub>	25°C	6	—	—	6, 0	—	—	—	4•	μA
	-55°C	6	—	—	6, 0	—	—	—	80•	
	+125°C	6	—	—	6, 0	—	—	—	80•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
All	0.3

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

**CD54HC109/3A**  
**CD54HCT109/3A**

T-46-07-07

**Switching Speed** (Limits with black dots (•) are tested 100%.)

**SWITCHING CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 6 \text{ ns}$ )

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_{CC}$ V	LIMITS								UNITS
			25°C				-55°C to +125°C				
			HC		HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay $CP \rightarrow Q, \bar{Q}$	$t_{PLH}$ $t_{PHL}$	2	—	175	—	—	—	265	—	—	ns
		4.5	—	35•	—	40•	—	53•	—	60•	
		6	—	30	—	—	—	45	—	—	
$\bar{S} \rightarrow Q$	$t_{PLH}$	2	—	120	—	—	—	180	—	—	
		4.5	—	24•	—	30•	—	36•	—	45•	
		6	—	20	—	—	—	31	—	—	
$\bar{S} \rightarrow \bar{Q}$	$t_{PHL}$	2	—	155	—	—	—	235	—	—	
		4.5	—	31	—	45	—	47	—	68	
		6	—	26	—	—	—	40	—	—	
$\bar{R} \rightarrow Q$	$t_{PHL}$	2	—	185	—	—	—	280	—	—	
		4.5	—	37	—	45	—	56	—	68	
		6	—	31	—	—	—	48	—	—	
$\bar{R} \rightarrow \bar{Q}$	$t_{PLH}$	2	—	170	—	—	—	255	—	—	
		4.5	—	34•	—	37•	—	51•	—	56•	
		6	—	29	—	—	—	43	—	—	
Transition Times	$t_{TLH}$ $t_{THL}$	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—	10	pF

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**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	$V_{CC}$ (6V)	OPEN	GROUND	$V_{CC}$ (6V)
CD54HC/HCT109	6,7,9,10	1-5,8,11-15	16	6,7,9,10	8	1-5,11-16
Dynamic	OPEN	GROUND	$1/2 V_{CC}$ (3V)	$V_{CC}$ (6V)	OSCILLATOR 50 kHz 25 kHz	
CD54HC/HCT109	—	8	6,7,9,10	1-3,5,11, 13-16	4,12	—

NOTE: Each pin except  $V_{CC}$  and Gnd will have a resistor of 2k-47k ohms.

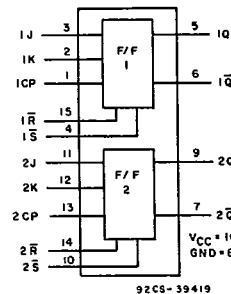
**Dual J-K Flip-Flop w/SET and RESET**

**CD54HC112/3A**  
**CD54HCT112/3A**

The RCA-CD54HC112 and CD54HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and  $\bar{Q}$  outputs. They change state on the negative-going transition of the clock pulse. Set and reset are accomplished asynchronously by low-level inputs.

The 54HCT logic family is functionally as well as pin compatible with the standard 54LS logic family.



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FUNCTIONAL DIAGRAM

**Package Specifications**

See Section 11, Fig. 11

**CD54HC112/3A**  
**CD54HCT112/3A**

T-46-07-07

**Static Electrical Characteristics** (Limits with black dots (•) are tested 100%)

CHARACTERISTICS	TEST CONDITIONS								UNITS	
	HC/HCT				V <sub>IN</sub>		LIMITS			
	V <sub>DD</sub>	V <sub>O</sub>	I <sub>O</sub>	V <sub>CC</sub> OR GND	HC V <sub>IL</sub> or V <sub>IH</sub>	HCT V <sub>IL</sub> or V <sub>IH</sub>	MIN.	MAX.		
Quiescent Device Current I <sub>CC</sub>	25°C	6	—	—	6, 0	—	—	—	4•	μA
	-55°C	6	—	—	6, 0	—	—	—	80•	
	+125°C	6	—	—	6, 0	—	—	—	80•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
1S, 2S	0.5
1K, 2K	0.6
1R, 2R	0.65
1J, 2J, 1CP, 2CP	1

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

**Switching Speed** (Limits with black dots (•) are tested 100%).

SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V <sub>CC</sub> V	LIMITS								UNITS
			25°C				-55°C to +125°C				
			HC		HCT		54HC		54HCT		
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.				
Propagation Delay $\overline{CP}$ to Q, $\overline{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	175	—	—	—	—	265	—	ns
		4.5	—	35•	—	35•	—	53•	—	53•	
		6	—	30	—	—	—	45	—	—	
$\overline{S}$ to Q, $\overline{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	155	—	—	—	235	—	—	
		4.5	—	31•	—	32•	—	47•	—	48•	
		6	—	26	—	—	—	40	—	—	
$\overline{R}$ to Q, $\overline{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	180	—	—	—	270	—	—	
		4.5	—	36•	—	37•	—	54•	—	56•	
		6	—	31	—	—	—	46	—	—	
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	—	10	—	10	pF

**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>CC</sub> (6V)	OPEN	GROUND	V <sub>CC</sub> (6V)
CD54HC/HCT112	5-7,9	1-4,8,10-15	16	5-7,9	8	1-4,10-16
Dynamic	OPEN	GROUND	1/2 V <sub>CC</sub> (3V)	V <sub>CC</sub> (6V)	OSCILLATOR	
CD54HC/HCT112	—	8	5-7,9	2-4,10-12, 14-16	50 kHz 1,13	25 kHz —

NOTE: Each pin except V<sub>CC</sub> and Gnd will have a resistor of 2k-47k ohms.

## Dual Retriggerable Monostable Multivibrator w/RESET

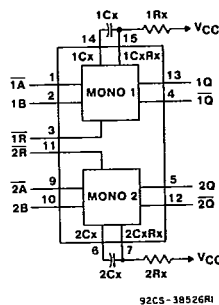
CD54HC123/3A  
CD54HCT123/3A

T-51-19

The RCA-CD54HC123 and CD54HCT123 are dual monostable multivibrators with resets. They are retriggerable and can be triggered by a negative-to-positive reset pulse. An external resistor ( $R_x$ ) and an external capacitor ( $C_x$ ) control the timing and accuracy for the circuit. Adjustment of  $R_x$  and  $C_x$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. Pulse triggering on the  $\bar{A}$  and B inputs occurs at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

Once triggered, the output pulse width may be extended by retriggering inputs  $\bar{A}$  and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing-edge triggering ( $\bar{A}$ ) and leading-edge triggering (B) inputs are provided for triggering from either edge of the input pulse. If either Mono is not used, each input on the unused device ( $\bar{A}$ , B and  $\bar{R}$ ) must be terminated high or low.

The minimum value of external resistance,  $R_x$ , is typically 500  $\Omega$ . The minimum value external capacitance,  $C_x$ , is 0 pF. The calculation for the pulse width is  $t_w = 0.45 R_x C_x$  at  $V_{cc} = 5$  V.



FUNCTIONAL DIAGRAM

### Package Specifications

See Section 11, Fig. 11

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### Static Electrical Characteristics (Limits with black dots (\*) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS								UNITS
		HC/HCT				$V_{IN}$		LIMITS		
		$V_{DD}$	$V_O$	$I_O$	$V_{CC}$ or GND	$V_{IL}$ or $V_{IH}$	$V_{IL}$ or $V_{IH}$	MIN.	MAX.	
Quiescent Device Current $I_{CC}$	25°C	6	—	—	6, 0	—	—	—	8*	$\mu A$
	-55°C	6	—	—	6, 0	—	—	—	160*	
	+125°C	6	—	—	6, 0	—	—	—	160*	

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All Inputs	0.35

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 360  $\mu A$  max. @ 25°C.

### Switching Speed (Limits with black dots (\*) are tested 100%).

SWITCHING CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r, t_f = 6$  ns,  $R_x = 10$  K $\Omega$ ,  $C_x = 0$ )

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_{CC}$ V	LIMITS								UNITS
			25°C				-55°C to +125°C				
			HC		HCT		54HC		54HCT		
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.				
Trigger Propagation Delay, $\bar{A}$ , B, $\bar{R}$ to Q	$t_{PLH}$	2	—	300	—	—	—	450	—	—	ns
		4.5	—	60*	—	60*	—	90*	—	90*	
		6	—	51	—	—	—	76	—	—	
$\bar{A}$ , B, $\bar{R}$ to $\bar{Q}$	$t_{PHL}$	2	—	320	—	—	—	480	—	—	ns
		4.5	—	64*	—	68*	—	96*	—	102	
		6	—	54	—	—	—	82	—	—	
Reset Propagation Delay, $\bar{R}$ to Q or $\bar{Q}$	$t_{PHL}$ $t_{PLH}$	2	—	215	—	—	—	325	—	—	ns
		4.5	—	43*	—	48*	—	65*	—	72*	
		6	—	37	—	—	—	55	—	—	
Output Transition Time	$t_{TLH}$ $t_{THL}$	2	—	75	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—	10	pF

**CD54HC123/3A**  
**CD54HCT123/3A**

T-51-19  
 T-43-21

**Burn-In Test-Circuit Connections**

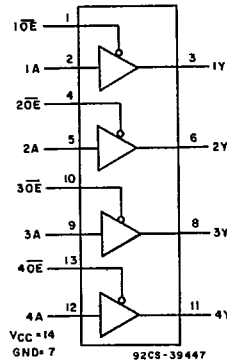
Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>CC</sub> (6V)	OPEN	GROUND	V <sub>CC</sub> (6V)
CD54HC/HCT123	4-7,12-15	1-3,8-11	16	4-7,12-15	8	1-3,9-11,16
Dynamic	OPEN	GROUND	1/2 V <sub>CC</sub> (3V)	V <sub>CC</sub> (6V)	OSCILLATOR	
CD54HC/HCT123	—	1,6,8,9,14	4,5,12,13	7,15,16	50 kHz	25 kHz
					2,3,10,11	—

NOTE: Each pin except V<sub>CC</sub> and Gnd will have a resistor of 2k-47k ohms.

**CD54HC125/3A**  
**CD54HCT125/3A**

**Quad 3-State Buffer**

The RCA-CD54HC125 and CD54HCT125 contain four independent three-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high-impedance state.



FUNCTIONAL DIAGRAM

**Package Specifications**

See Section 11, Fig. 10

**Static Electrical Characteristics** (Limits with black dots (•) are tested 100%)

CHARACTERISTICS	TEST CONDITIONS								UNITS	
	V <sub>DD</sub>	V <sub>O</sub>	I <sub>O</sub>	V <sub>CC</sub> or GND	V <sub>IN</sub>		LIMITS			
					HC or V <sub>IH</sub>	HCT or V <sub>IH</sub>	MIN.	MAX.		
Quiescent Device Current I <sub>CC</sub>	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C	6	—	—	6, 0	—	—	—	160•	
	+125°C	6	—	—	6, 0	—	—	—	160•	

**HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
nA, nOE	1

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

**CD54HC125/3A**  
**CD54HCT125/3A**

T-43-21

**Switching Speed** (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r, t_f = 6$  ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_{CC}$ V	LIMITS								UNITS		
			25°C				-55°C to +125°C						
			HC		HCT		54HC		54HCT				
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.						
Propagation Delay Time nA to nY	$t_{PLH}$ $t_{PHL}$	2	—	100	—	—	—	—	150	—	ns		
		4.5	—	20•	—	25•	—	30•	—	38•			
		6	—	17	—	—	—	26	—	—			
Enable Delay Time	$t_{PZH}$ $t_{PZL}$	2	—	125	—	—	—	190	—	ns			
		4.5	—	25•	—	25•	—	38•	—			38•	
		6	—	21	—	—	—	32	—			—	
Disable Delay Time	$t_{PHZ}$ $t_{PLZ}$	2	—	125	—	—	—	190	—			ns	
		4.5	—	25•	—	28•	—	38•	—				42•
		6	—	21	—	—	—	32	—				—
Output Transition Time	$t_{TLH}$ $t_{THL}$	2	—	60	—	—	—	90	—				ns
		4.5	—	12	—	12	—	18	—		18		
		6	—	10	—	—	—	15	—		—		
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—		pF		
3-State Output Capacitance	$C_o$	—	—	20	—	20	—	20	—				

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**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

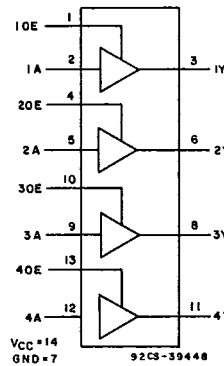
Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	$V_{CC}$ (6V)	OPEN	GROUND	$V_{CC}$ (6V)
CD54HC/HCT125	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	OPEN	GROUND	$1/2 V_{CC}$ (3V)	$V_{CC}$ (6V)	OSCILLATOR	
CD54HC/HCT125	—	7	3,6,8,11	14	50 kHz 1,2,4,5,9,10, 12,13	25 kHz —

NOTE: Each pin except  $V_{CC}$  and Gnd will have a resistor of 2k-47k ohms.

**Quad 3-State Buffer**

The RCA-CD54HC126 and CD54HCT126 contain four independent three-state buffers, each having its own output enable input, which when "LOW" puts the output in the high-impedance state.

**CD54HC126/3A**  
**CD54HCT126/3A**



FUNCTIONAL DIAGRAM

**Package Specifications**

See Section 11, Fig. 10

**CD54HC126/3A**  
**CD54HCT126/3A**

**Static Electrical Characteristics** (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS								UNITS
		HC/HCT				V <sub>IN</sub>		LIMITS		
		V <sub>DD</sub>	V <sub>O</sub>	I <sub>O</sub>	V <sub>CC</sub> OR GND	HC V <sub>IL</sub> or V <sub>IH</sub>	HCT V <sub>IL</sub> or V <sub>IH</sub>	MIN.	MAX.	
Quiescent Device Current I <sub>CC</sub>	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C	6	—	—	6, 0	—	—	—	160•	
	+125°C									

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
nA, nOE	1

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

**Switching Speed** (Limits with black dots (•) are tested 100%)

SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V <sub>CC</sub> V	LIMITS								UNITS
			25°C				-55°C to +125°C				
			HC		HCT		54HC		54HCT		
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.				
Propagation Delay Data to Outputs	t <sub>PLH</sub>	2	—	100	—	—	—	150	—	—	ns
	t <sub>PHL</sub>	4.5	—	20•	—	24•	—	30•	—	36•	
		6	—	17	—	—	—	36	—	—	
Enable Delay Times	t <sub>PZH</sub>	2	—	125	—	—	—	190	—	—	ns
	t <sub>PZL</sub>	4.5	—	25•	—	25•	—	38•	—	38•	
		6	—	21	—	—	—	32	—	—	
Disable Delay Times	t <sub>PHZ</sub>	2	—	125	—	—	—	190	—	—	ns
	t <sub>PLZ</sub>	4.5	—	25•	—	28•	—	38•	—	42•	
		6	—	21	—	—	—	32	—	—	
Output Transition Time	t <sub>TLH</sub>	2	—	60	—	—	—	90	—	—	ns
	t <sub>THL</sub>	4.5	—	12	—	12	—	18	—	18	
		6	—	10	—	—	—	15	—	—	
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	20	—	20	—	20	—	20	

**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>CC</sub> (6V)	OPEN	GROUND	V <sub>CC</sub> (6V)
CD54HC/HCT126	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	OPEN	GROUND	1/2 V <sub>CC</sub> (3V)	V <sub>CC</sub> (6V)	OSCILLATOR	
					50 kHz	25 kHz
CD54HC/HCT126	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—

NOTE: Each pin except V<sub>CC</sub> and Gnd will have a resistor of 2k-47k ohms.