Sample-and-hold amplifiers

LF198/LF298/LF398

DESCRIPTION

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1µF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

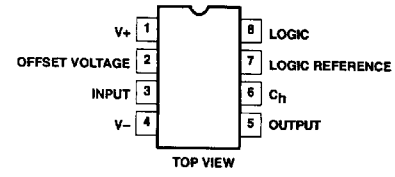
Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in 8-pin plastic DIP, 8-pin Cerdip, and 14-pin plastic SO packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Less than 10µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at CH=0.01µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

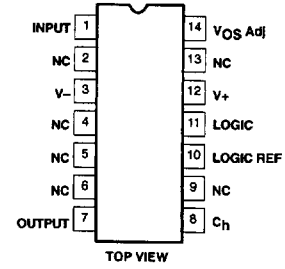
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

D[1] Package



TOP VIEW

NOTE:
1 SO and non-standard pinouts.

APPLICATION

- The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LF198FE	0580A
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	LF398D	0175D
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	LF398FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LF398N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-25°C to +85°C	LF298FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LF298N	0404B

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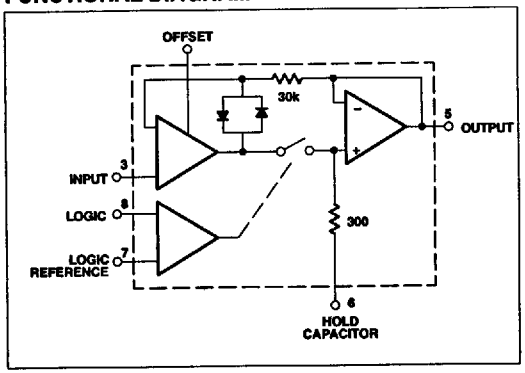
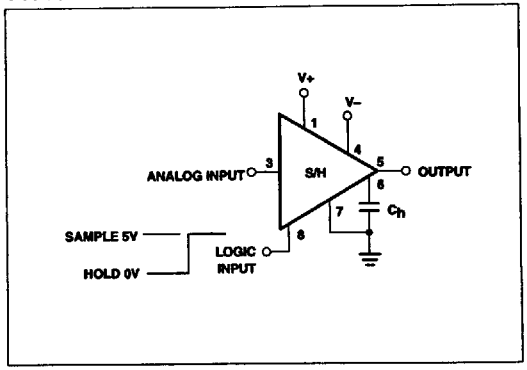
FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_A=25°C (still-air)[3]		
	F package	780	mW
	N package	1160	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	LF198	-55 to +125	°C
	LF298	-25 to +85	°C
	LF398	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, -30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

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DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply: unit is in "sample" mode; V_S = ±15V; T_J = 25°C; -11.5V3 V_{IN} ≤ +11.5V; C_H=0.01µF; and R_L = 10kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	T_J=25°C Full temperature range		1	3 5		2	7 10	mV
I_{BIAS}	Input bias current[4]	T_J=25°C Full temperature range		5	25 75		10	50 100	nA
	Input impedance	T_J=25°C		10^{10}			10^{10}		Ω
	Gain error	T_J=25°C, R_L=10k Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	%
	Feedthrough attenuation ratio at 1kHz	T_J=25°C, C_h=0.01µF	86	96		80	90		dB
	Output impedance	T_J=25°C, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω
	"HOLD" step[2]	T_J=25°C, C_h=0.01µF, V_{OUT}=0		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	T_J ≤ 25°C		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	T_J = 25°C		2	10		2	10	µA
	Leakage current into hold capacitor[4]	T_J=25°C, "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	ΔV_{OUT}=10V, C_h=1000pF C_h=0.01µF		4 20			4 20		µs
	Hold capacitor charging current	V_{IN}-V_{OUT}=2V		5			5		mA
	Supply voltage rejection ratio	V_{OUT}=0	80	110		80	110		dB
	Differential logic threshold	T_J=25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S=±15V, T_J=25°C, -11.5V ≤ V_{IN} ≤ +11.5V, C_h = 0.01µF, and R_L = 10kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.

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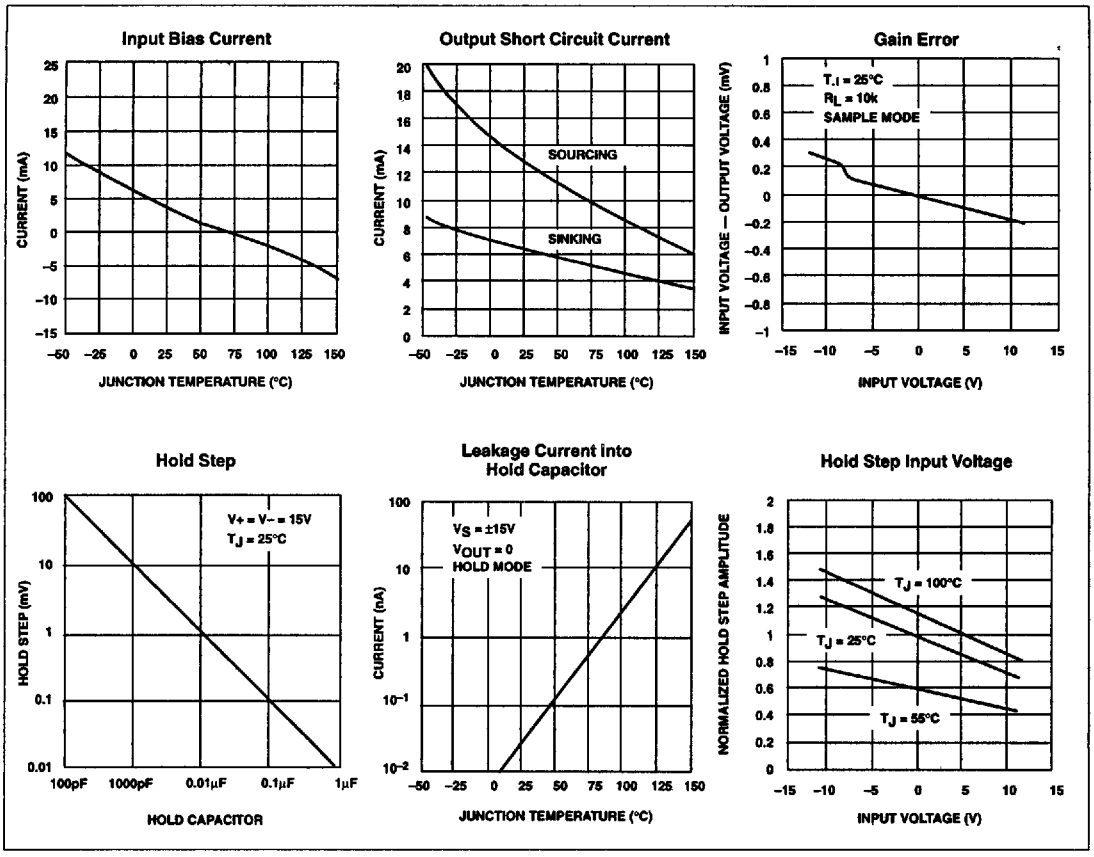
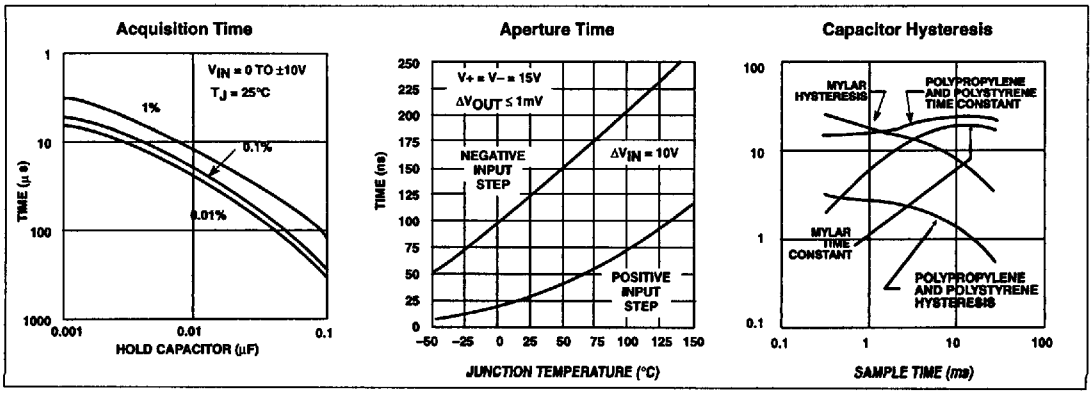
TYPICAL DC PERFORMANCE CHARACTERISTICS



TYPICAL AC PERFORMANCE CHARACTERISTICS



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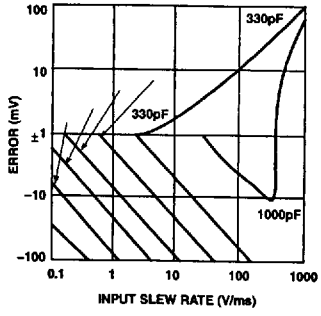
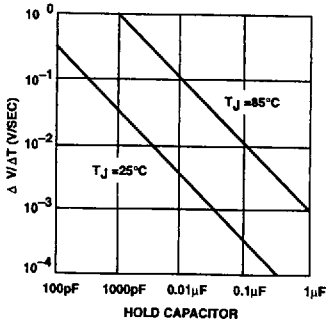
TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

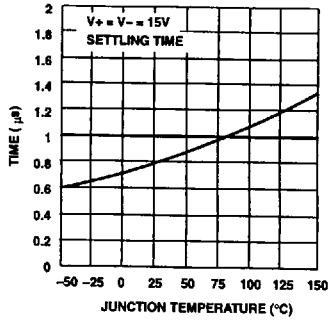
Dynamic Sampling Error



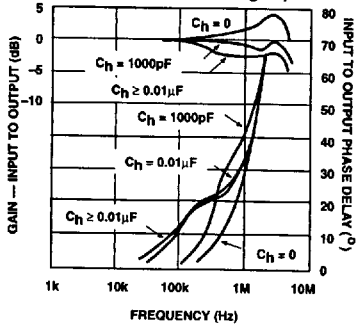
Output Droop Rate



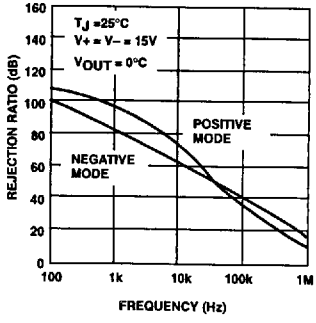
'Hold' Sampling Time



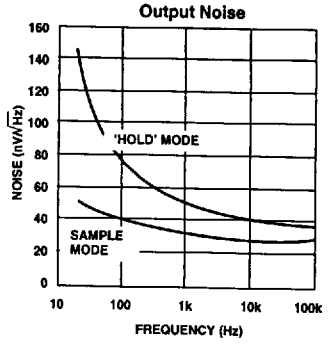
Phase And Gain
(Input to Output, Small-Signal)



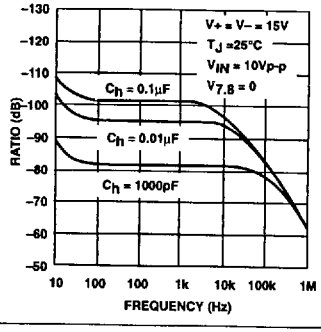
Power Supply Rejection



Output Noise



Feedthrough Rejection Ratio
(Hold Mode)



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