SERTECH LABS
580 Pleasant Street
Watertown, MA 02172
(617) 924-9280

TSC355
Timer

Features

- Timing – From Microseconds to Hours
- CMOS and HiNIL Compatible Inputs/Outputs
- High Current Drive Capability – 100 mA Source or Sink
- No Current Spiking on Output
- Pin Compatible With 555 Timer

General Description

The Teledyne Semiconductor 355 Timer is designed to be used as an accurate time delay device or as an astable oscillator in industrial control environments. Timing intervals of the 355 Timer are controlled by an external RC network.

The 355 triggers on the negative edge of the low going trigger pulse. Trigger pulse width must be shorter than the timing interval set by the RC combination. If the trigger is held low, the output will remain high until the trigger is driven high again.

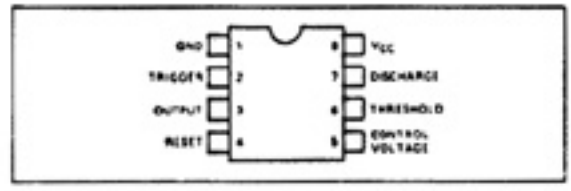
Typical Applications

Time Delay Generation
Clock Generation
Pulse Generation
Pulse Shaping
Pulse Width Modulation
Missing Pulse Detector

Connection Diagram

Order Part Numbers:

L Package	J Package
8-Pin Ceramic DIP	8-Pin Plastic DIP
(0°C ≤ T_A ≤ 70°C)	(0°C ≤ T_A ≤ 70°C)
355 AL/CL	355 AJ/CJ

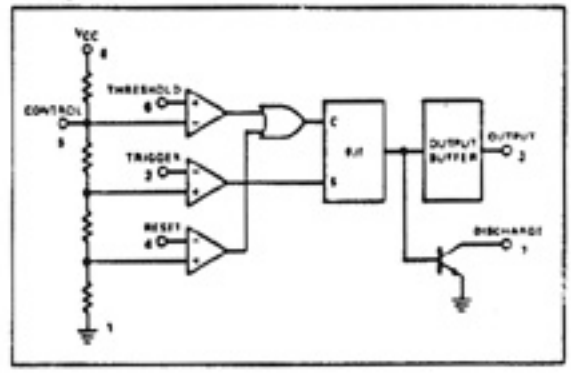


Absolute Maximum Ratings

Continuous Supply Voltage		16.5V
Pulsed Supply Voltage (<100ms)		18.0V
Input Voltage (Any Input)		−0.5V to +18V
Surge Sink Current (100ms at T_A = 25°C)		150mA
Storage Temperature	(L Package)	−65°C to +150°C
	(J Package)	−55°C to +100°C
Lead Temperature (1/16 inch from case, 10 seconds max)		300°C

NOTE: Exceeding the **absolute** maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Diagram



Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage	11		16	V
Free Air Operating Temperature Range — T_A	0	25	70	°C

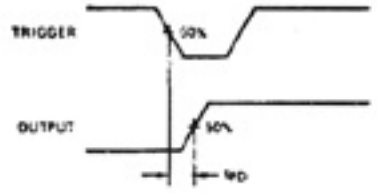
Electrical Characteristics

(Over recommended operating conditions unless otherwise noted).

Parameter	Conditions	Min	Typ	Max	Units
Supply Current	Low State Output (Note 1)				
	V_{CC} = 16V, R_L = ∞		15	20	mA
Timing Error	R_A, R_B = 1KΩ to 100KΩ				
Initial Accuracy	C = 0.1μF		1.0	3.0	%
Drift with Temperature					
(Monostable)	(Note 2)		300		ppm/°C
(Astable)			500		ppm/°C
Drift with Supply Voltage			0.4	0.7	%/V
Threshold Voltage	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Trigger Voltage	V_{CC} = 12V	5.0	5.4	5.8	V
	V_{CC} = 15V	6.3	6.75	7.2	V
Trigger Current	V_{CC} = 16V		1.3	10	μA
Reset Voltage	V_{CC} = 12V	4.3	4.8	5.3	V
	V_{CC} = 15V	5.5	6.0	6.5	V
Reset Current	V_{IN} = 1.5V		1.3	10	μA
Threshold Current	(Note 3) V_{IN} = 11V, V_{CC} = 15V				
	V_{IN} = 9V, V_{CC} = 12V		200	400	nA
Control Voltage Level	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Low Output Voltage	V_{CC} = 15V				
	I_{SINK} = 13mA		1.0	1.5	V
	I_{SINK} = 75mA		1.4	2.0	V
	I_{SINK} = 100mA		2.0		
High Output Voltage	I_{SOURCE} = 50mA				
	V_{CC} = 12V	9.0	10.2		V
	V_{CC} = 15V	12.0	13.2		V
	I_{SOURCE} = 100mA, V_{CC} = 15V		12.7		V
	I_{SOURCE} = 50μA				
	V_{CC} = 11V	9.0	9.4		V
	V_{CC} = 14V	12.0	12.4		V
Discharge Leakage Current	V_{CC} = 16V		20	100	nA
	$V_{DISCHARGE}$ = 15V				
Maximum Oscillator Frequency		100	300		kHz
Propagation Delay (t_{PD})	Trigger to Output		330		nsec

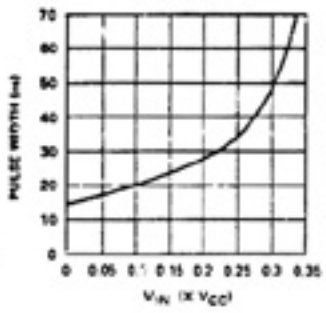
NOTES:
(1) Supply current when output is high is typically 1.0mA less.
(2) Tested at V_{CC} = 12V and V_{CC} = 15V.
(3) This will determine the maximum value of R_A + R_B. For 15V operation the maximum total is R = 10MΩ.

Switching Waveforms

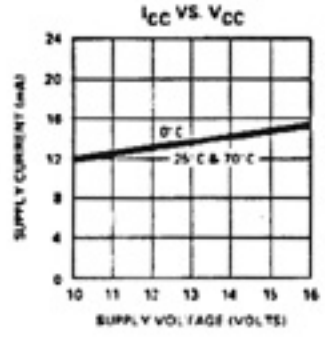


Typical Performance Characteristics

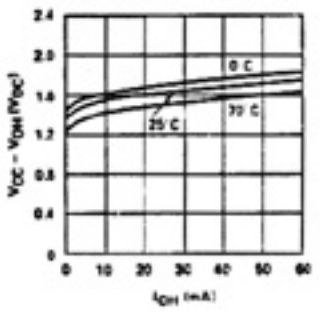
MINIMUM V_{IN} VS. INPUT PULSE WIDTH



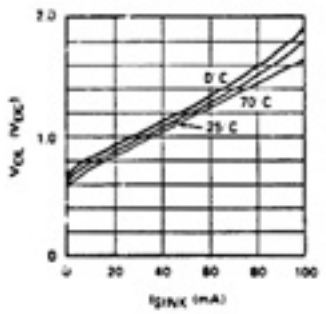
I_{CC} VS. V_{CC}



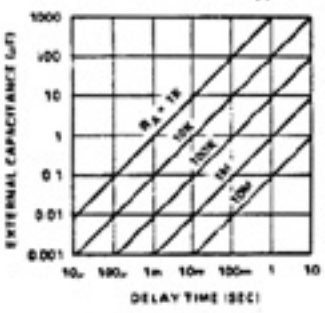
HIGH OUTPUT VOLTAGE



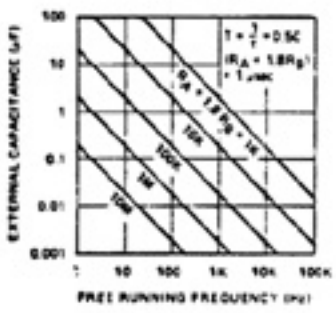
LOW OUTPUT VOLTAGE



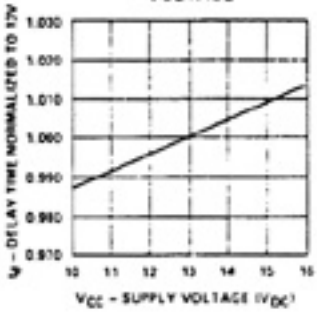
DELAY TIME VS. R_A, C



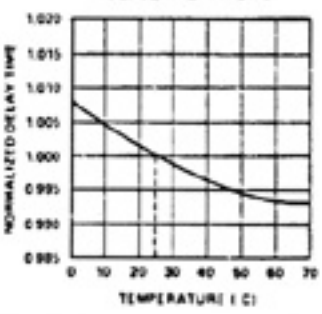
FREE-RUNNING FREQUENCY VS. R, C



DELAY TIME VS SUPPLY VOLTAGE



NORMALIZED DELAY TIME VS. TEMPERATURE



Circuit Control Description

Output, Pin 3 – The output logic level is normally in a "low" state, and goes "high" during the timing cycle.

Trigger, Pin 2 – The timing cycle is initiated by lowering the dc level at the trigger terminal below V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is complete, unless the succeeding trigger overlaps the normal end of the output pulse.

Threshold, Pin 6 – The timing cycle is complete when the voltage level at the threshold reaches $2/3V_{CC}$. At this point, the threshold comparator changes state, resets the internal flip-flop, and initiates the discharge cycle.

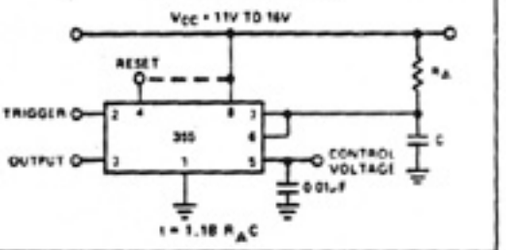
Control or FM, Pin 5 – The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 5. This terminal is internally biased at $2/3V_{CC}$. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. When not in use, the control terminals should be ac grounded through 0.01μF decoupling capacitors.

Discharge, Pin 7 – This terminal corresponds to the collector of the discharge transistor. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

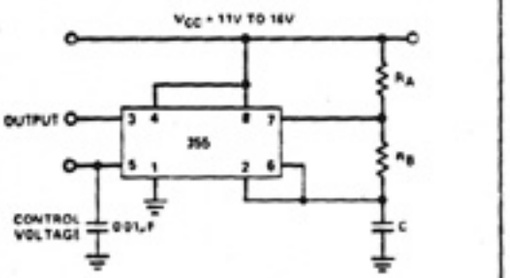
Reset, Pin 4 – The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the reset voltage is applied. When the reset signal is removed, the output remains "low" until retriggered. When not used, the reset terminal should be connected to V_{CC} in order to avoid any possibility of false resetting. When the timing circuit is operated in the astable mode, the reset terminal can be used for "on" and "off" keying of the oscillation.

Applications Information

Monostable Operation



Astable Operation



The charge time (Output High) is: $t_1 = 0.5 (R_A + R_B) C$

The discharge time (Output Low) is: $t_2 = 0.4 (R_B) C$

The total period is:

For < 5kHz: $T = t_1 + t_2 = 0.5 (R_A + 1.8 R_B) C$
For > 5kHz: $T = t_1 + t_2 = [0.5 (R_A + 1.8 R_B) C] + 1\mu sec$

The frequency of oscillation is: $f = \frac{1}{T} = \frac{2}{(R_A + 1.8 R_B) C}$

The duty cycle is: $D = \frac{R_B}{R_A + 1.8 R_B}$