24-Lead Dual-In-Line Plastic Package

H-1888

Single Chip TV Chroma Processor/Demodulator

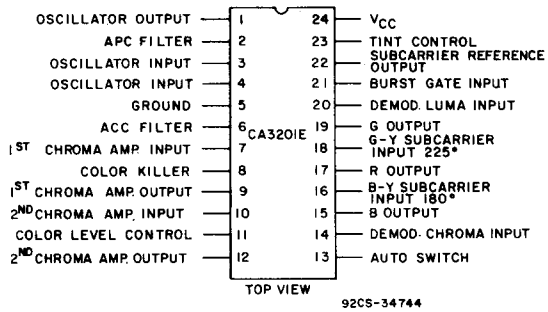
System Features

- *All chroma processing and demodulating circuitry on a single chip in a 24-lead plastic package*
- *Phase-locked subcarrier regeneration*
- *Linear dc controls for chroma gain and tint*
- *Defeatable dynamic "flesh correction"*
- *Three color-difference demodulators*
- *First chroma amplifier with ACC control and killer sensing*
- *Second chroma amplifier with gain control and color killer*
- *Operates from +12 V*
- *An input (Pin 20) is provided that can be used as a variable or fixed voltage source for dc level adjustment of the R-Y, B-Y, and G-Y outputs*

The RCA-CA3201E* is a monolithic silicon integrated circuit that performs the complete chroma processor and demodulating functions for color TV. The single chip contains all the features of the CA3158• chroma processor and the CA3145§ chroma demodulator.

The CA3201E is supplied in a 24-lead dual-in-line plastic package.

*Formerly RCA Developmental No. TA10660.
•The CA3158 is described in RCA data bulletin File No. 1170.
§The CA3145 is described in RCA data bulletin File No. 1175.



TERMINAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	15 V
OPERATING SUPPLY-VOLTAGE RANGE	10.8 to 13.2 V
DEVICE DISSIPATION:	
Up to T_A=55°C	1.25 W
Above T_A=55°C	Derate linearly at 13.3 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

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ELECTRICAL CHARACTERISTICS at T_A=25°C unless otherwise specified (see Fig. 1 for test circuit)

CHARACTERISTIC	TEST CONDITIONS										LIMITS			UNITS
	V1	V2	V3	K1	K2	GND	3.58 MHz	3.56 MHz	Note	Test	Min.	Typ.	Max.	
STATIC														
Supply Current	6.0 V	12.0 V	6.0 V							P24	40	55	70	mA
1st Chroma Bias	↓	↓	↓							P7	2.7	3.3	3.9	V
2nd Chroma Bias				Close						P10	3.1	3.5	3.9	
ACC Out										P6	6.1	7.0	7.9	
APC Out										P2	6.9	7.8	8.7	
Demodulation Bias										P14	3.0	3.4	3.8	
Subcarrier Bias										P18	5.2	5.6	6.0	
Tint Control	6.0 V	12.0 V	6.0 V							P23	7.2	7.7	8.3	
DYNAMIC														
RGB Out	6.0 V	12.0 V	6.0 V			P14	e1 2 Vp-p			P15,17,19	5.4	5.9	6.3	V
ΔR-B, R-G, B-G						↓					—	—	±350	mV
1st Chroma Max. Gain							e2 .25 Vp-p			P9	5.0	6.6	8.3	Ratio
2nd Chroma Max. Gain						P11, P14	e3 .1 Vp-p			P12	14.5	21	26	Ratio
VCO Output						P14	e4 1 Vp-p			P1	530	650	780	mV rms
VCO Nom. Phase Shift					Close	↓	↓			P1-P3	53	72	90	degrees
APC Det. Offset					Close				1	P2	−25	—	+25	mV
Tint Control Out										P23	480	605	730	mV
B-Y Conv. Gain	7.8 V						e1 2 Vp-p	e5 .3 Vp-p		P15/P14	10	15	19	Ratio
R-Y Conv. Gain										P17/P15	70	83	95	%
G-Y Conv. Gain										P19/P15	18	23	28	%
R-Y Output Phase Relative to B-Y Output											85	90	95	degrees
G-Y Output Phase Relative to B-Y Output											−120	−107	−95	degrees

NOTE 1. Reference to P2 without gate pulse.
Typical Pull-In = ± 350 Hz.
Typical Kill Level = 20 dB (100 mVp-p burst reference).

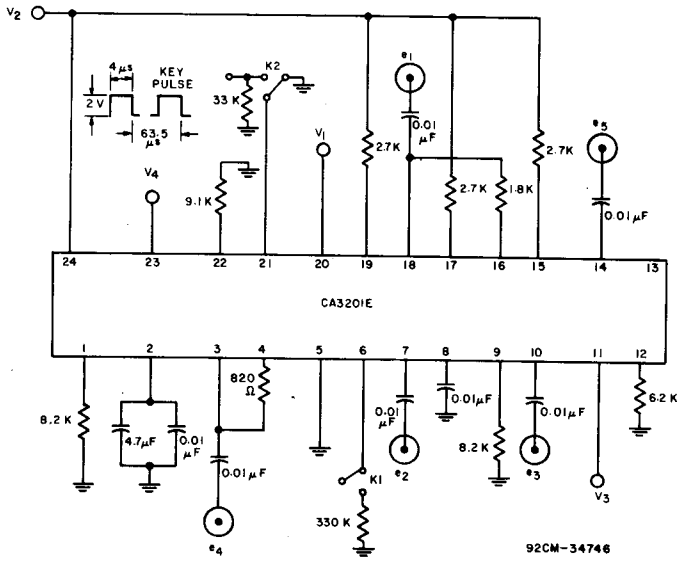

Fig. 1 - Test circuit.

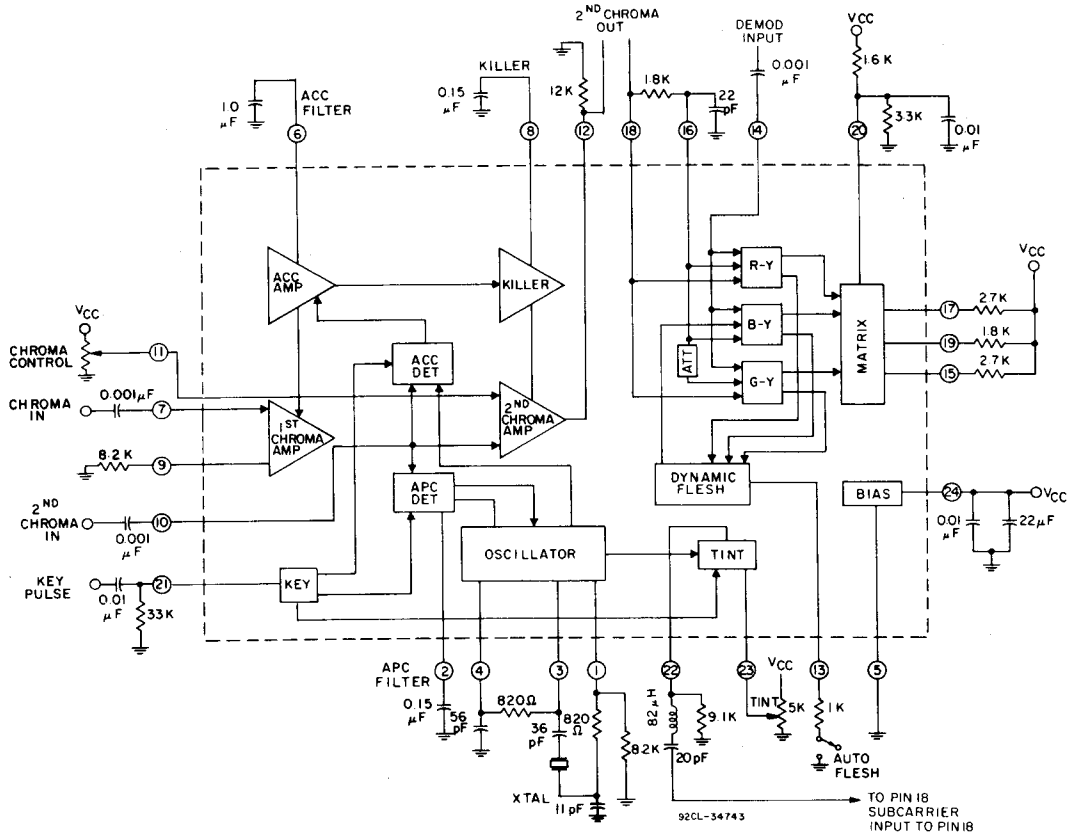

Fig. 2 - Functional block diagram of the CA3201E (see Figs. 3, 4, 7, 8 and 9).

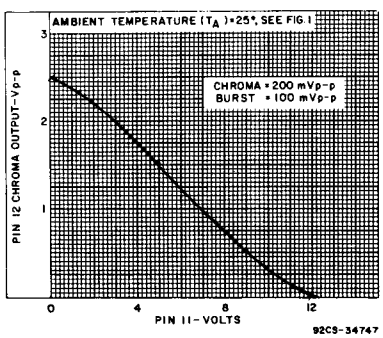

Fig. 3 - Typical saturation control vs. chroma output.

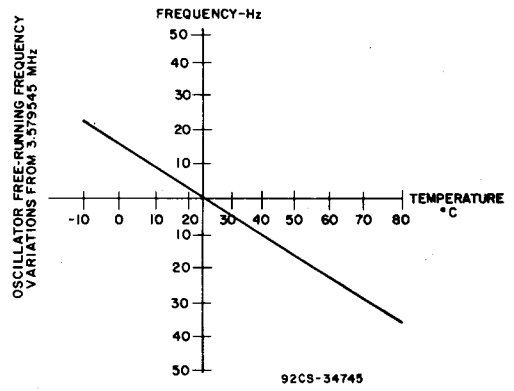

Fig. 4 - Typical oscillator frequency-temperature drift. (IC subjected to temperature only.)

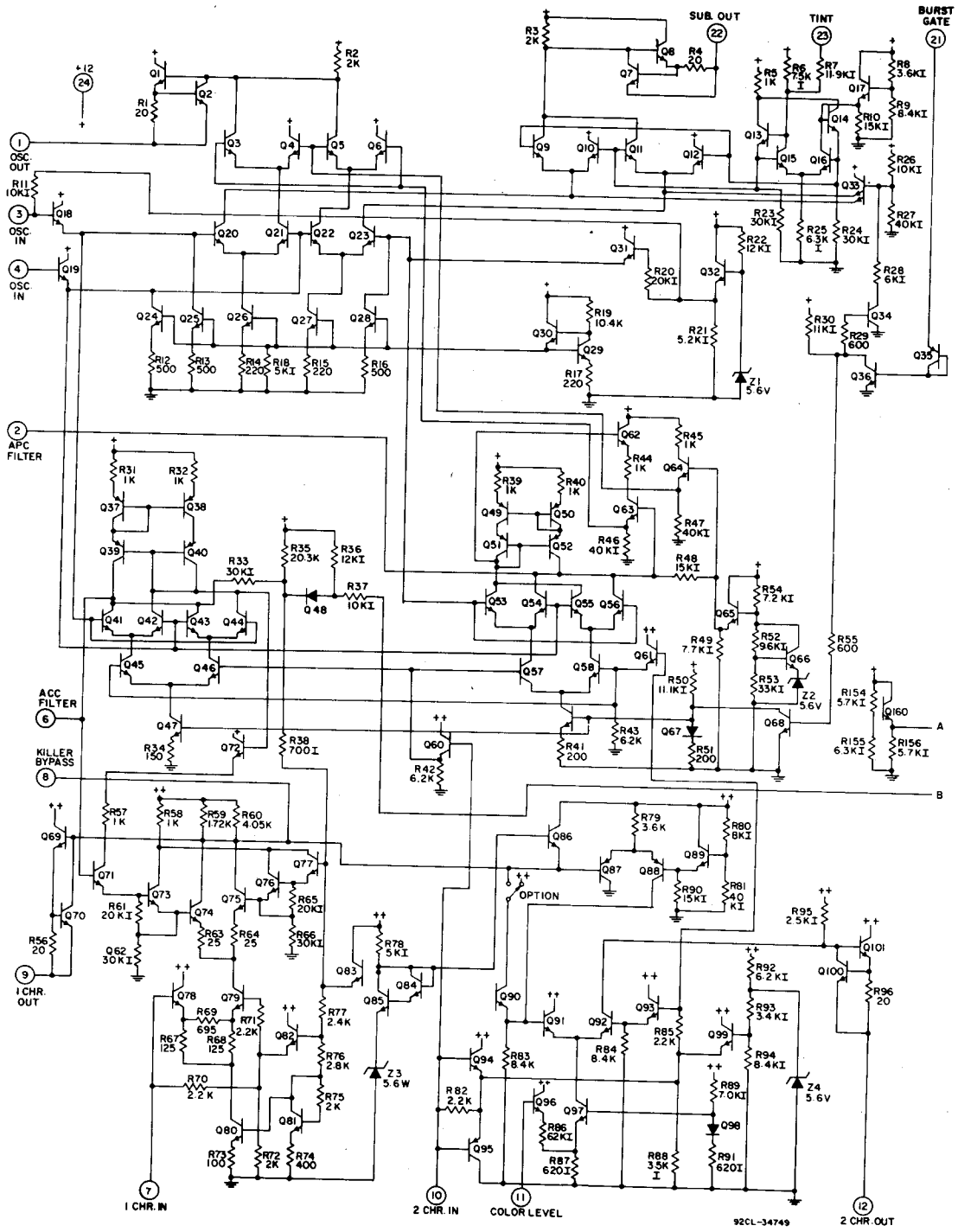

Fig. 5 - Schematic diagram of the CA3201E (Cont'd).

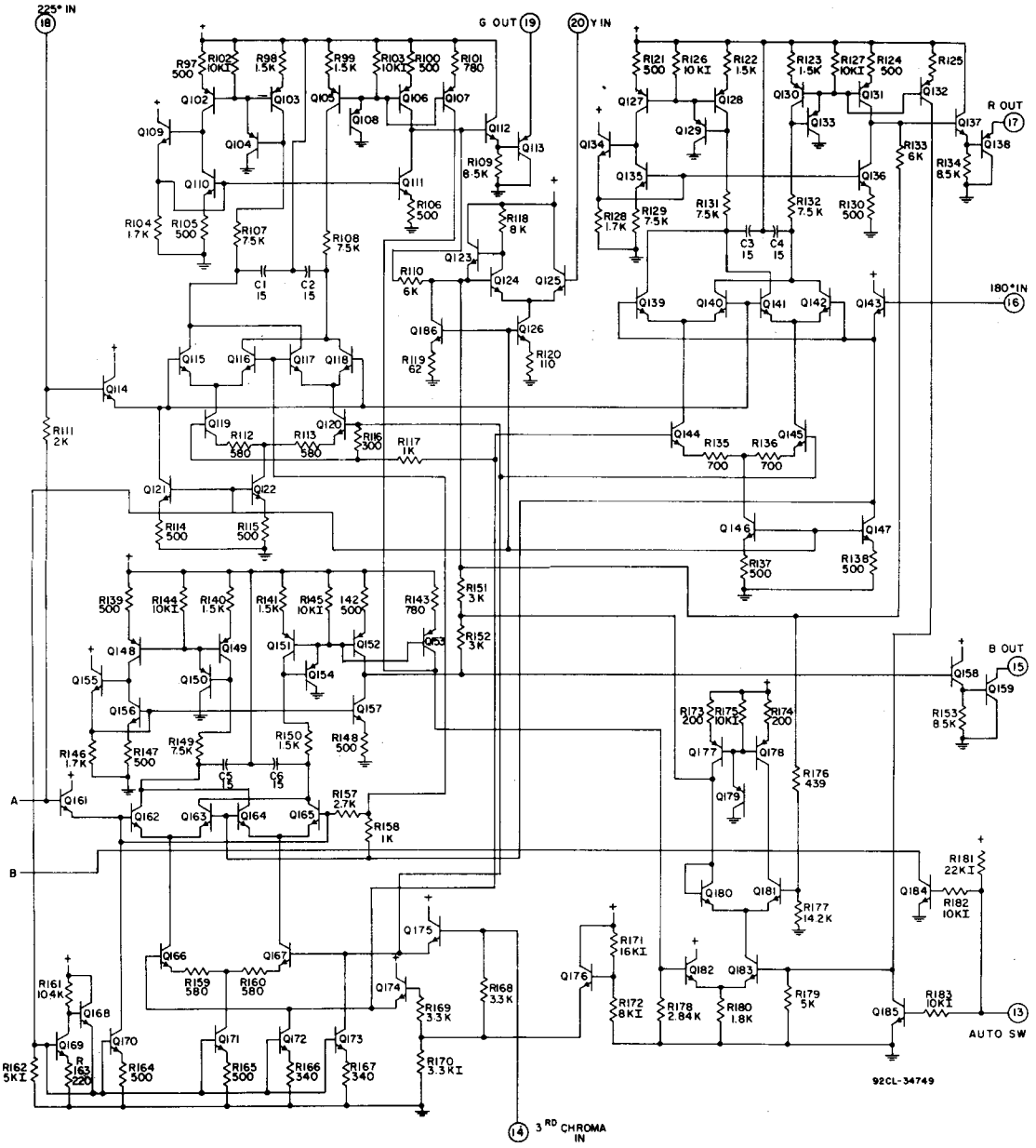

Fig. 5 - Schematic diagram of the CA3201E (Cont'd).

Circuit Description

The chroma input to pin 7 is amplified and, depending on the ACC voltage, is applied to pin 9. When the ACC voltage demands full gain to R59 and pin 9, the actuating signal for the color killer is developed on R60. The signal from pin 9 is applied to pin 10 for use by both the second chroma amplifier and the phase detectors. The signal swing at pin 10 is limited by Q94 and Q95. The gain of the second chroma amplifier to pin 12 is controlled by pin 11 voltage.

The signal at pin 10 is applied to the two phase detectors at Q46 and Q57. The current sources to the two phase detectors are turned on only during burst time as determined by the burst-gate input at pin 21. The oscillator signals for the phase detectors are derived from the oscillator signals at pin 3 and pin 4 and the quadrature phase difference is achieved the same way as in the oscillator. Both phase detectors convert their balanced outputs to single-ended outputs by use of current mirrors. The ACC voltage is

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developed across R33 and is filtered by an external capacitor at pin 6. ACC action is delayed by the small voltage applied to R33 by divider R35 and R38 (auto mode off). This delay offset is modified by R36 and Q48 when the "auto mode" switch is on. Because the duty cycle of the phase detectors is small, the base current of the ACC circuit (emitter follower Q71) is a drain on the ACC filter capacitor, and Q72 provides a compensating base current to the other side of the mirror. A similar circuit is used for the APC detector.

The external circuit of the oscillator, when tuned properly, provides a 90-degree phase shift from pin 1 to pin 3 and an additional 45-degree phase shift between pin 3 and pin 4. The voltage at pin 4 is shifted 45 degrees by an RC phase shifter and this voltage is applied to a series-tuned circuit comprised of a crystal and capacitor to pin 3, a resistor between pin 3 and pin 4, and a capacitor between pin 4 and ground. With the same current flowing through the resistor and capacitor, the voltage across the capacitor (pin 4 to

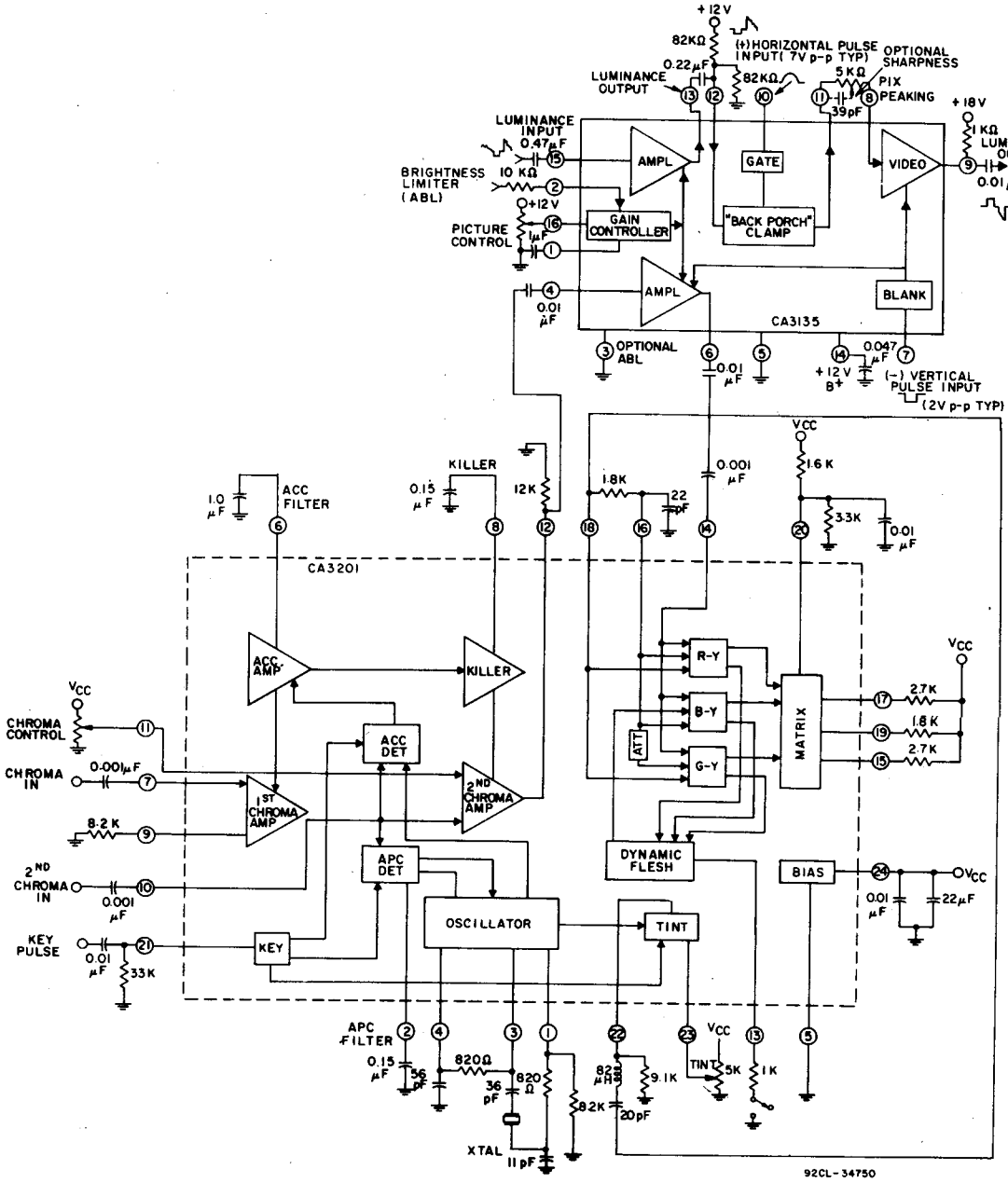

Fig. 6 - Typical two-package chroma-luma system for color TV receivers utilizing the CA3201E and CA3135.

ground) is in quadrature with the voltage across the resistor (pin 3 to pin 4). The differential amplifier, Q22 and Q23, is switched in quadrature with the differential amplifier, Q20 and Q21. Although the ac voltage amplitudes are different in all these places, the differential amplifiers are switched hard, and their current sources determine the amplitudes of currents combined in the oscillator. The combination can be varied by the APC control voltages to give a total phase of 90 degrees.

The complements of the oscillator quadrature currents are applied to another dc-controlled combination circuit (Q9-Q12) for tint control.

The CA3201E uses three color demodulators. The 3.58-MHz reference signals at 180 degrees and 225 degrees are matrixed to obtain the three phases for the demodulators. A "switchable automatic flesh" system modifies the B-Y demodulator out for fleshtone correction. The three demodulators are identical except for gain. The differential output current from the demodulators are filtered and processed to single-ended currents. Current mirrors provide a current gain of three and a current output for the auto-flesh circuit.

The auto-flesh comparator, Q182 and Q183, sees the R-Y signal on the Q183 side (when pin 13 is grounded—auto switch on) and the sum of the G-Y and B-Y signals on the other side. The auto-flesh output current is applied to the mid-point of the B-Y demodulator load.

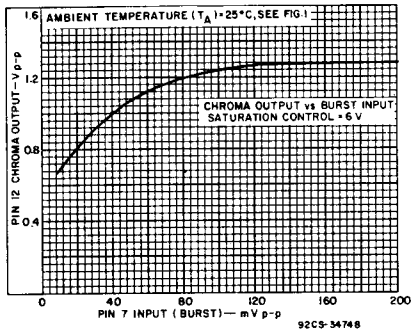

Fig. 7 - Typical ACC curve (burst-chroma ratio - 0.5).

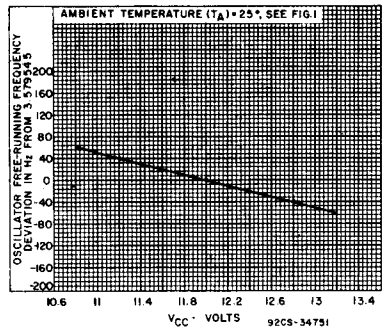

Fig. 8 - Typical oscillator frequency deviation vs. VCC.

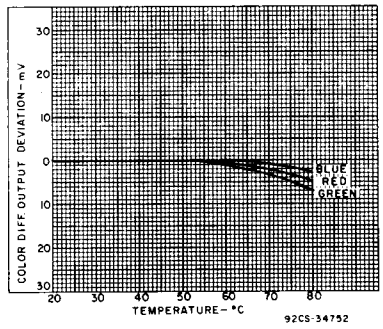

Fig. 9 - Typical dc output deviation vs. temperature.