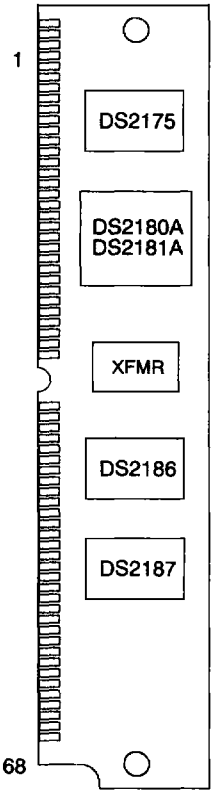
DALLAS SEMICONDUCTOR

DS2280/DS2281
T1 Line Card Stik
CEPT Line Card Stik

FEATURES

- Pretested, snap–in T1 or CEPT line card
- DS2280 T1 Line Card
  DS2281–075 75 ohm CEPT Line Card
  DS2281–120 120 ohm CEPT Line Card
- Consumes only 2 square inches or board space
- Performs four functions:
  - line interface
  - framing
  - monitoring
  - buffering
- DS2280 and DS2281 share the same pinout
- Includes line interface transformers and termination resistors
- Connects to both 1.544 MHz and 2.048 MHz backplanes
- Operates off a single +5V supply

PIN ASSIGNMENT



DESCRIPTION

The DS2280 and DS2281 are T1 and CEPT line cards that consume only two square inches of printed circuit board space. The cards are designed to plug into standard 68–pin single in–line connectors. They have been arranged for maximum flexibility and contain all the necessary hardware to connect directly to either T1, CEPT 75 ohms lines, or CEPT 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The monitoring and framing functions are performed by the DS2180A on the DS2280 and by the DS2181A on the DS2281. The buffering function is handled by the DS2175. The DS2280 and DS2281 provide all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). They also provide indication of frame errors, CRC–6 or CRC–4 errors, and bipolar violations.

OVERVIEW

The DS2280 contains four of Dallas Semiconductor's T1 integrated circuits: the DS2187 Receive Line Interface, the DS2186 Transmit Line Interface, the DS2180A T1 Transceiver, and the DS2175 Elastic Store. The DS2281 replaces the DS2180A with the DS2181A CEPT Transceiver. The operational specifics of each of these devices can be found in their individual data sheets. On the Line Card Stiks, the DS2187 connects to the receive signal through a 1:2 transformer. On the DS2280, the T1 line is properly terminated by two 200–ohm resistors (R1 and R2). On the DS2281–075, R1 and R2 are set to 150 ohms so that the CEPT lines can be properly terminated at 75 ohms. And on the DS2281–120, R1 and R2 are set at 240 ohms. The DS2187 recovers clock and data from the T1 or CEPT line and provides it to the DS2180A or DS2181A. The transceiver frames to the incoming data stream and provides status information on the received data. The DS2180A and DS2181A transceivers can be used in either the software or hardware modes. In the software mode, an external controller is used to access a set of internal registers via a serial port. These registers are used to configure the device and to retrieve monitoring information. In the hardware mode, the Stiks can be used without an external controller. In this mode, the serial port pins are redefined as device configuration pins. Please consult the DS2180A and DS2181A data sheets for full details on both the software and hardware modes.

The DS2280 and DS2281 also contain an elastic store, the DS2175. The DS2175 can perform two functions. First, it can be used to absorb clock rate and phase differences between the clock recovered by the DS2187 and a system backplane clock. It can also be used to connect the DS2280 to 2.048 MHz backplanes or to connect the DS2281 to 1.544 MHz backplanes.

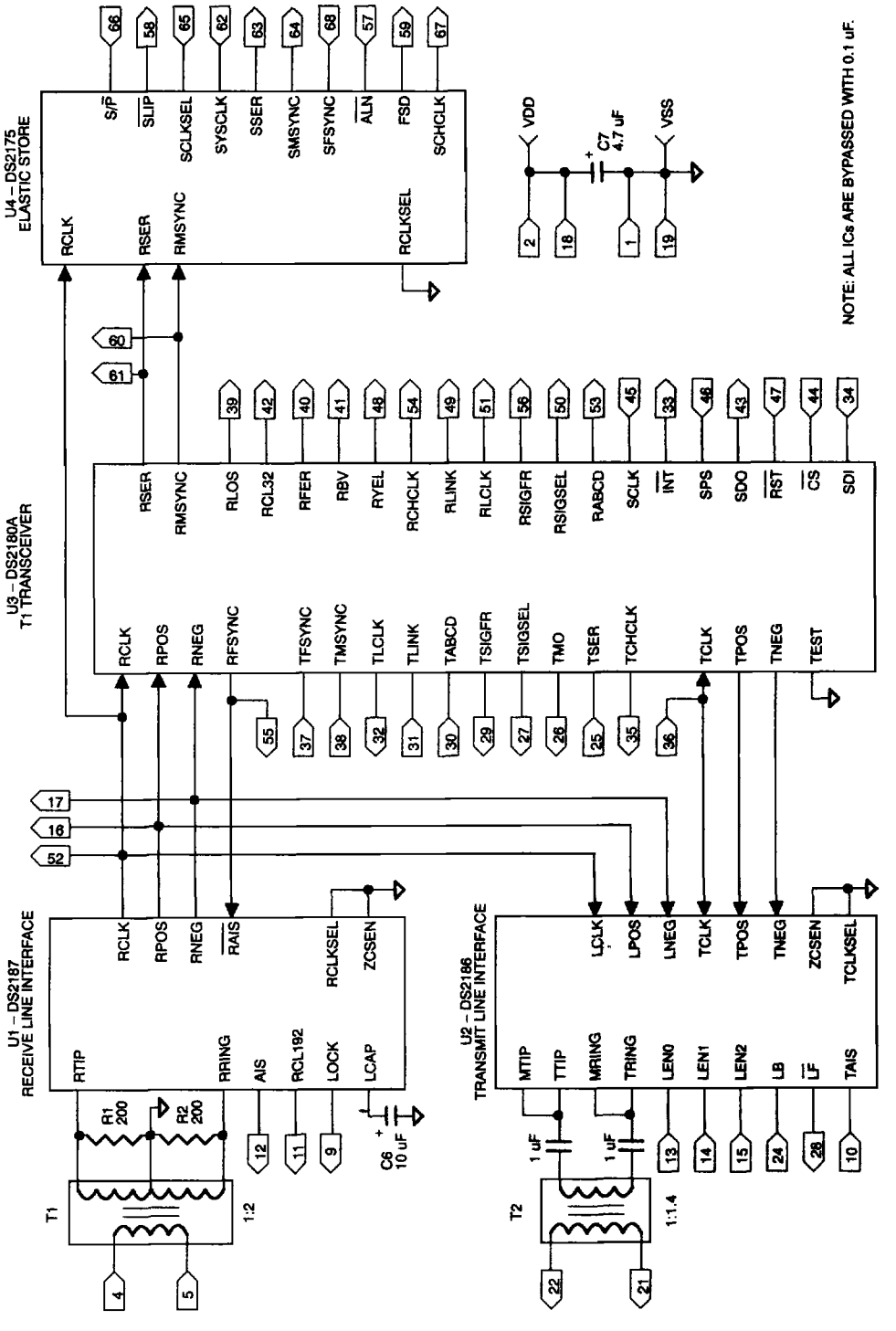
The DS2187, DS2180A, and DS2175 form the receive section of the DS2280. On the DS2281, the receive section is formed by the DS2187, DS2181A, and DS2175. The transmit section of the DS2280 and DS2181 is formed by the transceiver and the transmit line interface, the DS2186. Data that is to be transmitted onto the transmit T1 twisted wire pair or CEPT lines is clocked into the DS2180A or DS2181A transceivers via the transmit clock (TCLK). The transceivers format the data stream and add any additional information (signaling, CRC–6 or CRC–4, etc.) that might be necessary. The transceiver also transforms the data stream from a unipolar to a bipolar format and, if selected, it will perform B8ZS or HDB3 encoding. Bipolar data from the DS2180A or DS2181A is clocked into the DS2186 where it is level shifted and driven onto the transmit T1 twisted pair or CEPT line via a 1:1.4 transformer. On the DS2280, the waveshape of the transmitted pulses is selected via the line build out pins, LEN0 to LEN2. A schematic of the DS2280 is shown in Figure 1 and a schematic of the DS2281 is shown in Figure 2. The DS2280 and DS2281 are arranged for maximum flexibility. One possible configuration for each is shown in Figures 3 and 4.

The DS2280 and DS2281 are designed to connect into a standard 68–pin single in–line connector with a pin spacing pitch of 0.050 inches. Both inclined and vertical connectors are available from connector vendors such as AMP. A right angle connector will be offered by AMP in the near future. Table 1 lists a set of suitable connectors from AMP's MicroEdge™ line.

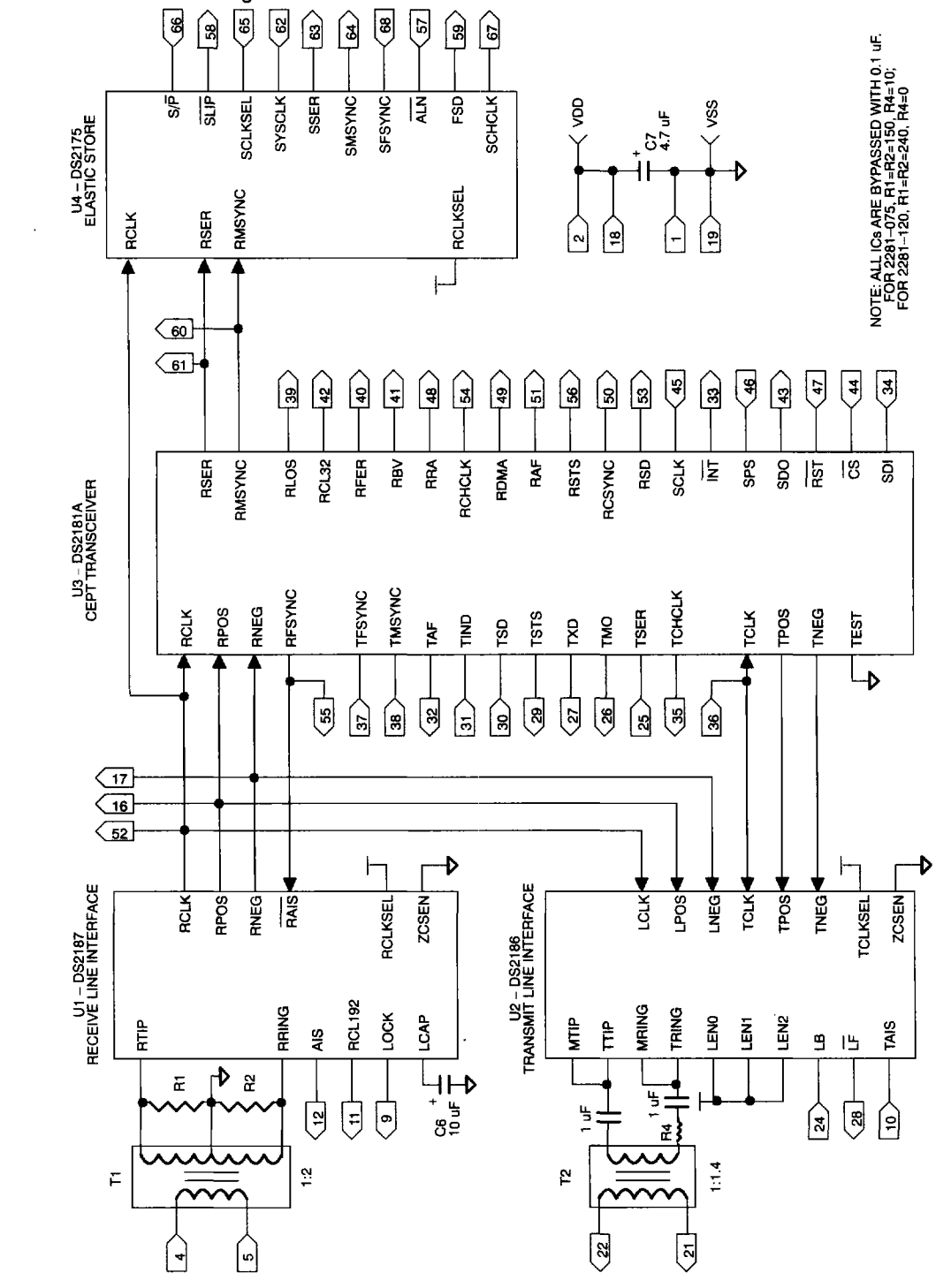
68 PIN CONNECTORS FOR DS2280 AND DS2281 Table 1

DESCRIPTION	VENDOR	PART #
Vertical Single Row with Center Posts (Tin)	AMP	821824–2
Vertical Single Row without Center Posts (Tin)	AMP	821824–7
Inclined Single Row with Center Posts (Tin)	AMP	821907–2
Inclined Single Row without Center Posts (Tin)	AMP	821907–6
Rt Angle Single Row with Center Post (Tin)	AMP	89–1439–35–68

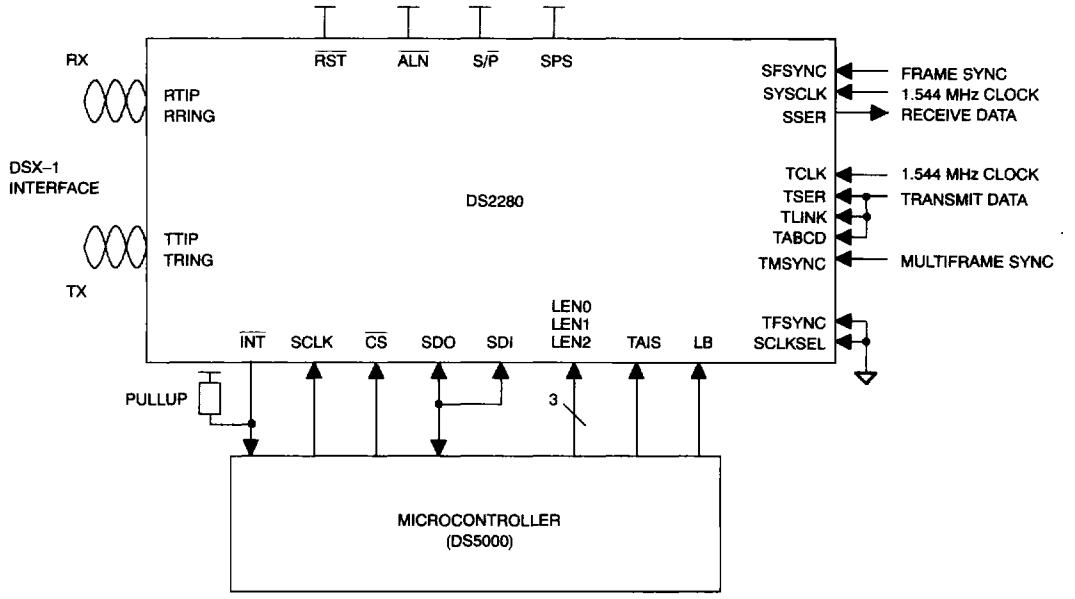
DS2280 SCHEMATIC Figure 1



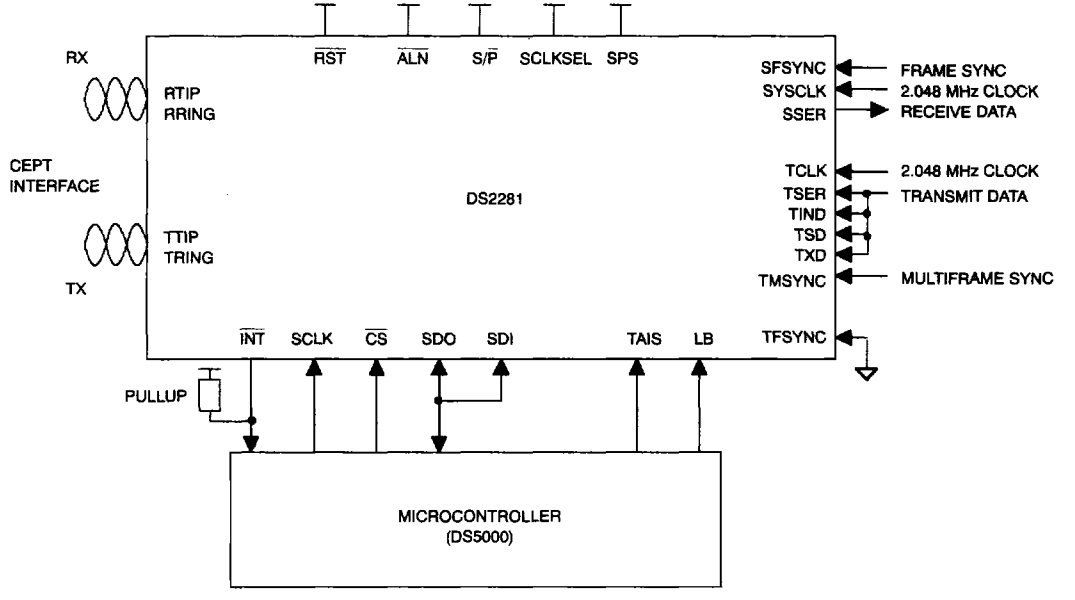
DS2281 SCHEMATIC Figure 2



TYPICAL DS2280 APPLICATION Figure 3



TYPICAL DS2281 APPLICATION Figure 4



PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DEVICE	DESCRIPTION
1	V_{SS}	–	–	**Ground.** Connect to 0.0 volt.
2	V_{DD}	–	–	**Positive Supply.** Connect to 5.0 volts.
3	NC	–	–	**No Connect.** Do not connect to this pin.
4 5	RTIP RRING	I	DS2187	**Receive Tip and Ring.** Connects directly to the receiver T1 twisted pair or CEPT lines.
6	NC	–	–	**No Connect.** Do not connect to this pin.
7	NC	–	–	**No Connect.** Do not connect to this pin.
8	NC	–	–	**No Connect.** Do not connect to this pin.
9	LOCK	O	DS2187	**Frequency Lock Indication.** High state indicates that the DS2187 is phase and frequency–locked to the incoming signal at RTIP and RRING.
10	TAIS	I	DS2186	**Transmit Alarm Indication Signal.** When strapped high, an unframed all ones signal is transmitted at TTIP and TRING at the TCLK rate.
11	RCL192	O	DS2187	**Receive Carrier Loss.** High state indicates that at least 192 consecutive zeros have been received at RTIP and RRING.
12	AIS	O	DS2187	**Receive Alarm Indication Signal.** High state indicates that the receive data stream at RTIP and RRING contains less than three zeros over two full frames of incoming data.
13 14 15	LEN0(2280) LEN1(2280) LEN2(2280)	I	DS2186	**Line Length Select.** State of these three pins determines the output T1 waveform shape. See Table 3.
13 14 15	NC(2281) NC(2281) NC(2281)	–	–	**No Connect.** Do not connect to this pin.
16 17	RPOS RNEG	O	DS2187	**Receive Positive and Negative Data.** Data extracted from the T1 or CEPT line by the DS2187.
18	V_{DD}	–	–	**Positive Supply.** Connect to 5.0 volts.
19	V_{SS}	–	–	**Ground.** Connect to 0.0 volt.
20	NC	–	–	**No Connect.** Do not connect to this pin.
21 22	TRING TTIP	O	DS2186	**Transmit Tip and Ring.** Connects directly to the transmit T1 twisted pair or CEPT line.
23	NC	–	–	**No Connect.** Do not connect to this pin.
24	LB	I	DS2186 DS2187	**Line Loopback.** When strapped high, clock and data received at RTIP and RRING is looped back to TTIP and TRING.
25	TSER	I	DS2180A DS2181A	**Transmit Serial Data.** NRZ data input, sampled on the falling edge of TCLK.
26	TMO	O	DS2180A DS2181A	**Transmit Multiframe Out.** Output of the internal multiframe counter; indicates multiframe boundaries.

PIN	SYMBOL	TYPE	DEVICE	DESCRIPTION
27	TSIGSEL (2280)	O	DS2180A	**Transmit Signaling Select**. A .667 KHz clock which identifies signaling frames A and C in 193E framing; a 1.33 KHz clock in 193S framing.
	TXD (2281)	I	DS2181A	**Transmit Extra Data**. Sampled on falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 in frame 0 when CAS is enabled.
28	$\overline{LF}$	O	DS2186	**Line Fault**. Open collector; active low output. Held low during an output driver fault or failure; 3–stated otherwise.
29	TSIGFR (2280)	O	DS2180A	**Transmit Signaling Frame**. High during signaling frames, low otherwise.
	TSTS (2281)	O	DS2181A	**Transmit Signaling Timeslot**. High during timeslot 16 of every frame, low otherwise.
30	TABCD (2280)	I	DS2180A	**Transmit ABCD Signaling Data**. When enabled via TCR.4 in the DS2180A, the LSB time of each channel will be sampled in signaling frames on falling edge of TCLK.
	TSD (2281)	I	DS2181A	**Transmit Signaling Data**. CAS signaling data input; sampled on falling edge of TCLK for insertion into outgoing timeslot 16 when enabled.
31	TLINK (2280)	I	DS2180A	**Transmit Link Data**. Sampled during the F–bit time on the falling edge of TCLK. Sampled in odd frames in 193E framing and in even frames for 193S if enabled via TCR.2 in the DS2180A.
	TIND (2281)	I	DS2181A	**Transmit International and National Data**. Sampled on the falling edge of TCLK during bit 1 of timeslot 0 of every frame (international) and/or during bit times 4 through 8 of timeslot 0 during non–align frames (national) when enabled.
32	TCLK (2280)	O	DS2180A	**Transmit Link Clock**. A 4 KHz demand clock for the TLINK input.
	TAF (2281)	O	DS2181A	**Transmit Alignment Frame**. High during frames containing the frame alignment signal, low otherwise.
33	$\overline{INT}$	O	DS2180A DS2181A	**Receive Alarm Interrupt**. Flags host controller during alarm conditions. Active low, open drain output.
34	SDI	I	DS2180A DS2181A	**Serial Data In**. Data for onboard registers. Sampled on the rising edge of SCLK.
35	TCHCLK	O	DS2180A DS2181A	**Transmit Channel Clock**. 192 KHz or 256 KHz clock which identifies timeslot (channel) boundaries.
36	TCLK	I	DS2186 DS2180A DS2181A	**Transmit Clock**. A 1.544 MHz or 2.048 MHz clock with the proper accuracy and jitter characteristics should be applied here.
37	TFSYNC	I	DS2180A DS2181A	**Transmit Frame Sync**. Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low, allowing TMSYNC to establish multiframe and frame alignment.
38	TMSYNC	I	DS2180A DS2181A	**Transmit Multiframe Sync**. May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows the internal multiframe counter to run free.

PIN	SYMBOL	TYPE	DEVICE	DESCRIPTION
39	RLOS	O	DS2180A DS2181A	**Receive Loss of Sync.** Indicates sync status; high when a re-sync is in progress, low otherwise.
40	RFER	O	DS2180A DS2181A	**Receive Frame Error.** Transitions high when either a frame or CRC or CAS multiframe error event occurs.
41	RBV	O	DS2180A DS2181A	**Receive Bipolar Violation.** Transitions high when a bipolar violation is detected.
42	RCL32	O	DS2180A DS2181A	**Receive Carrier Loss.** High state indicates that at least 32 consecutive zeros have been received at RTIP and RRING.
43	SDO	O	DS2180A DS2181A	**Serial Data Out.** Control and status information from the on-board registers. Updated on falling edge of SCLK, 3–stated during serial port write or when $\overline{CS}$ is high.
44	$\overline{CS}$	I	DS2180A DS2181A	**Chip Select.** Must be low to write to or read from the serial port.
45	SCLK	I	DS2180A DS2181A	**Serial Data Clock.** Used to read or write serial port registers.
46	SPS	I	DS2180A DS2181A	**Serial Port Select.** Tie to V_{DD} to select the serial port (software mode). Tie to V_{SS} to select the hardware mode.
47	$\overline{RST}$	I	DS2180A DS2181A	**Reset.** A high–low transition clears all internal registers and resets the receive side counters. A high–low–high transition will initiate a re–sync.
48	RYEL (2280)	O	DS2180A	**Receive Yellow Alarm.** High state indicates that a yellow alarm has been detected in the T1 data stream received at RTIP and RRING.
	RRA (2281)	O	DS2181A	**Receive Remote Alarm.** Transitions high when alarm detected, low when alarm cleared.
49	RLINK (2280)	O	DS2180A	**Receive Link Data.** In 193E framing mode, updated with extracted FDL data one RCLK before the start of odd frames and held until the next update. In 193S framing mode, updated with extracted S–bit data one RCLK before the start of even frames and held until the next update.
	RDMA (2281)	O	DS2181A	**Receive Distant Multiframe Alarm.** Transitions high when alarm detected, low when alarm cleared.
50	RSIGSEL (2280)	O	DS2180A	**Receive Signaling Select.** A 0.667 KHz clock which identifies signaling frames A and C in 193E framing; a 1.33 KHz clock in 193S framing.
	RCSYNC (2281)	O	DS2181A	**Receive CRC4 Sync.** Low–high transition indicates start of CRC4 multiframe, held high during CRC4 frames 0 through 7 and low during frames 8 through 15.
51	RLCLK (2280)	O	DS2180A	**Receive Link Clock.** A 4 KHz demand clock for RLINK.
	RAF (2281)	O	DS2181A	**Receive Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.

PIN	SYMBOL	TYPE	DEVICE	DESCRIPTION
52	RCLK	O	DS2187	**Receive clock**. A 1.544 MHz or 2.048 MHz clock that is recovered from the incoming data stream at RTIP and RRING by the DS2187. Fed to all the other devices on the DS2280 and DS2281.
53	RABCD (2280)	O	DS2180A	**Receive ABCD Signaling**. Extracted signaling data output, valid for each channel time in signaling frames. In non–signaling frames, RABCD outputs the LSB of each channel word.
	RSD (2281)	O	DS2181A	**Receive Signaling Data**. Extracted timeslot 16 data.
54	RCHCLK	O	DS2180A DS2181A	**Receive channel Clock**. 192 KHz or 256 KHz clock which identifies timeslot (channel) boundaries.
55	RFSYNC	O	DS2180A DS2181A	**Receive Frame Sync**. Extracted 8 KHz signal that indicates the beginning of each frame.
56	RSIGFR (2280)	O	DS2180A	**Receive Signaling Frame**. High during signaling frames, low during resync and non–signaling frames.
	RSTS (2281)	O	DS2181A	**Receive Signaling Timeslot**. High during timeslot 16 of every frame, low otherwise.
57	$\overline{\text{ALN}}$	I	DS2175	**Align**. When forced low, $\overline{\text{ALN}}$ recenters the buffer on the next system side frame sync boundary as determined by SFSYNC.
58	$\overline{\text{SLIP}}$	O	DS2175	**Frame Slip**. Held low for 65 SYSCLK cycles when a slip occurs. Active low, open drain output.
59	FSD	O	DS2175	**Frame Slip Direction**. State indicates direction of the last slip; latched on a slip occurrence. Low state indicates that the buffer is empty and a frame was repeated. High state indicates that the buffer is full and a frame was deleted.
60	RMSYNC	O	DS2180A DS2181A	**Receive Multiframe Sync**. Extracted multiframe sync; rising edge indicates the start of a multiframe.
61	RSER	O	DS2180A DS2181A	**Receive Serial Data**. Received NRZ serial data, updated on the rising edge of RCLK.
62	SYSCLK	I	DS2175	**System Clock**. A 1.544 MHz or 2.048 MHz data clock.
63	SSER	O	DS2175	**System Serial Data**. Updated on the rising edge of SYSCLK.
64	SMSYNC	O	DS2175	**System Multiframe Sync**. Slip–compensated multiframe output; used with RMSYNC to monitor depth of the DS2175 buffer real time.
65	SCLKSEL	I	DS2175	**System Clock Select**. Tie to V_{SS} for 1.544 MHz backplane applications; tie to V_{DD} for 2.048 MHz backplane applications.
66	S/$\overline{\text{P}}$	I	DS2175	**Serial/Parallel Select**. Tie to V_{SS} for parallel backplane applications; tie to V_{DD} for serial backplane applications.
67	SCHCLK	O	DS2175	**System Channel Clock**. Transitions high on channel boundaries.
68	SFSYNC	I	DS2175	**System Frame Sync**. Rising edge establishes system side frame boundaries.

T1 TRANSMIT LINE LENGTH SELECTION Table 3

LEN2	LEN1	LEN0	WAVEFORM SELECTED
0	0	0	Do not use
0	0	1	Do not use
0	1	0	Do not use
0	1	1	DSX–1 Crossconnect; 0 to 133 feet
1	0	0	DSX–1 Crossconnect; 133 to 266 feet
1	0	1	DSX–1 Crossconnect; 266 to 399 feet
1	1	0	DSX–1 Crossconnect; 399 to 533 feet
1	1	1	DSX–1 Crossconnect; 533 to 655 feet

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to V_{CC} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20		pF	1
Output Capacitance	C_{OUT}		40		pF	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		70	90	mA	2
Input Leakage	I_I	–1.0		+1.0	µA	3, 5
Output Leakage	I_O	–1.0		+1.0	µA	4
Output Current @ 2.4V	I_{OH}	–1.0			mA	6
Output Current @ 0.4V	I_{OL}	+4.0			mA	6

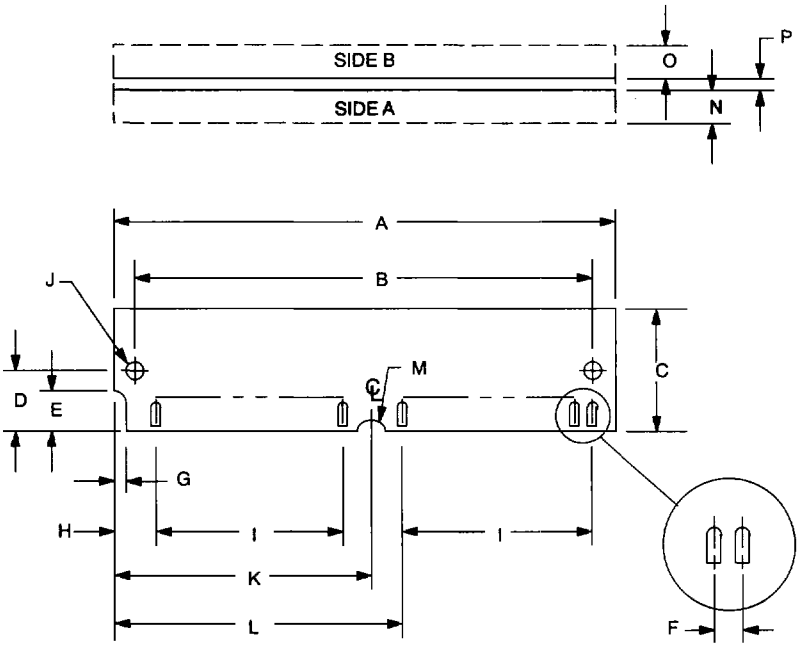
NOTES:

1. Does not apply to RTIP, RRING, TTIP, or TRING.
2. V_{DD}=5.25V and TCLK=2.048 MHz.
3. $V_{SS}<V_{IN}<V_{DD}$.
4. Applies to open collector outputs ($\overline{LF}$, $\overline{SLIP}$, $\overline{INT}$).
5. All inputs except RTIP and RRING.
6. All outputs except TTIP and TRING.

NOTE:

All AC Electrical Parametrics can be found in the individual data sheets on the DS2187, DS2186, DS2180A, DS2181A, and DS2175.

DS2280 T1 LINE CARD STIK
DS2281 CEPT LINE CARD STIK



PKG	68-PIN	
DIM	MIN	MAX
A IN.	4.045	4.055
B IN.	3.779	3.789
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.050 BSC	
G IN.	0.075	0.085
H IN.	0.245	0.255
I IN.	1.650 BSC	
J IN.	0.120	0.130
K IN.	1.850	1.950
L IN.	2.020	2.030
M IN.	0.057	0.067
N IN.		0.225
O IN.		0.290
P IN.		0.054