1. GENERAL

The Toshiba TC8833F is a singlechip CMOS voice recording / playback LSI based on ADM (Adaptive Delta Modulation). It can make use of ordinary or pseudo S - RAM to record voice data as well as playback only ROM.

2. FEATURES

- ☐ Can handle 64 K, 256 K, 512 K, 1M, 2M, or 4M - bit S - RAM, pseudo S - RAM, or ROM LSI chips as voice recording media.
- ☐ A maximum of four 1M bit memory chips can be connected to the TC8833F directly.
- ☐ Generates a dedicated refresh control signal for pseudo - SRAM.
- ☐ Supports both manual and CPU control modes.
- ☐ Can record and playback up to four phrases in the manual control mode and up to 128 phrases in the CPU - control mode.
- ☐ Supports four bit rates (32 K bps, 22 K bps, 16 K bps, and 11 K bps.)
- ☐ A block recording feature is incorporated.
- ☐ The built - in auto stand - by feature conserves electric power.
- ☐ 4 - and 8 - bit data buses are selectable in the CPU control mode.
- ☐ Incorporates a recording microphone amplifier and playback band - pas filter. .
- ☐ The stand - by feature permits backup of voice data.
- ☐ Built - in oscillation circuit for use wite a ceramic vibrator.
- ☐ 5 V single - source operation.
- ☐ 80 - pin mini - flat package.
- ☐ Terms used in this data sheet

  - o A phrase in the unit of words that are recorded or played back.
  - o A bit rate in the amount of data that is recorded or played back per second. It is expressed as bits per second (bps).

3. BLOCK DIAGRAM

3.1 TC8833F Block Diagram

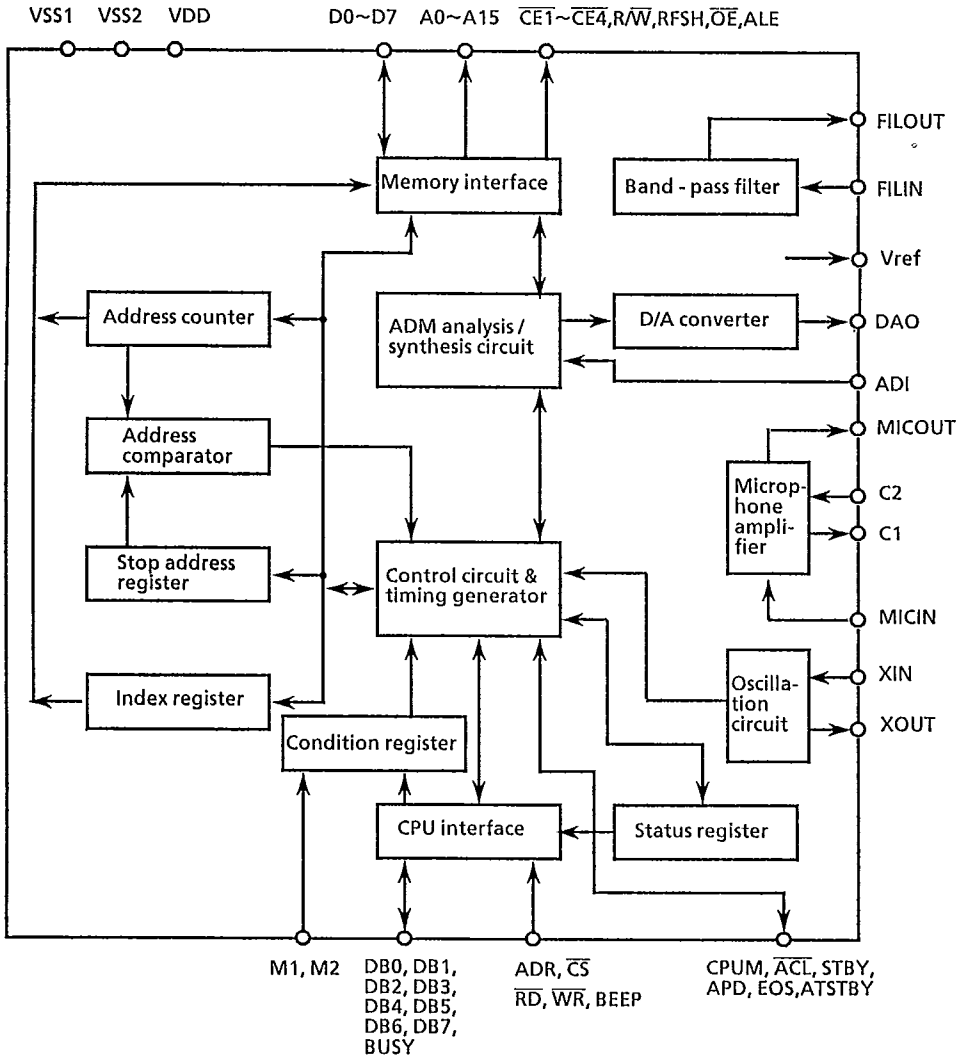


Fig 3.1 TC8833F block diagram

3.2 Block Diagram Description

(1) Address Counter
A 20 - bit counter that addresses external memory. The address counter can be loaded with address data or referenced through commands in the CPU control mode.

(2) Stop Address Register
A 20 - bit register that designates the address at which recording or playback is to be stopped. This register can be loaded with address data through a command in the CPU control mode but its contents cannot be read out.

(3) Address Comparator
Used to check for a match between the contents of the address counter and stop address register. The address counter is stopped when a match is found.

(4) Index Register
Contains the address of the index area in memory in the label index mode.

(5) Condition Register
A register used to store condition information such as the number of memory chips used, size, and bit rate.

(6) Status Register
An 8 - bit register that indicates the internal status of the TC8833F. The contents of this register may by read with a status command in the CPU control mode.

(7) Memory Interface
A circuit that interfaces with external memory.

(8) CPU Interface
An interface circuit for external microprocessors or other control devices. This circuit is connected to switches or similar devices in the manual control mode.

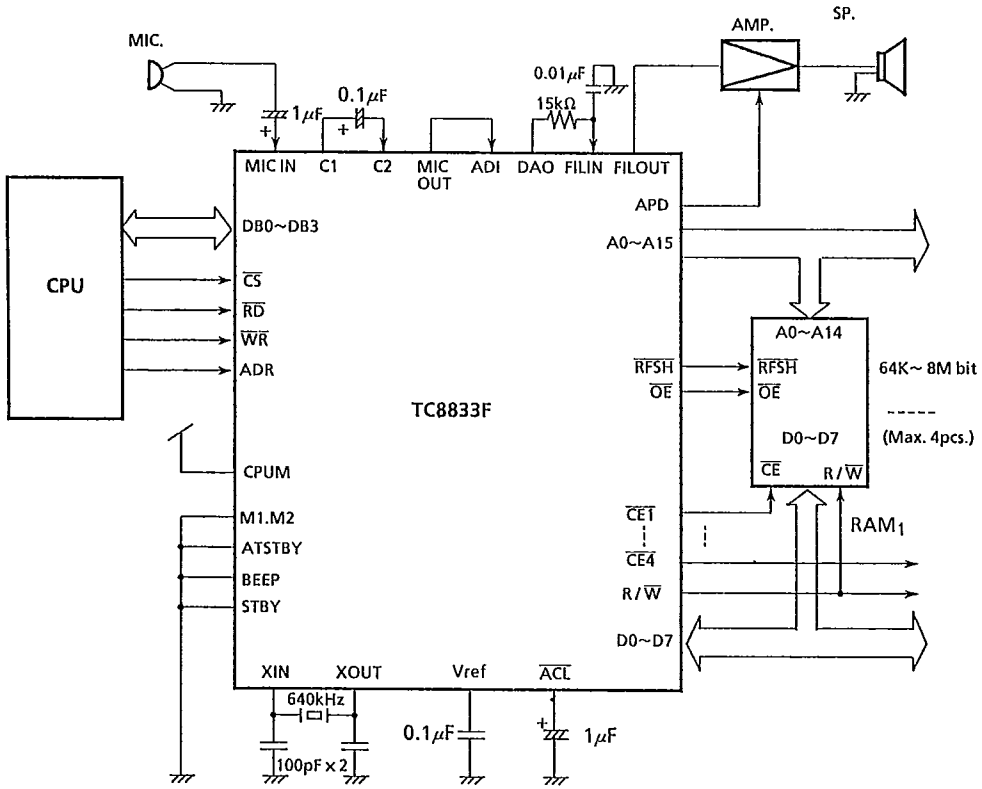
(9) ADM Analysis / Synthesis Circuit
Used to analyze or synthesize ADM data.

(10) Microphone amplifier
A microphone amplifier unit that attaches directly to a microphone. The output of the microphone amplifier swings around the analog reference voltage (Vref).

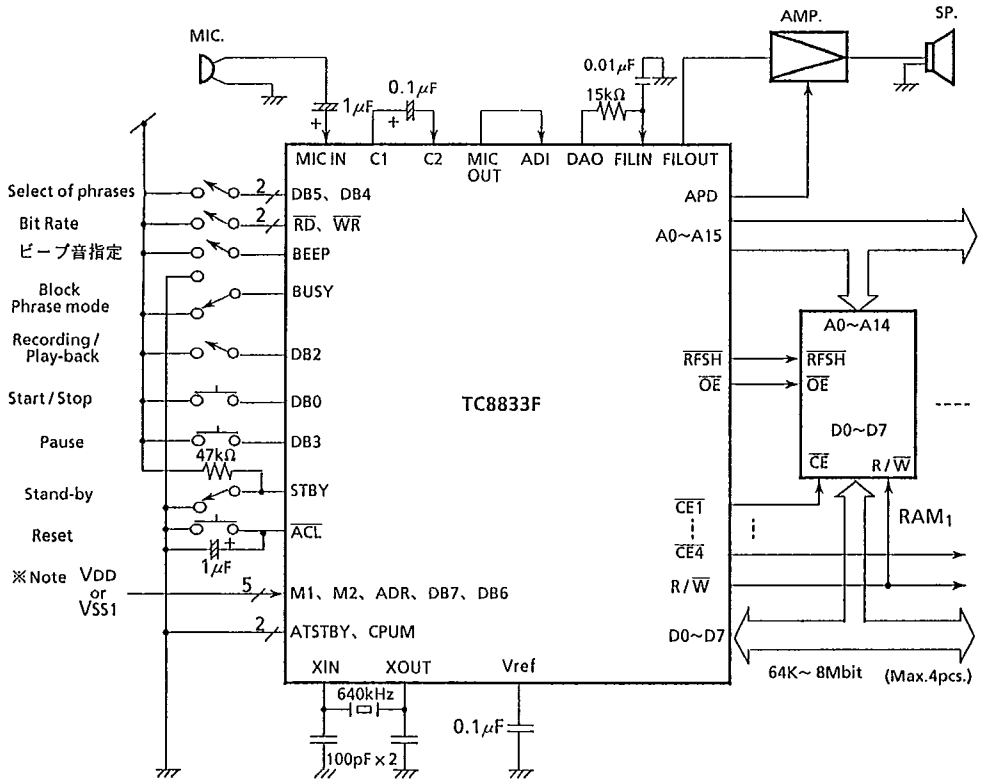
(11) Band - pass Filter
The TC8833F incorporates a primary high - pass filter and a secondary low - pass filter..

3.3 Example of Voice Recording System

3.3.1 CPU Control Type

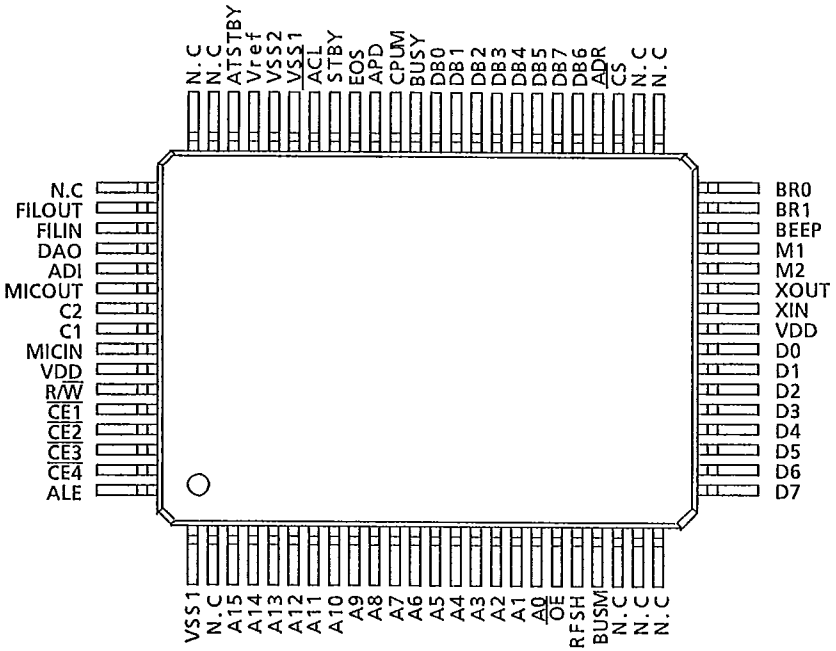


3.3.2 Manual Control Type



4. PIN ASSIGNMENT

4.1 Pin Connection



Note: NC pins must always be held open to maintain high voice quality.

4.2 Terminal Functions

Pin Name	Pin No.	Structure				Description
		Manual Control		CPU Control		
		Input / output	Pull - up / pull - down	Input / output	Pull - up / pull - down	
VSS1 VSS2	1 / 59 60	Power - source	–	Power - source	–	Supply power. These pins must be connected to the minus pin of the power supply. VSS1 is for a digital circuit and VSS2 for an analog circuit.
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	Out put	–	Out put	–	Address output pins. A0~A3 are multiplexed in time - division mode to carry address bits A0~A3 and A16~A19. These pins must be connected to the address input pins of the memory device. The pins are held in the high - impedance state in the bus request mode.
OE	19	Out put	–	Out put	–	Enables output to memory. This pin is held in the high - impedance state in the bus request mode.
RFSH	20	Out put	–	Out put	–	Refresh output pin for pseudo S - RAM. This pin may also be used as OE for static RAM. The pin is held in the high - impedance - state in the bus request mode.
BUSM	21	Out put	–	Out put	–	Bus request mode monitor output. Set to the Low level in the bus request mode.
D7 D6 D5 D4 D3 D2 D1 D	25 26 27 28 29 30 31 32	Input / output	–	Input / output	–	Memory data input / output pins. The pins are held in the high - impedance state in the bus request mode.

Pin Name	Pin No.	Structure				Description
		Manual Control		CPU Control		
		Input / output	Pull - up / pull - down	Input / output	Pull - up / pull - down	
VDD1 VDD2	33 74	Powe - source	–	Powe - source	–	Supply power. These pins must be connected to the plus pin of the power supply.
XIN XOUT	34 35	Input Output	–	Input Output	–	Oscillation circuit input / output pins. These pins must be connected to a 640 KHz ceramic vibrator and a capacitor.
M2 M1	36 37		–	Input	–	Used to select the number of external memory chips in the manual control mode.
BEEP	38	Input	Pull - down	Input	–	Used as the beep on / off inpt pin in the manual control mode. This pin must be held at the Low level in the CPU control mode.
$\overline{WR}$	39	Input	Pull - down	Input	–	Used as the write strobe input pin for DB0~DB8 in the CPU control mode. In the manual control mode, this pin is combined with pin $\overline{RD}$ to select the bit rate.
$\overline{RD}$	40	Input	Pull - down	Input	–	Used as the read strobe input pin for DB0~DB8 in the CPU control mode. In the manual control mode, this pin is combined with pin $\overline{WR}$ to select the bit rate.
$\overline{CS}$	43	Input	Pull - down	Input	–	Used as the chip select input pin in the CPU control mode. In the manual control mode, this pin is used to enable the chatter detection function.

M2	M1	Quantity
0	0	1
0	1	2
1	0	3
1	1	4

0 = Low level
1 = High level

Note : Pins with no pin name in their column are not connected (NC). These pins must be handled as open pins to maintain high voice quality.

Pin Name	Pin No.	Structure				Structure
		Manual Control		CPU Control		
		Input / output	Pull - up / pull - down	Input / output	Pull - up / pull - down	
ADR	44	Input	Pull - down	Input	–	Used as an address input pin in the CPU control mode. I- the manual control mode, this pin is combined with DB7 and DB6 to select the memory chip type.
DB6 DB7 DB5 DB4 DB3 DB2 DB1 DB0	45 46 47 48 49 50 51 52	Input	Pull - down	Input / Output	–	Serve as the bi - directional data bus in the CPU control mode. In the manual control mode, these pins provide the following functions : (1) DB7, DB6 Select the memory chip type. (2) DB4, DB5 Select the phrase. (3) DB3 Suspends the playback operation temporally. (4) DB2 Switches between the recording and stand-by modes. (5) DB1 Triggers recording. (6) DB0 Starts or stops recording or playback.
BUSY	53	Input	–	Output	–	Used as the BUSY output pin in the CPU control mode. In the manual control mode, this pin is used as the fixed - length recording / playback select pin.
CPUM	54	Input	Pull - down	Input / Output	–	Selects the CPU or manual control mode.
APD	55	Output	–	Output	–	Analog power - down control output.
EOS	56	Output	–	Output	–	End of Speech output. This pin is held at the Low level while the TC8833F is in the recording operating or pause state.
SYBY	57	Input	–	Input	–	Indicates that the TC8833F is in the stand -by state.
ACL	58	Input	–	Input	–	Reset input.
Vref	61	Output	–	Output	–	Analog circuit referencevoltage output.
ATSTBY	62	Input	–	Input	–	Used to select the auto stand - by mode in the manual control mode configuration.

Pin Name	Pin No.	Structure				Description
		Manual Control		CPU Control		
		Input / output	Pull - up / pull - down	Input / output	Pull - up / pull - down	
FILOUT	66	Output	–	Output	–	Built - in band - pass filter output.
FILIN	67	Input	–	Input	–	Built - in band - pass filter input.
DAO	68	Output	–	Output	–	Voice synthesis circuit voice signal output pin of voltage follower output type.
ADI	69	Input	–	Input	–	Voice analysis circuit voice signal input. The input signal must be biased to Vref of coupled with a capacitor.
MICOUT	70	Output	–	Output	–	Built - in microphone amplified second stage output.
C2	71	Input	–	Input	–	Built - in microphone amplified second stage input.
C1	72	Input	–	Input	–	Built - in microphone amplified first stage output.
MICIN	73	Input	–	Input	–	Built - in microphone amplified first stage input.
R/$\overline{W}$	75	Output	–	Output	–	Memory read / write output. This pin is held at the high - impedance state in the bus request mode.
$\overline{CE1}$ $\overline{CE2}$ $\overline{CE3}$ $\overline{CE4}$	76 77 78 79	Output	–	Output	–	Memory chip enable outputs. These pins must be used according to the number of memory chips installed, starting at $\overline{CE1}$. Pins $\overline{CE2}$ through $\overline{CE4}$ carry highest - order address bits (A16~A18) depending on the number of memory chips used.
ALE	80	Output		Output	–	Memory address latch output. This pin carries address bit A19 when only one memory chip is used. The pin is put into the high - impedance state if the TC8833F is put into the bus request mode in this configuration.

5. SPECIFICATIONS

5.1 Recording / Reproducing Part

Recording / playback method	ADM
D / A converter	10 - bit voltage type
Bit rate	Maximum number of phrases
Manual control mod: 4 phrases	CPU control mode: Label index mode: 128 phrases Direct mode: No limit
Address counter	A 20 - bit PS - RAM refresh circuit is built in.

5.2 Others

Recording microphone amplifier	2 stages, gain = 46 db (typical)
Playback filter	Secondary low-pass filter + Primary low - pass filter
Voice data memory	Supports memory chips with sizes up to 4M bits.
Oscillation frequency	640 KHz (typical)

5.3 Operation and Functions

The TC8833F may be configured either in the CPU control mode in which the TC8833F is control by a microprocessor or in the manual control mode in which the TC8833F is controlled via external switches.

5.4 Manual Control

The TC8833F can be put into the manual control mode by setting the CPUM pin to the Low level.

5.4.1 Selecting the Memory Size

You can select the size of memory chips to be used with the TC8833F from 64 K, 256 K, 512 K, 1M, 2M, and 4M bits by using the ADR, DB6, and DB, input pins. The table below shows the relationship between the three input pin settings and the memory sizes.

Size	DB7	DB6	ADR	Maximum number of Chips
64 kbit	0	0	0	4
256 kbit	0	0	1	4
512 kbit	0	1	0	4
1 Mbit	0	1	1	3
2 Mbit	1	0	0	2
4 Mbit	1	0	1	1
Inhibited	1	1	*	-

1 = High level
0 = Low level

* Do n't care

Do not set the three memory size setting pins to the setting designated as "inhibited." If the "inhibited" setting is used, both the out puts and inputs of the TC8833F would be unstable and cause the TC8833F to malfunction.

Note that different sizes of memory chips cannot be used with the TC8833F.

5.4.2 Selection of Bit Rate

The TC8833F supports four bit rates, namely, 32 K bps, 22 K bps, 16 K bps, and 11 K bps. Use the $\overline{WR}$ and $\overline{RD}$ pins to set the bit rate of the TC8833F as summarized in Table 5.1. The bit rates in the recording and playback modes are different so that the speech may be made rapidly or slowly in the playback mode. As with a tape recorder deck, the pitch of the played back speech gets lower in slow speech modes and higher in the rapid speech modes.

Table 5.1 Bit rate

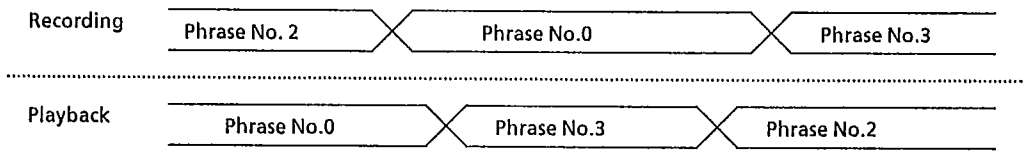
Bit rate	rate from oscirator	$\overline{WR}$	$\overline{RD}$
11 kbps	60 : 1	0	0
16 kbps	40 : 1	0	1
22 kbps	30 : 1	1	0
32 kbps	20 : 1	1	1

5.4.3 Selecting the Phrase

The TC8833F can record and play back maximum of four phrases. The phrase to be record or played back can be selected using the DB4 and DB5 input pins. The relationship between the phrase numbers and the pin settings are summarized the table below. You may select any phrase number.

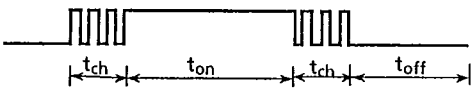
Phrase number	DB5	DB4
0	0	0
1	0	1
2	1	0
3	1	1

You can specify the phrase numbers in any order in the recording mode. You may record phrases, for example, in the order of phrase number 2, phrase number 0, phrase number 3, and phrase number 1. You may also play back the recorded phrase in any order.



5.4.4 Chatter Prevention Circuit

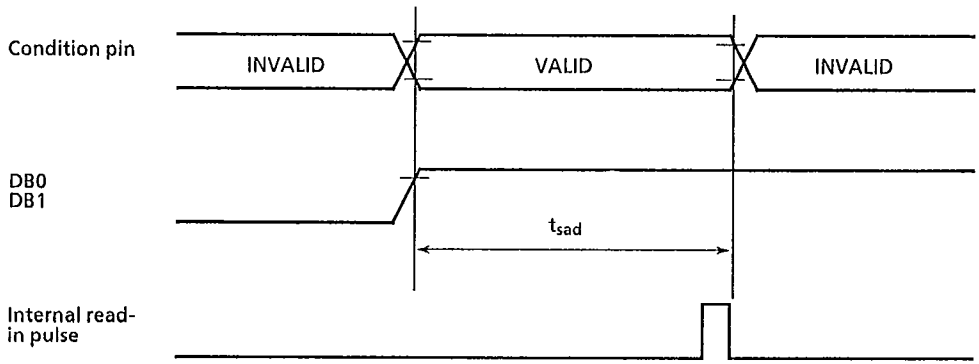
The chatter prevention circuit is used to prevent the switches connected to pins DB0, DB1, DB3, DB2, and BEEP from chattering in the manual control mode.



CS	ton	toff
L	40960/fclk minimum	20480/fclk minimum
H	400/fclk minimum	62.5 μs minimum

fclk = Oscillation frequency (Hz)

The eleven pins DB2, DB4, DB5, $\overline{RD}$, $\overline{WR}$, BUSY, M1, M2, ADR, DB6, and DB, are condition input pins. These condition input are read by the TC8833F when the IIigh level of DB0 and DB1 is established inside the TC8833F. Consequently, the inputs at these eleven pins are taken into the TC8833F after the sum of the maximum chatter sense time tch and the delay time 40 fclk. Accordingly, tsad must be greater than 20520 fclk when $\overline{CS}$ is set High and greater than 40 fclk when $\overline{CS}$ is set Low.



5.4.5 Starting Voice Recording or Playback

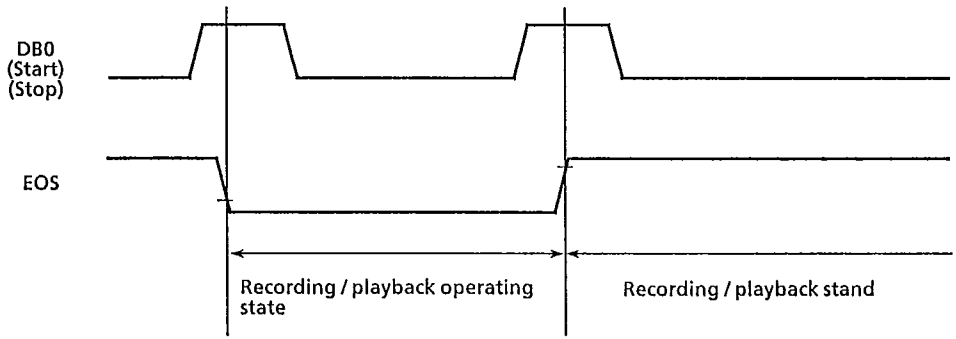
The TC8833F has a 20 - bit address counter that designates the memory locations into which voice data is stored. The TC8833F enters the recording stand - by state when pin DB2 is set to the High level and playback stand - by state when pin DB2 is set to the Low level.

(1) Starting Operation

The TC8833F switched its state from a stand - by state to an operating state when the state of pin DB0 or DB1 is set from Low to High level. The operating state that the TC8833F enters (recording of playback operating state) is determinedly the state of pin DB2.

(2) Stopping Operation

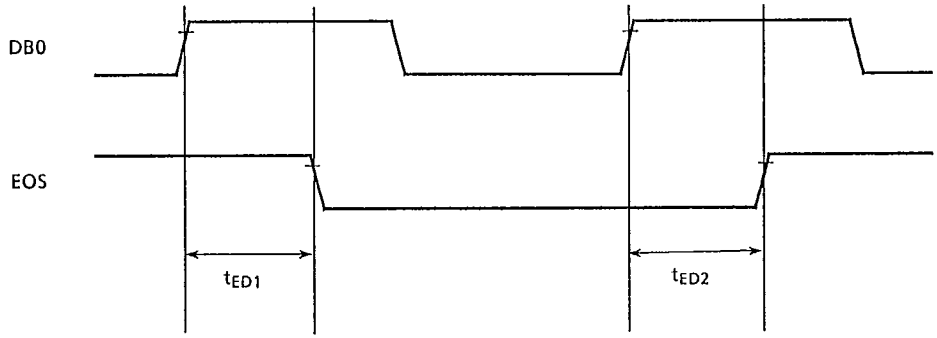
The TC8833F is switched from an operating state to a stand - by state by setting pin DB0 or DB1 from High to Low level. The pin used to stop the TC8833F may not necessarily be the same as the pin that is sued to start the TC8833F.



5.4.6 EOS (end-of-speech) Output

The EOS output pin indicates to the external world whether the TC8833F is in the recording / playback operations state or stand - by state. A High on this pin indicates that the TC8833F is in the recording / playback operations state and a low indicates that the TC8833F is in the recording / playback stand - by state.

EOS Delay Time



Symbol	Item	Maximum	Unit
t_{ED1}	EOS Delay time 1	20520 × SYS	sec
t_{ED2}	EOS Delay time 2	20520 × SYS	sec

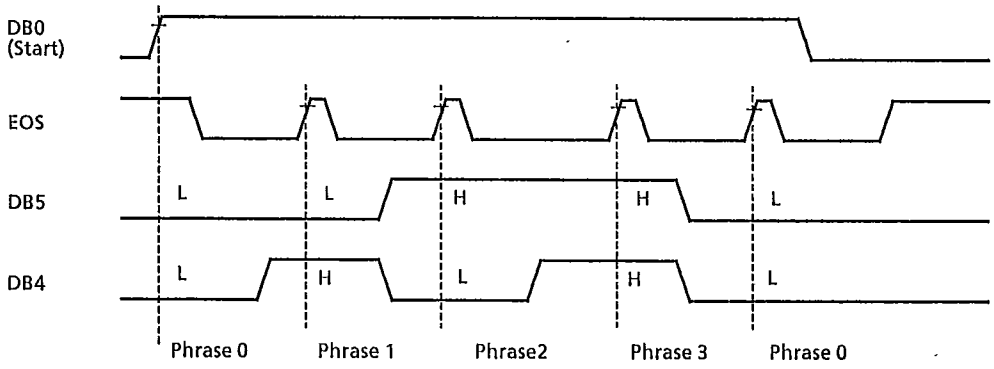
$SYS = 1/X_{IN}$ $SYS = 1.56\mu s$ @X_{IN} = 640KHz

5.4.7 Repeat Playback

The TC8833F plays back the phrase selected by pins DB4 and DB5 repeatedly if pin DB0 or DB1 is set and held High to place the TC8833F into the playback operating state.

The TC8833F stops the repeated mode playback when pin DB0 of DB1 is reset to the Low level and after the end address is sensed. In the repeated playback mode, since the TC8833F takes in status information from pins DB4, DB5, $\overline{RD}$, and $\overline{WR}$ before starting the playback of the specified phrase, the phrase to be played back next, bit rate, and other parameters may be altered by resetting the condition information before starting the iteration of the current phrase.

Repeated Mode Playback Example

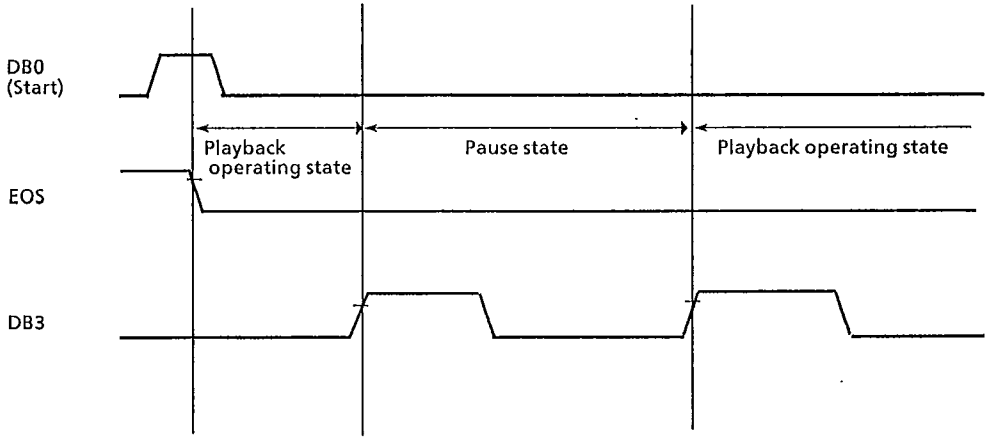


5.4.8 Pause Function

The TC8833F is instructed to suspend playback temporarily in the playback mode by setting pin DB3 from Low to High level. The TC8833F resumes the playback mode when pin DB3 is set fro Low to High level.

The pause function is valid only in the playback operating state and not available in any other states.

The TC8833F stops playback when pins DB0 and DB1 are set to the High level.



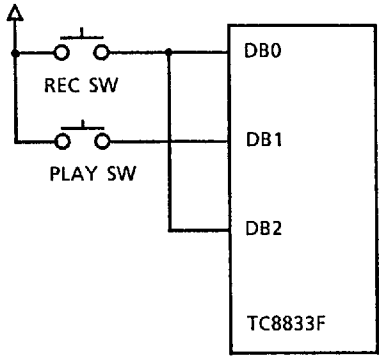
5.4.9 Applications

The TC8833F can generate various timing signals in the manual control mode so that is can be used for various applications. Some examples of TC8833F applications are given below.

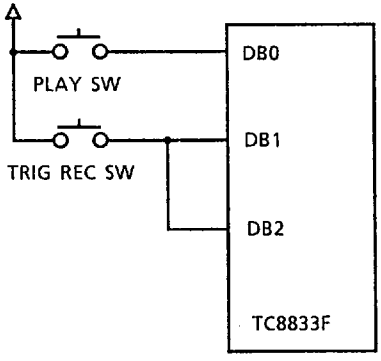
(1) Implementing the Recording and Playback Switches Separately

You can use dedicated switches for both recording and playback. Example 1 shows a TC8833F that used the recording and playback switches and Example 2 shows a TC8833F that uses the trigger recording and playback switches.

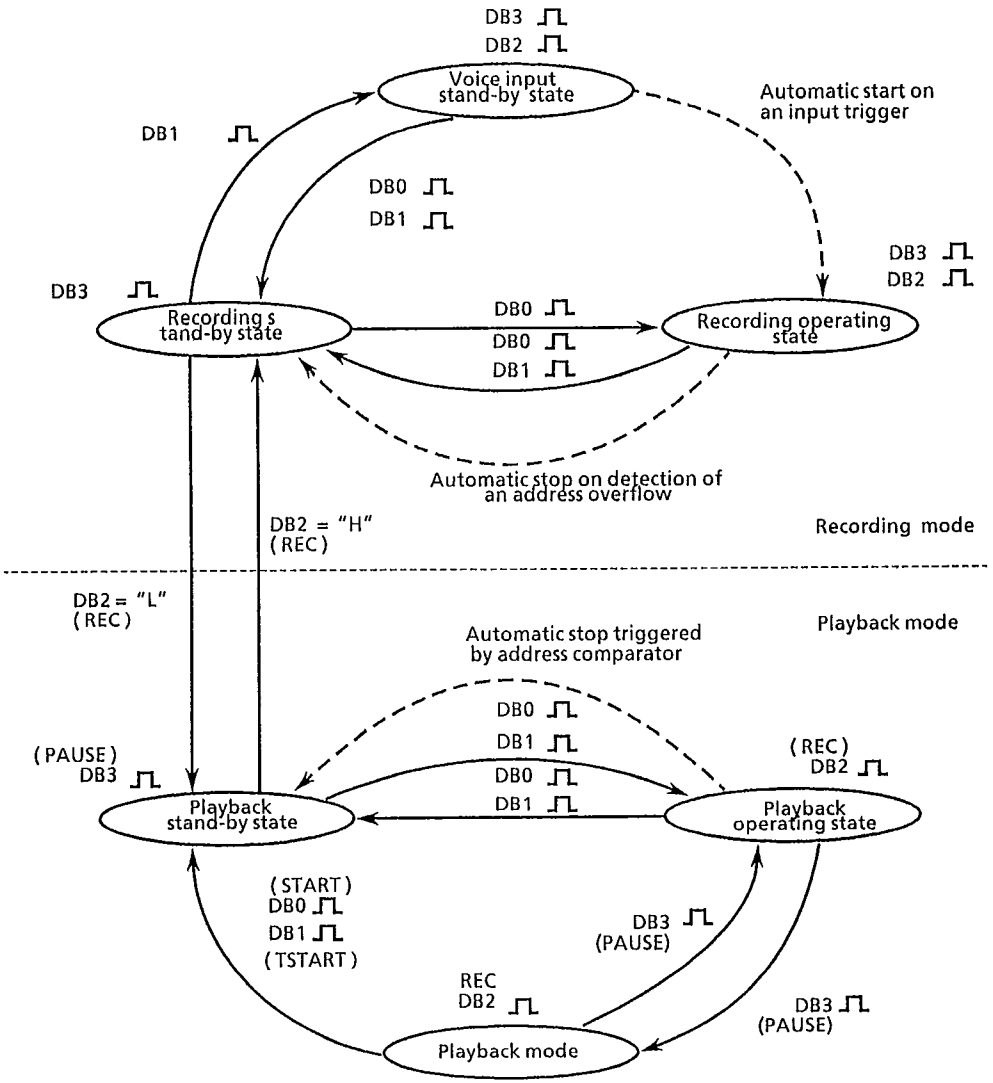
EX. 1



EX. 2



5.4.10 Manual Control Mode State Transition Diagram



5.4.11 Considerations

(1) The TC8833F cannot make repeated recording in the recording mode in the same manner as in the playback mode. Consequently, The TC8833F stops recording when it detects the end address even -if pin DB0 or DB1 (start signal) is set to and held at the High-level. To record next time, it is necessary to reset pin DB0 or -DB1 to the Low level.

(2) The TC8833F automatically resets its internal address counter to 400H when it stops operation following the detection of the end address.

(3) Pin DB0 (START) takes precedence over DB1 (TSTART) when both are set to the High level simultaneously. Pin DB1 (TSTART) is given priority when pin DB0 (START) is reset from High to Low level after both pins are set to the High level.

(4) The TC8833F enters the pause state when pins DB3 (PAUSE) and pin DB0 (START) or DB1 (TSTART) simultaneously in the playback mode. In this case, the address counter is set to the start address of the current phrase. This means that the TC8833F has entered the pause state immediately when it started the playback operation.

5.5 CPU Control Mode Operations

The TC8833F is programmed to be controlled by a microprocessor or another control device by setting the CPUM pin to the High level (CPU control mode).

In the CPU control mode, the pins that are used in the manual control mode are used for interfacing purposes and the operation of the TC8833F is controlled by the commands that are executed over the control and data lines. The TC8833F supports both the 4-bit and 8-bit data buses so that it can accommodate to various types of microprocessors.

In the CPU control mode, the TC8833F can run not only in the label index mode that is available in the manual control mode but also in the direct control mode in which commands are used to specify the start and stop addresses.

5.5.1 TC8833F Commands

In the CPU control mode, all operations of the TC8833F can be controlled using commands.

Four control lines, i.e., $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and ADR are used for controlling of the TC8833F by a CPU. The uses of these lines are summarized in Fig 5.5.1. The $\overline{RD}$ and $\overline{WR}$ signals are held disabled once command is executed until the internal processing terminates depending on the state of the BUSY flag that is set after the signals are accepted.

Fig 5.5.1 CPU USE

CPUM	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	ADR	Inhibited
1	0	0	0	*	INHIBITS
1	0	0	1	0	DATA READ
1	0	0	1	1	STATUS READ
1	0	1	0	0	COMMAND WRITE
1	0	1	0	1	CANCEL
1	1	0	0	*	BUSREQ MODE

*:Don't care

Combinations other than listed above perform no operation.

"Do not set the command control lines to the setting designated as "inhibited". If the "inhibited" setting is used, both the outputs and inputs of the TC8833F would be unstable and cause the TC8833F to malfunction.

5.5.2 CPU Control Line Description

The definition and use of the CPU control lines are given below (see Fig 5.5.1).

(1) Command Write : Used to write command words and data to the TC8833F.

(2) Data Read: Used to read data from the TC8833F.

(3) Cancel : Used to cancel the command that is currently being executed. The data to be written as a parameter with this command is arbitrary.

(4) Status : Used to read the contents of the status register in the TC8833F. Since the STATUS command can be executed while the TC8833F is in the busy state, it may be used to check whether the TC8833F is busy.

The bit definitions of the status register are given below.

DB0 (BUSY flag): Indicates the command processing state of the TC8833F. A High in this flag bit indicates that the TC8833F is executing a command and will accept no commands other than STATUS.

DB1 (EOS flag): Set to the Low level when the TC8833F is in the recording, playback, or pause state.

DB2 (RECORD flag): Set to the High level when the TC8833F is in the recording stand-by or recording operating state and to the Low level when the TC8833F is in the playback stand-by or playback operating state.

DB3 (BEEP flag): Set to the Highlevel when the TC8833F beeps.

The following status and data can be read when the TC8833F is in the 8-bit data bus mode:

DB4 (PAUSE flag) : Set to the High level when the TC8833F is in the pause state.

DB5-DB7 (XQ1-XQ3 data): Used t locate the current byte position of the command being executed. The current byte values listed in the table below indicate how many bytes have been processed. The TC8833F can accept OP code only when the byte position value indicated is 0.

Current byte position	XQ3	XQ2	XQ1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1

5.5.3 Command Description

(1) NOP
Does no operation.

DB3					DB0
	0	0	0	0	

(2) REC
Puts the TC8833F into the recording stand-by state.

DB3					DB0
	0	0	0	1	

(3) PLAY
Puts the TC8833F into the playback stand-by state.

DB3					DB0
	0	0	1	0	

(4) START
Starts recording or playback in the direct mode starting at the address designated by the address counter.

DB3					DB0
	0	0	1	1	

(5) STOP
Stops recording or playback. If the TC8833F is put in the record mode by LABEL command, the TC8833F loads the value of the address counter into the label index area. In the direct mode, this command is used to stop the recording or playback operation. If this command is issued when the TC8833F is in the pause state, the TC8833F enters the playback stand-by state.

DB3					DB0
	0	1	0	0	

(6) BUSREQ
Sets the memory interface pins into the high impedance state. A certain amount of time is required to actually put the pins into the high impedance state for reasons associated with pseudo S - RAM (see the description on the BUSREQ timing). when this input is Set again, the memory internal restores the origin state. A NOP command must be issued after the BUSREQ state is reset

DB3					DB0
	0	1	1	0	

(7) BEEP (Beep On / Off) DB3 | 0 | 1 | 1 | 1 | DB0

Causes the TC8833F to beep when this command is issued in the playback or recording stand - by state. Reissuing this command stops the beep.

(8) RESET (Reset On / Off) DB3 | 1 | 0 | 0 | 0 | DB0

Resets the internal circuitry of the TC8833F. The reset state can be cleared by issuing a NOP command.

(9) LABEL (Action By Label Mode) DB3 | 1 | 0 | 0 | 1 | DB0

The phrase number (0 - 127) is specified by the subsequent 2 nibbles of data in the 4 - bit control mode. The TC8833F starts recording or playback after this command is received. In the 8 - bit control mode, the phrase number is specified by the subsequent one nibble of data. The recording or playback operation is stopped by issuing a STOP command. In the recording mode, the TC8833F starts recording after loading the contents of the current address counter into the index area in memory. In the playback mode, the TC8833F starts playback after reading the start and stop address set from the index area in memory.

Phrase No.	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
0	*	0	0	0	0	0	0	0
1	*	0	0	0	0	0	0	1
2	*	0	0	0	0	0	1	0
125	*	1	1	1	1	1	0	1
126	*	1	1	1	1	1	1	0
127	*	1	1	1	1	1	1	1

(10) ADLD1 DB3 | 1 | 0 | 1 | 0 | DB0

Loads the subsequent 5 nibbles of data into the address counter in the 4-bit control mode. In the 8-bit control mode, the command loads the subsequent 3 nibbles of data into the address counter.

(11) ADLD2

DB3 | 1 | 0 | 1 | 1 | DB0

Loads the subsequent 5 nibbles of data into the stop address register in the 4-bit control mode. In the 8-bit control mode, the command loads the subsequent 3 nibbles of data into the stop address register.

(12) ADRD (Address Counter Value Read)

DB3 | 1 | 1 | 0 | 0 | DB0

Reads the content of the address counter. Data in read on the subsequent 5 read signals starting at the highest-order address position, 4 bits at time in the 4-bit control mode. In the 8-bit control mode, data is read on the subsequent 3 read signals starting at the highest-order address position, 8 bits at a time.

(13) DTRD (Memory Data Read)

DB3 | 1 | 1 | 0 | 1 | DB0

Reads the contents of memory. The data designated by the address counter is read on the subsequent 2 read signals in the 4-bit control mode. In the 8-bit control mode, data is read on the subsequent 1 read signal. The address counter is automatically incremented by 1 after the execution of a DTRD command. This command requires one dummy cycle. Consequently, two DTRD commands are required after decrement the address to be read by 1, with dummy data being read by the first command.

(14) DTWR (Memory Data Write)

DB3 | 1 | 1 | 1 | 0 | DB0

Writes data into memory. The subsequent 2 nibble of data are written into the address designated by the address counter in the 2-bit control mode. In the 8-bit control mode, the subsequent 1 nibble of data is written into memory. The address counter is automatically incremented by 1 after the execution of a DTWR command.

(15) CNDT (Condition Data Set)

DB3 | 1 | 1 | 1 | 1 | DB0

Initializes the TC8833F. This command must always be executed after system reset is carried out.

(a) BR1, BR0: Select the bit rate.

BR0	BR1	Bit rate
0	0	11 Kbps
0	1	16 Kbps
1	0	22 Kbps
1	1	32 Kbps

(b) FIX: Selects the block recording mode.
H = Set. L = Reset.

(c) R3, R2, R1, Select the memory type.

R3	R2	R1	Memory size
0	0	0	64 K
0	0	1	256 K
0	1	0	512 K
0	1	1	1 M
1	0	0	2 M
1	0	1	4 M

(d) M2, M1: Select the number of memory chips.

M2	M1	Memory Chips
0	0	1
0	1	2
1	0	3
1	1	4

(e) TRIG: Specifies the execution of trigger recording.
H=Enables trigger starting. L=Disables trigger starting.

(f) AOD: Detects a stop.
H=Detects a stop and stops addressing. L=Detects no stop.

(g) 4/8: Selects the 4- or 8-bi- date bus mode.
H=8bits (DB0-DB7). L=4bit- (DB0-DB3).

(h) CMSTBY CMSTBY: Enables or disables the stand-by state after termination of the CNDT command.
H=Puts the TC8833F into the stand-by state. L=Does not put the TC8833F into the stand-by state. This bit gets valid only after all bits are written with the CNDT command.

(i) T1-T4: Selects test modes 1 to 4.

T1 through T4 must be set all Low.

4 Bit BUS CONTROL

Command	First nibble				Second nibble				Third nibble			
	DB3	DB2	DB1	DB0	DB3	DB2	DB1	DB0	DB3	DB2	DB1	DB0
NOP	0	0	0	0	-	-	-	-	-	-	-	-
REC	0	0	0	1	-	-	-	-	-	-	-	-
PLAY	0	0	1	0	-	-	-	-	-	-	-	-
START	0	0	1	1	-	-	-	-	-	-	-	-
STOP	0	1	0	0	-	-	-	-	-	-	-	-
BUSREQ	0	1	1	0	-	-	-	-	-	-	-	-
BEEP	0	1	1	1	-	-	-	-	-	-	-	-
RESET	1	0	0	0	-	-	-	-	-	-	-	-
LABEL	1	0	0	1	PH3	PH2	PH1	PH0	*	PH6	PH5	PH4
ADLD1	1	0	1	0	A3	A2	A1	A0	A7	A6	A5	A4
ADLD2	1	0	1	1	A3	A2	A1	A0	A7	A6	A5	A4
ADRD	1	1	0	0	A3	A2	A1	A0	A7	A6	A5	A4
DTRD	1	1	0	1	D3	D2	D1	D0	D7	D6	D5	D4
DTWR	1	1	1	0	D3	D2	D1	D0	D7	D6	D5	D4
CNDT	1	1	1	1	R1	FIX	BR1	BR0	M2	M1	R3	R2

Command	4th nibble				5th nibble				6th nibble			
	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
NOP	-	-	-	-	-	-	-	-	-	-	-	-
REC	-	-	-	-	-	-	-	-	-	-	-	-
PLAY	-	-	-	-	-	-	-	-	-	-	-	-
START	-	-	-	-	-	-	-	-	-	-	-	-
STOP	-	-	-	-	-	-	-	-	-	-	-	-
BUSREQ	-	-	-	-	-	-	-	-	-	-	-	-
BEEP	-	-	-	-	-	-	-	-	-	-	-	-
RESET	-	-	-	-	-	-	-	-	-	-	-	-
LABEL	-	-	-	-	-	-	-	-	-	-	-	-
ADLD1	A11	A10	A9	A8	A15	A14	A13	A12	A19	A18	A17	A16
ADLD2	A11	A10	A9	A8	A15	A14	A13	A12	A19	A18	A17	A16
ADRD	A11	A10	A9	A8	A15	A14	A13	A12	A19	A18	A17	A16
DTRD	-	-	-	-	-	-	-	-	-	-	-	-
DTWR	-	-	-	-	-	-	-	-	-	-	-	-
CNDT	CMS TBY	4/8	AOD	TRIG	0	0	0	0	-	-	-	-

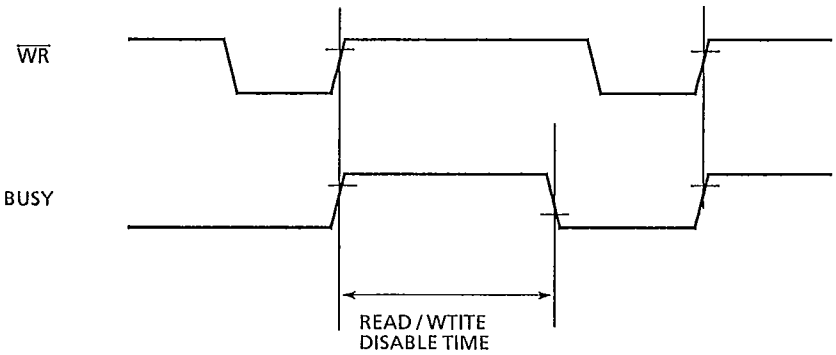
8 Bit BUS CONTROL

Command	First nibble								Second nibble							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
NOP	*	*	*	*	0	0	0	0	-	-	-	-	-	-	-	-
REC	*	*	*	*	0	0	0	1	-	-	-	-	-	-	-	-
PLAY	*	*	*	*	0	0	1	0	-	-	-	-	-	-	-	-
START	*	*	*	*	0	0	1	1	-	-	-	-	-	-	-	-
STOP	*	*	*	*	0	1	0	0	-	-	-	-	-	-	-	-
BUSREQ	*	*	*	*	0	1	1	0	-	-	-	-	-	-	-	-
BEEP	*	*	*	*	0	1	1	1	-	-	-	-	-	-	-	-
RESET	*	*	*	*	1	0	0	0	-	-	-	-	-	-	-	-
LABEL	*	*	*	*	1	0	0	1	*	PH6	PH5	PH4	PH3	PH2	PH1	PH0
ADLD1	*	*	*	*	1	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
ADLD2	*	*	*	*	1	0	1	1	A7	A6	A5	A4	A3	A2	A1	A0
ADRD	*	*	*	*	1	1	0	0	A7	A6	A5	A4	A3	A2	A1	A0
DTRD	*	*	*	*	1	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0
DTWR	*	*	*	*	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
CNDT	*	*	*	*	1	1	1	1	M2	M1	R3	R2	R1	FIX	BR1	BR0

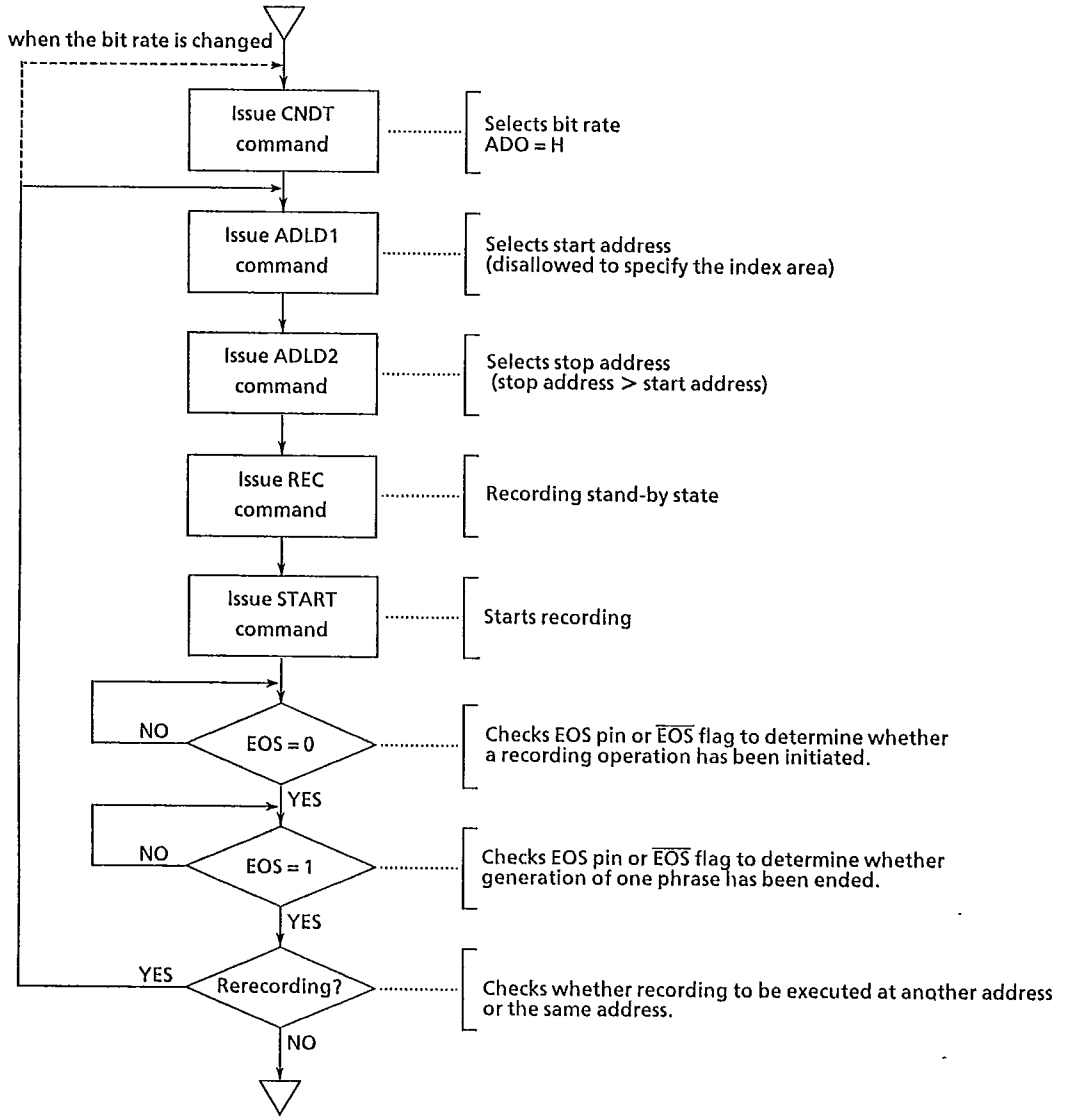
Command	Third nibble								4th nibble							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
NOP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
REC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PLAY	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
START	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
STOP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BUSREQ	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
BEEP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RESET	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LABEL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ADLD1	A15	A14	A13	A12	A11	A10	A9	A8	*	*	*	*	A19	A18	A17	A16
ADLD2	A15	A14	A13	A12	A11	A10	A9	A8	*	*	*	*	A19	A18	A17	A16
ADRD	A15	A14	A13	A12	A11	A10	A9	A8	*	*	*	*	A19	A18	A17	A16
DTRD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DTWR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CNDT	0	0	0	0	CMS TBY	4/8	AOD	TRIG	-	-	-	-	-	-	-	-

5.5.4 BUSY Output

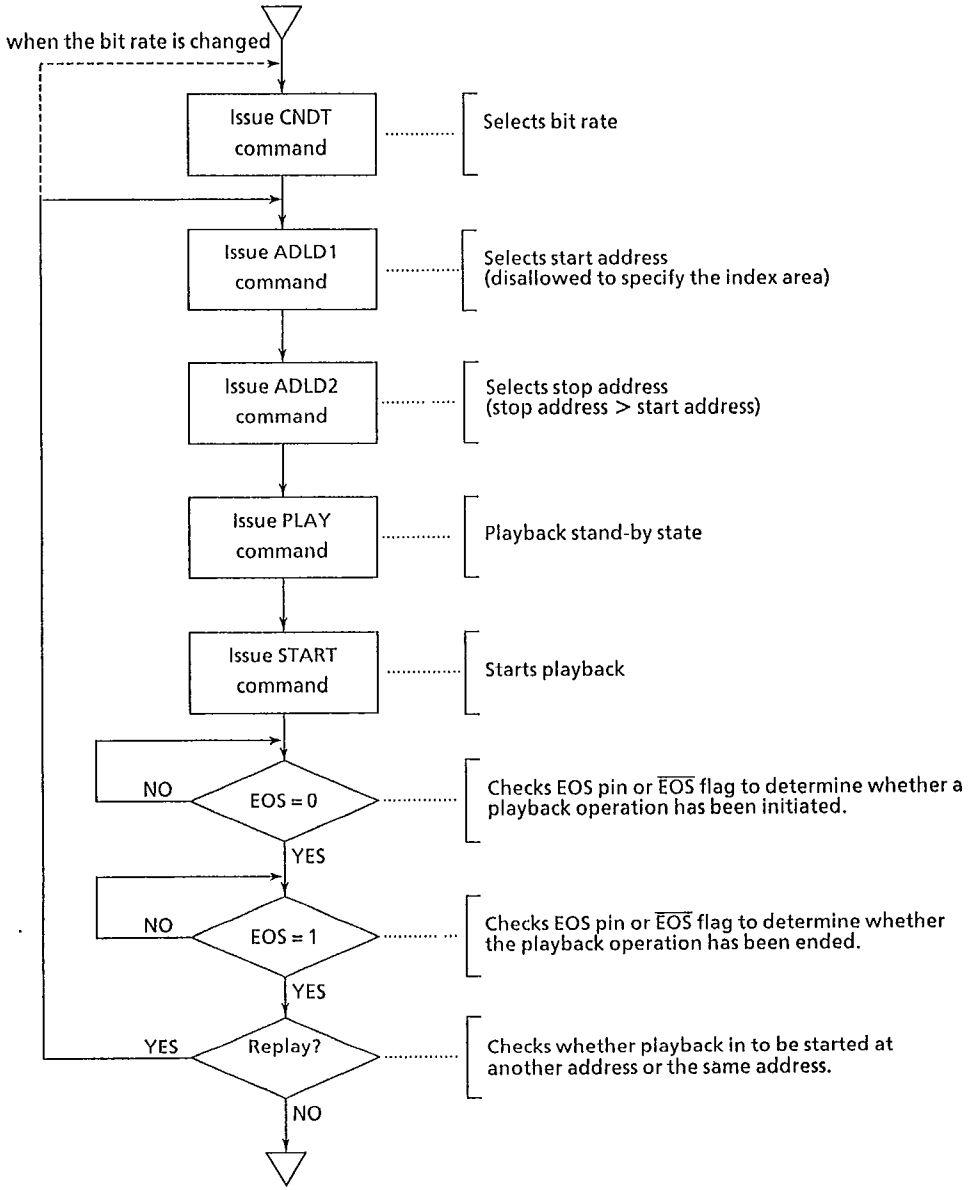
The TC8833F takes some time to execute its internal processing when is in instructed to read or writ data by the external CPU. After a write or read command is executed, a period occurs during which the subsequent access is inhibited (Read Write Disable Time). This period is called the busy period. The TC8833F sends the information identifying this period to the CPU controlling the TC8833F in the form of a BUSY flag. when the BUSY flag is set to the High level, the TC8833F accepts no command other than STATUS READ, CANCEL, and RESET. The BUSY flag is never set by the STATUS READ or CANCEL command.



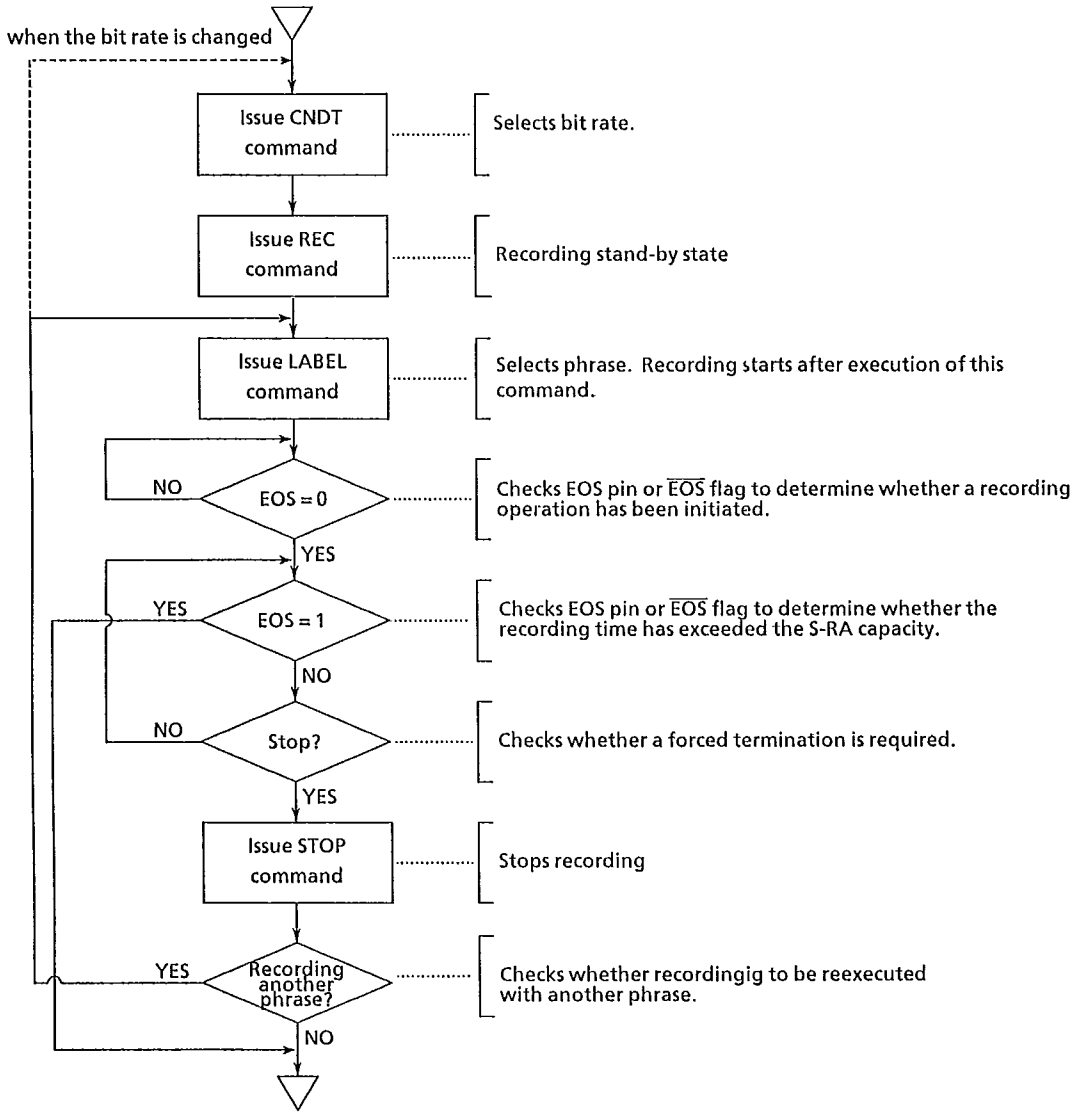
(1) Direct Mode Recording Process Flowchart



(2) Direct Mode Playback Process Flowchart



(3) Label Index Mode Recording Process Flowchart



(4) Label Index Mode Playback Proces- Flowchart

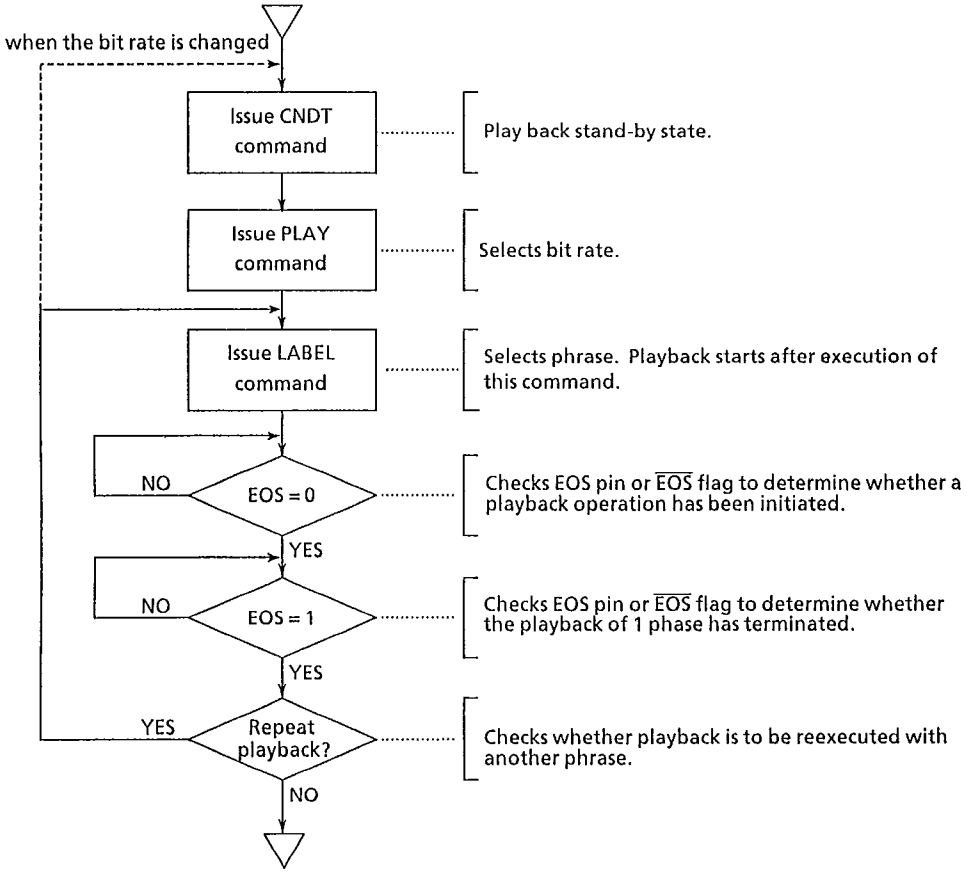


Fig 5.5.3 Label index mode playback sequence

5.6 Reset Operation

5.6.1 Reset Processin

The TC8833F is reset and all recording or playback operations are stopped when the pin ACL is set to the Low level or a RESET command is issued in the CPU control mode. In preparation for the use of pseudo S - RAM, the TC8833F resets at a timing that permits the self refreshing by pseudo S - RAM (see Figure 5 - 3 - 1). Consequently, a delay time of a maximum of 20 tsys (seconds) is required before the TC8833F actually resets itself (tsys = 1 / oscillation frequency).

5.6.2 TC8833F State After Reset

The TC8833F is put into the following state when pin ACL is reset to the High level or the RESET command is cleared in the CPU control mode:

(1) The playback stand - by state is turned on.
(2) The address counter is set to 400H.
(3) The address overflow detector is enabled.
(4) The bit rate is set to 11K bps.
(5) The data bus is set to the 4 - bit mode.
(6) The block recording flag (FIX) is disabled.
(7) The outputs A0, A16 - A3, A19, A4 - A15, and RFSH are all set to the Low level.
(8) The outputs CE1 - CE4, R / W, and OE are all set to the High - level.

5.6.3 Reset Processing at Power - On Time

The internal TC8833F circuitry is in an unstable state immediately after power is turned on. To run the TC8833F reliably, therefore, it is necessary to initiate a system reset using the ACL pin. Although a system reset may be attempted using a (RESET) command in the CPU control mode, such an attempt may not be executed properly since the contents of the reset register are unpredictable immediately after a power - on. Always use the ACL pin to perform a system reset at power - on time.

9097249 0025249 491 TOS3
TOSHIBA (UC/UP) 64E D

5.7 Stand-by Function

The TC8833F has the function to enter the stand - by state to sustain data in memory for extended periods and to conserve system power. By taking advantage of this feature, the user can take a backup copy of system data as well as memory data using a battery. There are three modes of placing the TC8833F into the stand - by state; the manual stand by mode in which the STBY pin is used to put the TC8833F into the stand - by state, the automatic stand by mode in which the TC8833F automatically enters the stand by state in the manual control mode, and the command stand - by mode in which a command is used in the CPU control mode to put the TC8833F into the stand - by state.

5.7.1 Manual Stand- by Mode

Setting pin STBY to the High level places the TC8833F into the stand - by state. The TC8833F remains in the stand - by state as long as pin STBY is held High. The stand - by state is cleared by resetting pin STBY to the Low level.

When pin STBY is set to the High level in the recording or playback operating state, the TC8833F takes actions to terminate the recording or playback operation and enters the stand - by state. If this occurs while the TC8833F is recording, the amount of data that has been recorded by the time pin STBY is set to the High level is valid.

5.7.2 Auto Stand-by Mode

The TC8833F automatically enters the stand - by state if no external operation is performed for a certain period of time while pin ATSTBY pin is held at the Low level in the manual control mode. The stand - by state that the TC8833F entered in this mode is reset and the TC8833F resumes normal operation immediately when either of pins DB0, DB1, or BEEP is set to the High level.

5.7.3 Command Stand-by Mode

The TC8833F can be put into the stand - by state using a command (CNDT) in the CPU control mode. The stand - by state that the TC8833F entered in the command stand - by mode is reset by setting pin CS to the Low level. That is, the TC8833F is reset from the stand - by state whenever an access is made to the TC8833F. The TC8833F does not take this access as carrying a command.

5.7.4 Stand-by State

The TC8833F takes the following actions when it enters the stand - by state:

a. Stops oscillation and stops all internal operations.
b. Disconnect the built - in pull - down resistances.
c. Shuts down power to the D / A converter.

d. Shuts down power to the microphone amplifier and band - pass filter.
e. Sets the microphone amplifier output to the high - impedance state.

5.7.5 Using the Stand-by State Function

The following precautions must be exercised when using the TC8833F stand - by function:

a. The auto stand - by function is disabled in the CPU control mode or when pin ATSTBY is set to the High level.
b. The TC8833F enters the stand - by state with all memory interface pins in the high - impedance state if pin STBY is set to the High level while the TC8833F is in the bus request state. Once this condition occurs, the memory interface pins remain in the high - impedance state even if the bus request state is reset. The memory interface pins are restored into the normal state by resetting the stand - by state and then resetting the bus request state.
c. The internal circuitry of the TC8833F is put into the stand - by state at the timing such that the pseudo S - RAM is put into the self - refreshing mode before the internal TC8833F circuitry enters the stand - by state. Consequently, a certain delay time is required. See Section 6.4, "AC Characteristics, " for the actual delay time required to put the TC8833F into the stand - by state.
d. The TC8833F is provided with the APD output that is used to shut down the external analog circuit.

5.8 Beep Function

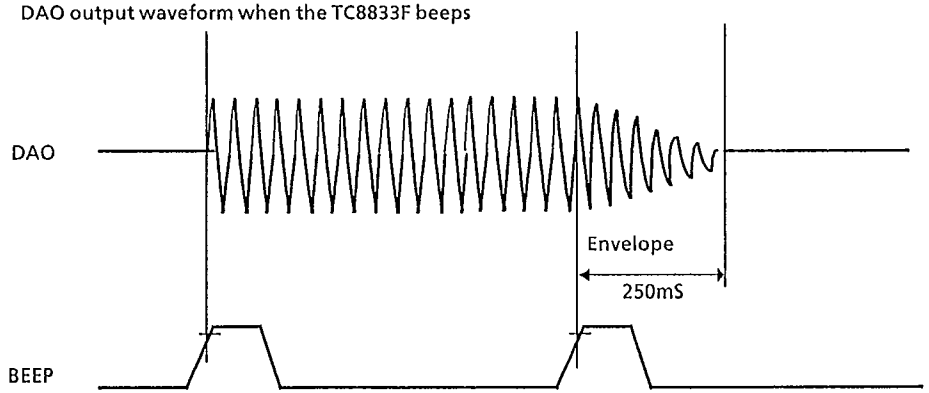
5.8.1 Using the Beep Function

The TC8833F sounds the beep when pin BEEP is set to the High level in the manual control mode. The TC8833F continues to beep as long as pin BEEP is held at the High level. The beep is stopped when pin BEEF is set to the Low level.
In the CPU control mode, the TC8833F starts beeping when a BEEP command is issued to the TC8833F. Issuing a second BEEP command stop the beep.

5.8.2 Specifications

The time required to converge the envelope of the 2 KHz DA0 waveform after the beep is turned off is 250 ms. The TC8833F can beep only in the recording or playback stand - by state. Attempts to sound the beep in any other states are ignored.

DAO output waveform when the TC8833F beeps



5.8.3 Considerations

Pin BEEP takes precedence over pin DB1 when both are set to the High level simultaneously. After the beep is stopped, the TC8833F takes the action directed by the START or TSTART signal that is automatically supplied. When the above mentioned condition occurs while the TC8833F is in a recording or playback operation, the sounds the beep after stopping the current operation.

5.9 Bus Request Mode

The bus request mode is used to electrically release the memory that is connected to the TC8833F. Since access to memory from external devices is enabled when this mode is on, memory data can be transferred at high speeds using a DMA controller or similar device.

5.9.1 Setting the Bus Request Mode

All memory interface pins are set to the high - impedance state by setting pins CHAT and CPUM to the High level setting pins BR0 and BR1 to the Low level is the manual control mode and by issuing a BUSREQ command is the CPU control mode. The bus request mode can be turned on only when the TC8833F is in the recording or playback stand - by state. The TC8833F sets pins BUSB to the Low level when it enters the bus request mode.

5.9.2 Establishing the Bus Request Mode

The bus request mode is established at the timing shown is Figure 5 - 9 - 1 for reasons associated with pseudo S - RAM. This is required because the bus request mode must be turned on after the pseudo S - RAM is put into the self - refreshing mode.

5.9.3 Passing Memory DATA is the Bus Request Mode

The pseudo S - RAM is in the self - refreshing mode when it enters the high - impedance state. If the TC8833F side of memory is disconnected in this state, the control inputs (CE, RFSH, etc.) get unstable, resulting in data corruption. To avoid this, pin RFSH must be pulled down and pin CEx must be pulled up. In this way, pseudo S - RAM can sustain its datam in the self refreshing mode until it is controlled by the receiving side (see Figure 5 - 6 - 3).

5.9.4 Resetting the Bus Request Mode

The TC8833F returns to the original bus mode when the bus request mode conditions are dissatisfied in the manual control mode or when a command is issued the second time in the CPU control mode. The TC8833F sets pin BUSM to the High level when the bus request mode is turned off.

5.10 Automatic Address Option Output Select Function

16 address pins (A0 - A15) are normally used to address TC8833F memory. The TC8833F provides the user with the option to redirect the higher order address bits (A16 - A19) to pins CE2, CE3, CE4, and ALE according to the number of memory chips installed. See Section 5.11, "Connecting Memory Chips," for examples of memory connection.

The table below summarizes the number of memory chips and address outputs to be used.

Address- Outputs

Number of memory chips	Input- setting		Output- (optiona- pins)				
	M2	M1	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	ALE
1	0	0	$\overline{CE1}$	(A18)	(A17)	(A16)	(A19)
2	0	1	$\overline{CE1}$	$\overline{CE2}$	(A17)	(A16)	ALE
3	1	0	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	(A16)	ALE
4	1	1	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	ALE

The number of memory chips is initialized to 4 at a reset time. This setting remains valid until the TC8833F enters the playback or recording state.

*$\overline{CE1}$ is not outputted when the accessed address overs 4Mbits. Therefore $\overline{OE}$ in used instead of $\overline{CE1}$ in this case.

5.11 Memory Map

Since a memory area for label indexes is required when the TC8833F is run in the label index mode in the manual or CPU control configuration, the area from addresses 0H through 3FFH cannot be used to store voice data. In the direct mode, on the other hand, the entire memory area is available as the voice data area.

Fig 5.11.1 Direct Mode Memory Map

	64 kbit	256 kbit	512 kbit	1 Mbit	2 Mbit	4 Mbit
MEMORY 1	00000H~ 01FFFH	00000H~ 07FFFH	00000H~ 0FFFFH	00000H~ 1FFFFH	00000H~ 3FFFFH	00000H~ 7FFFFH
MEMORY 2	02000H~ 03FFFH	08000H~ 0FFFFH	10000H~ 1FFFFH	20000H~ 3FFFFH	40000H~ 7FFFFH	80000H~ FFFFFH
MEMORY 3	04000H~ 05FFFH	10000H~ 17FFFH	20000H~ 2FFFFH	40000H~ 5FFFFH	80000H~ BFFFFH	-
MEMORY 4	06000H~ 07FFFH	18000H~ 1FFFFH	30000H~ 3FFFFH	60000H~ 7FFFFH	C0000H~ FFFFFH	-

Fig 5.11.2 Label Index Mode Memory Map

	64 kbit	256 kbit	512 kbit	1 Mbit	2 Mbit	4 Mbit
MEMORY 1	00400H~ 01FFFH	00400H~ 07FFFH	00400H~ 0FFFFH	00400H~ 1FFFFH	00040H~ 3FFFFH	00400H~ 7FFFFH
MEMORY 2	02000H~ 03FFFH	08000H~ 0FFFFH	10000H~ 1FFFFH	20000H~ 3FFFFH	40000H~ 7FFFFH	80000H~ FFFFFH
MEMORY 3	04000H~ 05FFFH	10000H~ 17FFFH	20000H~ 2FFFFH	40000H~ 5FFFFH	80000H~ BFFFFH	-
MEMORY 4	06000H~ 07FFFH	18000H~ 1FFFFH	30000H~ 3FFFFH	60000H~ 7FFFFH	C0000H~ FFFFFH	-

Fig 5.11.3 Label Index Area Memory Map

	RAM address (HEX)	RAM data							
		D7	D6	D5	D4	D3	D2	D1	D0
Phrase No.0 start address	00_H	A7	A6	A5	A4	A3	A2	A1	A0
	01_H	A15	A14	A13	A12	A11	A10	A9	A8
	02_H	-	-	-	-	A19	A18	A17	A16
	03_H	*	*	*	*	*	*	*	*
Phrase No.0 end address	04_H	A7	A6	A5	A4	A3	A2	A1	A0
	05_H	A15	A14	A13	A12	A11	A10	A9	A8
	06_H	-	-	-	-	A19	A18	A17	A16
	07_H	*	*	*	*	*	*	*	*
Phrase No.1 start address	08_H	A7	A6	A5	A4	A3	A2	A1	A0
	09_H	A15	A14	A13	A12	A11	A10	A9	A8
	$0A_H$	-	-	-	-	A19	A18	A17	A16
	$0B_H$	*	*	*	*	*	*	*	*
Phrase No.1 end address	$0C_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$0D_H$	A15	A14	A13	A12	A11	A10	A9	A8
	$0E_H$	-	-	-	-	A19	A18	A17	A16
	$0F_H$	*	*	*	*	*	*	*	*
Phrase No.126 end address	$3F4_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$3F5_H$	A15	A14	A13	A12	A11	A10	A9	A8
	$3F6_H$	-	-	-	-	A19	A18	A17	A16
	$3F7_H$	*	*	*	*	*	*	*	*
Phrase No.127 start address	$3F8_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$3F9_H$	A15	A14	A13	A12	A11	A10	A9	A8
	$3FA_H$	-	-	-	-	A19	A18	A17	A16
	$3FB_H$	*	*	*	*	*	*	*	*
Phrase No.127 end address	$3FC_H$	A7	A6	A5	A4	A3	A2	A1	A0
	$3FD_H$	A15	A14	A13	A12	A11	A10	A9	A8
	$3FE_H$	-	-	-	-	A19	A18	A17	A16
	$3FF_H$	*	*	*	*	*	*	*	*

Asterisks represent those bits that are not written by the TC8833F as a start or end address in the label index mode. Consequently, these bits may be used to store the phrase bit rate or other information.

5.12 Selecting the Phrase Block Mode

The recording time may be set to any value in ordinary phrase recording. If a phrase is are to be recorded over a prerecorded phrase, however, a new phrase may overwrite another existing phrase unless the recording time for the new phrase is shorter than that for the old phrase.

The TC8833F supports a phrase block mode in which the memory areas available for phrases are separately defined and limited. This ensures that new phrases can be recorded over prerecorded phrases without overwriting existing phrases in different areas.

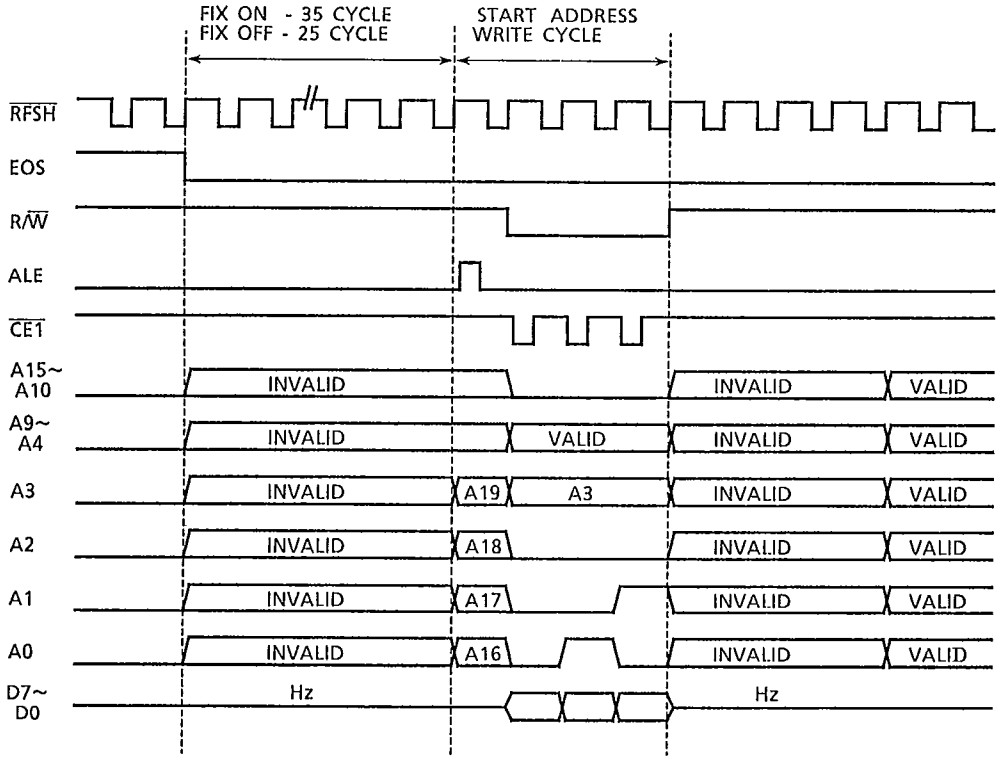
The phrase block mode is turned on by setting pin BUSY to the High level in the manual control mode and by specifying FIX in the CNDT mode in the CPU control mode. Memory areas are allocated to the phrases as summarized in the table below according to the size and number of memory chips.

Memory - size		DB7	DB6	ADR	M2	M1	Phrase No.0	Phrase No.1	Phrase No.2	Phrase No.3
	Quantity									
64K	1	0	0	0	0	0	00400H~ 01FFFH	*	*	*
	2	0	0	0	0	1	00400H~ 01FFFH	02000H~ 03FFFH	*	*
	3	0	0	0	1	0	00400H~ 01FFFH	02000H~ 03FFFH	04000H~ 05FFFH	*
	4	0	0	0	1	1	00400H~ 01FFFH	02000H~ 03FFFH	04000H~ 05FFFH	06000H~ 07FFFH
256K	1	0	0	1	0	0	00400H~ 01FFFH	02000H~ 03FFFH	04000H~ 05FFFH	06000H~ 07FFFH
	2	0	0	1	0	1	00400H~ 07FFFH	08000H~ 0FFFFH	*	*
	3	0	0	1	1	0	00400H~ 07FFFH	08000H~ 0FFFFH	10000H~ 17FFFH	*
	4	0	0	1	1	1	00400H~ 07FFFH	08000H~ 0FFFFH	10000H~ 17FFFH	18000H~ 1FFFFH
1M	0	0	1	1	0	0	00400H~ 07FFFH	08000H~ 0FFFFH	10000H~ 17FFFH	18000H~ 1FFFFH

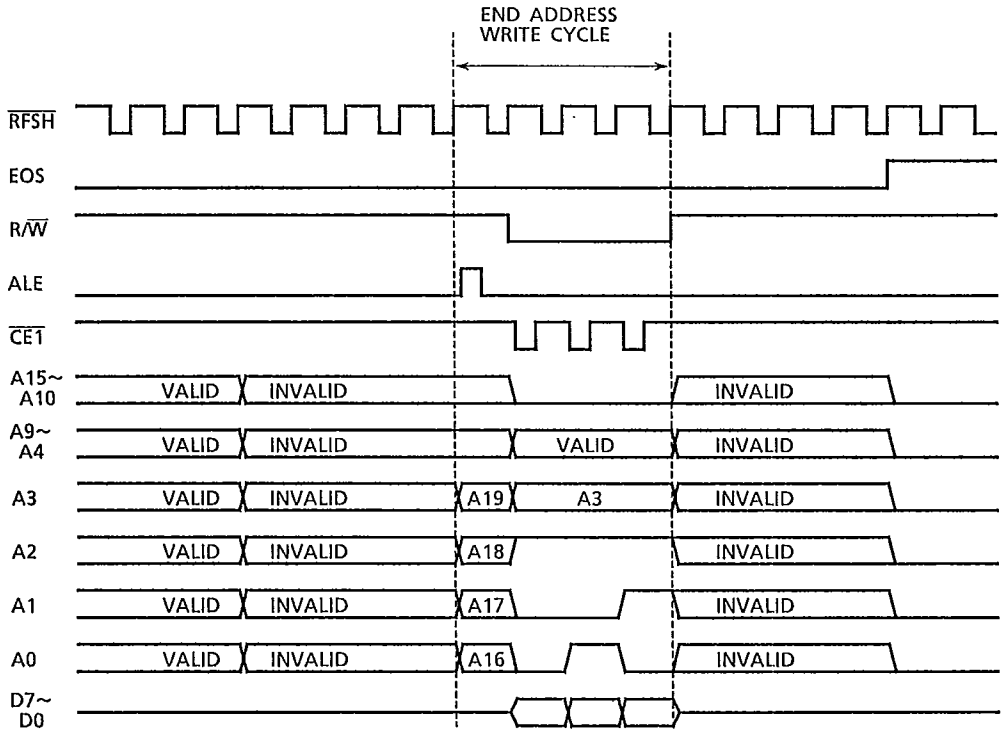
Asterisks in the table identify the phrases that are not available due to the lack of memory. The phrase - memory - area combinations other than listed above are not supported. Do not specify any phrase number other than 0, 1, 2, and 3 when performing block mode recording or playback in the label index mode in the CPU control configuration.

5.13 Memory Interface Timing

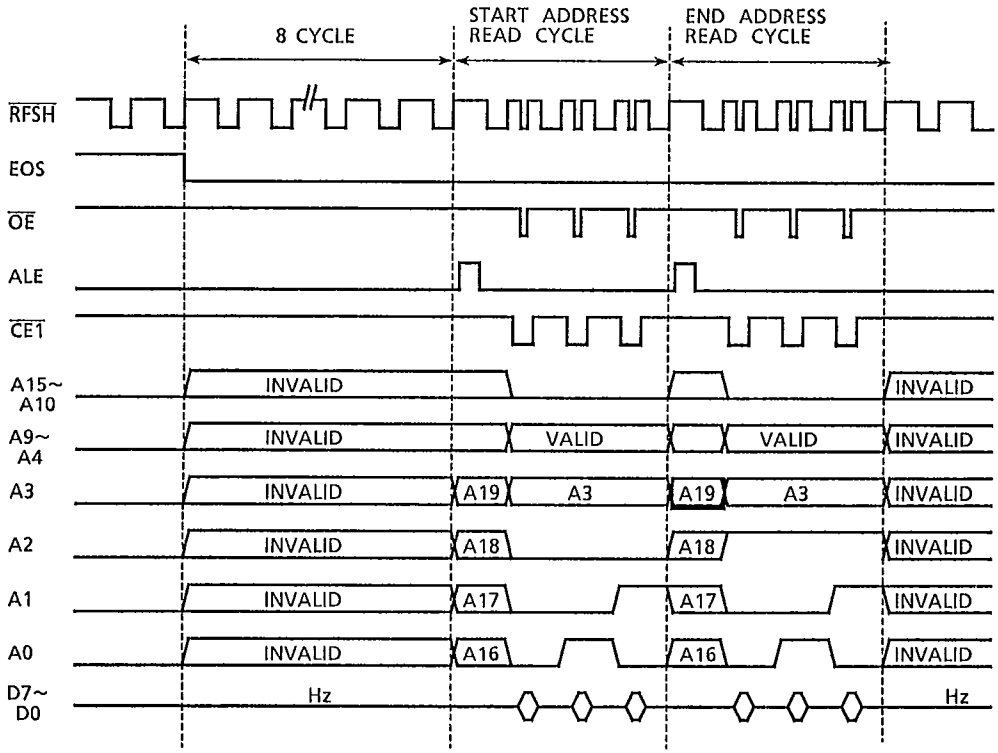
5.13.1 LABEL INDEX MODE - Start Address Write Cycle



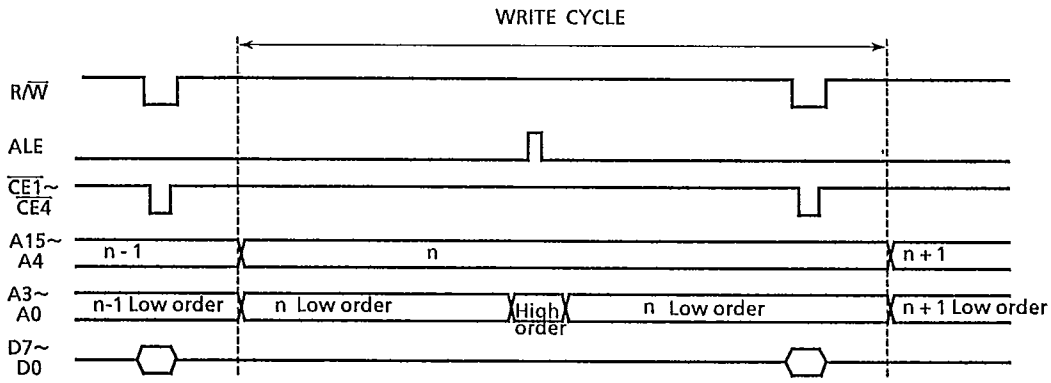
5.13.2 LABEL INDEX MODE - End Address Write Cycle



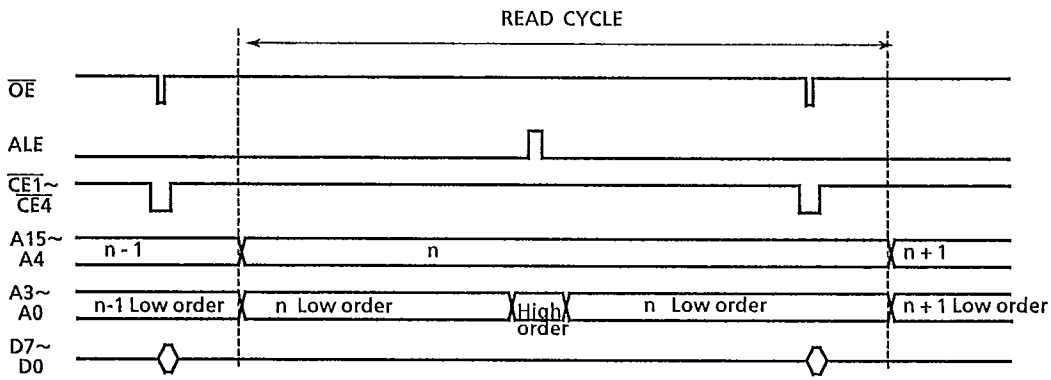
5.13.3 LABEL INDEX MODE - Star and End Address Read Cycle



5.13.4 Memory Write Cycle



Voice Data Write Cycle

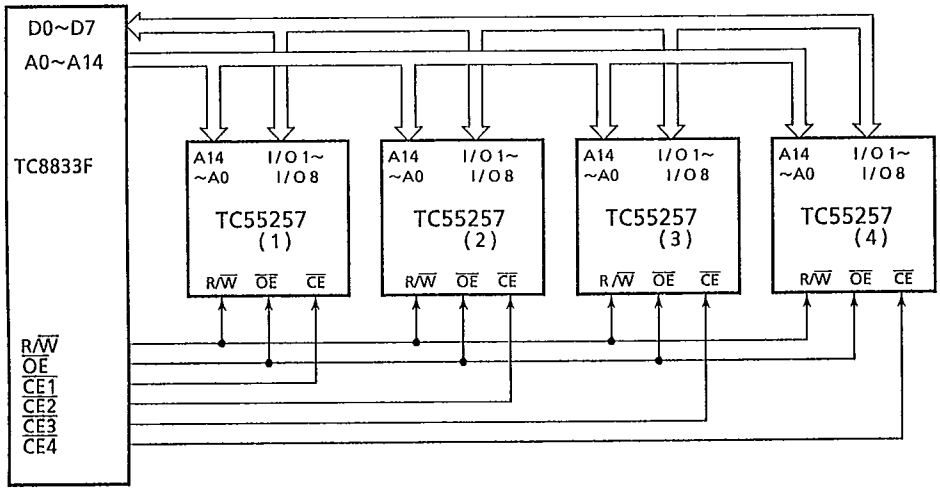


Voice Data Read Cycle

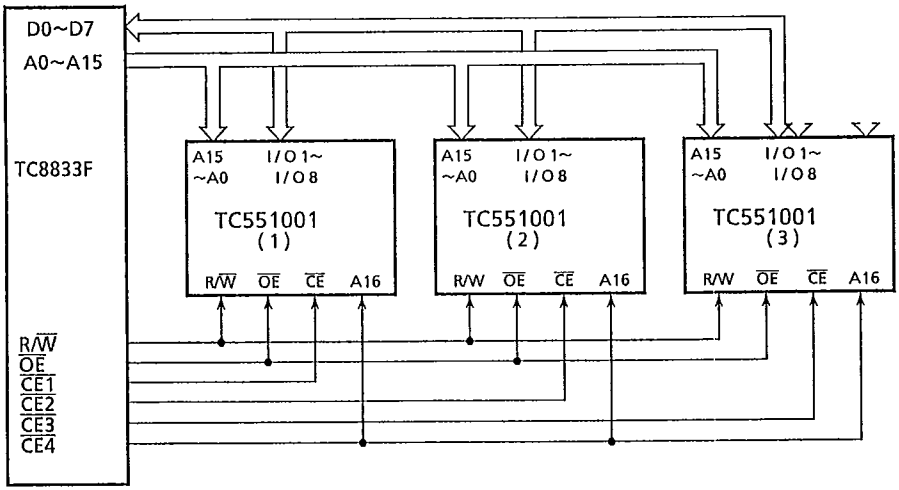
5.14 Connection Diagram

5.14.1 STATIC - RAM Connection Diagrams

256 k Bit × 4

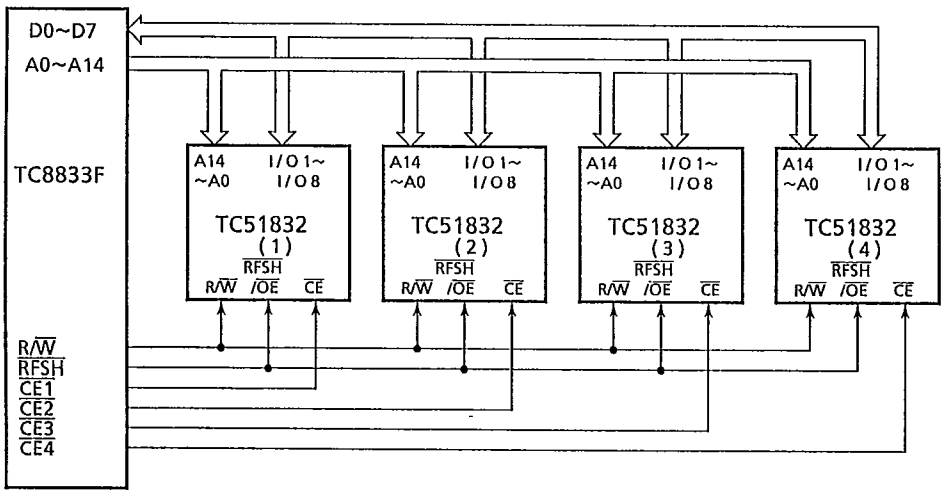


1 M Bit × 4



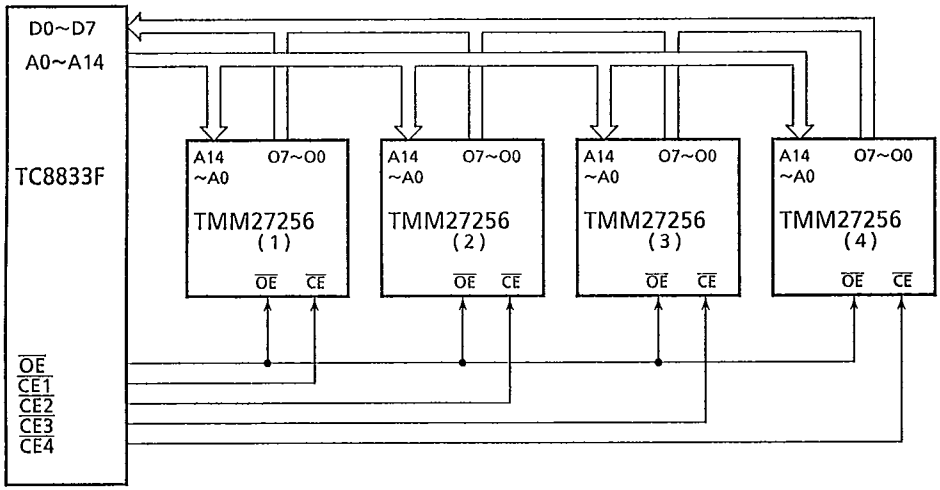
5.14.2 Pseudo Static - RAM Connection Diagram

256 k Bit × 4

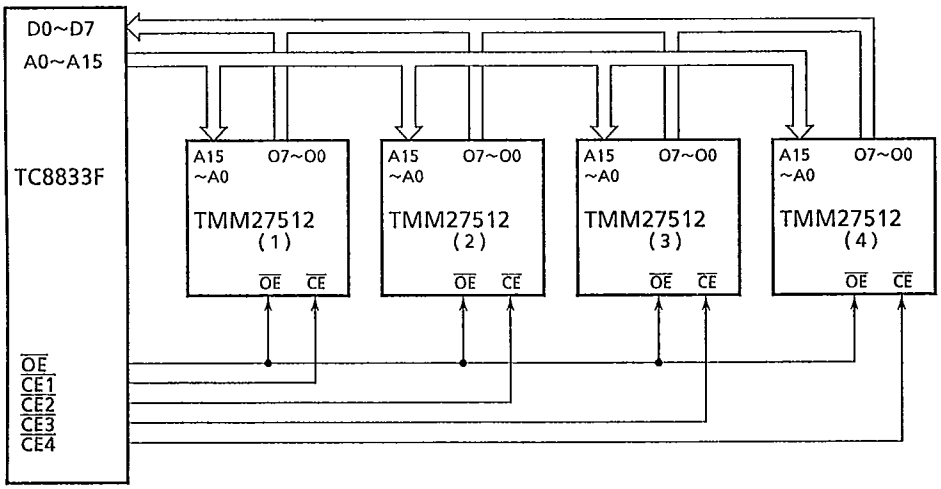


5.14.3 ROM Connection Diagrams

256 k Bit × 4



512 k Bit × 4

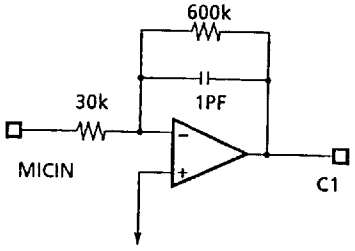


5.15 Analog Blocks

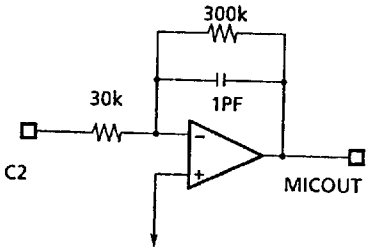
The TC8833F incorporates a microphone amplifier and a band - pass filter. It can be configured to form a voice recording / playback system simply by attaching an external microphone and loudspeaker amplifier.

5.15.1 Microphone Amplifier

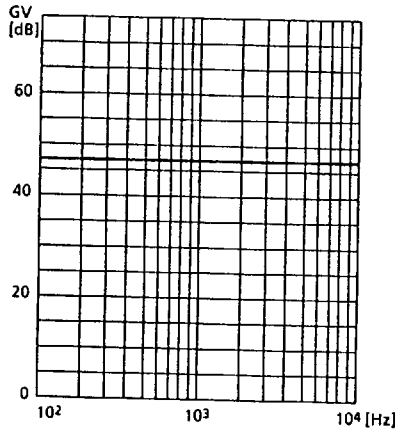
The microphone amplifier block is divided into two sub blocks, called the microphone amplifier 1 having a gain of approximately 20 dB and the microphone amplifier 2 having a gain of approximately 10 dB.



Microphone amplifier 1 equivalent circuit



Microphone amplifier 2 equivalent circuit

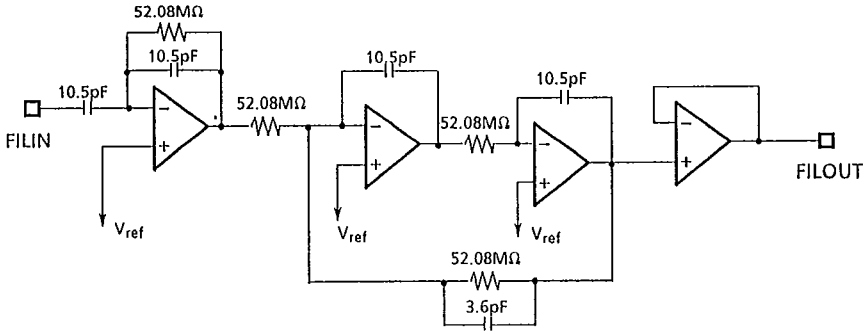


Microphone amplifier frequency characteristic

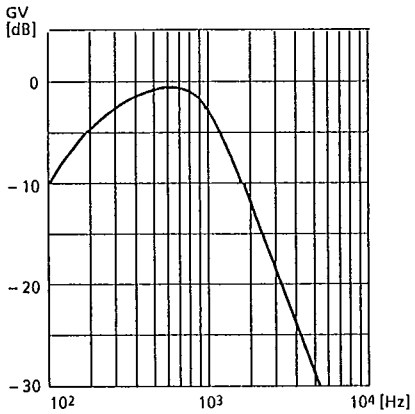
The above characteristic is obtained by measuring the output across pins MICIN and MICOUT with pins C1 and C2 coupled by a 0.1 -μF depletion - layer ceramic capacitor. The microphone amplifier 2 is enabled only when the TC8833F is in the recording stand - by state.

5.15.2 Filter Block

The TC8833F is provided with a primary high - pass filter and a secondary low-pass filter.



Band-pass filter equivalent circuit



Band-pass filter frequency characteristic

The above characteristic is obtained by measuring the output across pins FILIN and FILOUT.

Note: Digital noises may routed into the TC8833F, causing noise interferences. To suppress noise interferences, it is recommended that both analog and digital blocks be grounded separately.

6. ELECTRIC CHARACTERISTICS

6.1 Absolute Maximum Ratings

Symbol	Item	Specification	Unit
VDD	Power voltage	−0.3~6.0	V
VIN	Input voltage	−0.3~VDD + 0.3	V
VOUT	Output voltage	−0.3~VDD + 0.3	V
TSTG	Storage temperature	−55~125	°C

6.2 Recommended Operating Conditions

Symbol	Item	Specification	Unit
VDD	Power voltage	4.5~5.5	V
VIN	Input voltage	0~VDD	V
VOUT	Output voltage	0~VDD	V
TOPR	Storage temperature	−10~70	°C

6.3 DC Characteristics (VDD = 5.0 ± 10%, VSS = 0.0V, Ta = 75°C unless otherwise specified)

Symbol	Item	Condition	Specification			Unit	Remarks
			Minimum	Typical	Maximum		
f_{OPR}	Operating frequency	V_{DD} = 2.4~5.5V	512	640	768	KHz	
V_{OPR}	Operating power voltage	f_{OPR} = 512~768KHz	4.5	5.0	5.5	V	
V_{STBY}	Stand - by power voltage		2.2	—	5.5	V	
I_{DD} 1	Operating current consumption 1	Logic block	—	—	3.0	mA	
I_{DD} 2	Operating current consumption 2	Analog block	—	—	3.0	mA	
I_{DD} 3	Stand - by current consumption		—	—	3.0	μA	
V_{IH} 1	High level input current 1		VDD−0.6	—	—	V	1
V_{IL} 1	Low level input current 2		—	—	0.6	V	1
V_{IH} 2	High level input current 2		VDD−1.5	—	—	V	2
V_{IL} 2	Low level input current 2		—	—	1.5	V	2
V_{IH} 3	High level input current 3		2.2	—	—	V	3
V_{IL} 3	Low level input current 3		—	—	0.8	V	3
I_{OH}	High level input current	V_{OH} = 2.4V	−0.6	—	—	mA	
I_{OL}	Low level input current	V_{OL} = 0.4V	0.6	—	—	mA	
I_{IH} 1	High level output current 1	VDD = 5.0 V	25	50	100	μA	4
I_{IH} 2	Low level output current 2		—	—	1.0	μA	5
I_{IL} 1	High level input current 1		−50	−100	−200	μA	2
I_{IL} 2	Low level input current 2	VDD = 5.0 V	—	—	1.0	μA	6
V_{OUT}	Output voltage	V_{DD} = 5.0V	2.3	2.5	2.7	V	7
V_{STA}	Oscillation start voltage	f = 640KHz cera - lock	2.4	—	—	V	
V_{HOLD}	Oscillation hold voltage	f = 640KHz cera - lock	2.2	—	—	V	

Notes:

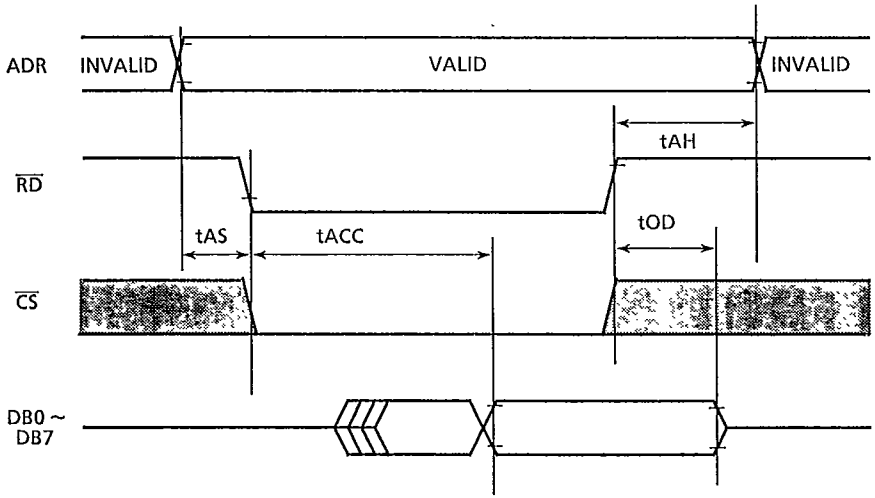
1. XIN pin.
2. $\overline{ACL}$ pin.
3. All input ad input / output pins excluding XIN.
4. Pins DB0, DB1, DB2, DB3, DB4, DB5, BEEP, $\overline{RD}$, $\overline{WR}$, and $\overline{CE}$ in the manual control mode.
5. Above listed pins and other input pins in the CPU control mode.
6. All input pins excluding $\overline{ACL}$.
7. Analog reference voltage output (Vref) pin.

6.4 AC Characteristics

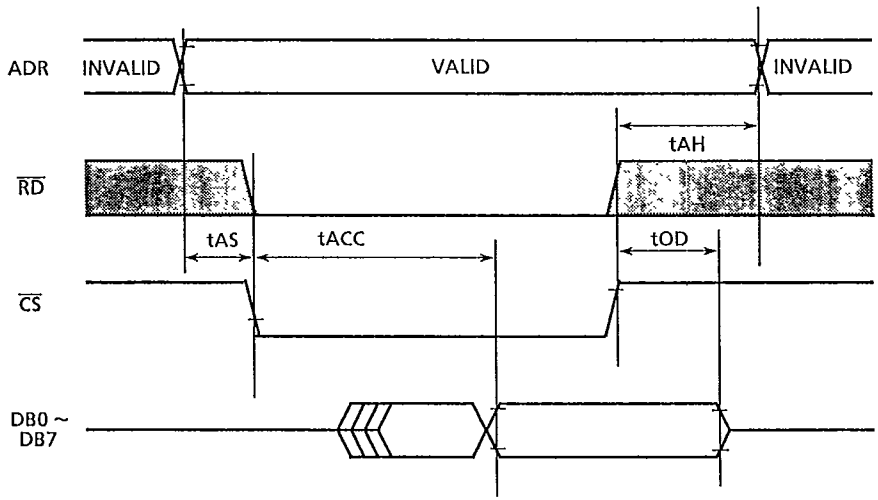
Symbol	Item	Specification		Unit
		Minimum	Maximum	
tAS	ADR setup time	100	—	ns
tAH	ADR hold time	20	—	ns
tACC	Read access time	—	220	ns
tOD	Output disable time	20	—	ns
tWRP	WR pulse width	250	1000	ns
tDS	Data setup time	250	—	ns
tDH	Data hold time	20	—	ns
tASM	Address setup time	1/2*SYS -200	—	ns
tAHM	Address hold time	1/2*SYS -200	—	ns
tCE	CE low - level pulse width	2*SYS -200	—	ns
tCSR	RFSH setup time	1/2*SYS -200	—	ns
tCHR	RFSH hold time	1/2*SYS -200	—	ns
tCS	OE setup time	1/2*SYS -200	—	ns
tCH	OE hold time	1/2*SYS -200	—	ns
tREF	RFSH low - level pulse width	SYS -200	—	ns
tDWS	Data input setup time	250	—	ns
tDWH	Data input hold time	0	—	ns
tOE	OE low - level pulse width	SYS -200	—	ns
tDCS	Data output setup time	1/2*SYS -200	—	ns
tDCH	Data output hold time	1/2*SYS -200	—	ns

SYS = 1 / XIN When XIN = 640 kHz SYS = 1.56μS

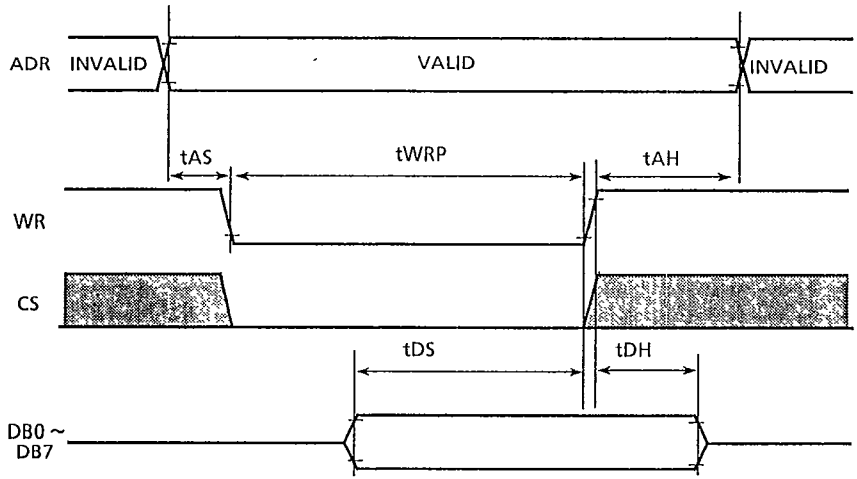
CPU I/F



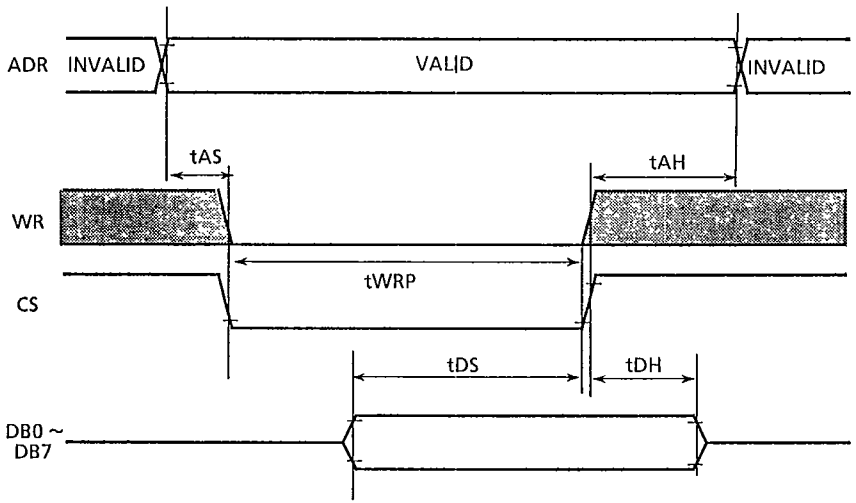
READ CYCLE (1)



READ CYCLE (2)



WRITE CYCLE (1)



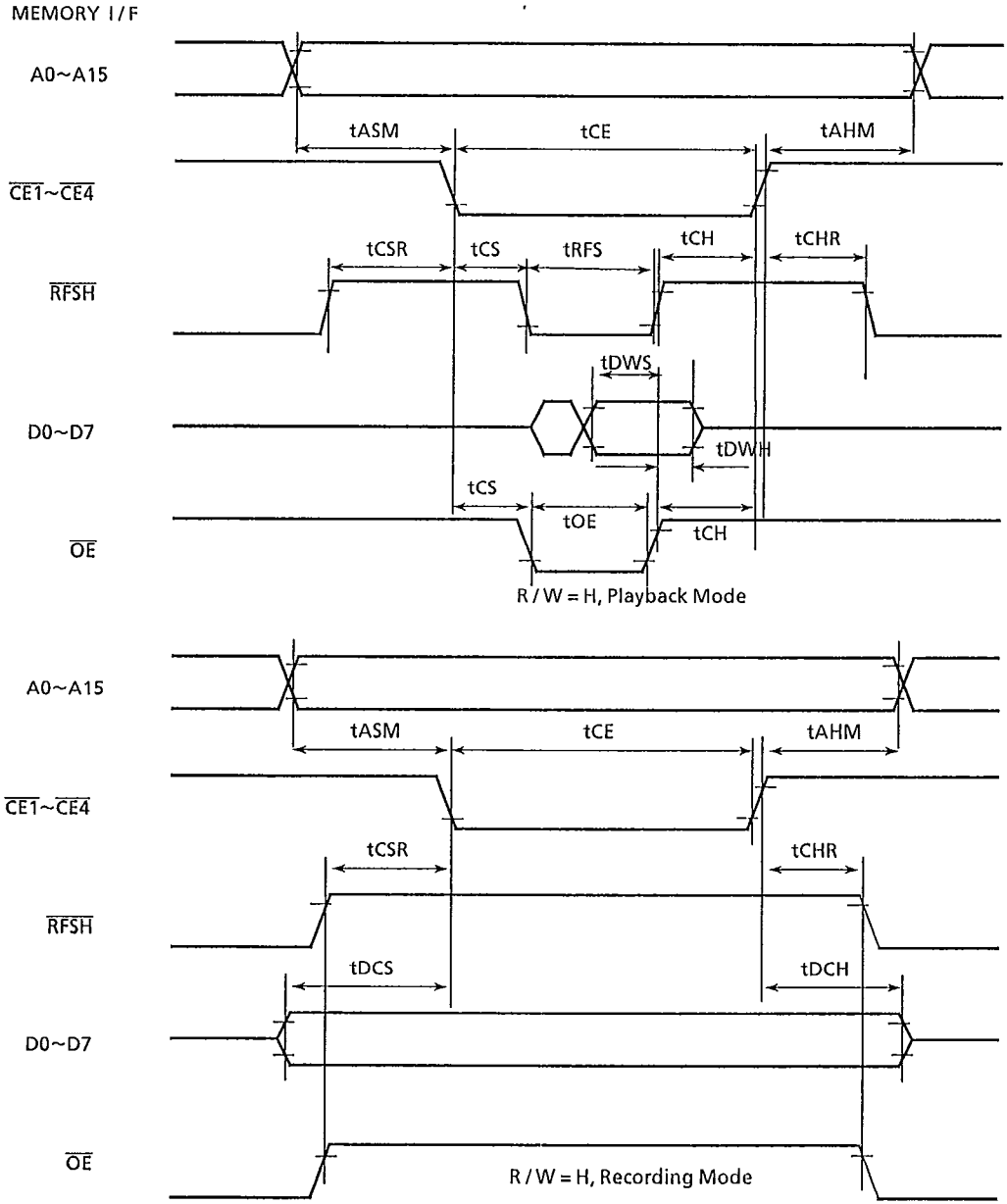
WRITE CYCLE (2)

MEMORY I/F

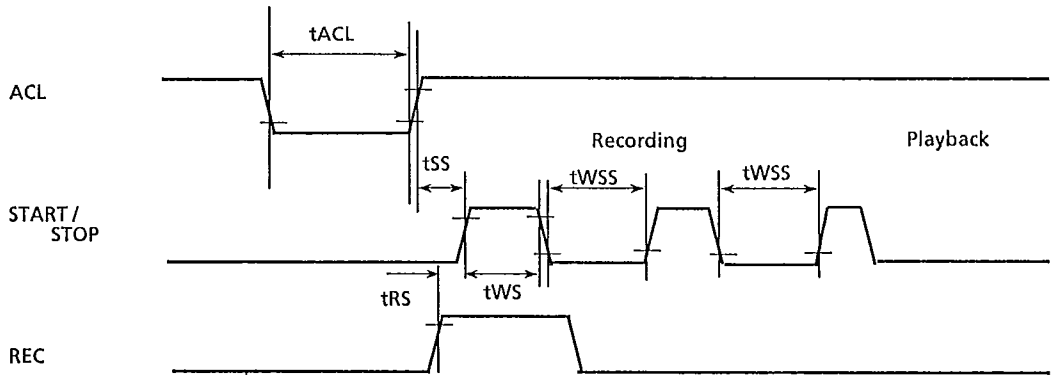
Symbol	Item	Specification	
		Minimum	Maximum
Ts CEf (A)	Address setup time to fall of CE	1/2*SYS - 200ns	—
Th CEr (A)	Address hold time from rise of CE	1/2*SYS – 200ns	—
Ts CEf (RFSHr)	RFSH rise time to fall of CE	1/2*SYS – 200ns	—
Ts RFSHf (CEf)	CE fall time to fall of RFSH	1/2*SYS – 200ns	—
Ts CEr (RFSHr)	RFSH rise time to rise of CE	1/2*SYS – 200ns	—
Th CEr (RFSHh)	RFSH = "H" hold time from rise of CE	1/2*SYS – 200ns	—
Tw RFSH1	RFSH low - level pulse width	SYS – 200ns	—
Ts RFSHr (D)	Data setup time to rise of RFSH	250ns	—
Th RFSHr (D)	Data hold time from rise of RFSH	0	—
Ts OEr (D)	Data setup time to rise of OE	250ns	—
Th OEr (D)	Data hold time from rise of OE	0	—
Ts OEf (CEf)	CE fall time to fall of OE	1/2*SYS – 200ns	—
TWOE1	OE low - level pulse width	SYS – 200ns	—
TWCE1	CE low - level pulse width	2*SYS – 200ns	—
Ts CEf (DO)	Data output setup time to fall of CE	1/2*SYS – 200ns	—
Ts CEf (RWf)	R/W = "L" setup time to fall of CE	1/2*SYS – 200ns	—
Th CEfr(DO)	Data output hold time from rise of CE	1/2*SYS – 200ns	—
Th CEfr(RWf)	R/W = "L" hold time from rise of CE	1/2*SYS – 200ns	—
Ts CEr (OEr)	OE rise time to rise of CE	1/2*SYS – 200ns	—

SYS = 1/XIN When XIN = 640 KHz SYS = 1.56μS

MEMORY I/F


A0~A15
tASM
tCE
tAHM
CE1~CE4
tCSR
tCS
tRFS
tCH
tCHR
RFSH
tDWS
D0~D7
tDWH
tCS
tOE
tCH
OE
R / W = H, Playback Mode
A0~A15
tASM
tCE
tAHM
CE1~CE4
tCSR
tCHR
RFSH
tDCS
tDCH
D0~D7
OE
R / W = H, Recording Mode

Manual Control



Symbol	Item	Specification		Unit
		Minimum	Maximum	
tACL	ACL pulse width	1.56	—	μs
tSS	Initialize time	2.25	—	ms
tWS	Start and stop pulse width	62.5 *(64)	—	μs (ms)
tWSS	Pulse inhibit time	7.8 *(39.8)	—	ms
tRS	REC setup time	7.8 *(39.8)	—	ms

Note In manual control mode:
*CHAT=L

6.5 Analog Block Characteristics

(1) Microphone Amplifier

(VSS1 = VSS2 = 0V, VDD - 5.0V, Ta = 25°C, fin = 1 KHz unless otherwise specified)

Item	Symbol	Applicable Pin	Condition	Specification			Unit
				Minimum	Typical	Maximum	
Passing band voltage gain	V_{IN1}	MICAMP1	VIN = 6mVp-p fin = 100Hz~10KHz	-	26	-	dB
Passing band voltage gain	V_{IN2}	MICAMP2	Output load = 100kΩ	-	20	-	dB
Total harmonic distortion	V_{G1}	MICAMP1	Vin = 6mVp-p	-	2	-	%
Total harmonic distortion	V_{G2}	MICAMP2	Vin = 6mVp-p	-	2	-	%
Maximum permissible input voltage	V_{IN1}	MICAMP1		-		200	mVp-p
Maximum permissible input voltage	V_{IN2}	MICAMP2		-		400	mVp-p
Input impedance	R_{IN1}	MICAMP1		-	30	-	kΩ
Input impedance	R_{IN2}	MICAMP2		-	30	-	kΩ

(2) Band - pass Filter

(VSS1 = VSS2 = 0V, VDD - 5.0V, Ta = 25°C, fin = 1 KHz unless otherwise specified)

Item	Symbol	Condition	Specification			Unit
			Minimum	Typical	Maximum	
Passing band voltage gain	V_G	Output load = 100kΩ 3pF	-	0	-	dB
Total harmonic distortion	T_{HD}	VIN = 1.0p-p	-	4	-	%
Maximum permissible input voltage	V_{IN}	FILIN	-	4.0	-	Vp-p
Output impedance	R_{OUT}	FILOUT	-	1	-	kΩ

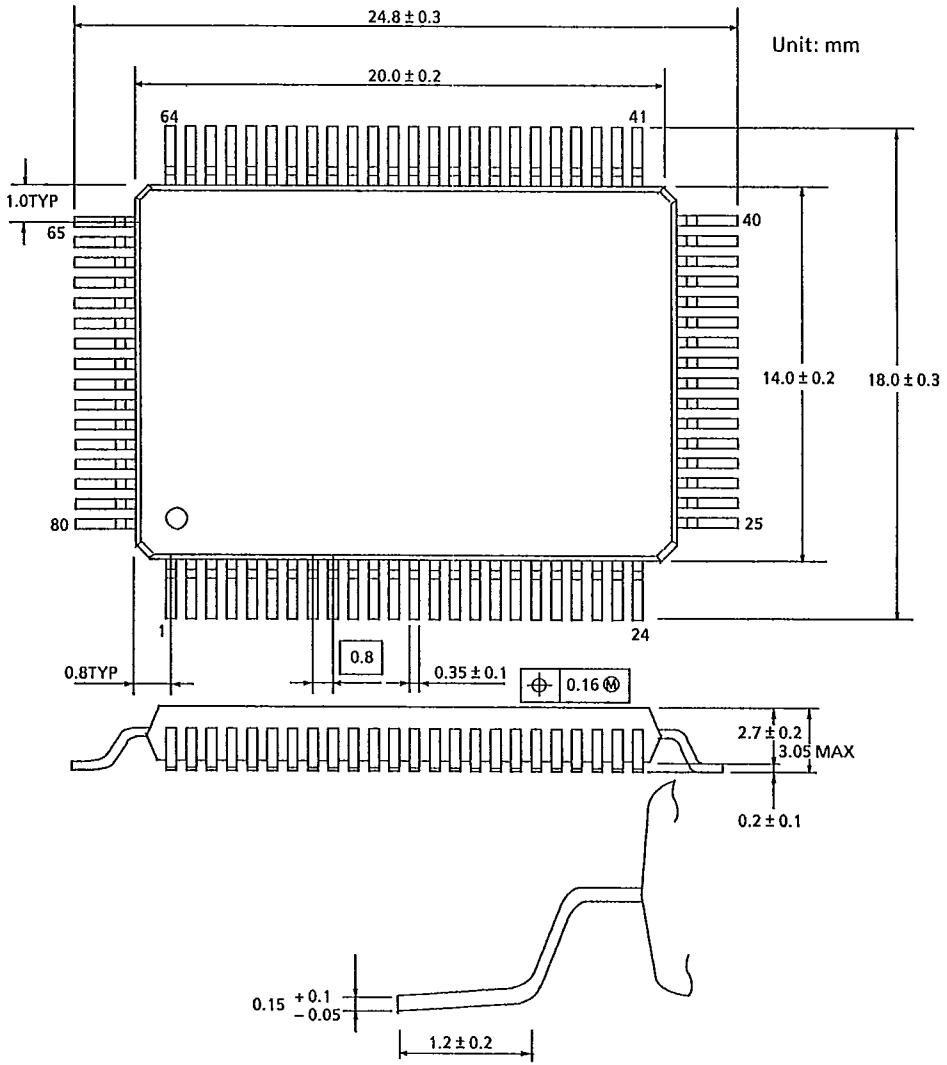
(3) ADM Analysis / synthesis Circuit

(VSS1 = VSS2 = 0V, VDD = 5.0V, Ta = 25°C, fin = 1KHz)

Item	Symbol	Condition	Specification			Unit
			Minimum	Typical	Maximum	
Maximum permissible input voltage	VIN	ADI	-	-	3.8	Vp-p

7. OUTLINE DRAWINGS

QFP80-P-1420A



Note: package dimensions include neither mold resin protrusions nor bars remaining on the tie bars.

8. APPLICATION CIRCUIT