

## Features

- **Fast Read Access Time - 55 ns**
- **Automatic Page Write Operation**  
Internal Address and Data Latches for 64 Bytes
- **Fast Write Cycle Times**  
Page Write Cycle Time: 2 ms maximum  
1 to 64 Byte Page Write Operation
- **Low Power Dissipation**  
60 mA Active Current  
100  $\mu$ A CMOS Standby Current
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$  Polling and Toggle Bit for End of Write Detection**
- **High Reliability CMOS Technology**  
Endurance: 100,000 Cycles  
Data Retention: 10 years
- **Single 5 V  $\pm$  10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

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**64K (8K x 8)  
High Speed  
CMOS  
E<sup>2</sup>PROM with  
Software Data  
Protection**

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## Description

The AT28HC64B is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 100  $\mu$ A.

The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by  $\overline{\text{DATA}}$  polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

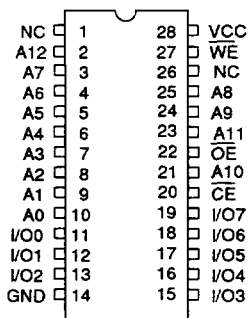
Atmel's 28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E<sup>2</sup>PROM for device identification or tracking.



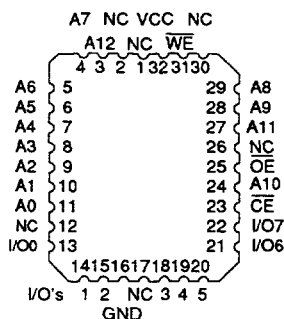
## Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

28D, 28P, 28S

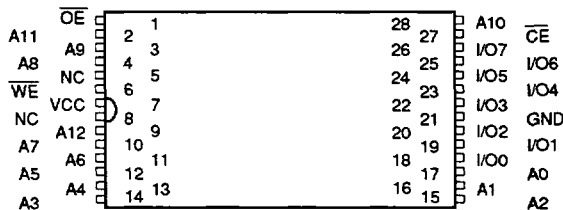


32J



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

28T



## Product Selection Guide

AT28HC64B										
Part Number	Speed	D	J	Package			Temp Range	Access Time	Operating Temperature Range	Availability
				P	S	T				
AT28HC64B	-55	•	•	•	•		C	55ns	0°C to +70°C	NOW
AT28HC64B	-70	•	•	•	•		C	70ns	0°C to +70°C	NOW
AT28HC64B	-70	•	•	•	•		I	70ns	-40°C to +85°C	NOW
AT28HC64B	-70	•					M/883	70ns	-55°C to +125°C	NOW
AT28HC64B	-90	•	•	•	•		C	90ns	0°C to +70°C	NOW
AT28HC64B	-90	•	•	•	•		I	90ns	-40°C to +85°C	NOW
AT28HC64B	-90	•					M/883	90ns	-55°C to +125°C	NOW
AT28HC64B	-12	•	•	•	•		C	120ns	0°C to +70°C	NOW
AT28HC64B	-12	•	•	•	•		I	120ns	-40°C to +85°C	NOW
AT28HC64B	-12	•					M/883	120ns	-55°C to +125°C	NOW

Package descriptions on page 33.