

MSM514102B/BL

4,194,304-Word × 1-Bit DYNAMIC RAM : STATIC COLUMN MODE TYPE

DESCRIPTION

The MSM514102B/BL is a new generation dynamic RAM organized as 4,194,304-word × 1-bit. The technology used to fabricate the MSM514102B/BL is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

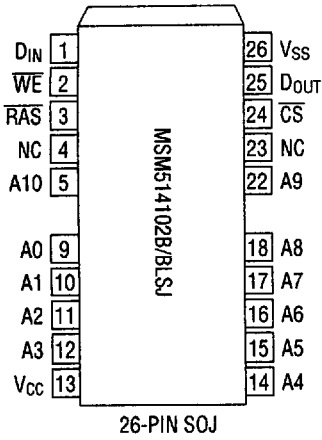
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 4,194,304-word × 1-bit organization
- Single 5V power supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate
- Refresh : 1024 cycles/16ms, 1024 cycles/128ms (L-version)
- Common I/O capability using "Early Write" operation
- \overline{CS} before \overline{RAS} refresh, Hidden refresh, \overline{RAS} -only refresh capability
- Multibit test mode capability
- Package :
 - 26-Pin 300mil Plastic SOJ (SOJ26-P-300)
 - 26-Pin 300mil Plastic TSOP (TSOP26-P-300-K) (TSOP26-P-300-L)
 - 20-Pin 400mil Plastic ZIP (ZIP20-P-400)

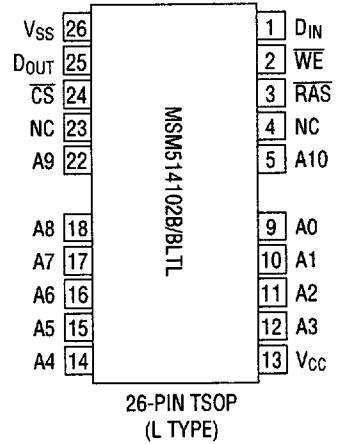
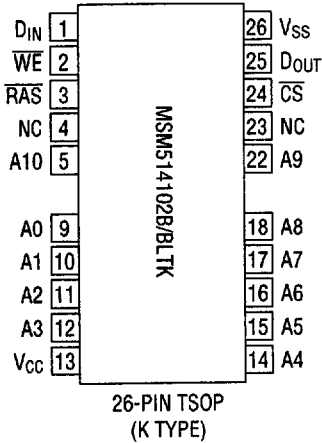
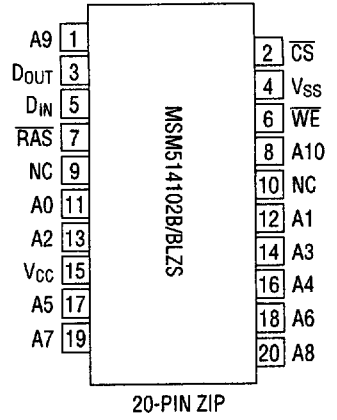
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating (Max.)	Standby (Max.)
MSM514102B/BL-60	60ns	30ns	15ns	110ns	550mW	5.5mW/ 1.1mW (L-version)
MSM514102B/BL-70	70ns	35ns	20ns	130ns	495mW	
MSM514102B/BL-80	80ns	40ns	20ns	150ns	440mW	
MSM514102B/BL-10	100ns	50ns	25ns	180ns	385mW	

PIN CONFIGURATION (TOP VIEW)

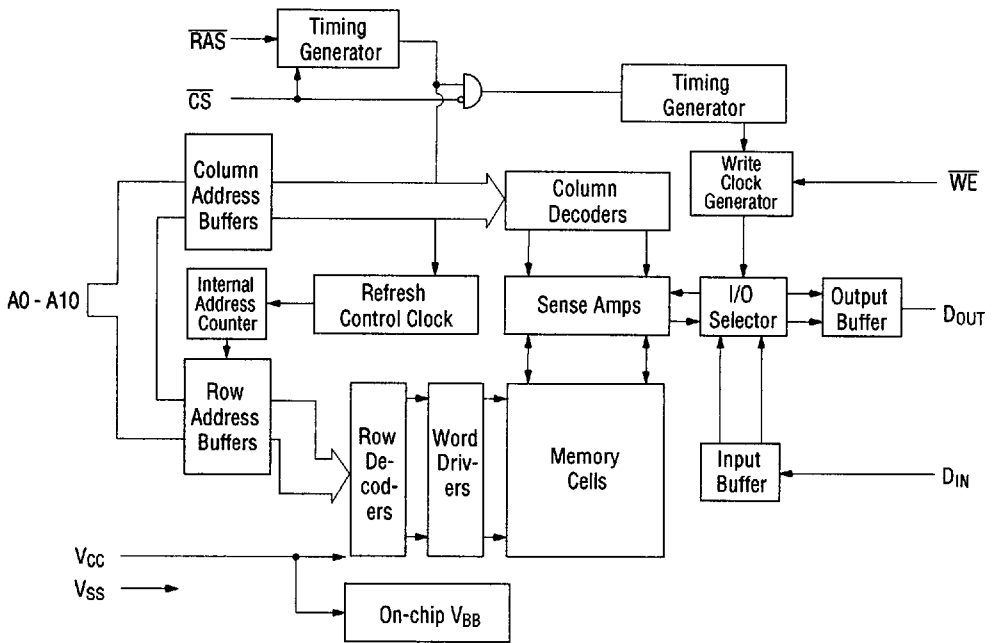


SJ=300mil



Pin Name	Function
A0 - A10	Address Input
RAS	Row Address Strobe
CS	Chip Select Input
D _{IN}	Data Input
D _{OUT}	Data Output
WE	Write Enable
V _{CC}	Power Supply (5V)
V _{SS}	Ground (0V)
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

 $(T_a = 0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Capacitance

 $(V_{CC} = 5V \pm 10\%, T_a = 25^\circ\text{C}, f = 1\text{MHz})$

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 - A_{10}, D_{IN}$)	C_{IN1}	—	6	pF
Input Capacitance (RAS, CS, WE)	C_{IN2}	—	7	pF
Output Capacitance (D_{OUT})	C_{VO}	—	7	pF

DC Characteristics

($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $70^\circ C$)

Parameter	Symbol	Condition	MSM514102 B/BL-60		MSM514102 B/BL-70		MSM514102 B/BL-80		MSM514102 B/BL-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -5.0$ mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2$ mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0V \leq V_i \leq 6.5V$; All other pins not under test = $0V$	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	D_{OUT} disable $0V \leq V_O \leq 5.5V$	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	\overline{RAS} , \overline{CS} cycling, $t_{RC} = \text{Min.}$	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	\overline{RAS} , $\overline{CS} = V_{IH}$	—	2	—	2	—	2	—	2	mA	1
		\overline{RAS} , $\overline{CS} \geq V_{CC} - 0.2V$	—	1	—	1	—	1	—	1	μA	1, 4
			—	200	—	200	—	200	—	200	μA	
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CS} = V_{IH}$ $t_{RC} = \text{Min.}$	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS} = V_{IH}$ $\overline{CS} = V_{IL}$ $D_{OUT} = \text{enable}$	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current (CS Before RAS Refresh)	I_{CC6}	\overline{RAS} cycling, \overline{CS} before \overline{RAS}	—	100	—	90	—	80	—	70	mA	1
Average Power Supply Current (Static Column Mode)	I_{CC9}	$\overline{RAS} = V_{IL}$ Address cycling, $t_{SC} = \text{Min.}$	—	90	—	80	—	70	—	60	mA	1
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125\mu s$ \overline{CS} before \overline{RAS} \overline{RAS} cycling $t_{RAS} = 1\mu s$	—	300	—	300	—	300	—	300	μA	1, 3, 4

- Notes:
1. Specified values are obtained with the output open.
 2. Address can be changed or less while $\overline{RAS} = V_{IL}$.
 3. $V_{CC} - 0.2V \leq V_{IH} \leq 6.5V$, $-1.0V \leq V_{IL} \leq 0.2V$.
 4. L-version

AC Characteristics (1/3)

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM514102 B/BL-60		MSM514102 B/BL-70		MSM514102 B/BL-80		MSM514102 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t _{RMW}	130	—	155	—	175	—	210	—	ns	
Static Column Mode Cycle Time	t _{SC}	35	—	40	—	45	—	55	—	ns	
Static Column Mode Read Modify Write Cycle Time	t _{SRMW}	60	—	60	—	65	—	80	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{\text{CS}}$	t _{CAC}	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	—	50	ns	4, 6, 7
Access Time from Last Write	t _{ALW}	—	55	—	65	—	75	—	95	ns	4, 7
Output Enable Time Reference to $\overline{\text{WE}}$	t _{OW}	—	20	—	20	—	20	—	25	ns	
Output Low Impedance Time from $\overline{\text{CS}}$	t _{CLZ}	0	—	0	—	0	—	0	—	ns	
Data Output Hold Time Reference to Column Address	t _{AOH}	5	—	5	—	5	—	5	—	ns	
Data Output Hold Time Reference to $\overline{\text{WE}}$	t _{WOH}	0	—	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay Time	t _{OFF}	0	20	0	20	0	20	0	25	ns	8
Transition Time	t _T	3	50	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t _{REF}	—	128	—	128	—	128	—	128	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Static Column Mode)	t _{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CS}}$ Pulse Width	t _{Cs}	15	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{\text{CS}}$ Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	20	—	ns	
Column Address Hold Time Reference to $\overline{\text{RAS}}$ (WRITE CYCLE)	t _{AWR}	50	—	55	—	60	—	75	—	ns	

AC Characteristics (2/3)

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM514102 B/BL-60		MSM514102 B/BL-70		MSM514102 B/BL-80		MSM514102 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Column Address Hold Time Reference to $\overline{\text{RAS}}$	t _{AR}	75	—	85	—	95	—	115	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	50	—	ns	
Column Address Hold Time Reference to RAS Precharge	t _{AH}	10	—	10	—	10	—	10	—	ns	
Column Address Hold Time Reference to $\overline{\text{WE}}$	t _{AHLW}	55	—	65	—	75	—	95	—	ns	
Last Write to Column Address Delay Time	t _{LWAD}	20	25	20	30	20	35	25	45	ns	7
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Reference to $\overline{\text{CS}}$	t _{RCH}	0	—	0	—	0	—	0	—	ns	9
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	10	—	10	—	15	—	20	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	15	—	20	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	45	—	50	—	60	—	75	—	ns	
Write Invalid Time	t _{WI}	10	—	10	—	10	—	10	—	ns	
Write Command Hold Time (D _{OUT} Disable)	t _{WH}	0	—	0	—	0	—	0	—	ns	10
Write Command to $\overline{\text{CS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	15	—	20	—	20	—	25	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	30	—	35	—	40	—	50	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	60	—	70	—	80	—	100	—	ns	10
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	20	—	ns	11
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—	60	—	75	—	ns	
$\overline{\text{CS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Set-up Time ($\overline{\text{CS}}$ Before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Hold Time ($\overline{\text{CS}}$ Before $\overline{\text{RAS}}$)	t _{CHR}	15	—	15	—	15	—	15	—	ns	

AC Characteristics (3/3)

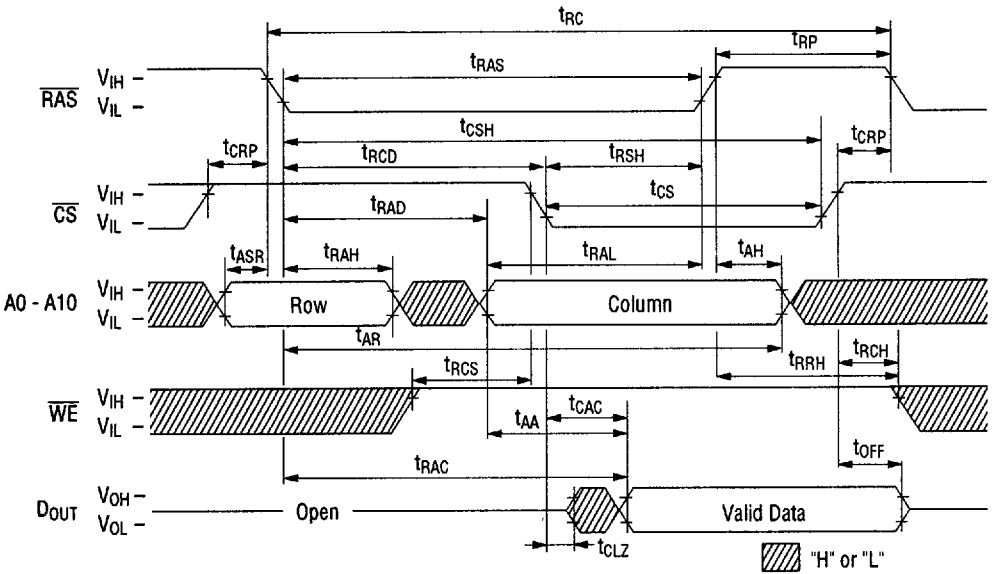
(V_{CC} = 5V ± 10%, T_a = 0 to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM514102 B/BL-60		MSM514102 B/BL-70		MSM514102 B/BL-80		MSM514102 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
\overline{CS} Precharge Time (Refresh Counter Test)	t _{CPT}	35	—	35	—	40	—	50	—	ns	
\overline{WE} to \overline{RAS} Precharge Time (\overline{CS} Before \overline{RAS})	t _{WRP}	10	—	10	—	10	—	10	—	ns	
\overline{WE} Hold Time from \overline{RAS} (\overline{CS} Before \overline{RAS})	t _{WRH}	10	—	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Set-up Time (Test Mode)	t _{WSR}	10	—	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Hold Time (Test Mode)	t _{WHR}	10	—	10	—	10	—	10	—	ns	

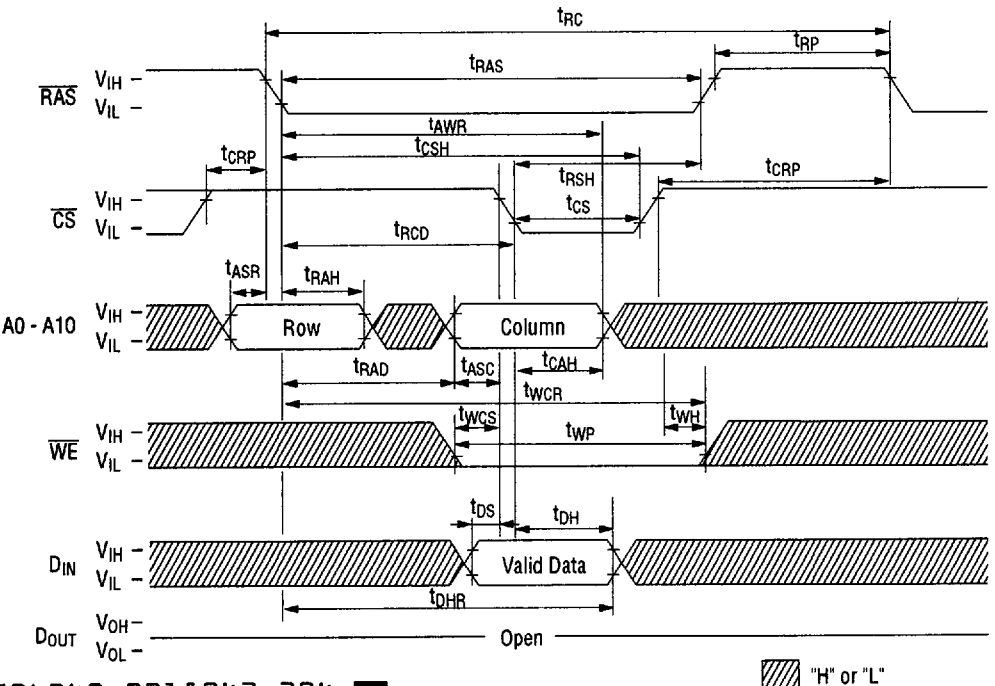
- Notes:
1. An initial pause of 200 μ s is required after power-up followed by eight or more initialization cycles ($\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, eight or more $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
 2. The AC characteristics assume $t_{\text{r}} = 5\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels of input signals for timing measurement. Transition times (t_{r}) are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
 5. Operating within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC} .
 6. Operating within the t_{RAD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled exclusively by t_{AA} .
 7. Operating within the t_{LWAD} (Max.) limit insures that t_{ALW} (Max.) can be met. t_{LWAD} (Max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (Max.) limit, then access time is controlled exclusively by t_{AA} .
 8. The t_{OFF} (Max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{WH} , t_{CWD} , t_{RWD} , t_{AWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{\text{WCS}} \geq t_{\text{WCS}}$ (Min.) and $t_{\text{WH}} \geq t_{\text{WH}}$ (Min.) the cycle is an Early Write cycle and the data out remains in a high impedance state throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}$ (Min.), $t_{\text{RWD}} \geq t_{\text{RWD}}$ (Min.) and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (Min.) the cycle is a Read Modify Write cycle and the data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of data out is indeterminate at access time.
 11. These parameters are referenced to $\overline{\text{CS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a read modify write cycle.
 12. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bit parallel test function. RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 13. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

TIMING WAVEFORM

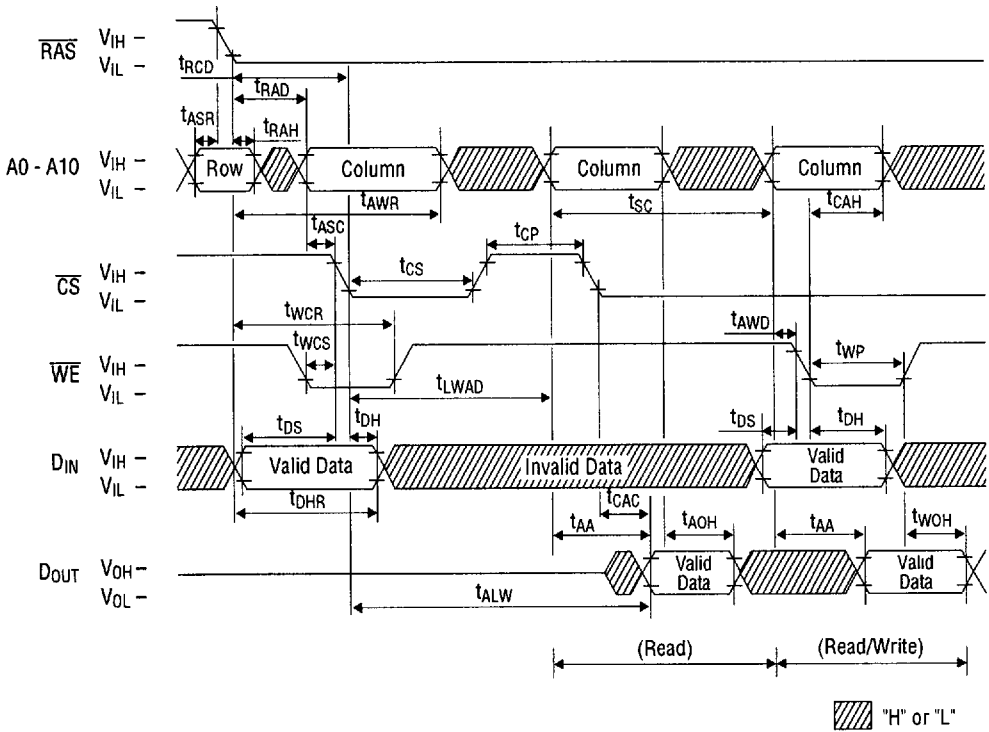
Read Cycle



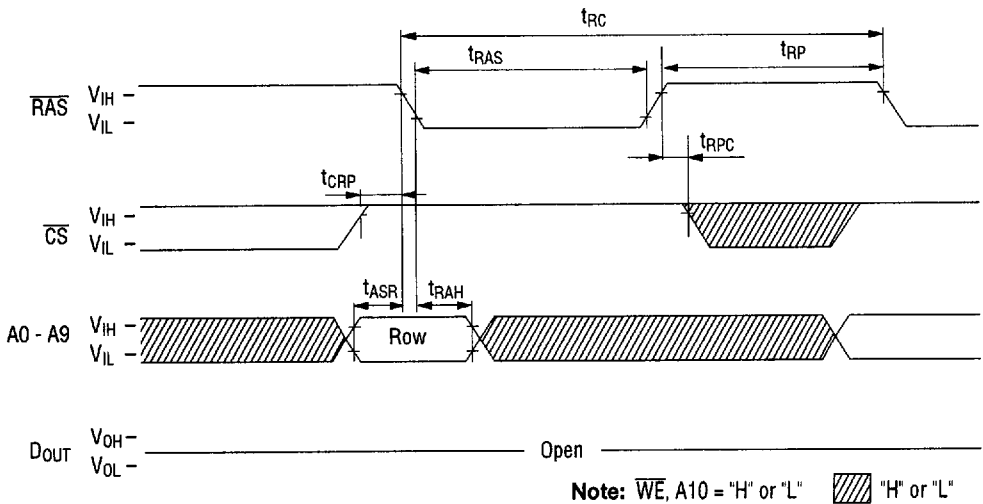
Write Cycle (Early Write)



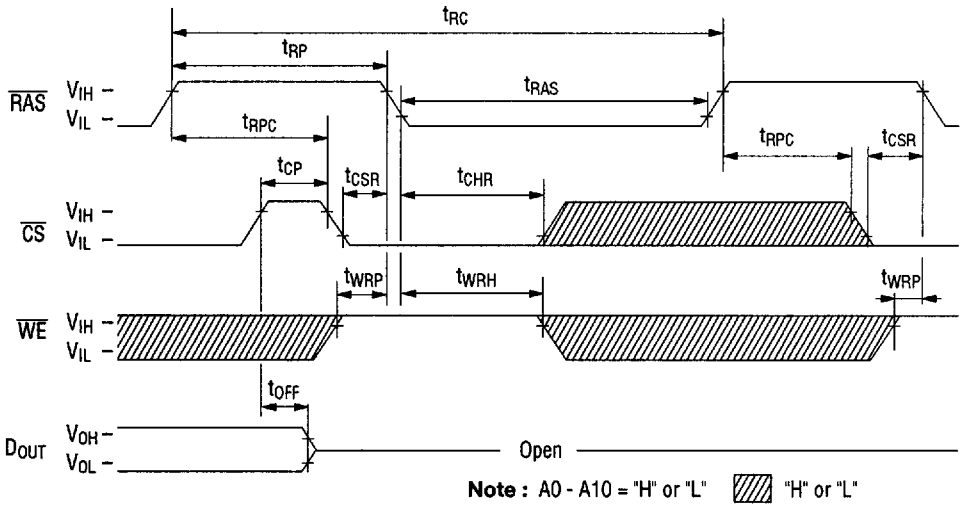
Static Column Mode Read/Write Mixed Cycle



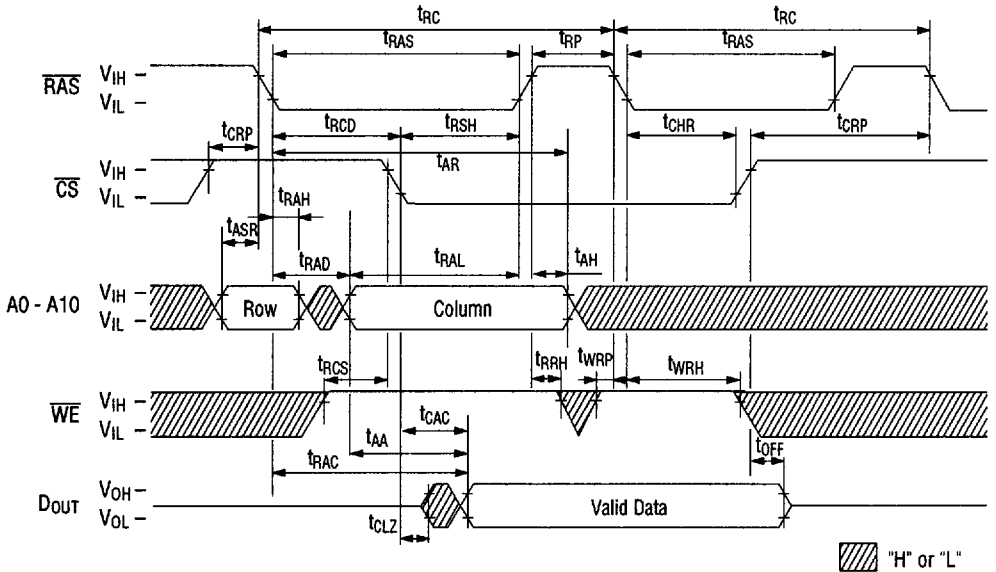
RAS-only Refresh Cycle



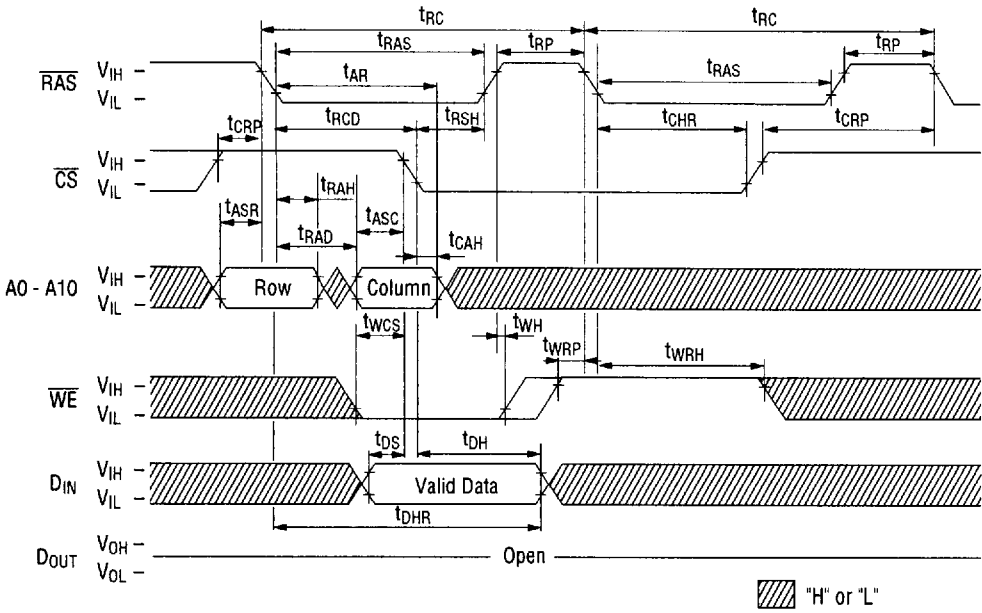
\overline{CS} Before \overline{RAS} Auto-refresh Cycle



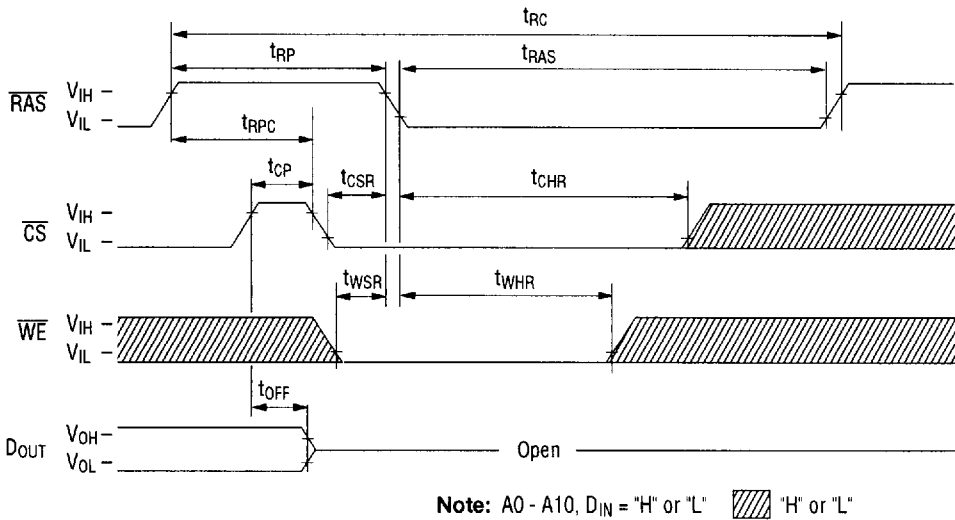
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



Test Mode Initiate Cycle



CS Before RAS Refresh Counter Test Cycle

