Z2130

CMOS DIGITAL DOWN CONVERTER/CARRIER TRACKER

FEATURES

- Numerically Controlled Oscillator
  - 32-Bit phase accumulator
  - 10-Bit phase/8-Bit amplitude Look-Up Table
  - 40 MHz Maximum clock speed
  - Quadrature Sine and Cosine Outputs
- Complex Multiplier
  - 8-Bit complex data inputs
  - 40 MHz throughput
  - Truncated 9-Bit complex summed products
- First/Second Order Loop Filter
  - Variable gain control of frequency or phase discriminator data
  - Selectable 1st or 2nd order filtering
  - Internal saturation protection
  - 28-Bit phase/frequency control signal
  - High carrier recovery loop update rates
- Complex Integrate and Dump Filters
  - 19-Bit Integration accumulator
  - Variable dump rate option
  - 40 MHz accumulation rate
  - Internal or external dump control options
- Digital I/F Sampling Logic
  - Internal I/Q input data signal coupling option
  - Reduced power mode
- Versatile I/O Interface Configuration
  - Fixed or pseudo-floating point signal formats
  - Single or dual A/D conversion input operation

GENERAL DESCRIPTION

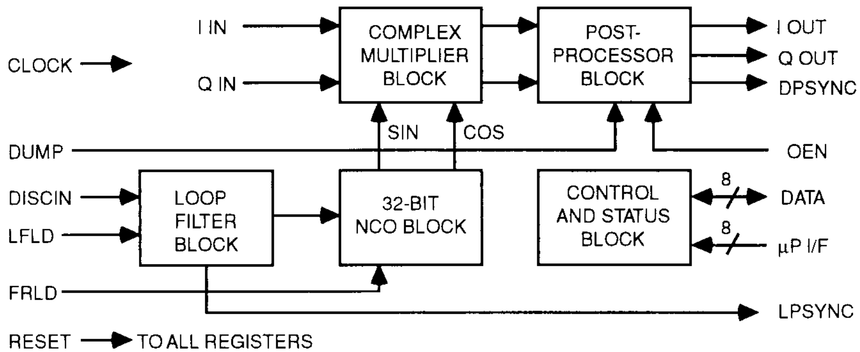
The Z2130 contains a Numerically Controlled Oscillator (NCO) and complex multiplier to demodulate the signal and produce a discriminator function that enables the demodulator to track either the phase or the frequency of the received carrier signal. The digital downconverter eliminates the need for a D/A converter at the output of the NCO, along with the associated analog circuitry.

Closed loop control of the NCO is achieved with a first or second order Loop Filter which accepts phase or frequency discriminator information. This will typically be generated by a Z2120 demodulator ASIC. The Z2130 is designed to operate efficiently with or without additional general purpose processor support to permit the loop to be updated at the symbol rate for all symbol rates. In applications where fast acquisition requires adaptive carrier loops the Z2130 allows the tracking loop parameters to be updated without disturbing the tracking process.

GENERAL DESCRIPTION (Continued)

The Z2130 offers a unique I/F sampling mode where a narrow bandwidth signal is sampled with a single A/D converter. In this mode a full complex multiply is not necessary, and the power consumption is reduced by an internal power down mode.

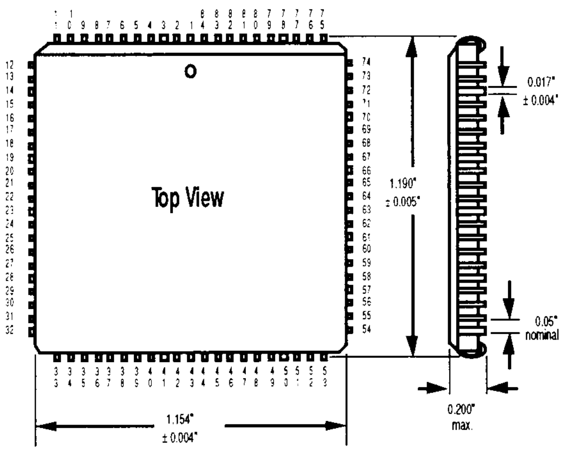
At the output of the complex multiplier the resulting multiplier products represent downconverted baseband information which are then fed into programmable Integrate and Dump filters to provide baseband filtering. The integration period can be synchronous with the sampling rate or controlled by an external clock .



Z2130 Block Diagram

PIN CONFIGURATION

Package: 84-Pin PLCC
Thermal coefficient, θ_{ja} = 36°/W



Note: (1) Tolerances on pin spacing are not cumulative.
(2) Dimensions at seating plane

PIN CONNECTIONS

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{SS}	29	I_{IN4}	57	$DISCIN_5$
2	$DATA_7$	30	I_{IN5}	58	$DISCIN_4$
3	$DATA_6$	31	I_{IN6}	59	$DISCIN_3$
4	$DATA_5$	32	I_{IN7}	60	$DISCIN_2$
5	$DATA_4$	33	V_{SS}	61	$DISCIN_1$
6	$DATA_3$	34	Q_{IN0}	62	$DISCIN_0$
7	$DATA_2$	35	Q_{IN1}	63	LPSYNC
8	$DATA_1$	36	Q_{IN2}	64	V_{SS}
9	$DATA_0$	37	Q_{IN3}	65	DPSYNC
10	WRSTB	38	Q_{IN4}	66	Q_{OUT7}
11	V_{DD}	39	Q_{IN5}	67	Q_{OUT6}
12	CSEL	40	Q_{IN6}	68	Q_{OUT5}
13	READ	41	Q_{IN7}	69	Q_{OUT4}
14	$ADDR_0$	42	V_{DD}	70	Q_{OUT3}
15	$ADDR_1$	43	V_{SS}	71	Q_{OUT2}
16	$ADDR_2$	44	$\overline{OEN}$	72	Q_{OUT1}
17	$ADDR_3$	45	I.C.	73	Q_{OUT0}
18	$ADDR_4$	46	$DISCIN_{15}$	74	V_{DD}
19	FRLD	47	$DISCIN_{14}$	75	V_{SS}
20	LFLD	48	$DISCIN_{13}$	76	I_{OUT7}
21	DUMP	49	$DISCIN_{12}$	77	I_{OUT6}
22	CLOCK	50	$DISCIN_{11}$	78	I_{OUT5}
23	V_{SS}	51	$DISCIN_{10}$	79	I_{OUT4}
24	$\overline{RESET}$	52	$DISCIN_9$	80	I_{OUT3}
25	I_{IN0}	53	$DISCIN_8$	81	I_{OUT2}
26	I_{IN1}	54	V_{SS}	82	I_{OUT1}
27	I_{IN2}	55	$DISCIN_7$	83	I_{OUT0}
28	I_{IN3}	56	$DISCIN_6$	84	V_{DD}

Note:
I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

FUNCTION BLOCK DESCRIPTION

CONTROL AND STATUS BLOCK

The Control and Status Block provides the means to set and control all the functions of the Z2130 and to determine the status of some useful parameters. This function includes the microprocessor interface used to write the control parameters into the control registers and to read the status parameters from the status registers.

COMPLEX MULTIPLIER BLOCK

The Complex Multiplier Block is the core of the demodulator. In this block the complex input samples are multiplied by the complex output samples from the NCO Block. The resulting outputs are the I and Q signals:

$$IDAT = I_{IN} \cdot \cos(wt) - Q_{IN} \cdot \sin(wt)$$
$$QDAT = I_{IN} \cdot \sin(wt) + Q_{IN} \cdot \cos(wt)$$

where $w = 2\pi f_{OUT}$

The 8-bit input signals result in 17 bit outputs which are then truncated to 10 bits. When using the Direct I.F. Sampling Mode the Q channel inputs are set to zero and so are the NCO outputs to the Q channel multipliers. In this way the power consumption of these two multipliers is reduced to zero in this mode.

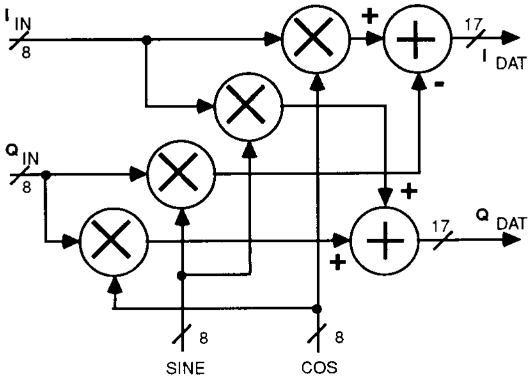
POST-PROCESSOR BLOCK

The 10-bit I and Q channel products from the Complex Multiplier Block are fed into Integrate and Dump filters to integrate the samples in each symbol period. The Dump process can be controlled manually, either by means of the **DUMP** input or under processor (software) control, or automatically under the control of the Dump counter. In the Automatic Dump Mode the dump occurs each time the counter counts down to zero from its preset value. This is determined by the Dump Count value loaded into bits 2-0 in Post-Processor Control Register 2 according to the equation:

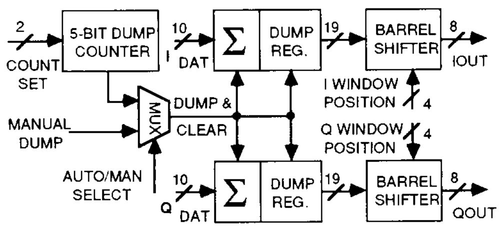
$$\text{Samples between Dumps} = 2^{(\text{Dump Count} + 1)}$$

allowing the dump to occur every 2, 4, 8, 16, 32, 64, 128 or 256 samples. Theoretically the 19-bit outputs of the Integrators allow a minimum of 512 integrations per dump without overflow, but in practice this number will generally be at least 1024 samples per dump. These outputs are then fed into Barrel Shifters and 8-bit signals are derived from the Barrel Shifters according to the setting of the data in Post Processor Control Register 0 (address 00_H). The maximum levels of the signals can easily be calculated from the number of integrations since the increase in the wordlength is directly related to this number.

FUNCTION BLOCK DIAGRAMS



COMPLEX MULTIPLIER BLOCK



POST-PROCESSOR BLOCK

FUNCTION BLOCK DESCRIPTION (Continued)

LOOP FILTER BLOCK

The Loop Filter Block first converts the frequency discriminator input signal from its input format into 8-bit data for the loop filter according to the settings of bits 6 and 7 in Loop Filter Control Register 0. The format of the I and Q signals is then converted from 8 or 16-bit Fixed Point or 8-bit Floating Point formats into 8-bit Fixed Point format. In the 8-bit Floating Point Mode (used with the Z2120 DQPSK Demodulator) the signals are first expanded into 22-bit Fixed Point format according to the value of the exponent. In both this mode and the 16-bit Input Mode the signals are fed into a Barrel Shifter and 8-bit signals are derived from the Barrel Shifter according to the setting of bits 4-0 in Loop Filter Control Register 0. The Loop Filter transfer function can be set up to be either first or second order and the coefficient values can be adjusted in powers of 2 from 2^0 to 2^{21}. The overall transfer function is:

$$\text{Transfer Fn.} = K1 + {}^1\!/\!_4\, K2 \,.\, \frac{z^{-1}}{1 - z^{-1}}$$

The $^1/_4$ factor is introduced because the signal in the integrator path of the loop is divided by four after the integrator by truncating the 2 LSBs of the signal. This signal is then added to the signal in the direct path such that the LSBs of the signal are aligned.

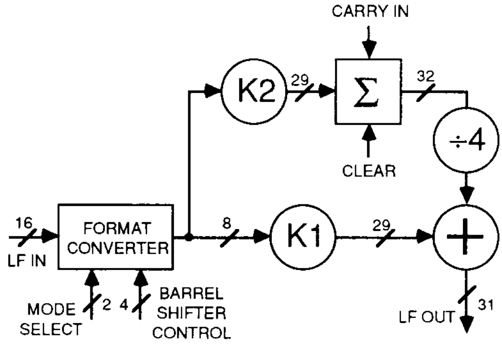
NCO BLOCK

The on-chip Numerically Controlled Oscillator (NCO) Block generates the carrier signal for the downconverter. The output frequency of the NCO is determined by the value of the control word Δ-Phase, which is made up of the Frequency Control Word (FCW) input data and the output of the Loop Filter. The Loop Filter output can be added to or subtracted from the FCW to allow operation with frequency discriminators having either positive or negative characteristics. The NCO has 32-bit resolution so that the output frequency is given by the equation:

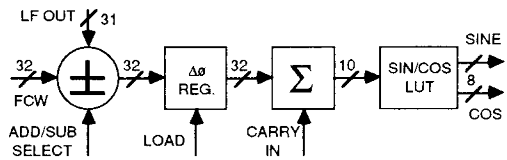
$$f_{OUT} = \frac{\Delta\text{-Phase} \,.\, f_{CLK}}{2^{32}} = \frac{(FCW \pm LF_{OUT}) \,.\, f_{CLK}}{2^{32}}$$

The FCW data sets the nominal frequency of the NCO and is stored in the NCO FCW Registers. The 8 MSBs of the phase of the accumulator are available as an output signal at the **$DISC_{15\text{-}8}$** pins when the Discriminator Input Mode is not set to the 16-bit Mode (bits 7-6 ≠ 00 in address $0A_H$). A new frequency should not be loaded into the NCO within eight clock cycles of the previous one.

FUNCTION BLOCK DIAGRAMS



LOOP FILTER BLOCK



NCO BLOCK

INPUT SIGNALS

RESET
The RESET input is asynchronous and active low, and clears all the registers in the device. When RESET goes low all the registers are cleared within 50 nsecs, and normal operation will resume after this signal returns to the high state.

CLOCK
All synchronous functions performed within the Z2130 are referenced to the rising edge of the CLOCK input. This signal should nominally be a square wave at a maximum frequency of 40MHz. A non-repetitive CLOCK waveform is permissible provided the minimum duration of the positive and negative pulses in the signal are always greater than 10 nsec.

CSEL
The CSEL input is used to control the reading and writing of data from and to the Z2130. It is active low. When this input is high all I/O on the $DATA_{7\text{-}0}$ bus is inhibited.

OEN
The Output Enable signal is used to enable and disable the $IOUT_{7\text{-}0}$ and $QOUT_{7\text{-}0}$ outputs. When OEN is set low the outputs are enabled, and when it is set high they will go into a high impedance state. This allows these outputs to be connected to a bus if required.

WRSTB
The WRSTB input is used to latch the data on the $DATA_{7\text{-}0}$ bus into the internal parameter and Mode Control Registers. On the rising edge of the WRSTB input the information on the $DATA_{7\text{-}0}$ bus is latched into the register selected by the $ADDR_{4\text{-}0}$ lines.

READ
The READ input is used to enable the data on the $DATA_{7\text{-}0}$ bus to be read from the internal registers. When the READ input is set low the information on the $DATA_{7\text{-}0}$ bus can be read from the register selected by the $ADDR_{4\text{-}0}$ lines provided that CSEL is also low.

$ADDR_{4\text{-}0}$
The five address lines $ADDR_{4\text{-}0}$ control the selection of internal registers for writing and reading information to and from the $DATA_{7\text{-}0}$ bus. The mapping of the I/O data into the internal registers is shown in the tables:

$DATA_{7\text{-}0}$
The 8-bit $DATA_{7\text{-}0}$ bus is a bidirectional port that is used to write and read information to and from the internal registers of the Z2130. The specific register locations are accessed by address signals $ADDR_{4\text{-}0}$ and the data direction by WRSTB and READ.

Write Mode:

$ADDR_{4\text{-}0}$	Function
00_H	Post-Processor Control Register 0
01_H	Post-Processor Control Register 1
02_H	Post-Processor Control Register 2
03_H	Miscellaneous Mode Register
04_H	NCO FCW Register 0 (Bits 7-0)
05_H	NCO FCW Register 1 (Bits 15-8)
06_H	NCO FCW Register 2 (Bits 23-16)
07_H	NCO FCW Register 3 (Bits 31-24)
08_H	NCO Mode Control Register
09_H	Sampling Mode Control Register
$0A_H$	Loop Filter Control Register 0
$0B_H$	Loop Filter Control Register 1
$0C_H$	Loop Filter Control Register 2
$0D_H$	Loop Filter Control Register 3

Read Mode:

$ADDR_{4\text{-}0}$	Function
00_H	NCO Accumulator Value (Bits 7-0)
01_H	NCO Accumulator Value (Bits 15-8)
02_H	NCO Accumulator Value (Bits 23-15)
03_H	NCO Accumulator Value (Bits 31-24)
04_H	Loop Filter Output Value (Bits 7-0)
05_H	Loop Filter Output Value (Bits 15-8)
06_H	Loop Filter Output Value (Bits 23-16)
07_H	Loop Filter Output Value (Bits 31-24)
08_H	Loop Filter Input Value
09_H	Complex Mult. Input Value (NCO Cos)
$0A_H$	Complex Mult. Input Value (NCO Sin)
$0B_H$	Complex Mult. Input Value (I signal)
$0C_H$	Complex Mult. Input Value (Q signal)
$0D_H$	Complex Mult. Output Bits 15-8 (I x Cos)
$0E_H$	Complex Mult. Output Bits 15-8 (Q x Sine)
$0F_H$	Complex Mult. Output Bits 15-8 (Q x Cos)
10_H	Complex Mult. Output Bits 15-8 (I x Sin)
11_H	I Channel I & D Filter Input Bits 9-2
12_H	Q Channel I & D Filter Input Bits 9-2
13_H	Status Register

$I_{IN7\text{-}0}$ and $Q_{IN7\text{-}0}$

$I_{IN7\text{-}0}$ and $Q_{IN7\text{-}0}$ ($I/Q_{IN7\text{-}0}$) are the 8-bit In-phase and Quadrature channel input signals, respectively. The signals are sampled on the rising edges of **CLOCK**. The I channel signals are always fed directly into the Complex Multiplier Block, but the Q channel signals are only used in the Complex Input Mode, using two A/D converters. The input data should be in Two's Complement format.

$DISC_{IN15\text{-}0}$

$DISC_{IN15\text{-}0}$ is the 16-bit discriminator input signal from the demodulator used in conjunction with the Z2130. In the case of the Z2120 this is the **$DATA_{7\text{-}0}$** output signal from address 00_H. When using an analog demodulator the discriminator output should be digitized for use with the Z2130.

FRLD

The **Frequency Load** input causes a new frequency to be loaded into the NCO when the NCO is in the Manual Update Mode. This frequency will be the sum or difference of the data loaded into the FCW registers and the Loop Filter output. The load process begins on the rising edge of the **CLOCK** following the falling edge of **FRLD**. The maximum NCO update rate is once every eight **CLOCK** cycles. The NCO frequency will be updated automatically each time the Loop Filter is updated if bit 6_H in address $0B_H$ is set low.

LFLD

The Loop Filter **Load** input causes the Loop Filter to be updated with the current value of the $DISC_{IN15\text{-}0}$ signal when the Loop Filter is in the Manual Update Mode. The update process occurs on the rising edge of the **CLOCK** following the falling edge of **LFLD**. The maximum Loop Filter update rate is once every eight **CLOCK** cycles. If bit 6 in address $0B_H$ is set low the NCO will also be updated each time this happens. In this case the maximum NCO rate is once every eight **CLOCK** cycles, as dictated by the NCO.

DUMP

The **Dump** input causes the outputs of the Integrate and Dump Filters to be dumped into their output registers (and the integrators cleared) when the Integrate and Dump Filters are in the Manual Dump Mode. The dump process occurs on the rising edge of the **CLOCK** following the falling edge of **DUMP**. The maximum dump rate is once every two **CLOCK** cycles unless bit 3 in address 03_H is set high, in which case the dump process will occur continuously, i.e., every clock cycle, thereby effectively bypassing the Integrate and Dump Filters altogether.

OUTPUT SIGNALS

$IOUT_{7\text{-}0}$ and $QOUT_{7\text{-}0}$

The **$IOUT_{7\text{-}0}$** and **$QOUT_{7\text{-}0}$** ($I/QOUT_{7\text{-}0}$) signals are the In-phase and Quadrature phase outputs of the Z2130. When using the Z2120, these signals should be connected to the **$IDATA_{11\text{-}0}$** and **$IDATA_{11\text{-}0}$** inputs and when using the Z3310 they should be connected to the $I_{IN2\text{-}0}$ and $Q_{IN2\text{-}0}$ inputs.

DPSYNC

The **Dump Sync** signal indicates that a dump has taken place and new data is available at the **$I/QOUT_{7\text{-}0}$** outputs. This signal can be used to synchronize the reading of the output data and is particularly useful when the Integrate and Dump Filters are in the Automatic Dump Mode.

LPSYNC

The Loop Filter **Sync** signal indicates that the Loop Filter input has been updated. It can be used to keep track of this function when the Loop Filter is in the Automatic Update Mode.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125	°C (Plastic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	Volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD}+0.3	Volts
I_I	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

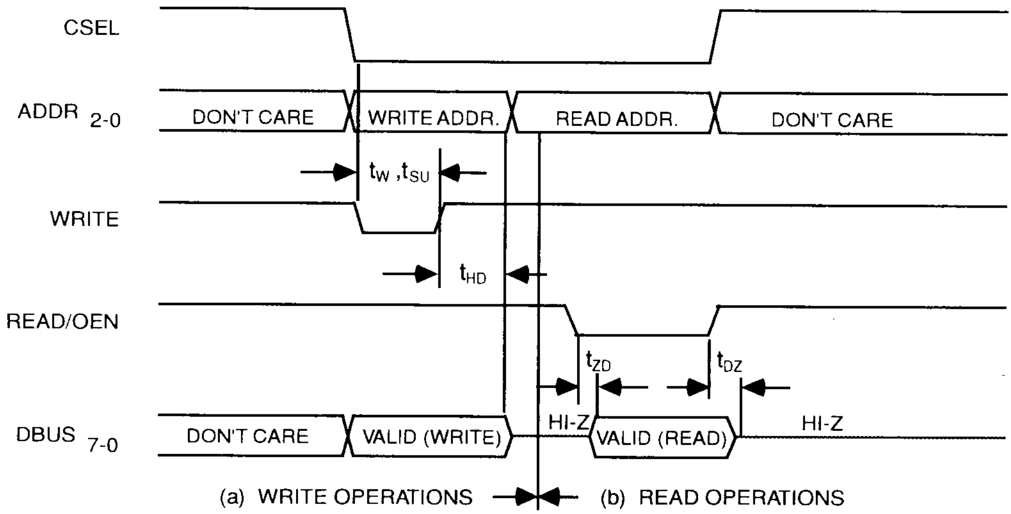
Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial)
T_a	Operating Temperature (Ambient)	0 to +70	°C (Commercial)

D.C. CHARACTERISTICS

Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			4.0	mA/MHz	f_{MCLK}= 40 MHz
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**CSEL**, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–130	–45	–15	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

MICROPROCESSOR INTERFACE TIMING

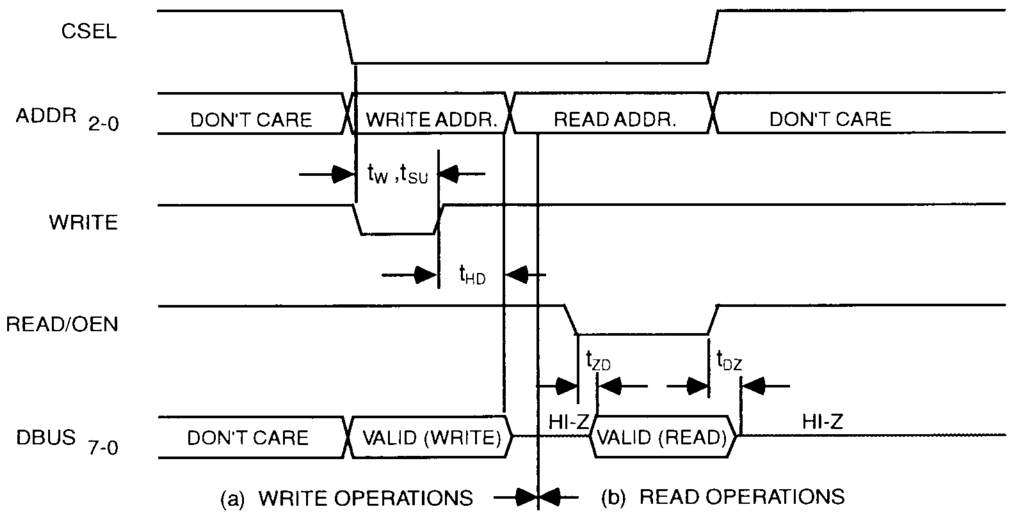


MICROPROCESSOR INTERFACE A.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70°C

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{SU}	**CSEL**, **ADDR**, **DBUS** to **WRITE** setup and **CLKEN** and **I/QDATA** to **CLOCK** setup	5		nsec.	
t_{DH}	**WRITE** to **CSEL**, **ADDR**, **DBUS** hold and **CLKEN** and **I/QDATA** to **CLOCK** hold	5		nsec.	
t_W	**WRITE** pulse width	5		nsec.	
t_{ZD}	**DBUS** Valid from Hi-Z state		10	nsec.	
t_{DZ}	**DBUS** Valid from Hi-Z state		10	nsec.	
t_{DO}	**I/QOUT** Valid from **DRDY**		10	nsec.	Load = 15 pF

MICROPROCESSOR INTERFACE TIMING



MICROPROCESSOR INTERFACE A.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70°C

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{SU}	**CSEL**, **ADDR**, **DBUS** to **WRITE** setup and **CLKEN** and **I/QDATA** to **CLOCK** setup	5		nsec.	
t_{DH}	**WRITE** to **CSEL**, **ADDR**, **DBUS** hold and **CLKEN** and **I/QDATA** to **CLOCK** hold	5		nsec.	
t_W	**WRITE** pulse width	5		nsec.	
t_{ZD}	**DBUS** Valid from Hi-Z state		10	nsec.	
t_{DZ}	**DBUS** Valid from Hi-Z state		10	nsec.	
t_{DO}	**I/QOUT** Valid from **DRDY**		10	nsec.	Load = 15 pF

PROGRAMMING THE Z2130

The functions of the Z2130 are programmed by means of the Parameter and Mode Control Registers in addresses 00_H to $0D_H$ and internal parameters can be read from the Parameter Registers in addresses 00_H to 13_H.

INPUT DATA (WRITE MODE)

Address 00_H: Post-Processor Control Register 0. Reset Value: 00_H

Bits 3-0: Sets position of I channel Viewport according to the table below:

Bits 7-4: Sets position of Q channel Viewport according to the table below:

Bits 7-4 or 3-0	**Window position**
0_H	Bits 3-0 of output in bits 7-4 of window
1_H	Bits 4-0 of output in bits 7-3 of window
2_H	Bits 5-0 of output in bits 7-2 of window
3_H	Bits 6-0 of output in bits 7-1 of window
4_H	Bits 7-0 of output in bits 7-0 of window
5_H	Bits 8-1 of output in bits 7-0 of window
6_H	Bits 9-2 of output in bits 7-0 of window
7_H	Bits 10-3 of output in bits 7-0 of window
8_H	Bits 11-4 of output in bits 7-0 of window
9_H	Bits 12-5 of output in bits 7-0 of window
A_H	Bits 13-6 of output in bits 7-0 of window
B_H	Bits 14-7 of output in bits 7-0 of window
C_H	Bits 15-8 of output in bits 7-0 of window
D_H	Bits 16-9 of output in bits 7-0 of window
E_H	Bits 17-10 of output in bits 7-0 of window
F_H	Bits 18-11 of output in bits 7-0 of window

This range allows the full range of outputs to be viewed with a 4-bit window, in addition to an 8-bit window.

Address 01_H: Post-Processor Control Register 1. Reset Value: 00_H

Bit 0: Setting this bit low causes the output data seen in the I channel Integrate and Dump filter to be saturated on overflow.

Bit 1: Setting this bit low causes the output data seen in the Q channel Integrate and Dump filter to be saturated on overflow. The saturation on overflow function eliminates the ambiguity caused by the cyclic overflow characteristics of Two's Complement arithmetic.

Address 02_H: Post-Processor Control Register 2. Reset Value: 00_H

Bits 2-0: Dump Count. Sets the number of samples between dumps for the Integrate and Dump filters in the Automatic Dump Mode from 2 to 256, according to the equation: Samples between dumps = $2^{(\text{Dump Count} + 1)}$

Bit 3: Sets the Integrate and Dump filters into the Automatic Dump Mode when set high and into the Manual Dump Mode when set low.

Bit 4: Sets the device into a test mode when set high. Do not use.

Bit 5: I Accumulator Carry In

Bit 6: Q Accumulator Carry In

Setting one or both of these bits high causes the carry inputs of the I or/and Q channel to be activated. These bits should be set to zero for normal operation

Address 03_H: Control Register. Reset Value: 00_H.

Bit 0: Setting this bit high loads the output of the Loop Filter into the NCO once only. This bit must be reset before it becomes active again. Bit 1 (below) must be set low ot bit 6 in address B must be set high to enable this function.*

Bit 1: Setting this bit high loads the discriminator input data into the Loop Filter once only. This bit must be reset before it becomes active again.*

Bit 2: Setting this bit high causes the Integrate and dump filters to dump once only. This bit must be reset before it becomes active again.*

* The corresponding input pin must be tied to V_{CC} to enable these functions to be performed in this way.

Bit 3: Setting this bit high causes the **DUMP** input signal to bypass the synchronizing circuit and allows continuous dumping, i.e. causes the Integrate and Dump filters to be disabled, or bypassed. When this bit is set low the maximum dump rate is once every two samples.

Addresses 04_H through 07_H: NCO Frequency Control Word (FCW) Registers: Reset Values: 00_H

These four registers store the initial 32-bit Frequency Control Word for the NCO as shown in the table:

Address	Bits	FCW bits
04_H	7-0	7-0
05_H	7-0	15-8
06_H	7-0	23-16
07_H	7-0	31-24

Address 08_H: NCO Mode Control Register: Reset Value: 00_H

Bit 0: NCO Carry In. Setting this bit high adds one LSB to the Δ-Phase word of the NCO. This is primarily used for test purposes and is normally set to zero.

Bit 1: Test bit. Always set to zero for normal operation.

Bit 2: Loop Filter Add/Subtract Control Bit. When this bit is set high the output of the loop filter is added to the FCW to form the Δ-Phase word for the NCO. Setting it low causes the output of the loop filter to be subtracted, allowing for correct operation when the frequency discriminator data is reversed.

Address 09_H: Control Register. Reset Value: 00_H

Bit 0: Used for test purposes only, should always be set to zero.

Bit 1: Q Channel input disable. Setting this input high disables the Q channel input and should be done when the Z2130 is used in the Direct I.F. Sampling Mode, using a single A/D Converter. In addition, the NCO outputs to the Q Channel section of the complex multiplier are disabled, effectively shutting down two of the four multiplier units and reducing power consumption.

Address $0A_H$: Loop Filter Control Register 0. Reset Value: 00_H

Bits 3-0: Loop gain control. Selects which eight bits of the 8-bit floating Point (Z2120) Mode (after conversion to 22-bit fixed point data) are selected for the input of the loop filter according to the table. The overall loop gain of the filter is inversely proportional to the value of this data:

Bits 3-0	Input bits selected
0_H	7-0
1_H	8-1
2_H	9-2
3_H	10-3
4_H	11-4
5_H	12-5
6_H	13-6
7_H	14-7
8_H	15-8
9_H	16-9
A_H	17-10
B_H	18-11
C_H	19-12
D_H	20-13
E_H	21-14
F_H	Not used

Bit 4: Test bit. Always set to zero for normal operation.

Bit 5: Sets the Loop filter update into the Automatic Update Mode when set high and into the Manual Update Mode when set low.

Bits 7-6: Selects the Frequency Discriminator Input Mode according to the table below:

Bit 7	Bit 6	Mode
0	0	16-bit Input
1	0	8-bit Input
X	1	8-bit Floating Point

The 8-bit floating Point Mode is designed to facilitate interfacing the Z2130 to the Z2120, with its 8-bit floating point frequency discriminator output. The format of the data in this mode is: Bits 7-5: mantissa, Bits 4-0: exponent. The value of the signal represented by the data in this mode is (Bits 7-5) x $2^{(\text{Bits } 4\text{-}0)}$. This signal is converted into a 22-bit fixed point number and used in the same way as the signal in the 16-bit Input Mode. The 8 MSBs of the $DISCIN_{15\text{-}0}$ bus are bidirectional. In all cases the 8 MSBs of the phase output of the NCO ($PHASE_{31\text{-}24}$) will be output on these pins when Bit 7 is set high.

Address $0B_H$: Loop Filter Control Register 1. Reset Value: 00_H

Bits 1-0: Sets the number of samples between updates of the Loop Filter in the Automatic Update Mode from 8 to 64, according to the equation:
Samples between updates = $2^{(\text{Update Count} + 3)}$

Bit 2: Setting this bit low sets K1 to zero in the Loop Filter.

Bit 3: Setting this bit low resets the accumulator in the Loop filter. This can be used to control the accumulator when erratic behavior is experienced and can also be used to effectively set K2 to zero.

Bit 4: Loop filter Accumulator Carry In. Setting this bit high adds one LSB to the Loop Filter Accumulator. This can be used to correct for drift in the loop filter accumulator, but this bit will normally be set to zero.

Bit 5: Sets the device into a test mode when set high. Do not use.

Bit 6: When this bit is set low it causes the NCO to be updated automatically each time the input of the Loop filter is updated. This is the normal mode of operation.

Address $0C_H$: Loop Filter Control Register 2. Reset Value: 00_H.

Bits 4-0: Gain 1. Sets the value of K1 in the Loop Filter according to the equation:
$K1 = 2^{(\text{Gain1})}$

Address $0D_H$: Loop Filter Control Register 3. Reset Value: 00_H

Bits 4-0: Gain 2. Sets the value of K2 in the Loop Filter according to the equation:
$K2 = 2^{(\text{Gain2})}$

Bit 5: When this bit is set low the data shown in the Viewport will be caused to saturate on overflow. This Saturation Mode eliminates the ambiguity caused by the cyclic characteristics of Two's Complement arithmetic on overflow.

READ MODE

Some of the internal parameters of the Z2130 can be read out of the device by reading registers 00H to 13H. Many of these parameters will not be useful in most applications primarily because they change every clock cycle and will therefore not be readable by a conventional microprocessor, especially the multi-byte parameters.

Addresses 00_H through 03_H: 32-bit NCO Accumulator value, as shown in the table below. This register is the actual NCO accumulator register and the value of this data will change every clock cycle.

Address	Bits	Accumulator bits
00_H	7-0	7-0
01_H	7-0	15-8
02_H	7-0	23-16
03_H	7-0	31-24

Addresses 04_H through 07_H: 32-bit Loop Filter output value, as shown in the table below. This register is the actual Loop Filter output register and the value of this data will change each time the Loop Filter is updated.

Address	Bits	Loop Filter bits
04_H	7-0	7-0
05_H	7-0	15-8
06_H	7-0	23-16
07_H	7-0	31-24

Address 08_H: 8-bit Loop Filter input value. This is the signal loaded into the Loop Filter after format conversion and scaling in the Barrel Register.

Addresses 09_H through $0C_H$: Complex multiplier input values, as shown in the table below. This data will change every clock cycle.

Address	Bits	Signal
09_H	7-0	COS_{7-0} from NCO
$0A_H$	7-0	SIN_{7-0} from NCO
$0B_H$	7-0	I_{IN7-0}
$0C_H$	7-0	Q_{IN7-0}

Note that when the Z2130 is used in the Direct I.F. Sampling Mode the Q_{IN7-0} data will be the output of the Pre-Processor Block.

Addresses $0D_H$ through 10_H: Output values of the individual multipliers in the Complex Multiplier Block, as shown in the table below. Only the MS Bytes are available, and this data will change every clock cycle.

Address	Bits	Signal
$0D_H$	15-8	COS x I_{IN}
$0E_H$	15-8	SIN x Q_{IN}
$0F_H$	15-8	COS x Q_{IN}
10_H	15-8	SIN x I_{IN}

Addresses 11_H through 12_H: Integrate and Dump Filter inputs, as shown in the table below. Only the MS Bytes are available, and this data will change every clock cycle.

Address	Bits	Signal
11_H	9-2	I_{IN}
12_H	9-2	Q_{IN}

Address 13_H: Status Flag Register. This address contains the status of various attributes of the Z2130. Reset value 00_H.

Bits 0 and 1: I and Q channel Integrate and Dump Filter accumulator status bits respectively in Saturate Mode. If these bits are set low they indicate that the outputs of the I and/or Q channel accumulators are saturated. These bits are only effective when the Saturate Mode is turned on by setting bits 0 and/or 1 in address 01_H.

Bits 2 and 3: I and Q channel Integrate and Dump Filter accumulator status bits respectively in Overflow Mode. If these bits are set low they indicate that the outputs of the I and/or Q channel accumulators have overflowed. Since this occurs irrespective of whether the Saturate Mode is turned on or not these bits can be used to determine overflow or saturation at any time. Further, if bit 2 is set low and bit 0 isn't (the same applies to bits 3 and 1 also), then this is an indication that the Saturation Mode is not set and can be used to check this status.

Bits 4 and 5: I and Q channel Viewport status bits, respectively. If these bit are set low they indicate that the signals in the I and/or Q channel Viewports are saturated and the positions of the windows should be raised to higher levels.

Bit 6: Loop Filter accumulator status. If this bit is low it indicates that the accumulator is saturated and should be reset to resume correct operation by momentarily setting bit 3 in address 0_H low.

Bit 7: This bit displays the status of the adder/subtracter between the Loop Filter and the NCO. Provided that the MSB of the FCW is set to zero (normal operating mode) then if this bit is low the Loop Filter output is being added to the FCW and if it is high the Loop Filter output is being subtracted. If the MSB of the FCW is set to one then the function of this flag is reversed.

PROGRAMMING THE Z2130

REGISTER MEMORY MAP SUMMARY

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	FUNCT. BLOCK
00	Q Viewport Position (4 bits)				I Viewport Position (4 bits)				Post Proc.
01							QSAT (0=ON)	ISAT (0=ON)	Post Proc.
02		Carry In (QAcc)	Carry In (IAcc)	Test (set to 0)	AutoDump (1=Auto)	Dump Count (3 bits)			Post Proc.
03					Sync Dump (0=Sync)	µP Dump (↑)	µP LF. Ld. (↑)	µP Fr. Ld. (↑)	Control
04	NCO Frequency Control Word Bits 7-0								NCO
05	NCO Frequency Control Word Bits 15-8								NCO
06	NCO Frequency Control Word Bits 23-16								NCO
07	NCO Frequency Control Word Bits 31-24								NCO
08						Add/Sub (Add=1)	Test (Set to 0)	Carry In (NCO)	NCO
09							IF Smplng (1=ON)	Test (Set to 0)	Control
0A	DISCIN Mode Select (2 bits)		Auto Lp.Ld. (1=ON)	Test (Set to 0)	DISCIN Gain (2110A and 2120 modes) (4 bits)				Loop Filter
0B		NCO Ld. (0=Auto)	Test (Set to 0)	Carry In (LF Acc.)	LF Acc.Rst (0=RST)	K1 Off (0=OFF)	Loop Update Rate		Loop Filter
0C				K1 Gain Factor (5 bits)					Loop Filter
0D			VP Sat. (0=ON)	K2 Gain Factor (5 bits)					Loop Filter

Notes: See register descriptions for more detailed information of function of register contents.

Do not set unlabelled bit locations or bit locations labelled "Test" to "1"

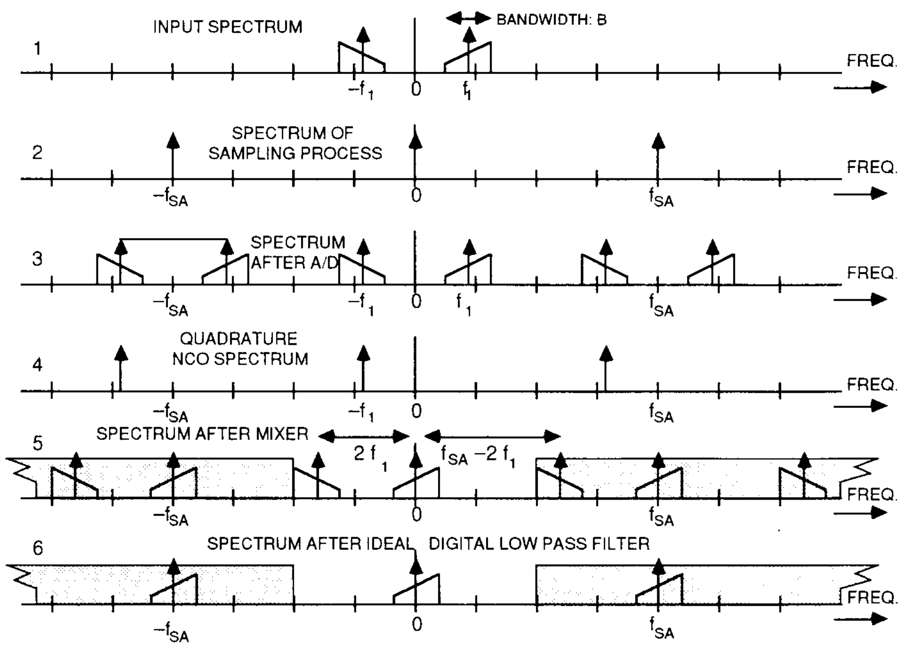
↑ Indicates that the function is enabled on the rising edge of this bit.
The bit must then be reset before the function can be enabled again.

APPLICATIONS INFORMATION

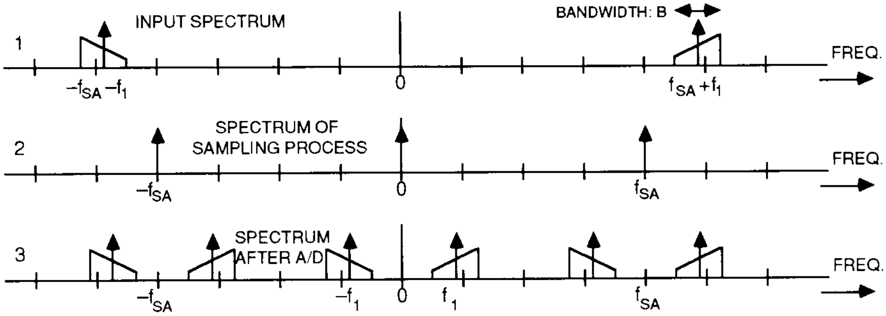
The Z2130 can be used in two different ways; the one chosen will usually be dependent on the application. In data rate applications up to approximately 10% of the sample clock rate it can be used with a single A/D converter (ADC); and this is referred to as the Direct I.F. Sampling Mode. For high speed data applications it is necessary to use the Z2130 in the full Quadrature Sampling Mode, i.e., using a conventional quadrature signal source and using the on-chip NCO in the quadrature mode.

USING THE Z2130 WITH A SINGLE ADC IN THE DIRECT I.F. SAMPLING MODE

In this mode the incoming signal is fed directly into the complex multiplier and converted to baseband. In this mode only two of the four multipliers in the complex multipler are used The sine and cosine inputs to the unused multiplers are shut down as well as the signal inputs from the Q Channel, reducing the block power consumption by a factor of two. In the Direct I.F. Sampling Mode the device does not make a true single-sideband conversion from I.F. to baseband, unlike the full Quadrature Sampling Mode, using two A/D converters. The consequence of this is shown spectrally in the diagram below. The input signal is a real signal and has the spectrum shown in line 1; this is then sampled with a signal at the frequency f_{SA} (line 2), resulting in the spectrum shown in line 3. When this is modulated with the complex signal of the quadrature NCO (line 4), the spectrum after the mixer is as shown in line 5. The sections shown inside the shaded areas are the aliases of the baseband signal beyond the Nyquist frequency and are not of concern. The signals inside the primary Nyquist region consist of the desired signal and a spectrally reversed image signal which is separated from the former by f_1, the I.F. frequency before sampling. This signal has to be removed by filtering at this point. In the Z2130 an Integrate and Dump filter is provided for this purpose. This type of first order filter provides more than 25 dB of attenuation of the unwanted signal if the bandwidth B of the signal is less than 10% of the sampling frequency. In this example the input signal was shown at a low I.F. frequency. ($f_1 < \frac{1}{2} f_{SA}$, i.e. the signal was inside the primary Nyquist region.) However, provided that $B < \frac{1}{2} f_{SA}$ this is not necessary; as long as the input is completely contained in any of the non-primary Nyquist regions ($N.\frac{1}{2} f_{SA}$ to $(N+1).\frac{1}{2} f_{SA}$). This is shown in the second diagram, where it can be seen that in line 3 of the diagram the high frequency input has the same spectrum after sampling as the low frequency input had in the original case and consequently the processes following this are identical to those in the original case.



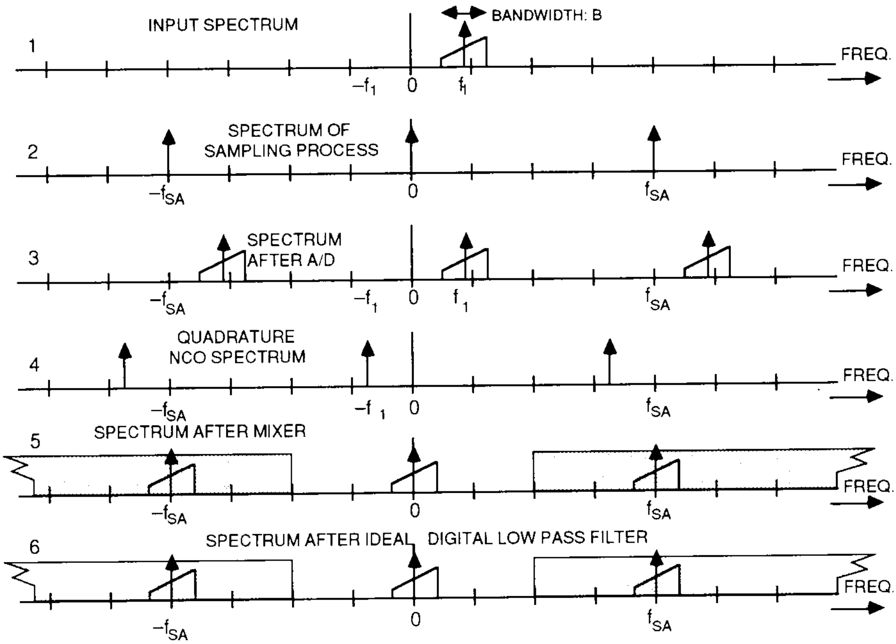
SPECTRA OF SIGNALS IN DIRECT I.F. SAMPLING MODE



SPECTRA OF SIGNALS IN DIRECT I.F. SAMPLING MODE WHEN THE I.F. FREQUENCY IS HIGHER THAN THE SAMPLING FREQUENCY

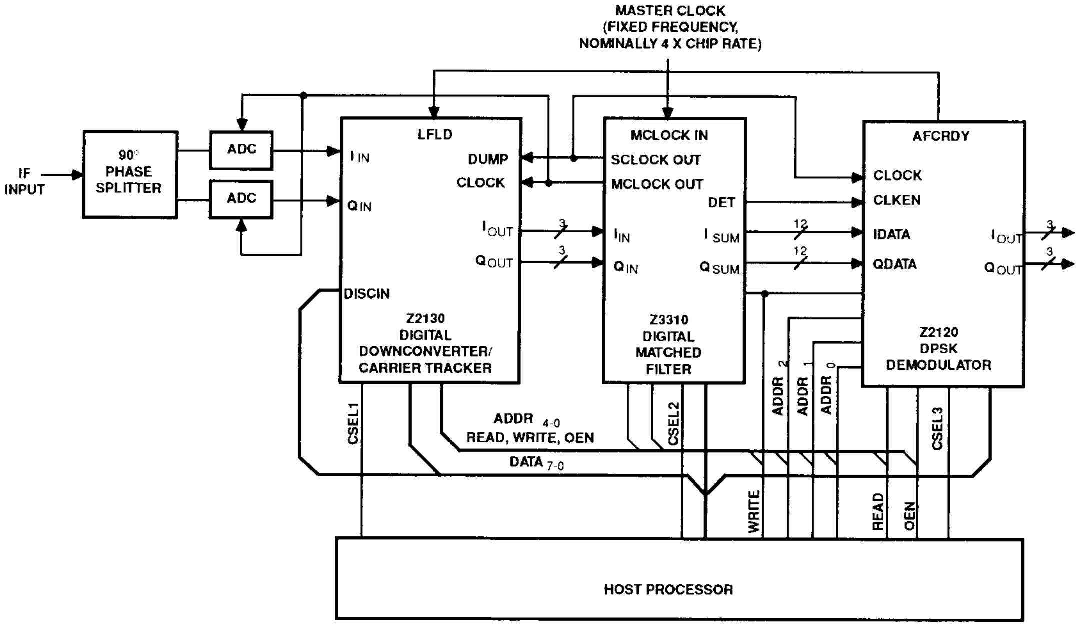
USING THE Z2130 WITH TWO ADCs

Signals with higher symbol rates (more than 10% of f_{SA}) can be processed with the Z2130 by using the Quadrature Sampling Mode. In this mode the device is used to perform a true single-sideband conversion to baseband and the image sideband associated with the Direct I.F. Sampling Mode does not appear. This is shown in the diagram below. Since both the input and NCO signals are now complex the spectrally reversed image found in the Direct I.F. Sampling Mode no longer exists and only the Nyquist limit constrains the maximum value of B.



SPECTRA OF SIGNALS IN QUADRATURE SAMPLING MODE

APPLICATIONS INFORMATION



TYPICAL WIDE-BAND APPLICATION: A SPREAD SPECTRUM DEMODULATOR

By combining the Z2130 with the Z3310 Digital Matched Filter and the Z2120 Differential PSK Demodulator chips a very simple spread spectrum receiver may be realized. The sampling rate should nominally be four times the chipping rate to generate two samples per chip for the Z3310 by dumping every two cycles. The DET output of the Z3310 provides the CLKEN signal for the Z2120 for synchronous processing. The table gives typical parameters for the Z2130 setup to operate in this mode. The value for the NCO FCW in this example will set the NCO frequency to $f_{CLK}/8$. This should, of course, be set as appropriate for the application, as should the loop gain parameters. The discriminator gain is shown set to its maximum value here. The gain would normally be set to a lower value during the inital acquisition stage and then set to this value after carrier acquisition is complete.

ADDR	DATA	Primary Result
00	00	I and Q viewport set to position 0
01	00	I and Q saturation enabled
02	08	Set auto dump every 2 cycles
03	00	Not used
04	00	Sets bits 7-0 of NCO to zero
05	00	Sets bits 15-8 of NCO to zero
06	00	Sets bits 23-16 of NCO to zero
07	20	Sets bits 31-24 of NCO to 10_H
08	04	Set normal (positive) discrim. mode
09	00	Set Quadrature Sampling mode
0A	40	Set 2120 mode, manual loop load, set disc. gain to max. value
0B	0C	Set auto NCO load, 2nd. oder loop
0C	0E	K1=16,384 (2^{14})
0D	0A	Viewport sat. enabled, K2=1024 (2^{10})

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