2M X 32 DRAM Card

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
STI322000C1-60Vx	60ns	15ns	110ns
STI322000C1-70Vx	70ns	18ns	130ns
STI322000C1-80Vx	80ns	20ns	150ns

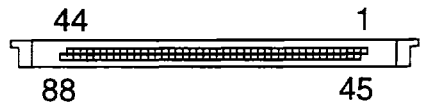
- Dimensions—2.13" wide x 3.37" long x 0.13" thick
- Meets specifications for JEDEC and JEIDA 88-pin DRAM cards
- 88-pin, two piece connector with keying
- PDx pins for card configuration information
- CBR, $\overline{RAS}$ only, or Hidden refresh capability
- Normal or Self-refresh options
- 2048 cycles/32ms normal refresh
  —or—
  2048 cycles/128ms self-refresh
- 3.3V power supply

GENERAL DESCRIPTION

The Simple Technology STI322000C1 is a 2M bit x 32 Dynamic RAM high density memory card. The Simple Technology STI322000C1 consist of four CMOS 2M x 8 bit DRAMs in 28-pin SOJ package. The circuit board is enclosed in a credit-card sized frame and 88-pin connector package as specified for JEDEC and JEIDA standard card packaging.

The card's small package size makes it suitable for use in small portable computers, palmtops, etc. System memory upgrades are simplified due to the fact that the system box does not need to be opened or otherwise disassembled.

The STI322000C1-xxV is an IC DRAM card with 3.3V power supply and normal refresh. The STI322000C1-xxVS is an IC DRAM card with 3.3V power supply and self-refresh. The cards are intended for 88-pin IC DRAM card sockets.



View From Outside The Card 0189

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	23	$\overline{CAS_0}$	45	V_{SS}	67	V_{SS}
2	DQ_0	24	$\overline{CAS_1}$	46	DQ_{16}	68	$\overline{CAS_3}$
3	DQ_1	25	V_{CC}	47	DQ_{17}	69	NC
4	DQ_2	26	$\overline{RAS_2}$	48	DQ_{18}	70	$\overline{W}$
5	DQ_3	27	NC	49	DQ_{19}	71	PD_1
6	DQ_4	28	PD_2	50	DQ_{20}	72	PD_3
7	DQ_5	29	PD_4	51	DQ_{21}	73	V_{SS}
8	DQ_6	30	PD_6	52	DQ_{22}	74	PD_5
9	NC	31	NC	53	DQ_{23}	75	PD_7
10	DQ_7	32	NC	54	NC	76	PD_8
11	V_{CC}	33	NC	55	NC	77	NC
12	NC	34	DQ_8	56	V_{SS}	78	NC
13	A_0	35	V_{CC}	57	A_1	79	NC
14	A_2	36	DQ_9	58	A_3	80	DQ_{24}
15	NC	37	NC	59	A_5	81	DQ_{25}
16	A_4	38	DQ_{10}	60	A_7	82	DQ_{26}
17	V_{CC}	39	DQ_{11}	61	A_9	83	DQ_{27}
18	A_6	40	DQ_{12}	62	NC	84	DQ_{28}
19	A_8	41	DQ_{13}	63	V_{SS}	85	DQ_{29}
20	A_{10}	42	DQ_{14}	64	NC	86	DQ_{30}
21	NC	43	DQ_{15}	65	NC	87	DQ_{31}
22	$\overline{RAS_0}$	44	V_{SS}	66	$\overline{CAS_2}$	88	V_{SS}

Pin Names

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS_0}$, $\overline{RAS_2}$	Row Adress Strobe
$\overline{CAS_0}$-$\overline{CAS_3}$	Column Address Strobe
PD_1-PD_8	Presence Detect
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

PD_1=NC, PD_2=NC, PD_3=V_{SS},PD_4=V_{SS}, for 8 MB Card using 2Mx8 chips and PD_5=NC for single bank

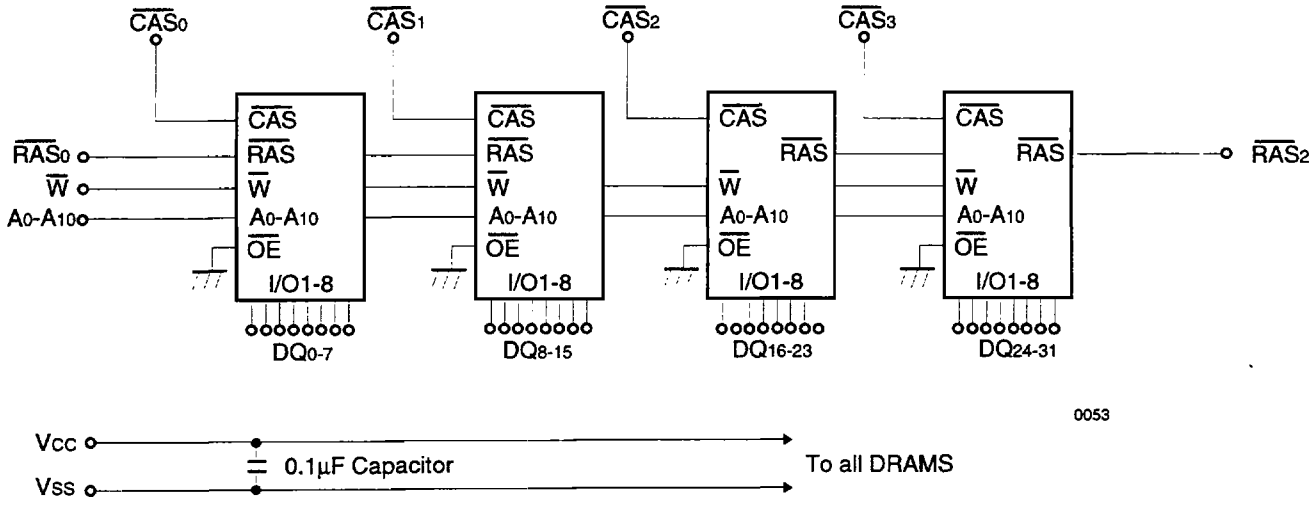
Access Time

Pin	60ns	70ns	80ns
PD_6	NC	V_{SS}	NC
PD_7	NC	NC	V_{SS}

Refresh Type

Pin	Normal Refresh	Self-Refresh
PD_8	NC	V_{SS}

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATION CHARACTERISTICS—NORMAL REFRESH

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI...-60V	I_{CC1}	—	400	mA
	STI...-70V		—	360	mA
	STI...-80V		—	320	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	8	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	STI...-60V	I_{CC3}	—	400	mA
	STI...-70V		—	360	mA
	STI...-80V		—	320	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	STI...-60V	I_{CC4}	—	320	mA
	STI...-70V		—	280	mA
	STI...-80V		—	240	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	4	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI...-60V	I_{CC6}	—	400	mA
	STI...-70V		—	360	mA
	STI...-80V		—	320	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}, all other pins not under test=0V)		I_{IL}	-20	20	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		I_{OL}	-5	5	µA
Output High Voltage Level (I_{OH}=-2.0mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2.0mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

DC AND OPERATION CHARACTERISTICS—SELF REFRESH

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI...-60VS	I_{CC1}	—	400	mA
	STI...-70VS		—	360	mA
	STI...-80VS		—	320	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	4	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	STI...-60VS	I_{CC3}	—	400	mA
	STI...-70VS		—	360	mA
	STI...-80VS		—	320	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	STI...-60VS	I_{CC4}	—	320	mA
	STI...-70VS		—	280	mA
	STI...-80VS		—	240	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	1200	µA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI...-60VS	I_{CC6}	—	400	mA
	STI...-70VS		—	360	mA
	STI...-80VS		—	320	mA
Self Refresh Current ($\overline{RAS}$=$\overline{CAS}$=V_{IL}, DQ_X=W=A_X=V_{CC}-0.2V or 0.2V)		I_{CC5}	—	1000	µA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}, all other pins not under test=0V)		I_{IL}	-20	20	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		I_{OL}	-5	5	µA
Output High Voltage Level (I_{OH}=-2.0mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2.0mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A=25 °C)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0-A_{10})	C_{IN1}	—	20	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	28	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_2$)	C_{IN3}	—	14	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	7	pF
Input/Output Capacitance ($DQ_{0\text{-}7,\ 8\text{-}15,\ 16\text{-}23,\ 24\text{-}31}$)	CDQ_1	—	7	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=3.3V±10%, See notes 1, 2)

Parameter	Symbol	STI...-60Vx		STI...-70Vx		STI...-80Vx		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		12		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	10		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6

continued on the next page

AC CHARACTERISTICS (continued)

Parameter	Symbol	STI...-60Vx		STI...-70Vx		STI...-80Vx		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Refresh period (normal)	t_{REF}		32		32		32	ms	
Refresh period (self-refresh)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge (C-B-R counter test)	t_{CPT}	20		30		30		ns	
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		-50		ns	12
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	110		130		150		ns	12
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		100		µs	12

NOTES

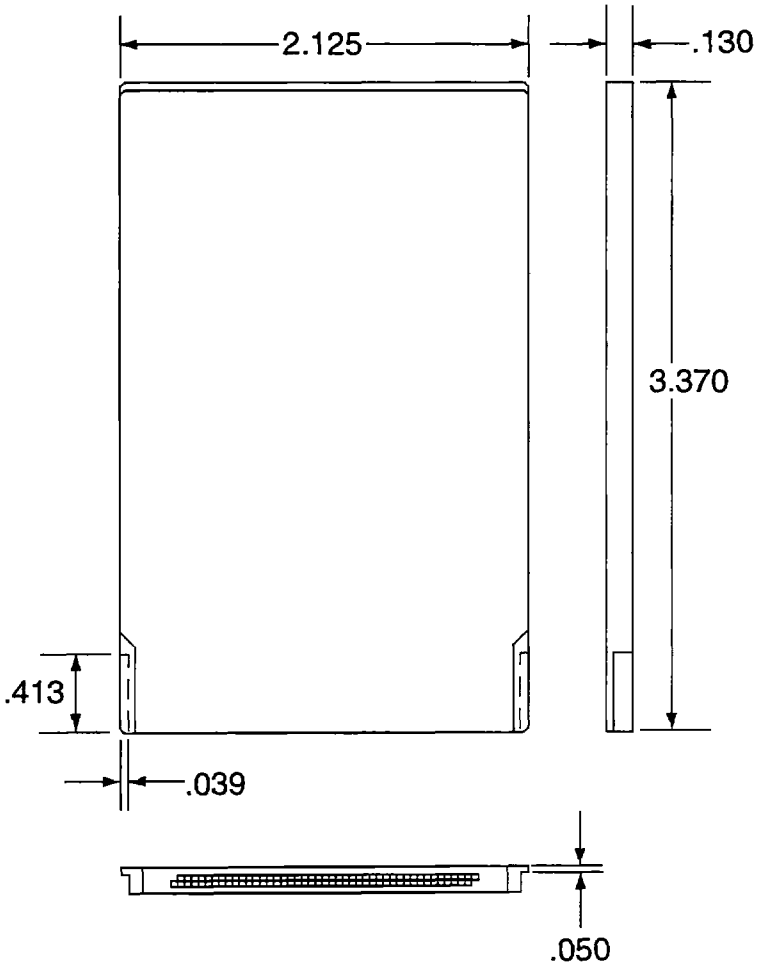
1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. 2048 cycle of Burst Refresh must be executed within 128ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

For the normal refresh option, please refer to attached Timing Chart I. For the self-refresh option, please refer to attached Timing Charts I and VI.

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED