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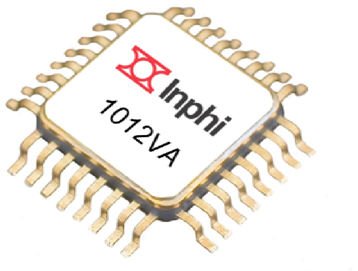
1012VA
DC to 10 GHz Differential Variable Gain Amplifier
Data Sheet



Applications

- Broadband test & instrumentation
- Automatic test equipment
- Differential ADC drivers
- Single ended to differential conversion
- RF sampling receivers
- RF gain blocks
- Broadband precision signal generation and amplification

Features

- Broadband: DC to 10 GHz (3 dB)
- Differential input and output
- 12 to 26 dB variable differential gain
- Input common mode range: ± 500 mV
- Up to 2 Vpp differential output
- Low input referred noise: 5 nV/√Hz
- Gain flatness: ± 0.5 dB to 6.5 GHz
- Great linearity: 1.5 % THD to 10 GHz
- Input return loss: 20 dB to 5 GHz
- Output return loss: 15 dB to 5 GHz
- CMRR: >20 dB to 10 GHz
- Available in QFP package

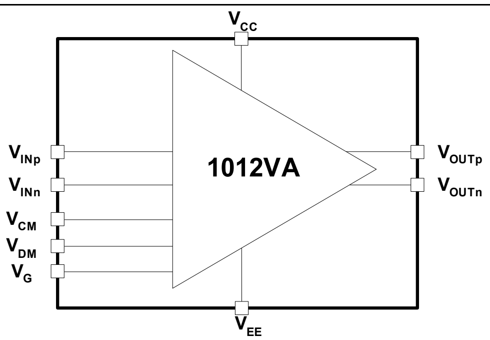
Description

The 1012VA is a general-purpose differential variable gain amplifier with a maximum differential gain of 27 dB, dynamic range of >14 dB and maximum differential output amplitude of 2 Vpp. Because it is a true DC to 10 GHz (3 dB) amplifier with good linearity, gain flatness and return loss, it is ideally suited to test and instrumentation applications in which a variable, loop-leveled differential or single-ended signal is required. The excellent distortion performance makes the 1012VA a great solution for 6 to 8 bit RF sampling receivers.

The 1012VA operates from +5.0 V (V_{CC}) and -5.2 V (V_{EE}) power supplies and ground.

The 1012VA is available in an 8 x 8 mm, 32-lead quad flat package (QFP). Evaluation boards with SMA connectors are also available.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter[1]	Symbol	Conditions	Min	Max	Unit
Positive Supply Voltage	V_{CC}		---	6.0	V
Negative Supply Voltage	V_{EE}		-6.0	---	V
Input Voltage	V_{INp}, V_{INn}		-1	1	V
Differential Input Voltage	V_{Inp}-V_{INn}		-0.5	0.5	V
Output Voltage	V_{OUTp}, V_{OUTn}		-2.0	2.0	V
Control Inputs	V_{CM}, V_{DM}, V_G		V_{EE} -1.0	V_{CC}+1.0	V
Operating Temperature (Junction) - Die	T_J		---	+175	°C
Operating Temperature (Case) - Packaged	T_C		---	+125	°C
Shipping/Storage Temperature	T_{STORE}		---	+125	°C
Humidity	RH		0	100	%
ESD protection (HBM)[2]	V_{ESD}	V_{CC},V_{EE}, GND	>500	---	V
		Inputs and output	>100	---	V
		DC control inputs	>500	---	V

Notes:

[1] Absolute maximum ratings have not been verified by testing.

[2] As per JESD22-A114-B. ESD testing has not been completed.

Operating Conditions

Important Note:

Unused I/O should be terminated with 50 Ω to GND for all specifications to be met.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Positive Power Supply Voltage	V_{CC}		4.90	5.0	5.25	V
Negative Power Supply Voltage	V_{EE}		-5.46	-5.2	-5.10	V
Positive Supply Current	I_{CC}		---	235	260	mA
Negative Supply Current	I_{EE}		---	295	320	mA
Power Dissipation	P_D		---	2.7	3.1	W
Control Inputs Voltages	V_{CM}, V_{DM}		V_{EE}	---	V_{CC}	V
	V_G		-3.0	---	+2.0	V
Control Inputs Currents	I_{VG}, I_{VDM}		-1.0	---	+1.0	mA
	I_{VCM}		-2.0	---	+2.0	mA
Operating Temperature (Junction) - Die	T_J		+15	---	+150	°C
Operating Temperature (Case) - Packaged	T_C		10	---	70	°C

DC Specifications

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any I/O.
- Power sequencing is required. For power up and power down operation, please see page 4.

NOTE – The specifications below apply only to packaged parts.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input DC resistance	R_{in}	To ground	45	50	55	Ω
Maximum Gain (differential)	A_{VD}	$(V_{OUTp}-V_{OUTn})/(V_{INp}-V_{INn})$ at 100 MHz	26	27	28	dB
Maximum Gain (single-ended)	A_{VS}	V_{OUTp} $/(V_{INp}-V_{INn})$ at 100 MHz	20	21	22	dB
Minimum Gain (differential)		$(V_{OUTp}-V_{OUTn})/(V_{INp}-V_{INn})$ at 100 MHz	---	---	12	dB
Minimum Gain (single-ended)		V_{OUTp} $/(V_{INp}-V_{INn})$ at 100 MHz	---	---	6	dB
Maximum Differential Input Amplitude			200	---	---	mVpp
Maximum Output Amplitude		Each output	1.0	---	---	Vpp
Output DC resistance	R_{out}	To internally-generated reference	45	50	55	Ω
Input common-mode range[1]	V_{ICM}		-0.5	---	0.5	V
Output-referred Differential DC offset		$V_{OUTp}-V_{OUTn}$; $V_{DM} = 0$ V	-50	---	50	mV
Output common-mode offset		$(V_{OUTp} + V_{OUTn})/2$; $V_{CM} = 0$ V	-50	---	50	mV
Minimum output common-mode offset adjust value		$(V_{OUTp} + V_{OUTn})/2$; $V_{CM} = V_{EE}$		-100	-50	mV
Maximum output common-mode offset adjust value		$(V_{OUTp} + V_{OUTn})/2$; $V_{CM} = V_{CC}$	50	100		mV
Minimum output differential-mode offset adjust value		$V_{OUTp}-V_{OUTn}$; $V_{DM} = V_{CC}$		-100	-50	mV
Maximum output differential-mode offset adjust value		$V_{OUTp}-V_{OUTn}$; $V_{DM} = V_{EE}$	50	100		mV
Gain stability		At 100 MHz, over case temperature range	-0.3	---	0.3	dB

Notes:

[1] Based on simulation: not yet characterized.

AC Specifications

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Bandwidth (3 dB)			9	9.6	12	GHz
Bandwidth (± 0.5 dB)			---	6.5	---	dB
Low Frequency Gain flatness		DC to 100 MHz	-0.9	---	0.1	dB
Noise Figure[1]	NF	f = 500 MHz, differential input, max. gain	---	11.0	11.5	dB
		f = 500 MHz, differential input, 6 dB gain	---	22.5	23.5	dB
Single-Ended Output Total Harmonic Distortion[2]	THD	DC to 5 GHz	---	1.6	2.5	%
		DC to 10 GHz	---	1.7	2.5	%
Common mode rejection ratio	CMRR	DC to 10 GHz	20	---	---	dB
Input Return Loss (Single-Ended)	IRL	DC to 5 GHZ	18	20	---	dB
		5 to 10 GHz	10	12	---	dB
Output Return Loss (Single-Ended)	ORL	DC to 5 GHZ	14	15	---	dB
		5 to 10 GHz	9	10	---	dB

Notes:

[1] Noise figure is 3 dB higher for single-ended input.

[2] 100 mVpp SE input at maximum gain, 200 mVpp SE input for SE gain ≤14 dB.

Step Response Specification

To measure the step response of the amplifier, a fast step is applied to the input of the amplifier and the output voltage is measured over time. Input step rise time affects the response, and should be limited based on the amplifier's bandwidth and/or rise time. For these tests, we limit the input pulse bandwidth to approximately 10 GHz by setting the 10%-90% rise time to 35 ps.

Parameter	Definition
V_{OUT}	Output voltage difference between baseline and the value measured 100 ns after pulse has settled on (Vx) which all ratio-based specifications are related.
Settling Time	Time between output voltage crossing 50% of V_{OUT} to the last crossing of Vh or Vl near initial transient, whichever is greater. Vh = Vx + 2% V_{OUT} and Vl = Vx - 2% V_{OUT}. Vx is the voltage measured at 100 ns.
Overshoot	Ratio of highest output voltage deviation near initial transient to V_{OUT}.
Drift	Ratio of the deviation in output amplitude after a long time (allowing devices to reach a new thermal equilibrium, ~ 1 ms) to V_{OUT}.
Rise time	Time interval on the initial transient from 20% to 80% of V_{OUT}.

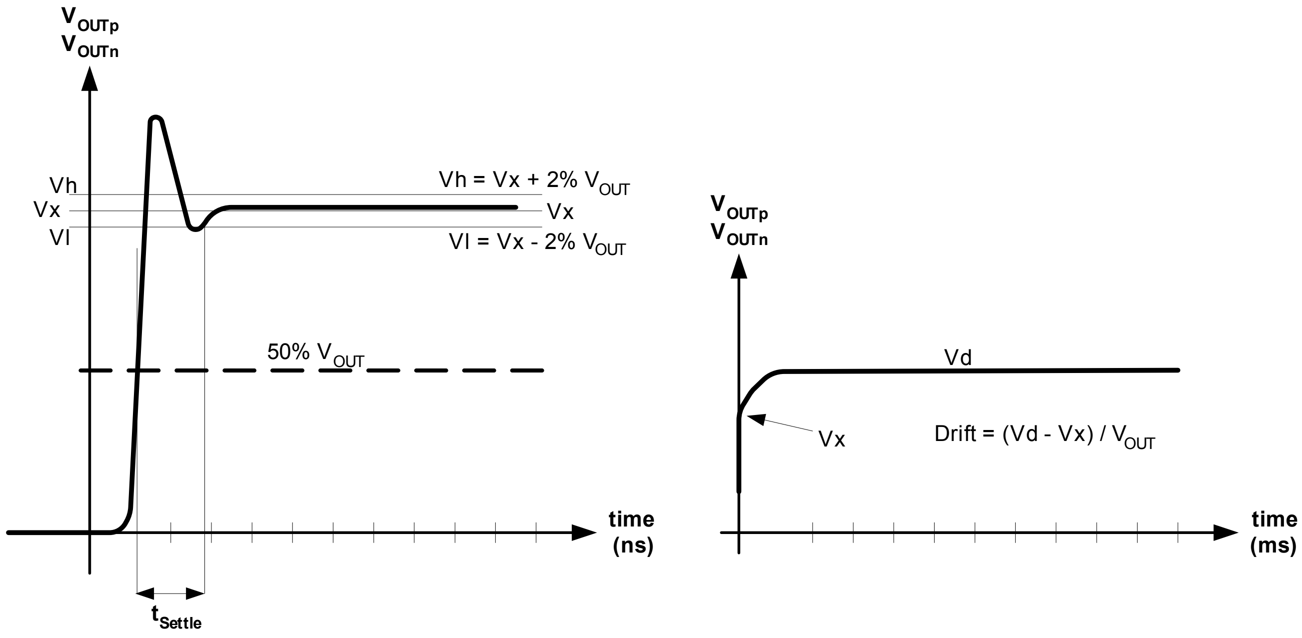
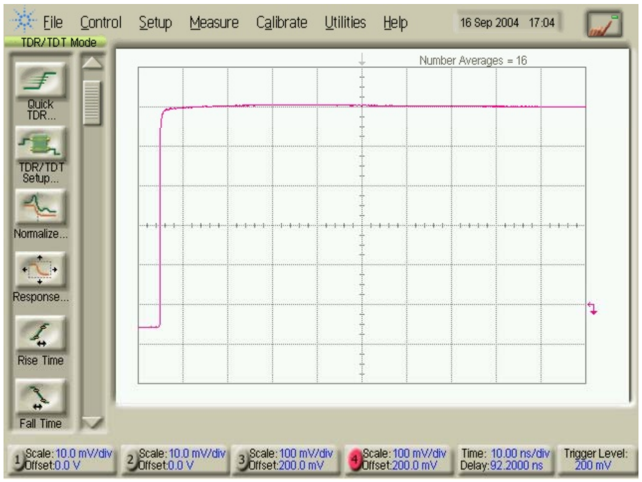


Figure 1. Settling time (left) and output drift (right) definitions.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Settling Time	$t_{Settling}$	Within 2 % of the output potential measured 100 ns after input step	---	---	2	ns
Overshoot			---	---	2.5	%
Output Drift	Vd	Difference between potential at output between 100 ns and 5 ms after input step	-5	---	5	%
Output Rise Time	t_r		45	50	60	ps

Typical Characteristics



1 Scale: 10.0 mV/div Offset: 0.0 V
2 Scale: 10.0 mV/div Offset: 0.0 V
3 Scale: 100 mV/div Offset: 200.0 mV
4 Scale: 100 mV/div Offset: 200.0 mV
Time: 10.00 ns/div Delay: 92.2000 ns
Trigger Level: 200 mV

Figure 2. Typical pulse response of the 1012VA showing very flat response over 100 ns to a 50 mV single-ended step applied to V_{INp}.

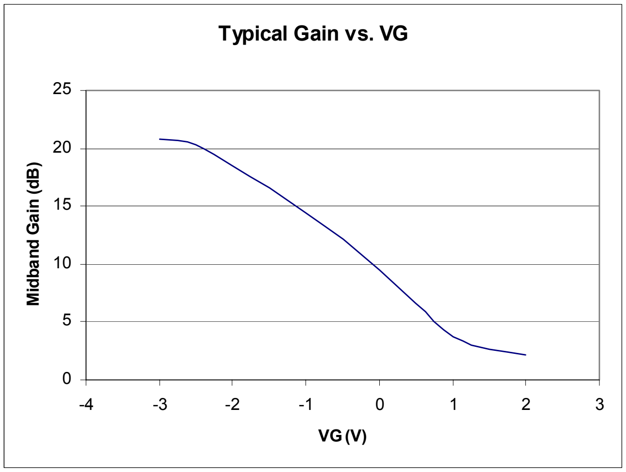


Figure 3. Typical mid-band (100 MHz) single-ended gain (A_{VS}) vs. V_G

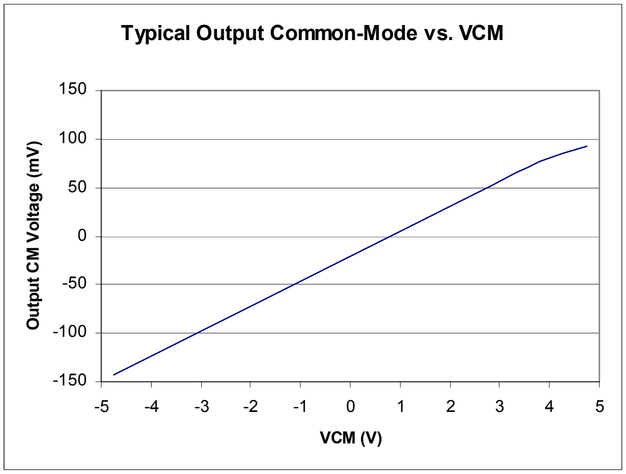


Figure 4. Typical output common-mode voltage vs. V_{CM} control voltage. The voltage is calculated as the average of the two outputs: $(V_{OUTp} + V_{OUTn})/2$.

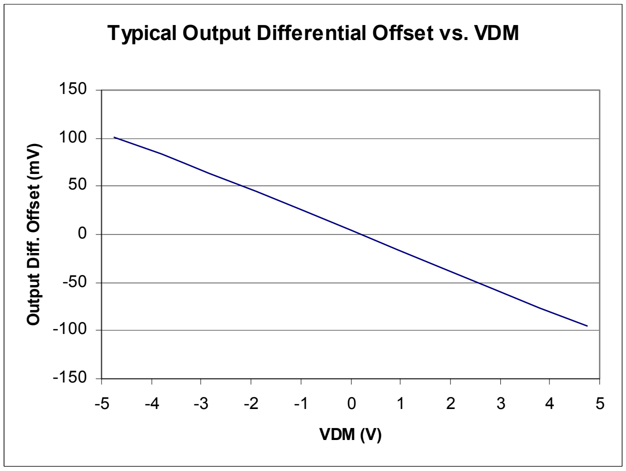


Figure 5. Typical output differential offset voltage vs. V_{DM} control voltage. The differential offset is calculated as the difference of the two outputs: V_{OUTp} - V_{OUTn}. Input referred differential offset is the output differential offset divided by the differential gain.

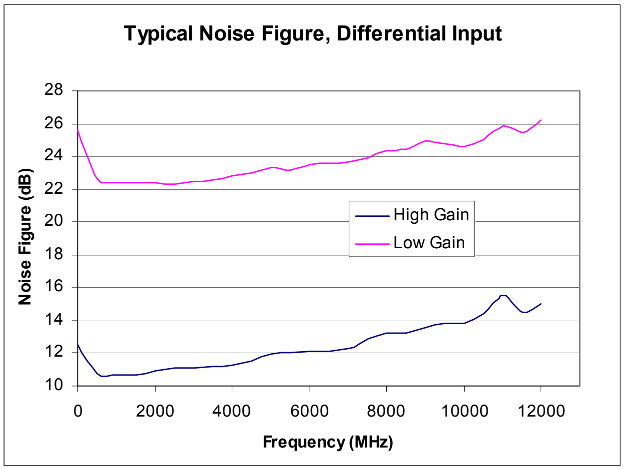


Figure 6. Typical noise figure vs. frequency for the 1012VA with differential inputs. Measurements were made using a single-ended noise source at the input and a single-ended noise figure meter at the output then subtracting 3 dB from the result. High gain is approximately 20 dB, low gain is approximately 6 dB.

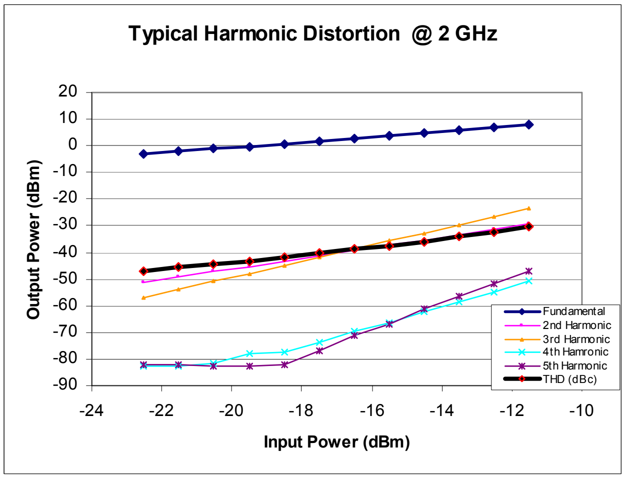


Figure 7. Typical harmonic distortion behavior for the 1012VA for single-ended input. The spectrum analyzer set the noise floor to about –83 dBm. High- and low-gain response is nearly identical, save for a shift in the input power axis.

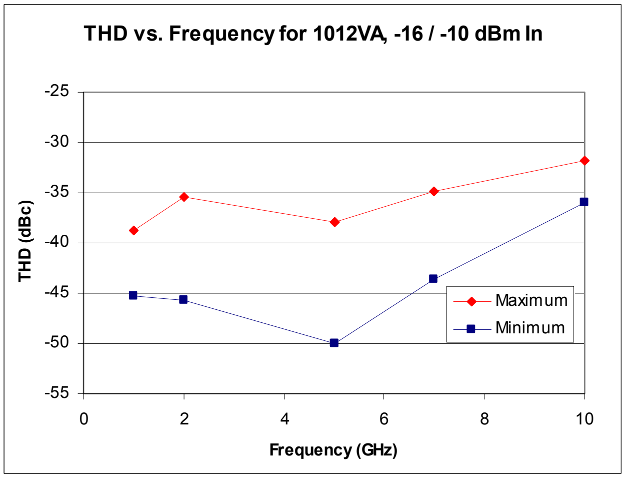


Figure 8. THD for the 1012VA over all operating conditions with a fixed, single-ended input sinusoid at 100 mVpp (-16 dBm) for high gain, 200 mVpp (-10 dBm) for low gain. By comparing this data to **Figure 9**, the odd-ordered harmonic distortion, one notes that even-ordered harmonics dominate the response away from 2 GHz.

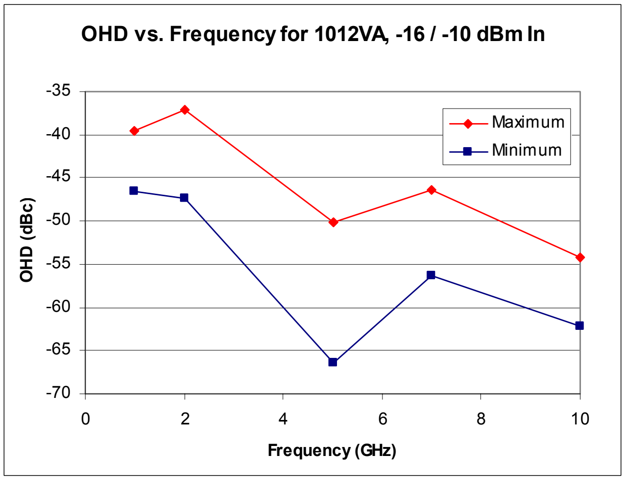


Figure 9. Odd Harmonic Distortion (OHD) for the 1012VA over all operating conditions with a fixed, single-ended input sinusoid at 100 mVpp (-16 dBm) for high gain, 200 mVpp (-10 dBm) for low gain. When the output is taken differentially, the even-ordered harmonics cancel, and the OHD is representative of the waveform's distortion.

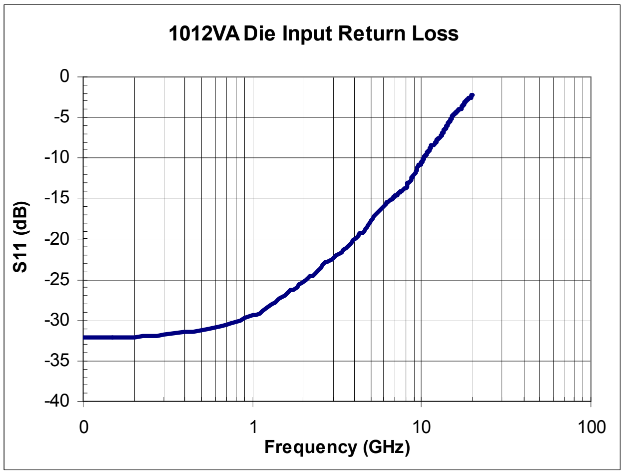


Figure 10. Typical S11 parameter on a 1012VA die for single-ended input.

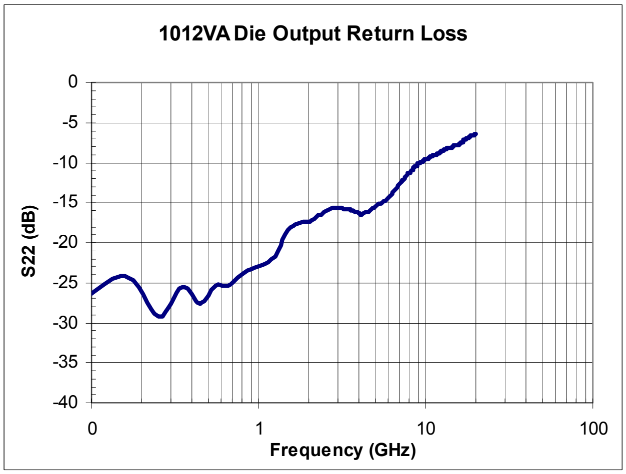


Figure 11. Typical S22 parameter on a 1012VA die for single-ended input.

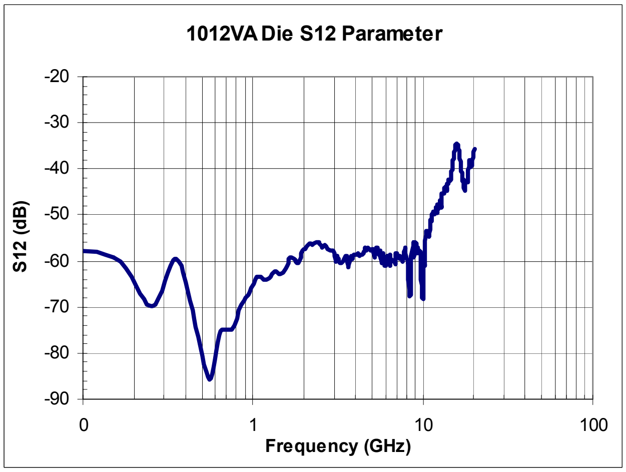


Figure 12. Typical S12 parameter (single-ended) on a 1012VA die.

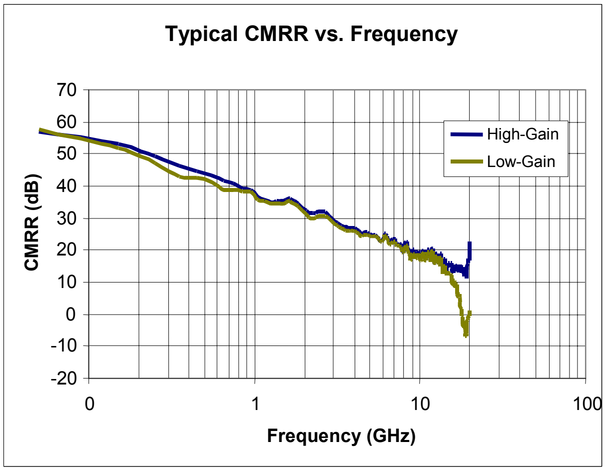


Figure 13. Common-mode rejection ratio vs. frequency for the 1012VA shown for both high and low gain. Differential-mode gain was divided by the common-mode gain measured using a power divider at the 1012VA input.

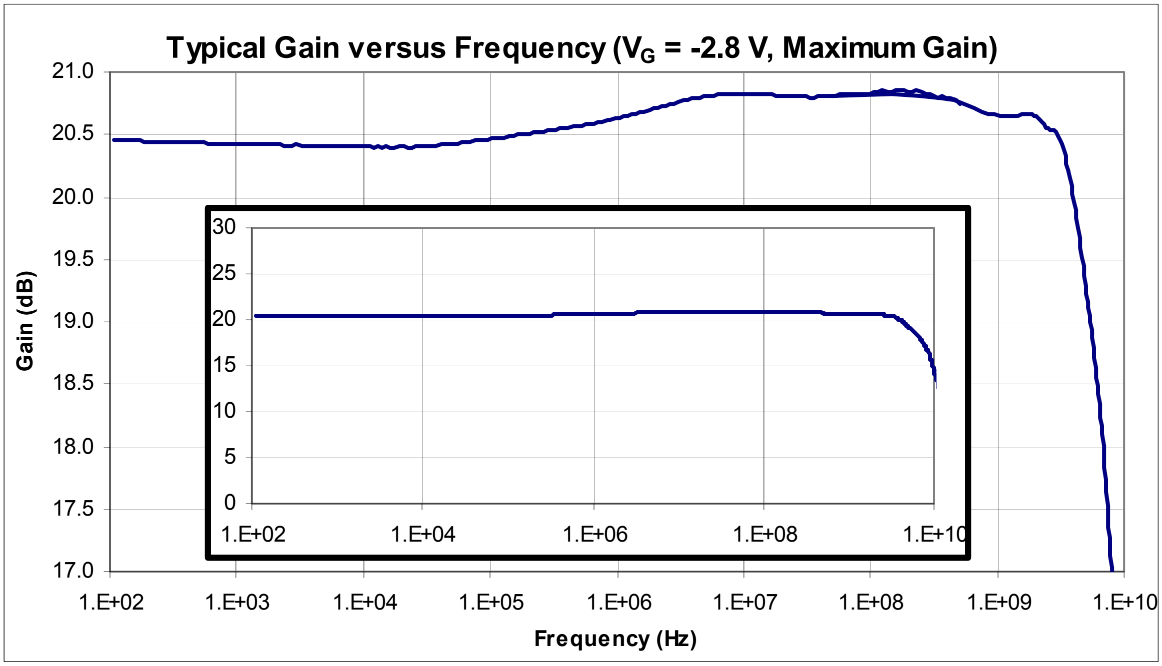


Figure 14. Typical single-ended gain (A_{VS}) vs. frequency characteristic for 1012VA (V_G=-2.8 V, max. gain).

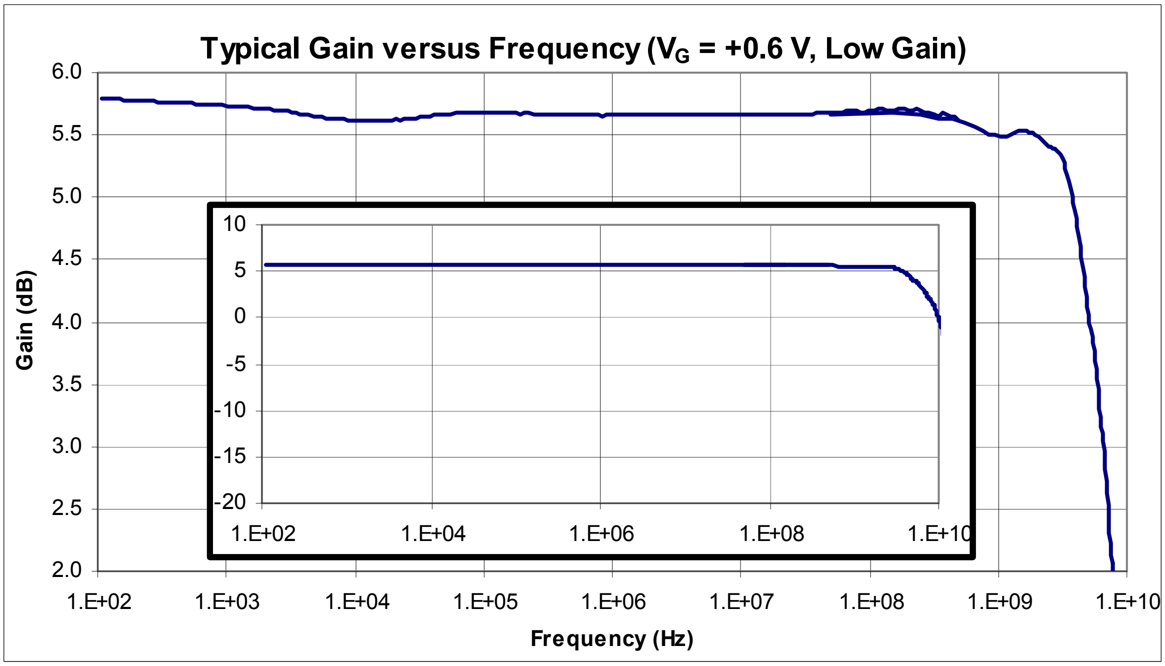
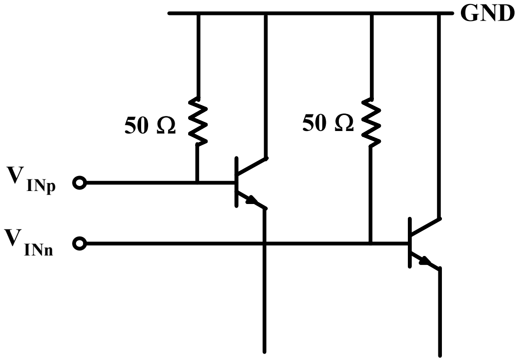
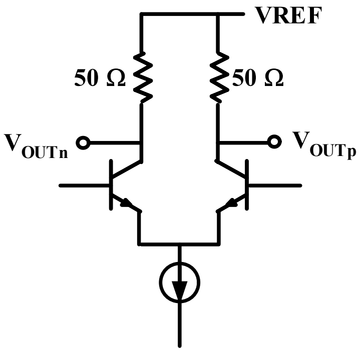
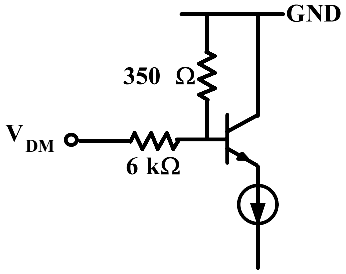


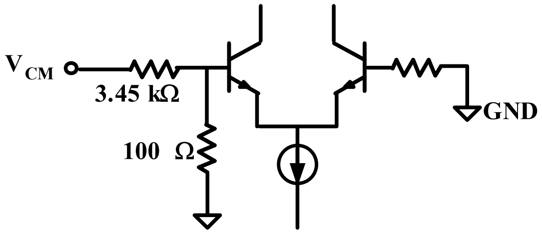
Figure 15. Typical single-ended gain (A_{VS}) vs. frequency characteristic for 1012VA (V_G=+0.6 V, low gain).

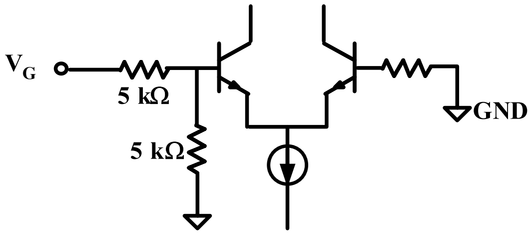
1012VA I/O Equivalent Circuits



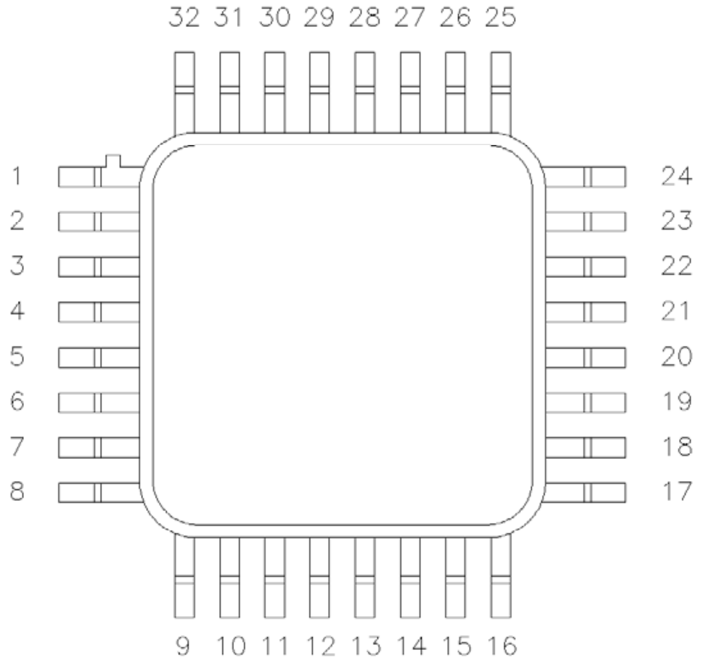








32-Lead QFP Pin Out

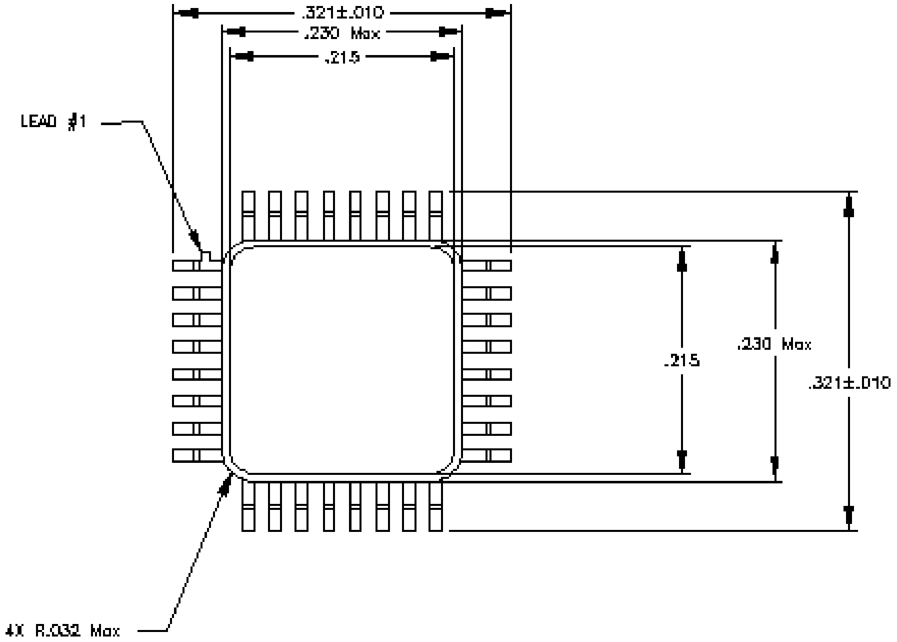


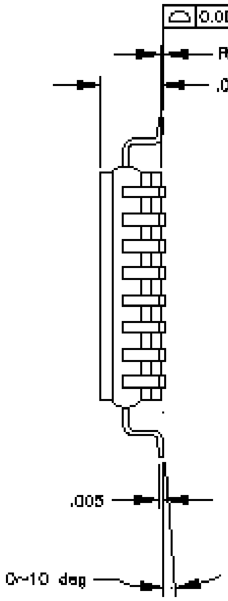
Name	Pin	Description	Function
V_{INp}	3	Non-inverting input. Internally terminated 50 Ω to GND.	Input
V_{INn}	6	Inverting input. Internally terminated 50 Ω to GND.	Input
V_{OUTp}	22	Non-inverting output. Always terminate to 50 Ω to GND.	Output
V_{OUTn}	19	Inverting output. Always terminate to 50 Ω to GND.	Output
V_{DM}	26	Output differential-mode offset adjust	Input
V_{CM}	15	Output common-mode offset adjust	Input
V_G	10	Gain control adjust	Input
GND	1, 2, 4, 5, 7, 8, 12, 13, 17, 18, 20, 21, 23, 24, 28, 29	Ground	Supply
V_{EE}	14, 30	Power Supply: Connect to –5.2 V	Supply
V_{CC}	11, 27	Power Supply: Connect to 5.0 V	Supply
NC	9, 16, 25, 31, 32	Not connected	

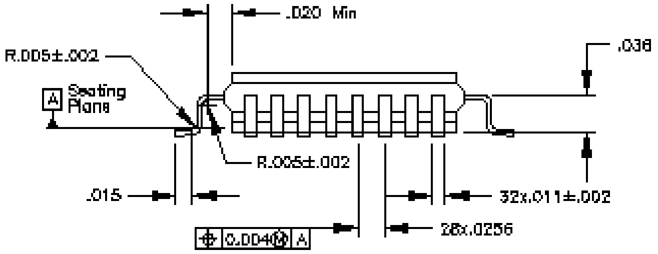
Notes:

- The top and bottom of the package are connected to GND internally.
- Connecting the bottom of the 1012VA package to circuit board GND is not required.

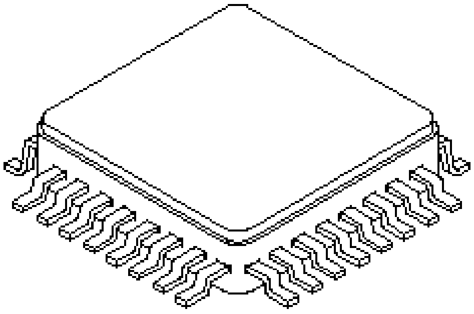
32-Lead QFP Package Information





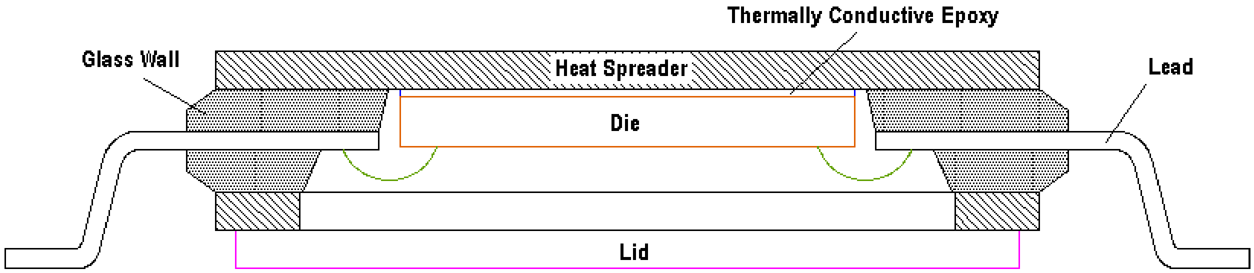


Plating Specification: 50~200 uinch Ni/50 uinch Au



1012VA QFP Package Thermal Characteristics

The 1012VA is packaged in a 32-lead quad flat pack (QFP) with gold plated Kovar base, leads and lid, as well as Corning 7052 glass walls. The package has an internal heat spreader to improve thermal management. The package main thermal path is upwards and its construction is sketched below. **It is recommended to attach a heat sink to the package heat spreader**. The package heat spreader and lid are internally connected to ground. The 1012VA in QFP package is designed to operate with a case temperature up to 70 °C. The user must design the system so that this temperature specification is satisfied.



Values of thermal resistance for different airflow conditions are reported in the table below. Case-to-ambient thermal resistance (θ_{CA}) is estimated with the assumption that the package lid is soldered to a metal pad on a four-layer board. Board stack-up and dimensions are as per JEDEC standard JESD51-7. The metal pad has thermal vias connected to the top buried ground planes as per JEDEC standard JESD51-5. These thermal resistance values are shown for the QFP packaged part only (no external heat sink).

Symbol	Description	Value	Unit
θ_{JC}	Junction-to-Case thermal resistance	25.8	°C/W
$\theta_{CA\ 0}$	Case-to-Ambient thermal resistance, still air	53.6	°C/W
$\theta_{CA\ 100}$	Case-to-Ambient thermal resistance, 100LFPM airflow	51.4	°C/W
$\theta_{CA\ 200}$	Case-to-Ambient thermal resistance, 200LFPM airflow	49.9	°C/W
$\theta_{CA\ 300}$	Case-to-Ambient thermal resistance, 300LFPM airflow	48.8	°C/W
$\theta_{CA\ 500}$	Case-to-Ambient thermal resistance, 500LFPM airflow	47.3	°C/W

Note that an external heat sink is **not** factored into the thermal resistance values shown here.

Order Information

Part No.	Description
1012VA-S02QFP	DC to 10 GHz Differential Amplifier in QFP Package
1012VA -S02QFPEVB	DC to 10 GHz Differential Amplifier in QFP Package on an Evaluation Board with SMA Connectors

Contact Information

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Limited Qualification Notification

NOTE: The 1012VA has been tested to meet the DC and AC electrical specifications outlined in this data sheet, except where noted. While the 1012VA has not undergone full qualification testing (i.e. it has not been subjected to high temperature operation life test), a number of other products fabricated in the same semiconductor process and packaged in the same QFP have completed full qualification testing and have been demonstrated to be reliable. Contact Inphi Corporation for more details.
As of the date of this datasheet release, the Absolute Maximum Ratings have not been fully tested.

Updates From Previous Version 1.1

1. Changed product revision from S01 to S02
2. Changed BW spec from 7 GHz to 10 GHz, nominally.
3. Updated CMRR and Return Loss data with new BW.
4. Changed THD and Gain Flatness specifications