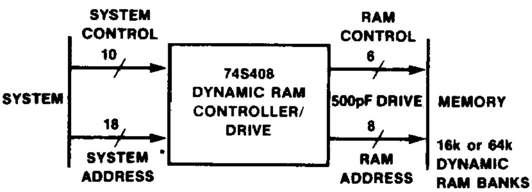
64K Dynamic RAM Controller/Driver

SN74S408/DP8408A
SN74S408-2/DP8408A-2

Features/Benefits

- All DRAM drive functions on one chip have on-chip high-capacitance-load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMs: Capable of addressing up to 256K words
- Propagation delays of 25 nsec typical at 500-pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Six operating modes support externally-controlled access and refresh, automatic access, as well as special memory initialization access
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408, DP8408A

MODE	MODE OF OPERATION
0,1,2	Externally-controlled refresh
3	Externally-controlled All-$\overline{RAS}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}
6	Auto access, fast t_{RAH}
7	Set end of count

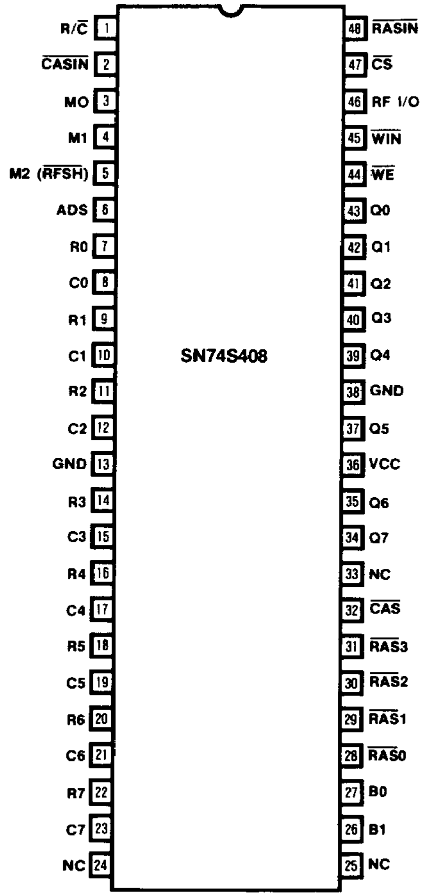


74S408 Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S408	48 N, D	Com
SN74S408-2	48 N, D	Com, Speed Option

Pin Configuration



NC = NO CONNECTION

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Block Diagram

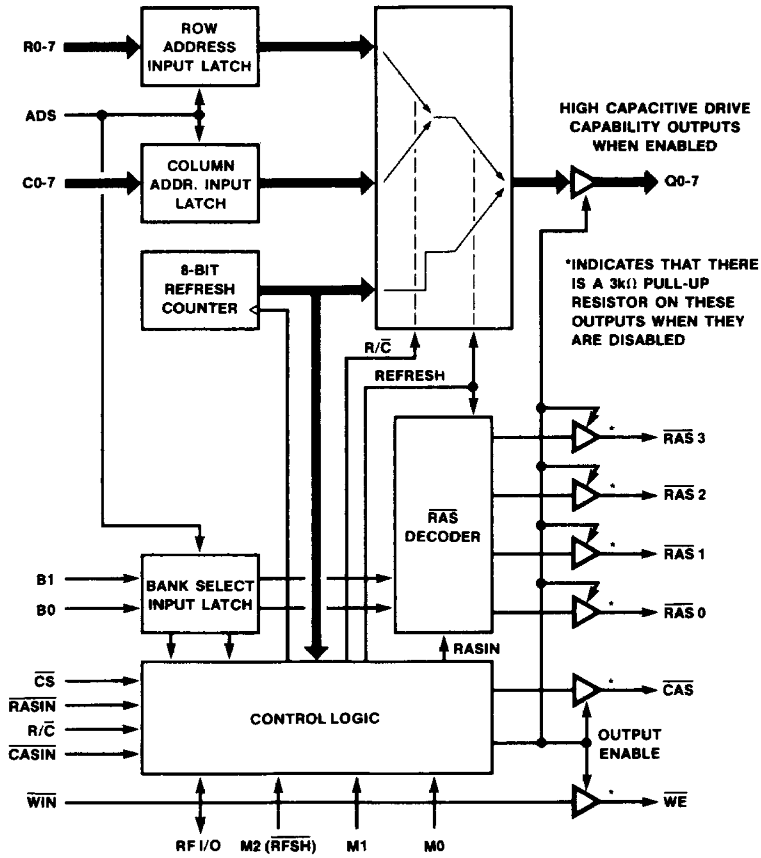


Figure 1. 74S408 Functional Block Diagram

Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74S408 to drive all 16K and 64K DRAMs and addresses up to 256K words. Since the 74S408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S408's 6 operating modes offer externally-controlled or on-chip automatic access and externally-controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25nsec. The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 74S408 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, or 64Ks. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—$V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. Recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3).

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0, 1, 2 and 3.

R/$\overline{C}$: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$: Column Address Strobe Input—Inhibits $\overline{CAS}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{CS}$: Chip Select Input—Three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 6 modes of operation of the 74S408 as depicted in Table 1.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active (low) when M2 = 0 (modes 0, 1, 2 or 3) and the End-of-Count output is at 127 or 255 (see Table 3).

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 5 and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3 and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S408 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$, 500pF loads for Q_0-Q_7 and $\overline{WE}$, and 150 pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S408 Driving Any 16K or 64K DRAMs

The 74S408 can drive any 16K or 64K DRAMs. The on-chip 8-bit counter with selectable End-of-Count can support refresh of 128 or 512 rows, while the 8 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K or 64K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S408, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals M_0, M_1, M_2. Selecting M_2, M_1, M_0 = 0,0,0 or 0,0,1 or 0,1,0 will result at the same operating mode designated as mode 0,1,2 (see Table 2).

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0,1,2	0 0 0	0 0 1	0 1 0	Externally-controlled refresh	RF I/O = EOC
3	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 2. 74S408 Mode Select Options

74S408 Functional Mode Descriptions

Modes 0, 1, 2—Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto R_0-R_7 outputs, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $M_2(\overline{RFSH})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{RASIN}$ and $\overline{RFSH}$ as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $M_2(\overline{RFSH})$ can transition low simultaneously because the refresh counter becomes valid on the output but t_{RFLCT}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_2(\overline{RFSH})$ initially can again have the same edge as $\overline{RASIN}$, but then can maintain a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

Mode 3—Externally Controlled All-$\overline{RAS}$ Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S408 for the next write cycle.

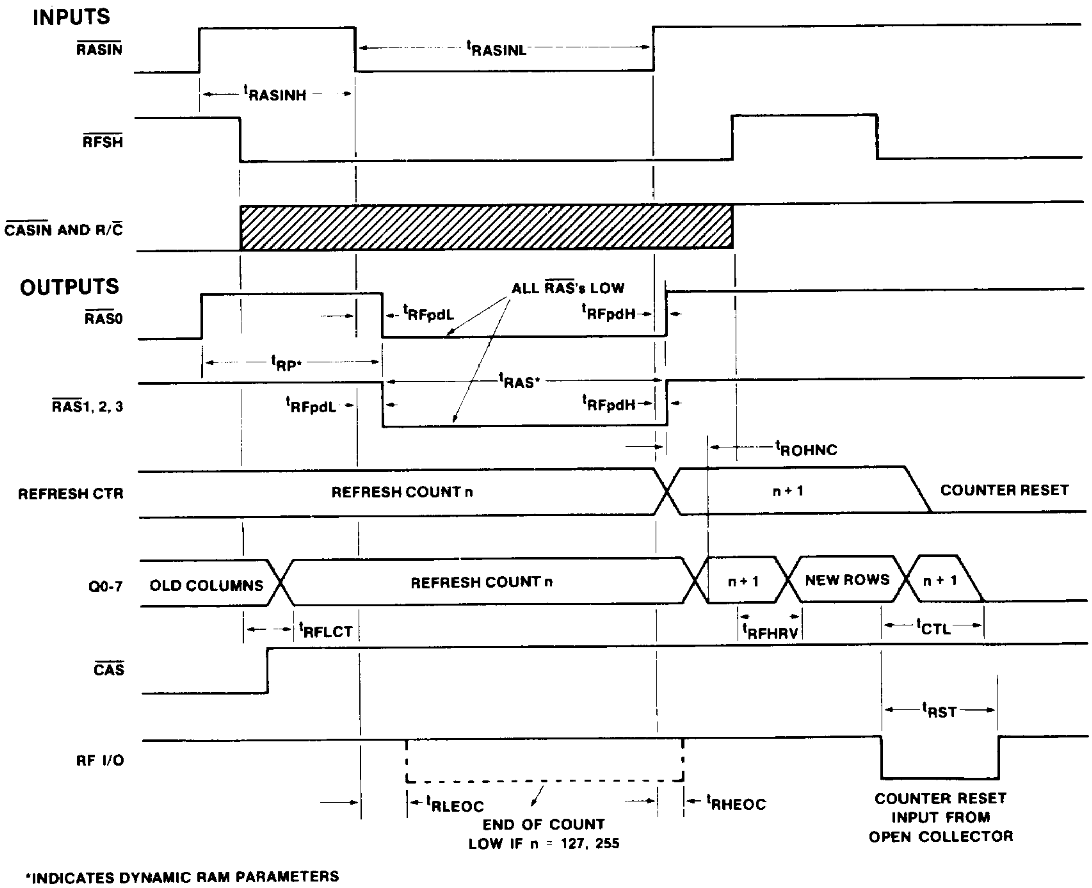


Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

Mode 4—Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 (RFSH) and R/C high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided CS is set low. The column address latch contents are output after R/C goes low. RASIN can go low after the row addresses have been set up on Q0-Q7. This selects one of the RAS outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/C can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic CAS Generation

In a normal memory access cycle CAS can be derived from inputs CASIN or R/C. If CASIN is high, then R/C going low switches the address output drivers from rows to columns. CASIN then going low causes CAS to go low approximately 40 ns later, allowing CAS to occur at a predictable time (see Figure 4b). For maximum system speed, CASIN can be kept low, since CAS will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after R/C goes low (see Figure 4a). Most DRAMs have a column address set-up time before CAS (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/C can go low a time delay (t_{RPDL} + t_{RAH} − t_{RHA}) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

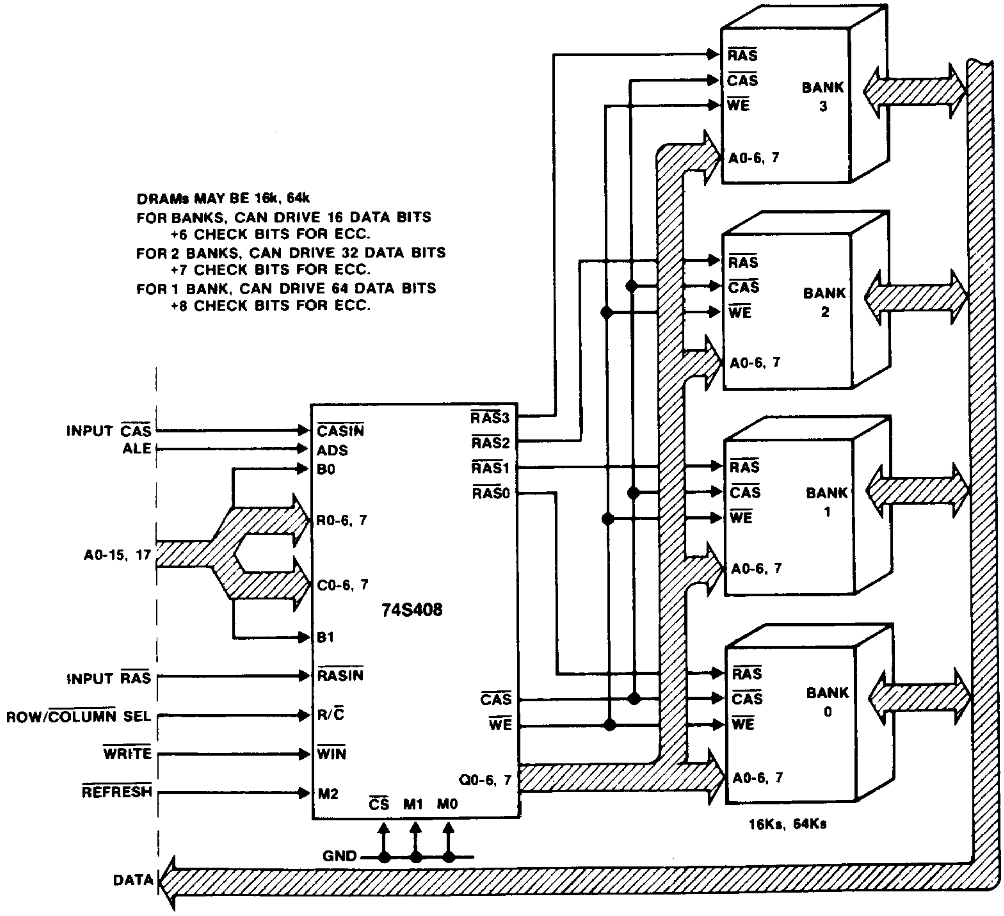
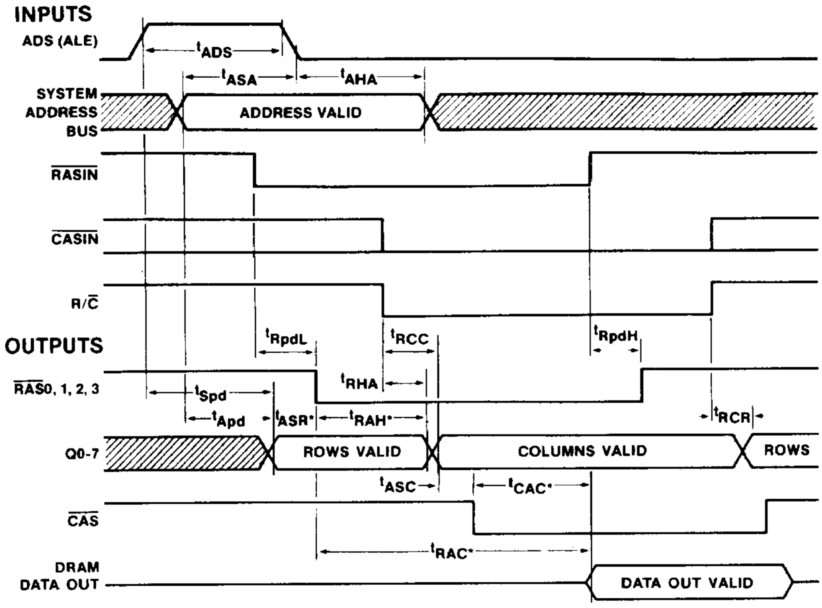
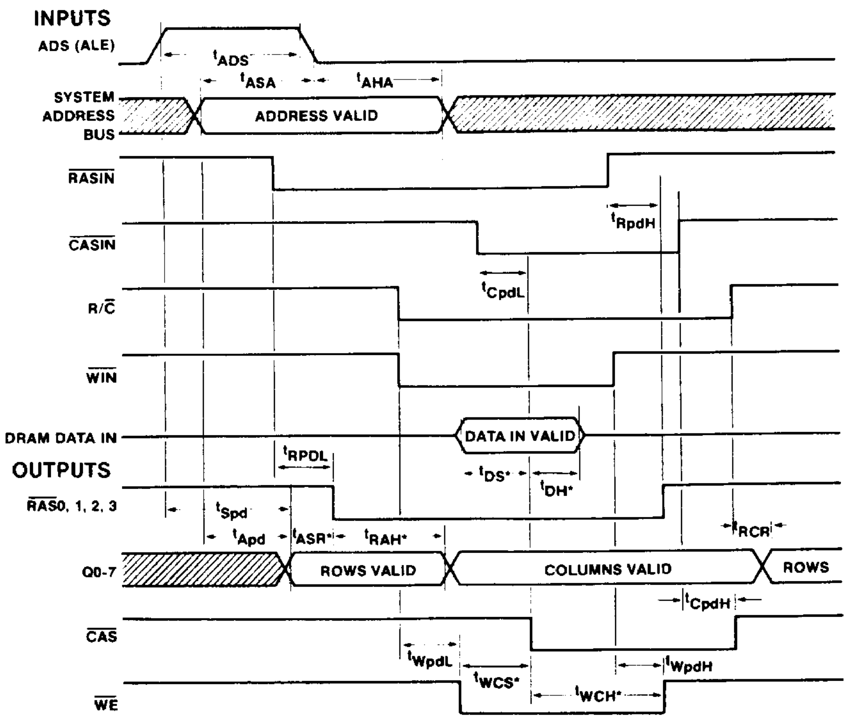


Figure 3. Typical Application of 74S408 Using Externally Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4a. Read Cycle Timing (Mode 4)



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4b. Write Cycle Timing (Mode 4)

Mode 5—Automatic Access

In the Auto Access mode all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. Inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and the output control signals are derived internally from one input signal ($\overline{RASIN}$) minimizing timing-skew problems, thereby reducing memory-access time substantially and allowing the use of slower DRAMs.

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S408 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ Is output low.

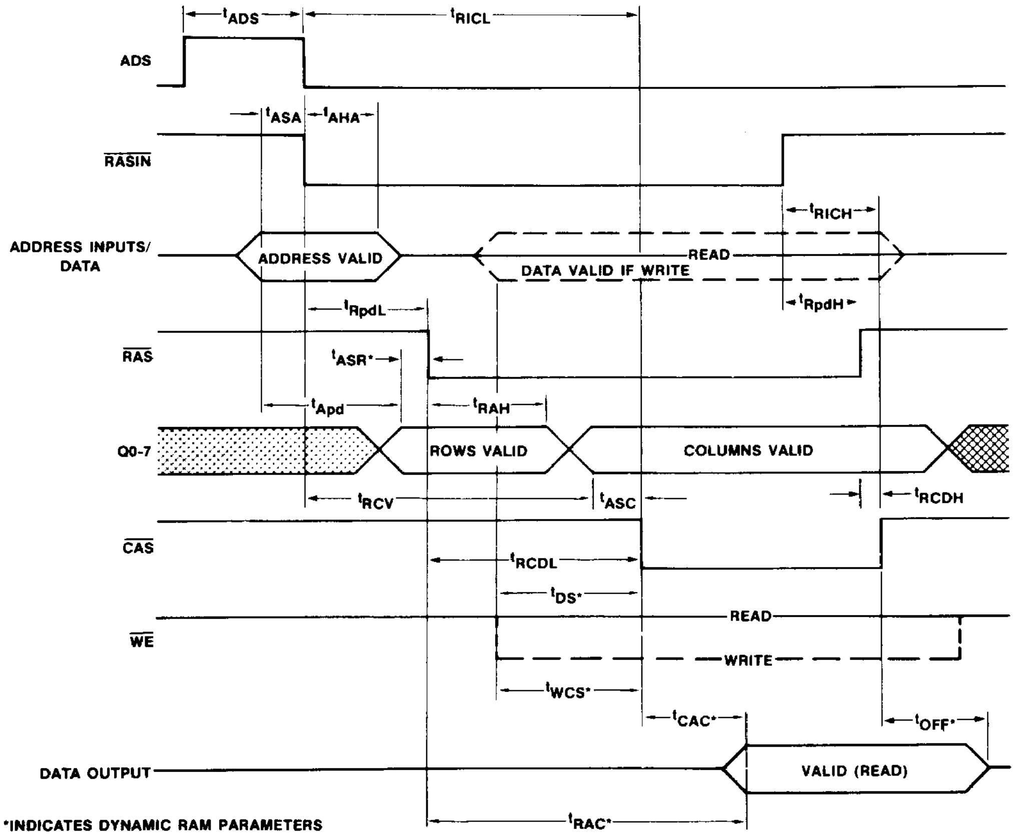


Figure 5a. Modes 5, 6 Timing ($\overline{CASIN}$ High in Mode 6)

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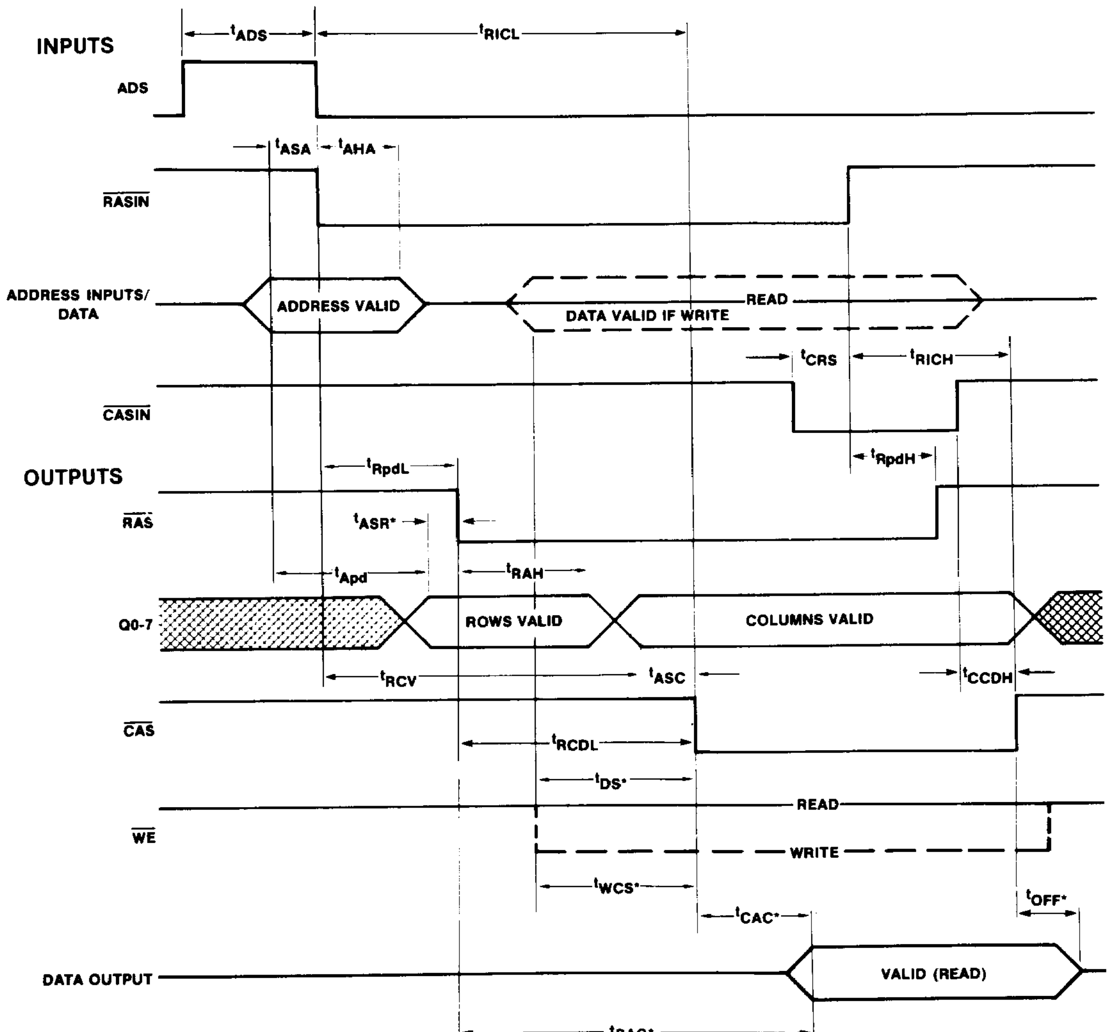
This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Mode 6—Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.



*INDICATES DYNAMIC RAM PARAMETERS

Figure 5b. Mode 6 Timing, Extended CAS

Mode 7—Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

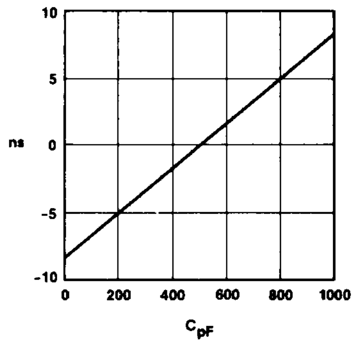


Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

SN74S408/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} .... -0.5 V to 7.0 V
Storage temperature range .... -65° to +150°C
Input voltage .... -1.5 V to 5.5 V
Output current .... 150 mA
Lead temperature (soldering, 10 seconds) .... 300°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408 MIN	'S408 TYP	'S408 MAX	'S408-2 MIN	'S408-2 TYP	'S408-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.25		5.25	V
T_A	Operating free-air temperature		0		+75	0		+75	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			50			ns
t_{RST}	counter reset pulse width	Figure 2	70			70			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 75°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{OD}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408 MIN	'S408 TYP	'S408 MAX	'S408-2 MIN	'S408-2 TYP	'S408-2 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	50	63	80	50	63	80	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	40	48	60	40	48	60	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	120		30	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Fibure 4b,4a		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	60	15	30	60	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	58		40	58	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X , Figure 2		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			3			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			35			ns

Switching Characteristics: (Cont.)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 7 R1 = 3.5k R2 = 1.5K		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 7 R2 = 1k, S1 open		20	40		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 7 R1 = 3.5k R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 7 R1 = 1k, S2 open		25	50		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 7 R2 = 750 Ω S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF Figure 7 R2 = 750Ω, S1 open		40	75		45	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 7, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF Figure 7 R2 = 750Ω S1 open		50	80		50	80	ms

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

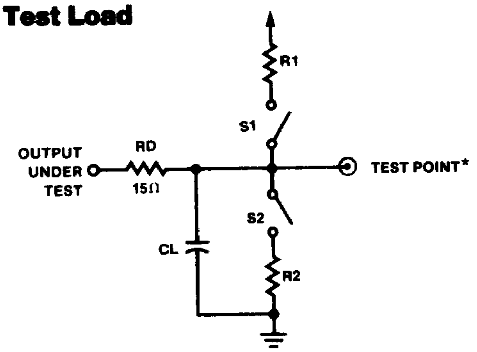
Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Test Load



R_1, R_2 = 4.7K Except as specified

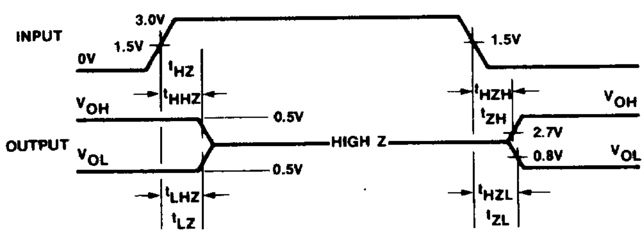


Figure 7. Waveform

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.