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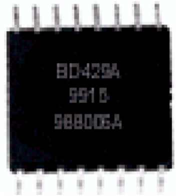
BD429/DEI0429 FAMILY
ARINC 429/RS-422 Line Driver
Integrated Circuit

FEATURES

- ARINC 429 Line Driver for HI speed (100 Kbps) and LOW speed (12.5 Kbps) data rates
- Pin for Pin replacement part for industry standard ARINC 429 Line Drivers
- Available in a 16L SOICW, 16L CERDIP, 16L Ceramic SOP, and 28L PLCC
- Low EMI RS-422 line driver mode for data rates up to 100 kHz
- Adjustable slew rates via two external capacitors
- Inputs are TTL and CMOS compatible
- Low quiescent power of 125 mW (typical)
- Programmable output differential range via VREF pin
- Outputs are fused for failsafe overvoltage protection
- Drives full ARINC load of 400 Ω and 30,000 pF
- Extended (-55/+85 °C) and Military (-55/+125 °C) temperature ranges
- 100% Final Testing



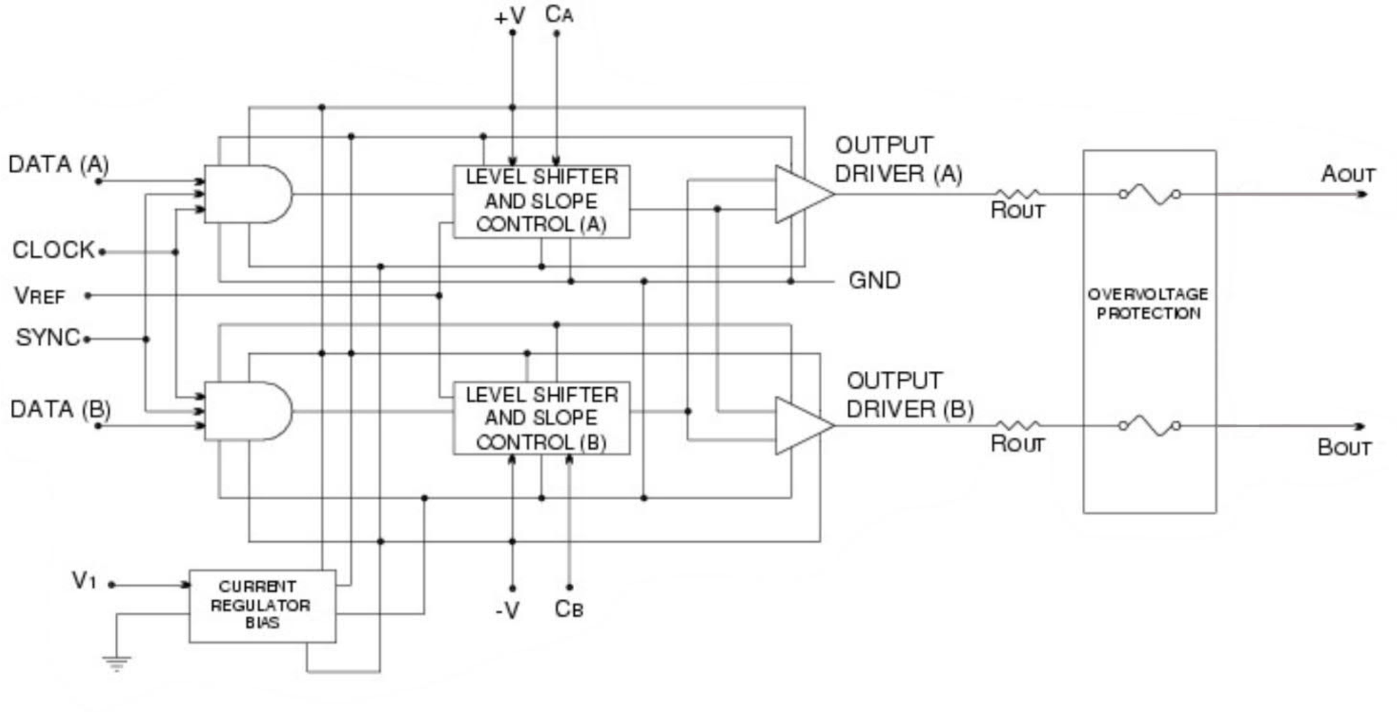


Figure 1: Block Diagram

GENERAL DESCRIPTION

The BD429 ARINC Line Driver Circuit is a bipolar monolithic IC designed to meet the requirements of several general aviation serial data bus standards. These include the differential bipolar RZ types such as ARINC 429, ARINC 571, and ARINC 575, as well as the differential NRZ types such as the RS-422 standard.

FUNCTIONAL DESCRIPTION

Modes: The BD429 operates in either a 429 mode or a 422 mode as controlled by the 429/422′ pin.

429 Mode: In 429 mode, the serial data is presented on the DATA(A) and DATA(B) inputs in the dual rail format defined in the MARK 33 Digital Information Transfer System – ARINC Specification 429-10. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the VREF input and is normally tied to +5 V along with V1 to produce output levels of +5 V, 0 V, and –5 V on each output for ±10 V differential outputs. See Figure 5.

422 Mode: In 422 mode, the serial data is presented on DATA(A) input. The driver is enabled by the SYNC and CLOCK inputs. The outputs swing between 0 V and +5 V if VREF is at +5 V. See Figure 6.

Output Resistance: The driver output resistance is 75 Ω ±20% at room temperature; 37.5 Ω on each output. The outputs are also fused for failsafe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on CA and CB. Typical values are 75 pF for 100 Kbps data and 50pF for 12.5 Kbps data.

Table 1: Truth Table

	429/422' NOTE 1	SYNC NOTE 2	CLOCK NOTE 2	DATA(A) NOTE 2	DATA(B) NOTE 2	A_{OUT}	B_{OUT}	COMMENTS
429 MODE	H	L	X	X	X	0	0	NULL
	H	X	L	X	X	0	0	NULL
	H	H	H	L	L	0	0	NULL
	H	H	H	H	H	0	0	NULL
	H	H	H	H	L	$+V_{REF}$	$-V_{REF}$	LOGIC 1
	H	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOGIC 0
422 MODE	L	L	X	X	X	$+V_{REF}$	0	NULL
	L	X	L	X	X	$+V_{REF}$	0	NULL
	L	H	H	L	X	0	$+V_{REF}$	LOGIC 0
	L	H	H	H	X	$+V_{REF}$	0	LOGIC 1

NOTES:
1. The 429/422' pin is internally pulled up to V_1 through a 10 kΩ resistor. So, if no external connection is made to this pin, it will force the chip into the 429 mode.
2. X = Don’t care.

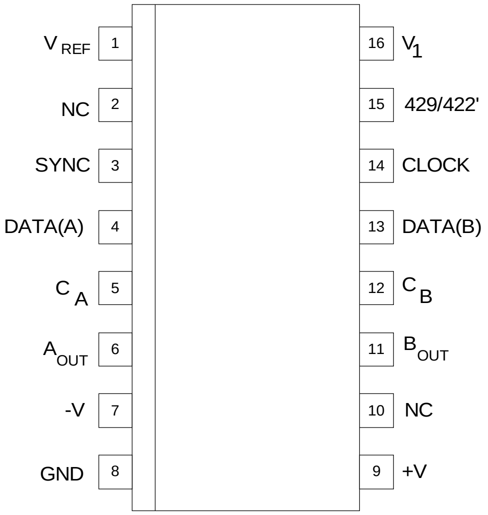


Figure 2 DIP, SOIC & CSOP Pinout

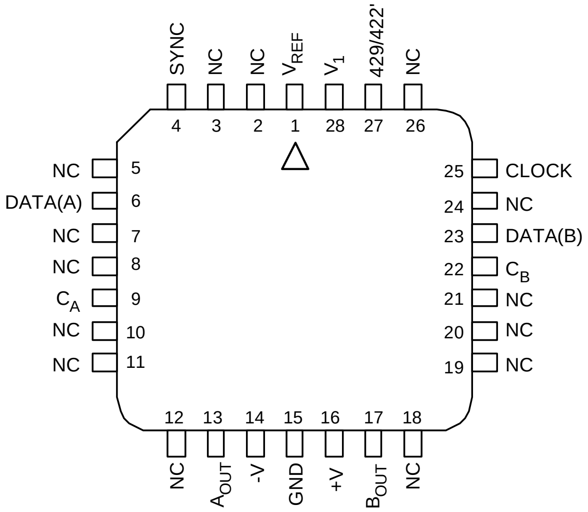


Figure 3 PLCC Pinout

Table 2 Pin Descriptions

NAME	DESCRIPTION
V_{REF}	Analog Input. The voltage on V_{REF} sets the output voltage levels on A_{OUT} and B_{OUT}. The output logic levels swing between $+V_{REF}$, 0 V, and $–V_{REF}$ volts.
NC	No Connect
SYNC	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
DATA(A) DATA(B)	Logic inputs. These signals contain the Serial Data to be transmitted on the ARINC 429 data bus. Refer to Figure 5 and Figure 6.
C_A C_B	Analog Nodes. External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typical CA = CB = 75 pF for 100 Kbps data and CA = CB = 500 pF for 12.5 Kbps data. *
AOUT BOUT	Outputs. These are the line driver outputs which are connected to the aircraft serial data bus.
-V	Negative Supply Input. –15 V nominal.
GND	Ground.
+V	Positive Supply Input. +15 V nominal.
CLOCK	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
429/422'	Logic Input. Mode control for ARINC 429 and RS-422 modes. An internal 10 kΩ pull up resistor keeps the chip in ARINC 429 mode when there is no external connection. This creates a default logic 1, enabling the ARINC 429 mode. A forced logic 0 enables the RS-422 mode.
V_1	Logic Supply Input. +5 V nominal.

* CA and CB pin voltages swing between ±5 V. Any electronic switching of the capacitor on the pins must not inhibit the full voltage swings.

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Voltage between pins +V and –V		40	V
V_1 Maximum Voltage	V_1	7	V
V_{REF} Maximum Voltage	V_{REF}	6	V
DATA(A) Max Input Voltage DATA(B) Max Input Voltage	$V_{DATA(A)}$ $V_{DATA(B)}$	(GND-0.3) to (V_1 + 0.3)	V
Lead Soldering Temperature (10 sec duration, thru-hole packges)	T_{SLD}	280	ºC
Storage Temperature	T_{STG}	-65 to +150	ºC
Max Junction Temperature Ceramic Package & Plastic Package short term operation	$T_{J\ MAX1}$	+175	ºC
Max Junction Temperature Plastic Package Limit (prolonged operation)	$T_{J\ MAX2}$	+145	ºC
Output Short Circuit Duration	See Note 1		
Output Over-Voltage Protection	See Note 2		

Notes.

1. One output at a time can be shorted to ground indefinitely
2. Both outputs are fused at between 0.5 Amp DC and 1.0 Amp DC to prevent an over-voltage fault from coupling onto the system power bus.

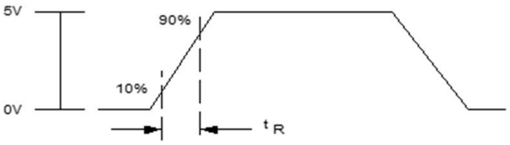
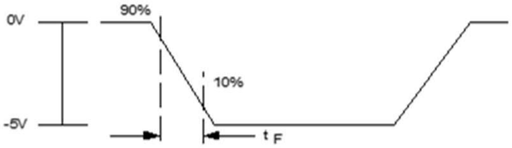
Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Positive Supply Voltage	+V	11.4		16.5	V
Negative Supply Voltage	-V	-11.4		-16.5	V
V_1	V_1	4.75	5	5.25	V
V_{REF} (For ARINC 429)	V_{REF}	4.75	5	5.25	V
V_{REF} (For other applications)	V_{REF}	3		6	V
Operating Temperature (Plastic Package)	T_A	-55		+85	ºC
Operating Temperature (Ceramic Package)	T_A	-55		+125	ºC

Table 5 DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent +V supply current	IQ+V	No Load. 429 mode. DATA = CLOCK = SYNC = LOW	-	2	-	mA
Quiescent -V supply current	IQ-V	No Load. 429 mode. DATA = CLOCK = SYNC = LOW	-	5	-	mA
Quiescent V_1 supply current	IQV_1	No Load. 429 mode. DATA = CLOCK = SYNC = LOW	-	4	-	mA
Quiescent V_{REF} supply current	IQV_{REF}	No Load. 429 mode. DATA = CLOCK = SYNC = LOW	-	10	-	uA
Logic 1 Input V	V_{IH}	No Load.	2.0	-	-	V
Logic 0 Input V	V_{IL}	No Load.	-	-	0.6	V
Logic 1 Input I	I_{IH}	No Load.	-	-	10	uA
Logic 0 Input I	I_{IL}	No Load. (429/422´ Pin I_{IL} = -2mA max)	-	-	-20	uA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to Ground	-80	-	-	mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to Ground	80	-	-	mA
Output Voltage HIGH (+1)	V_{OH}	No Load. 429 Mode.	V_{REF} - 0.25	V_{REF}	V_{REF} + 0.25	V
Output Voltage NULL (0)	V_{NULL}	No Load. 429 Mode.	-250	-	+250	mV
Output Voltage LOW (-1)	V_{OL}	No Load. 429 Mode.	$-V_{REF}$ – 0.25	$-V_{REF}$	$-V_{REF}$ + 0.25	V
Timing Capacitor Charge Current C_A (+1) C_B (-1) C_A (-1) C_B (+1)	I_{CT} + -	No Load. 429 Mode. SYNC = CLOCK = HIGH C_A and C_B held at zero volts.	-	+200 –200	-	uA uA
+V Short Circuit Supply Current	ISC (+V)	Output short to ground	-	-	+150	mA
-V Short Circuit Supply Current	ISC (-V)	Output short to ground	-	-	-150	mA
Resistance on each output	R_{OUT}	Room Temp Only	-	37.5	-	Ω
Input Capacitor	C_{IN}	-	-	-	15	pF
Conditions (unless otherwise noted.): Temperature: -55 to +125 °C Ceramic, -55 to +85 °C Plastic, +V = +11.4 to +16.5 V, –V = -11.4 to –16.5 V; V_1 = V_{REF} = +5 V ±5%, 429/422' = open circuit						

Table 6 AC Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Output Rise Time A_{OUT} or B_{OUT} $C_A = C_B = 75$ pF $C_A = C_B = 500$ pF	t_R t_R	1.0 5.0	2.0 15.0	us us	
Output Fall Time A_{OUT} or B_{OUT} $C_A = C_B = 75$pF $C_A = C_B = 500$pF	t_F t_F	1.0 5.0	2.0 15.0	us us	
Input to Output Propagation Delay	t_{PNH} t_{PNL}	-	3.0	us	See Figure 4
A_{OUT} / B_{OUT} Skew Spec.	-	-	500	ns	

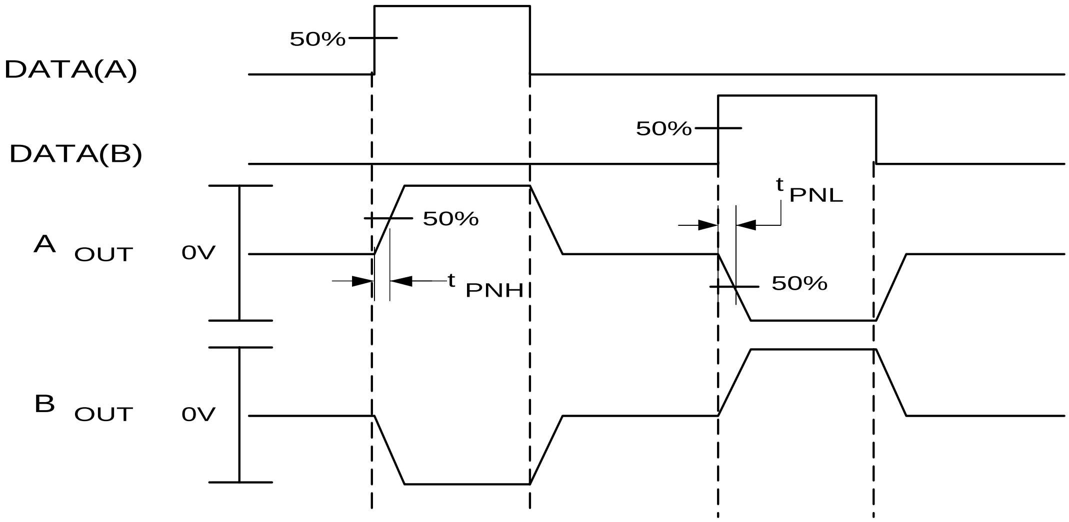


Figure 4: Propagation Delay

The figures below show the output waveforms for the ARINC 429 and RS-422 modes of operation. The output slew rates are controlled by timing capacitors C_A and C_B. They are charged by ±200 uA nominal. Slew Rate (SR) measured as V/us, is calculated by: $SR = 200/C$, where C is in pF

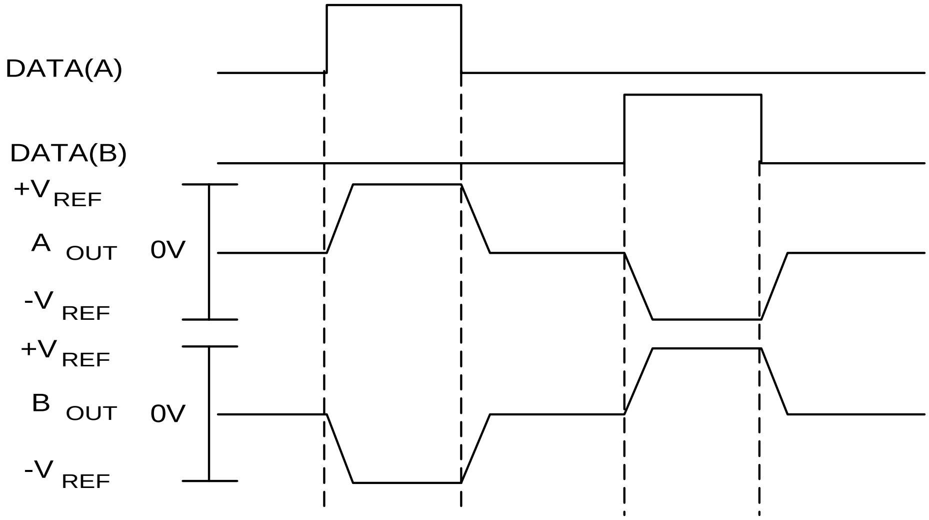


Figure 5: ARINC 429 Waveforms

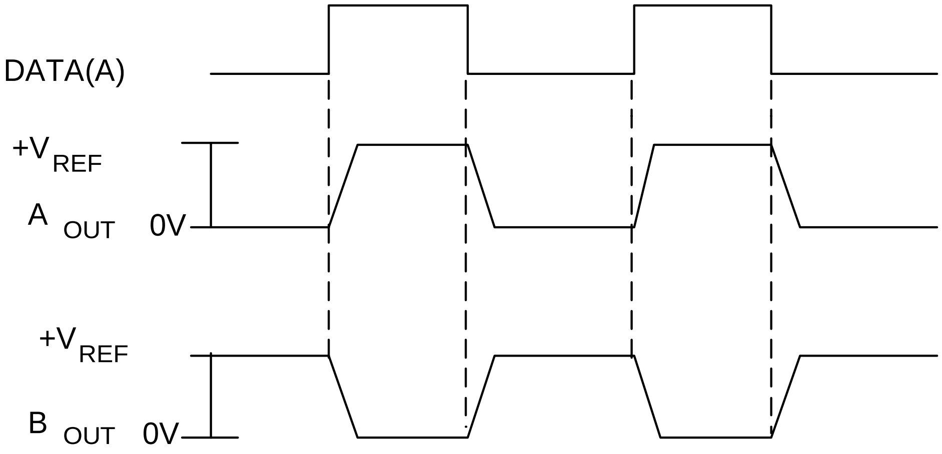


Figure 6: RS-422 Waveforms

APPLICATION INFORMATION

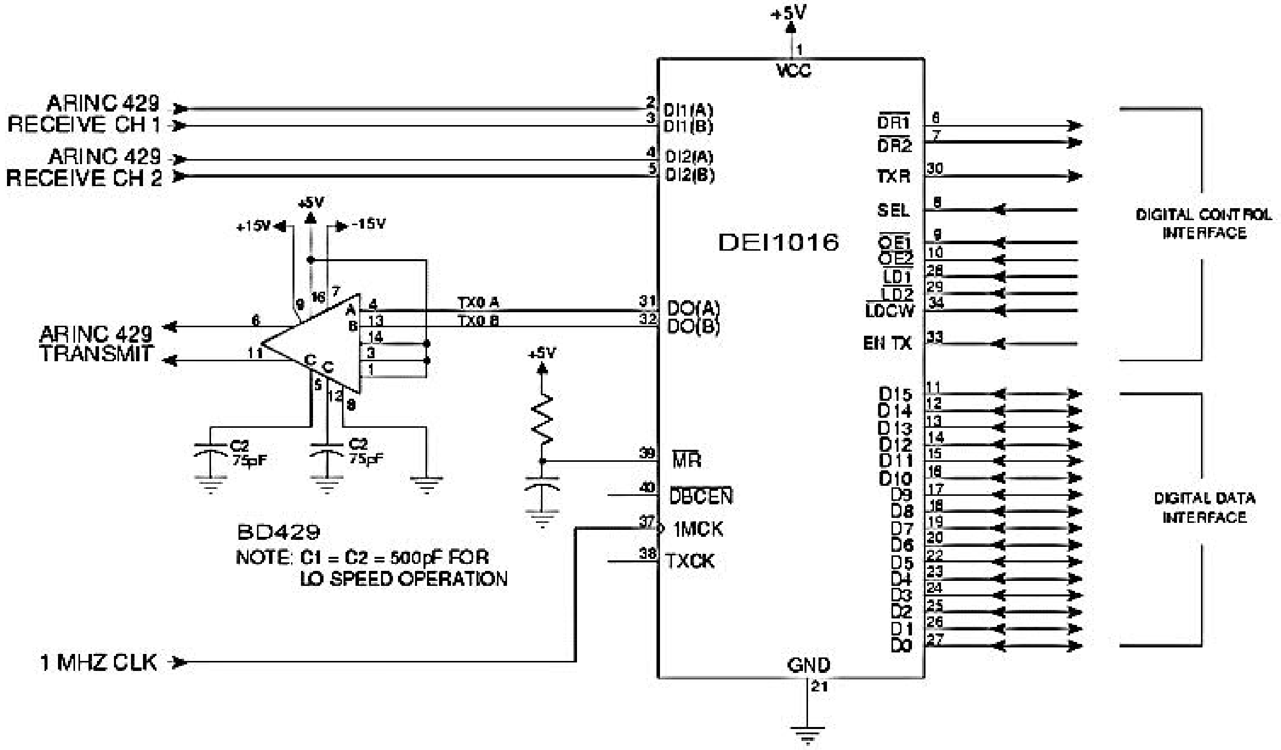


Figure 7: Typical Transceiver/Line Driver Interconnect

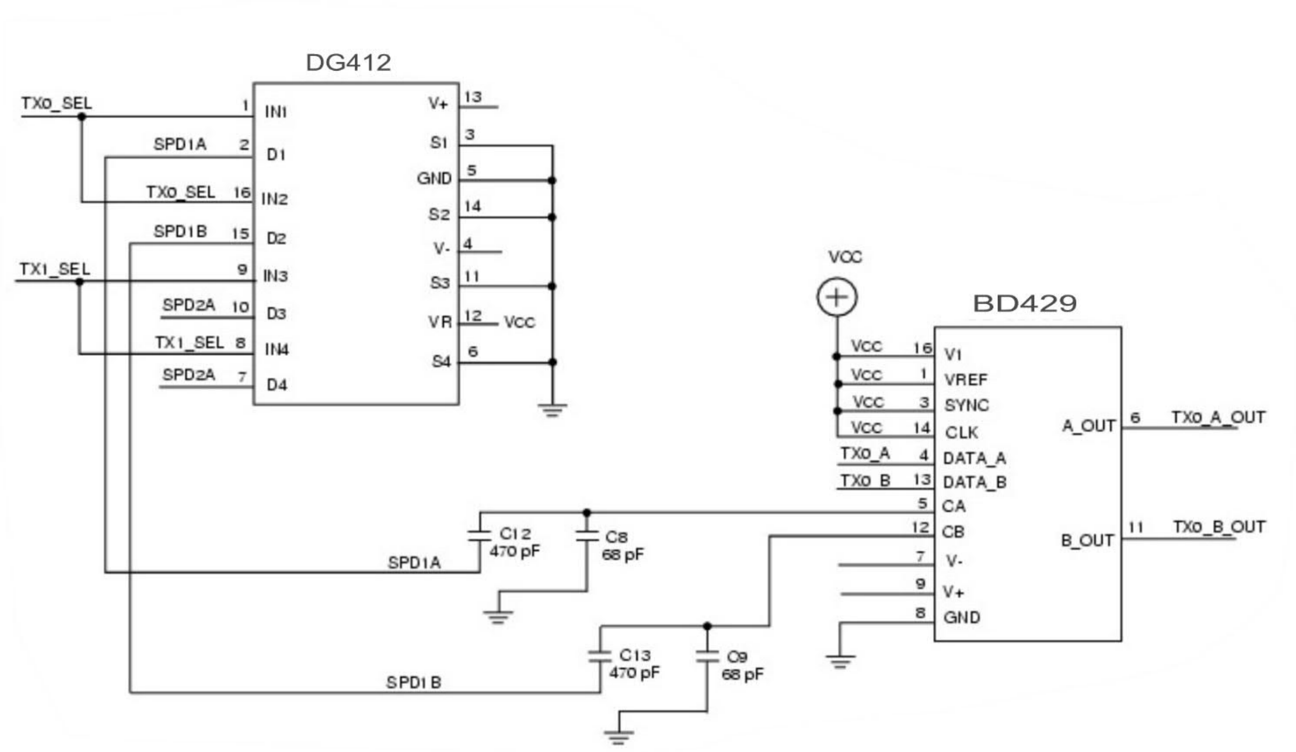


Figure 8: Example Use of Switching Capacitors for High-Speed/Low-Speed Operation

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100 Kbps) with high capacitive loads and high data duty cycles.

Power dissipation may be estimated from Error! Reference source not found. Device power dissipation (Pd) is indicated for 100% data duty cycle with no word gap null times and should be adjusted for the appropriate data duty cycle (DC). Pd(application) = DC * [Pd(table) - 145] + 145 mW, where DC is the application data duty cycle, Pd(table) is the Pd from the table for the indicated data rate and bus load, and 145 mW is the quiescent power. The application's data duty cycle (DC) for 100 Kbps operation is calculated as:

DC = (total bits transmitted in 10 s period / 1,000,000)
= (32 x total ARINC words transmitted in 10 s period / 1,000,000).

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. Place vias on the signal/power traces close to the IC to maximize heat flow to the internal power planes. If possible, design a solid heat spreader land under and beyond the IC to maximize heat flow from the device.

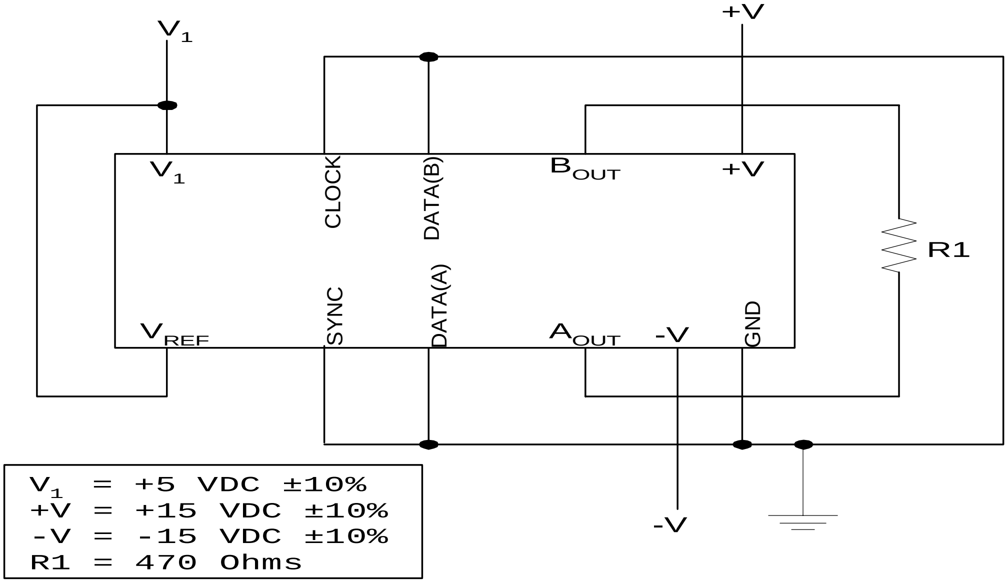
Table 7 Power Dissipation Estimation

DATA RATE (Kbps)	LOAD	+V @ 15 V (mA)	-V @ -15 V (mA)	V_1, V_{REF} @ 5 V (mA)	BD429 POWER (mW)	LOAD POWER (mW)
0 to 100	NONE	2.0	-5.0	4	125	0
12.5	FULL	16	19.0	4	485	60
100	FULL	48	51.0	4	1194	325
12.5	HALF	6.0	8.0	4	196	30
100	HALF	22	25	4	561	162
100% Duty Cycle, Full Load = 400 Ω / 30,000 pF Half Load = 4,000 Ω / 10,000 pF						

SCREENING INFORMATION

Table 8 Screening Process

SCREENING STEP	PLASTIC STANDARD	PLASTIC BURN IN	CERAMIC STANDARD	CERAMIC BURN IN
THERMAL CYCLE MIL-883 TM1010 Cond C	NO	NO	10 Cycles	10 Cycles
CONSTANT ACCELERATION MIL-883 TM2001 Cond E	NO	NO	YES	YES
GROSS & FINE LEAK MIL-883 TM1014	NO	NO	YES	YES
BURN IN MIL-883 TM1015 Cond. A	NO	160 h @ +125 °C	NO	96 h @ +125 °C
ELECTRICAL TEST:				
ROOM TEMPERATURE	100%	100%	100%	100%
HIGH TEMPERATURE	100% @ +125 °C	100% @ +125 °C	100% @ +125 °C	100% @ +125 °C
LOW TEMPERATURE	0.65% AQL @-55 °C	0.65% AQL @-55 °C	0.65% AQL @-55 °C	0.65% AQL @-55 °C



V_1 = +5 VDC ±10%
+V = +15 VDC ±10%
-V = -15 VDC ±10%
R1 = 470 Ohms

Figure 9: Burn-In Schematic

PACKAGE INFORMATION

Table 9 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θJC / θJA (°C/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-Free CODE	Pb Free DESIGNATION	JEDEC MO
16L CERAMIC DIP	16 CERDIP	35 / 75	HERMETIC	SnPb solder	Not Pb-free	MS-030-AC
16L CERAMIC DIP, GREEN	16 CERDIP G	35 / 75	HERMETIC	Sn Solder Sn96.5/Ag 3/Cu 0.5 e3	Pb Free solder terminals	MS-030-AC
16L SOIC WIDE BODY, GREEN	16 SOIC WB G	25 / 75 (4L PCB)	MSL 1 260 °C	NiPdAu e4	RoHS Compliant	MS-013-AA
16L CERAMIC SOP	16 CSOP	23 / TBD	HERMETIC	Au e4	Pb Free solder terminals	na
28L PLCC	28 PLCC	25 /55 (4L PCB)	MSL 3 235 °C	SnPb	Not Pb-free	MS-018-AB
28L PLCC, GREEN	28 PLCC G	25 /55 (4L PCB)	MSL 3 245 °C	Matte Sn e3	RoHS Compliant	MS-018-AB

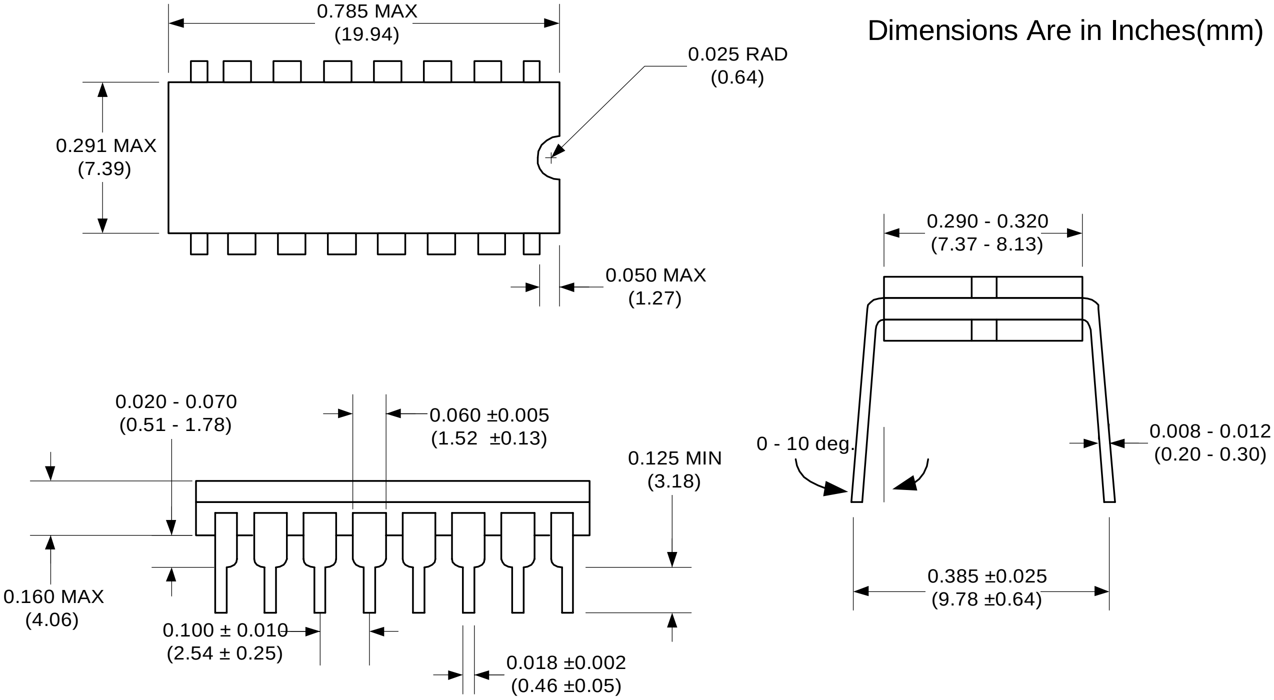


Figure 10 16L CERDIP Mechanical Outline

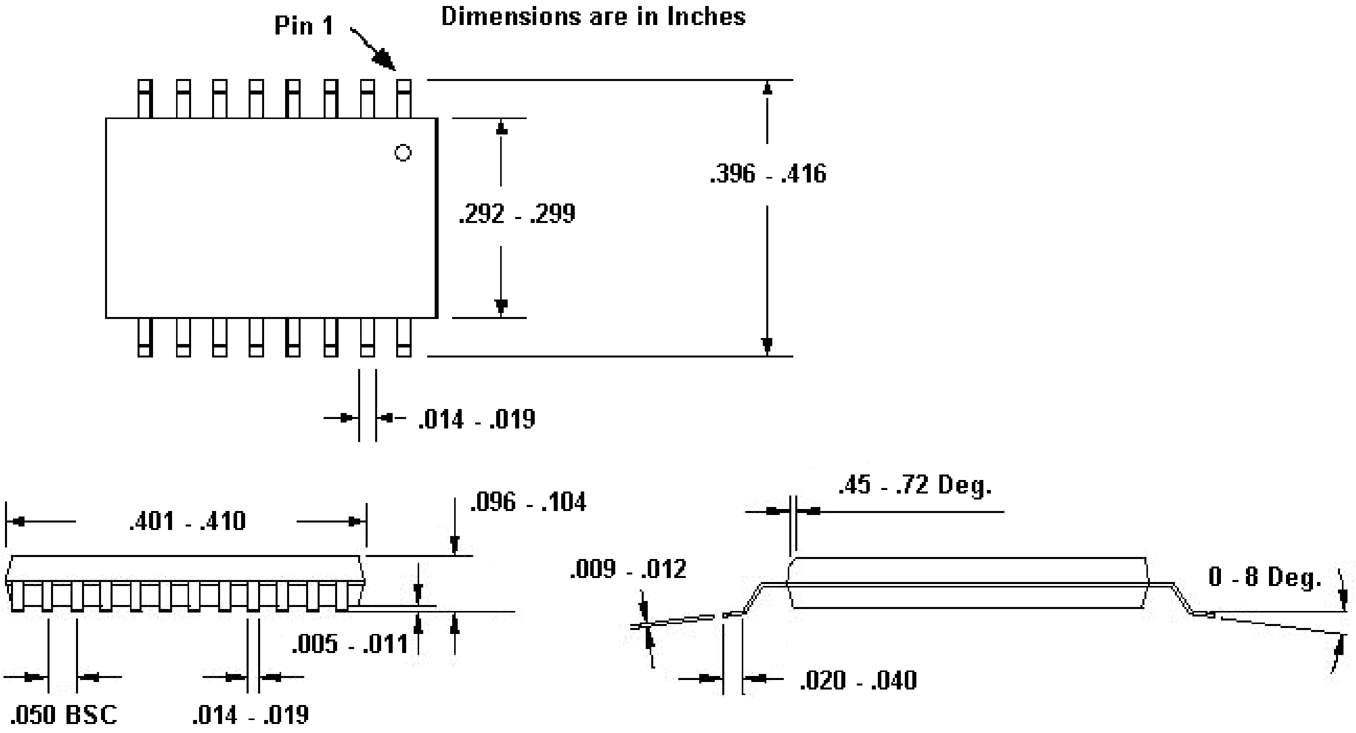


Figure 11 16L SOIC WB Mechanical Outline

NOTES: 1. ALL DIMENSIONS IN INCH.
2. LEAD COPLANARITY AFTER FORM TO BE WITHIN .004.

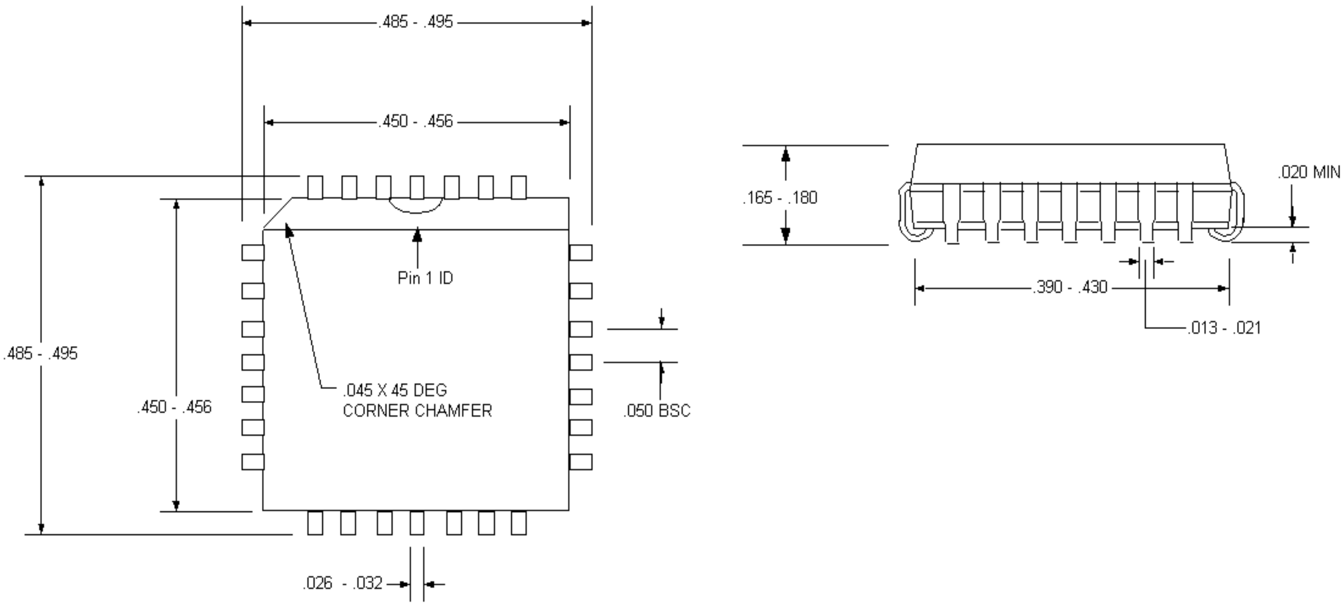


Figure 12 28L PLCC Mechanical Outline

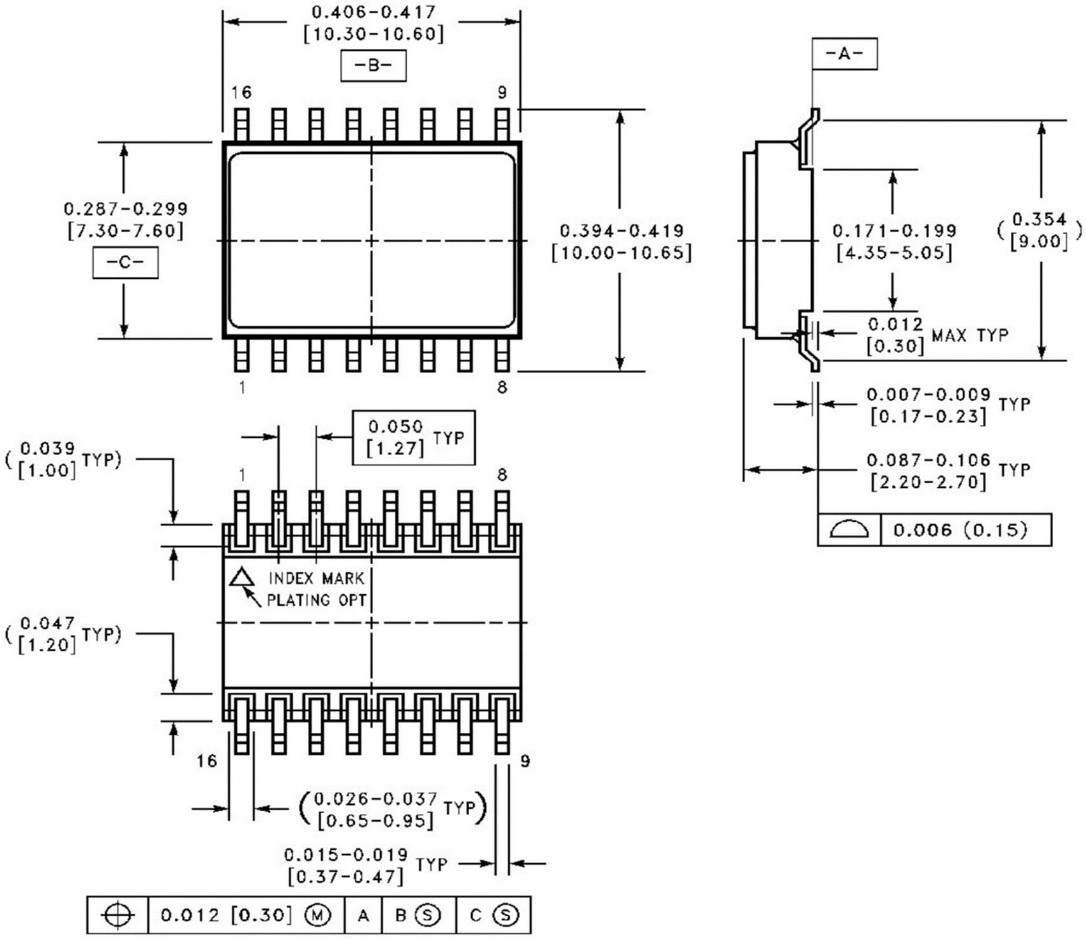


Figure 13 16L CSOP Mechanical Outline

ORDERING INFORMATION

Table 10 Ordering Information

DEI PART NUMBER (2)	MARKING (1)	PACKAGE	TEMP RANGE (°C)	PROCESSING
BD429	BD429	16 CERDIP	-55 / +125	CERAMIC BURN IN
BD429-G	BD429 E3 (1)	16 CERDIP G	-55 / +125	CERAMIC BURN IN
BD429A-G	BD429A E4 (1)	16 SOIC WB G	-55 / +85	PLASTIC STANDARD
BD429A1-G	BD429A1 E4 (1)	16 SOIC WB G	-55 / +85	PLASTIC BURN IN
BD429B	BD429B	28 PLCC	-55 / +85	PLASTIC STANDARD
BD429B-G	BD429B E3 (1)	28 PLCC G	-55 / +85	PLASTIC STANDARD
DEI0429-WMS	DEI0429-WMS	16 CSOP	-55 / +125	CERAMIC STANDARD
DEI0429-WMB	DEI0429-WMB	16 CSOP	-55 / +125	CERAMIC BURN IN

Notes:

1. All packages marked with Lot Code and Date Code. “E3” or “E4” after Date Code Denotes Pb Free category.
2. Suffix legend: -XYZ: X = package code, Y = temperature range code, Z = process flow code.