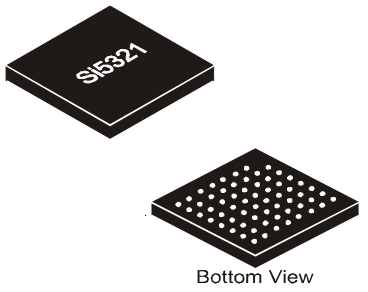
Si5321-XC5

SONET/SDH Precision Clock Multiplier IC

Features

- Ultra-low jitter clock output with jitter generation as low as 0.3 ps_{RMS}
- No external components (other than a resistor and bypassing)
- Input clock ranges at 19, 39, 78, 155, 311, or 622 MHz
- Output clock ranges at 19, 39, 78, 155, 311, 622, 1244, or 2488 MHz
- Digitally-controlled output phase adjust
- Maximum range includes 693 MHz for 10 GbE FEC support
- Digital hold for loss-of-input clock
- Support for 255/238 (15/14), 255/237 (85/79), and 66/64 FEC scaling (ITU-T G.709 and IEEE 802.3ae)
- Selectable loop bandwidth
- Loss-of-signal alarm output
- Low power
- Small size (9 x 9 mm)
- Backwards compatible with Si5320



Ordering Information:

See page 33.

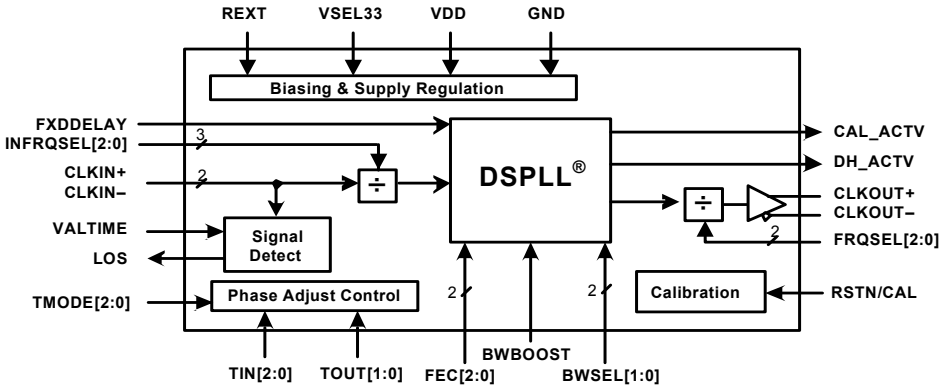
Applications

- SONET/SDH line/port cards
- Terabit routers
- Core switches
- Digital cross connects

Description

The Si5321-XC5 is a precision clock multiplier that exceeds the requirements of high-speed communication systems, including OC-192/OC-48 and 10 Gigabit Ethernet. This device phase locks to an input clock in the 19, 39, 78, 155, 311 or 622 MHz frequency range and generates a frequency-multiplied clock output that can be configured for operation in the 19, 39, 78, 155, 622, 1244, or 2488 MHz frequency range. Silicon Laboratories DSPLL® technology provides PLL functionality with unparalleled performance. It eliminates external loop filter components, provides programmable loop parameters, and simplifies design. FEC rates are supported by selectable forward and reverse 255/238 (15/14), 255/237 (85/79), and 66/64 (33/32) conversion factors. The ITU-T G.709 255/237 rate and the IEEE 802.3ae 66/64 rate are supported when using a 155 MHz or higher rate input clock. The performance and integration of Silicon Laboratories' Si5321-XC5 clock IC provides high-level support of the latest specifications and systems. It operates from a single 3.3 V supply.

Functional Block Diagram



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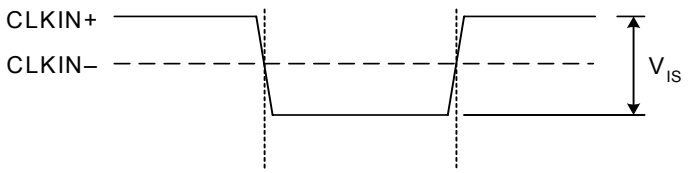
1. Electrical Specifications

Table 1. Recommended Operating Conditions

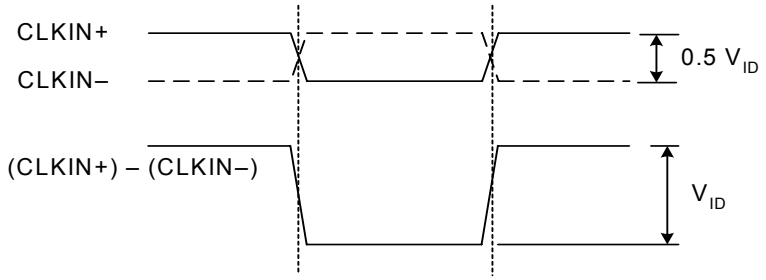
Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–20[2]	25	85	°C
Si5321-XC5 Supply Voltage[3], 3.3 V Supply	V_{DD33}		3.135	3.3	3.465	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The Si5321-XC5 is guaranteed by design to operate at –40° C. All electrical specifications are guaranteed for an ambient temperature of –20 to 85° C.
3. The Si5321-XC5 specifications are guaranteed when using the recommended application circuit (including component tolerance) of Figure 6 on page 16.



A. Operation with Single-Ended Clock Input*

Note: When using single-ended clock sources, the unused clock input on the Si5321 must be ac-coupled to ground.



B. Operation with Differential Clock Input

Note: Transmission line termination, when required, must be provided externally.

Figure 1. CLKIN Voltage Characteristics

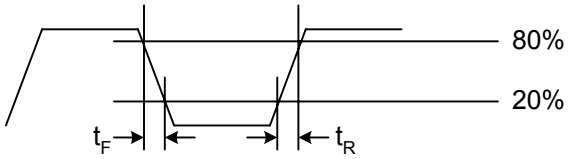


Figure 2. Rise/Fall Time Measurement

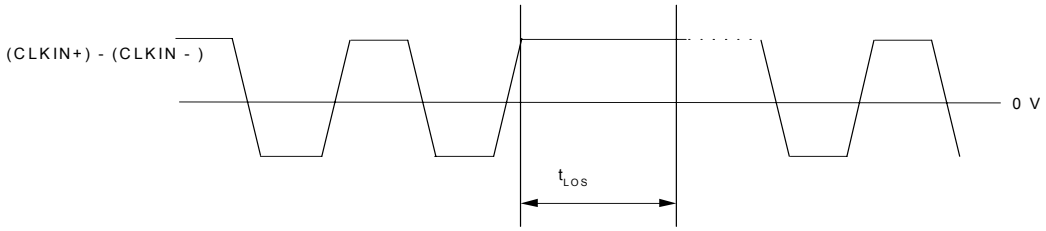


Figure 3. Transitionless Period on CLKIN for Detecting a LOS Condition

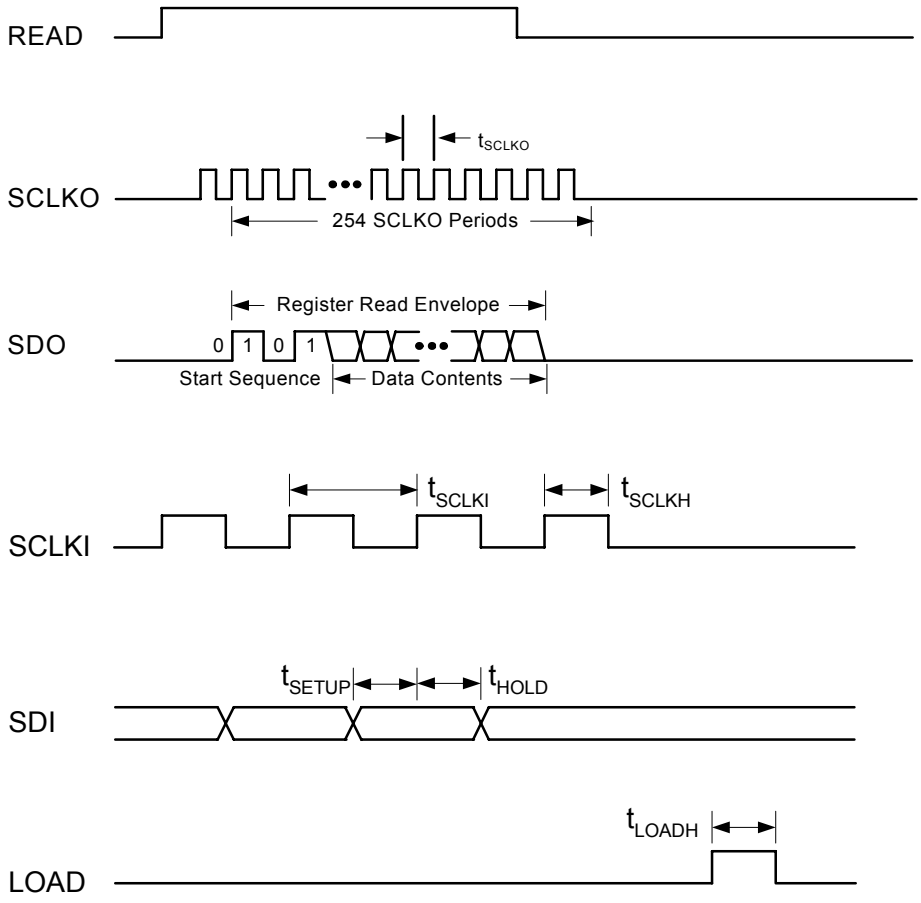


Figure 4. Output Phase Adjust Timing Diagrams

Table 2. DC Characteristics, V_{DD} = 3.3 V

(V_{DD33} = 3.3 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current 1	I_{DD}	622.08 MHz In, 19.44 MHz Out	—	141	155	mA
Supply Current 2	I_{DD}	19.44 MHz In, 622.08 MHz Out	—	135	145	mA
Power Dissipation Using 3.3 V Supply Clock Output	P_D	19.44 MHz In, 622.08 MHz Out	—	445	479	mW
Common Mode Input Voltage[1,2,3] (CLKIN)	V_{ICM}		1.0	1.5	2.0	V
Single-Ended Input Voltage[2,3,4] (CLKIN)	V_{IS}	See Figure 1A	200	—	500[4]	mV_{PP}
Differential Input Voltage Swing[2,3,4] (CLKIN)	V_{ID}	See Figure 1B	200	—	500[4]	mV_{PP}
Input Impedance (CLKIN+, CLKIN–)	R_{IN}		—	80	—	kΩ
Differential Output Voltage Swing (CLKOUT)	V_{OD}	100 Ω Load Line-to-Line, FRQSEL[0:2] = 011	750	825	1100	mV_{PP}
Output Common Mode Voltage (CLKOUT)	V_{OCM}	100 Ω Load Line-to-Line	1.4	1.8	2.2	V
Output Short to GND (CLKOUT)	$I_{SC(–)}$		–60	—	—	mA
Output Short to V_{DD25} (CLKOUT)	$I_{SC(+)}$		—	15	—	mA
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	0.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	50	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	50	µA
Internal Pulldowns (LVTTL Inputs)	I_{pd}		—	—	50	µA
Input Impedance (LVTTL Inputs)	R_{IN}		50	—	—	kΩ
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = 0.5 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = 0.5 mA	2.0	—	—	V

Notes:

1. The Si5321-XC5 device provides weak 1.5 V internal biasing that enables ac-coupled operation.
2. Clock inputs may be driven differentially or single-endedly. When driven single-endedly, the unused input should be ac-coupled to ground.
3. Transmission line termination, when required, must be provided externally.
4. Although the Si5321-XC5 device can operate with input clock swings as high as 1500 mV_{PP}, Silicon Laboratories recommends maintaining the input clock amplitude below 500 mV_{PP} for optimal performance.

Table 3. AC Characteristics
(V_{DD33} = 3.3 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock Frequency (CLKIN) FEC[2:0] = 000 (non FEC)	f_{CLKIN}	No FEC Scaling, FXDDELAY = 1				
INFRQSEL[2:0] = 001			19.436	—	21.685	
INFRQSEL[2:0] = 010			38.872	—	43.369	MHz
INFRQSEL[2:0] = 011			77.744	—	86.738	
INFRQSEL[2:0] = 100			155.48	—	173.48	
INFRQSEL[2:0] = 101			310.97	—	346.95	
INFRQSEL[2:0] = 110			621.95	—	693.90	
Input Clock Frequency (CLKIN) FEC[2:0] = 001 (forward FEC)	f_{CLKIN}	255/238 FEC Scaling, FXDDELAY = 1				
INFRQSEL[2:0] = 001			18.142	—	20.239	
INFRQSEL[2:0] = 010			36.284	—	40.478	MHz
INFRQSEL[2:0] = 011			72.568	—	80.955	
INFRQSEL[2:0] = 100			145.13	—	161.91	
INFRQSEL[2:0] = 101			290.27	—	323.82	
INFRQSEL[2:0] = 110			580.54	—	647.64	
Input Clock Frequency (CLKIN) FEC[2:0] = 010 (reverse FEC)	f_{CLKIN}	238/255 FEC Scaling, FXDDELAY = 1				
INFRQSEL[2:0] = 001			20.826	—	23.234	
INFRQSEL[2:0] = 010			41.652	—	46.465	MHz
INFRQSEL[2:0] = 011			83.305	—	92.934	
INFRQSEL[2:0] = 100			166.61	—	185.87	
INFRQSEL[2:0] = 101			333.22	—	371.74	
INFRQSEL[2:0] = 110			666.44	—	743.47	
Input Clock Frequency (CLKIN) FEC[2:0] = 100 (forward FEC)	f_{CLKIN}	255/237 FEC Scaling Minimum input frequency is in the 155 MHz range, FXDDELAY = 1				
INFRQSEL[2:0] = 001			N/A	N/A	N/A	
INFRQSEL[2:0] = 010			N/A	N/A	N/A	MHz
INFRQSEL[2:0] = 011			N/A	N/A	N/A	
INFRQSEL[2:0] = 100			144.52	—	161.23	
INFRQSEL[2:0] = 101			289.05	—	322.46	
INFRQSEL[2:0] = 110			578.11	—	644.92	
Input Clock Frequency (CLKIN) FEC[2:0] = 101 (reverse FEC)	f_{CLKIN}	237/255 FEC Scaling Minimum input frequency is in the 155 MHz range, FXDDELAY = 1				
INFRQSEL[2:0] = 001			N/A	N/A	N/A	
INFRQSEL[2:0] = 010			N/A	N/A	N/A	MHz
INFRQSEL[2:0] = 011			N/A	N/A	N/A	
INFRQSEL[2:0] = 100			167.31	—	186.66	
INFRQSEL[2:0] = 101			334.62	—	373.31	
INFRQSEL[2:0] = 110			669.25	—	746.61	

Note: The Si5321-XC5 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x clock multiplication function with an option for additional frequency scaling by a factor of 255/238, 238/255, 255/237, 237/255, 66/64, or 64/66 for FEC rate conversion.

Table 3. AC Characteristics (Continued)
(V_{DD33} = 3.3 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock Frequency (CLKIN) FEC[2:0] = 110 (forward FEC) INFRQSEL[2:0] = 001 INFRQSEL[2:0] = 010 INFRQSEL[2:0] = 011 INFRQSEL[2:0] = 100 INFRQSEL[2:0] = 101 INFRQSEL[2:0] = 110	f_{CLKIN}	66/64 FEC Scaling Minimum input frequency is in the 155 MHz range, FXDDELAY = 1	 N/A N/A N/A 150.79 301.58 603.16	 N/A N/A N/A — — —	 N/A N/A N/A 168.22 336.44 672.88	MHz
Input Clock Frequency (CLKIN) FEC[2:0] = 111 (reverse FEC) INFRQSEL[2:0] = 001 INFRQSEL[2:0] = 010 INFRQSEL[2:0] = 011 INFRQSEL[2:0] = 100 INFRQSEL[2:0] = 101 INFRQSEL[2:0] = 110	f_{CLKIN}	64/66 FEC Scaling Minimum input frequency is in the 155 MHz range, FXDDELAY = 1	 N/A N/A N/A 160.36 320.72 641.46	 N/A N/A N/A — — —	 N/A N/A N/A 178.90 357.80 715.59	MHz
Input Clock Rise Time (CLKIN)	t_R	Figure 2	—	—	11	ns
Input Clock Fall Time (CLKIN)	t_F	Figure 2	—	—	11	ns
Input Clock Duty Cycle	C_{DUTY_IN}		40	50	60	%
CLKOUT Frequency Range FRQSEL[2:0] = 001 FRQSEL[2:0] = 000 FRQSEL[2:0] = 100 FRQSEL[2:0] = 010 FRQSEL[2:0] = 101 FRQSEL[2:0] = 011 FRQSEL[2:0] = 110 FRQSEL[2:0] = 111	 f_{O_19} f_{O_39} f_{O_78} f_{O_155} f_{O_311} f_{O_622} f_{O_1250} f_{O_2500}		 19.436 38.872 77.744 155.48 310.97 621.95 1243.9 2487.8	 — — — — — — — —	 21.685 43.369 86.738 173.48 346.95 693.90 1387.8 2775.6	MHz
CLKOUT Rise Time	t_R	Figure 2; differential; after 3 cm of 50 Ω FR4 stripline, FRQSEL[0:2] = 011	—	190	220	ps
CLKOUT Fall Time	t_F	Figure 2; differential; after 3 cm of 50 Ω FR4 stripline, FRQSEL[0:2] = 011	—	190	220	ps
Output Clock Duty Cycle	C_{DUTY_OUT}	Differential: (CLKOUT+) – (CLKOUT–), FRQSEL[0:2] = 011	48	—	52	%
RSTN/CAL Pulse Width	t_{RSTN}		20	—	—	ns

Note: The Si5321-XC5 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x clock multiplication function with an option for additional frequency scaling by a factor of 255/238, 238/255, 255/237, 237/255, 66/64, or 64/66 for FEC rate conversion.

Table 3. AC Characteristics (Continued)
(V_{DD33} = 3.3 V ±5%, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transitionless Period Required on CLKIN for Detecting a LOS Condition. INFRQSEL[2:0] = 001 INFRQSEL[2:0] = 010 INFRQSEL[2:0] = 011 INFRQSEL[2:0] = 100 INFRQSEL[2:0] = 101 INFRQSEL[2:0] = 110	t_{LOS}	Figure 3	 $^{24}/_{fo\_622}$ $^{16}/_{fo\_622}$ $^{12}/_{fo\_622}$ $^{10}/_{fo\_622}$ $^{9}/_{fo\_622}$ $^{8}/_{fo\_622}$	 — — — — — —	 $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$	s
Recovery Time for Clearing an LOS Condition VALTIME = 0 VALTIME = 1	t_{VAL}	Measured from when a valid reference clock is applied until the LOS flag clears	 1.6 90	 — —	 3.2 220	ms
Register Read Out READ Clock High	t_{READH}		1	—	—	µs
Register Read Out Serial Clock (SCLKO) Frequency	$1/t_{SCLKO}$		—	—	4.86	MHz
Register Read Out Clock High to Output Valid	t_{CHOV}		10	—	—	ns
Output Phase INC/DEC Serial Clock (SCLKI) Frequency	$1/t_{SCLKI}$		—	—	1.5	MHz
Output Phase INC/DEC Serial Clock (SCLKI) Clock High	t_{SCLKH}		300	—	—	ns
Output Phase INC/DEC Serial Data (SDI) Setup Time	t_{SETUP}		300	—	—	ns
Output Phase INC/DEC Serial Data (SDI) Hold Time	t_{HOLD}		300	—	—	ns
Output Phase INC/DEC Parallel Load (LOAD) Clock High	t_{LOADH}		300	—	—	ns
Output Phase Delay Inc/Dec Resolution	t_{CDELAY}		—	3.22	—	ns
Fine Adjust Delay Inc/Dec Resolution	t_{FDELAY}		—	100	—	ps

Note: The Si5321-XC5 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x clock multiplication function with an option for additional frequency scaling by a factor of 255/238, 238/255, 255/237, 237/255, 66/64, or 64/66 for FEC rate conversion.

Table 4. AC Characteristics (PLL Performance Characteristics)
(V_{DD33} = 3.3 V ±5%, TA = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 800 Hz Bandwidth (BWSEL[1:0] = 10 and BWBOOST = 0; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 8 Hz	1000	—	—	ns
		f = 80 Hz	100	—	—	ns
		f = 800 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.9	1.2	ps
		50 kHz to 80 MHz	—	0.27	0.35	ps
CLKOUT RMS Jitter Generation FEC[2:0] = 001, 010, 100, 101, 110, 111	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.9	1.2	ps
		50 kHz to 80 MHz	—	0.27	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.6	11	ps
		50 kHz to 80 MHz	—	3.6	10.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 001, 010, 100, 101, 110, 111	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.7	9.2	ps
		50 kHz to 80 MHz	—	3.0	10.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 800 Hz	—	800	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 800 Hz	—	0.0	0.05	dB
Wander/Jitter at 1600 Hz Bandwidth (BWSEL[1:0] = 10 and BWBOOST = 1; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)		f = 16 Hz	500	—	—	ns
		f = 160 Hz	50	—	—	ns
		f = 1600 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	.80	1.0	ps
		50 kHz to 80 MHz	—	.25	.30	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.4	10.0	ps
		50 kHz to 80 MHz	—	3.0	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 1600 Hz	—	1600	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 1600 Hz	—	0.0	0.05	dB
Wander/Jitter at 1600 Hz Bandwidth (BWSEL[1:0] = 01 and BWBOOST = 0; FXDDELAY = 1)						

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5321-XC5 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±5%, TA = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (see Figure 10)	$J_{TOL(PP)}$	f = 16 Hz	1000	—	—	ns
		f = 160 Hz	100	—	—	ns
		f = 1600 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.8	1.2	ps
		50 kHz to 80 MHz	—	0.27	0.35	ps
CLKOUT RMS Jitter Generation FEC[2:0] = 001, 010, 100, 101, 110, 111	$J_{GEN(RMS)}$	12 kHz to 20 MHz,	—	0.9	1.2	ps
		50 kHz to 80 MHz,	—	0.27	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz,	—	6.7	10.0	ps
		50 kHz to 80 MHz,	—	3.0	5.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 001, 010, 100, 101, 110, 111	$J_{GEN(PP)}$	12 kHz to 20 MHz,	—	6.5	10.0	ps
		50 kHz to 80 MHz,	—	3.0	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 1600 Hz	—	1600	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 1600 Hz	—	0.0	0.1	dB
Wander/Jitter at 3200 Hz Bandwidth (BWSEL[1:0] = 01 and BWBOOST = 1; FXDDELAY = 1)						
Jitter Tolerance (see figure 7)		f = 32 Hz	500	—	—	ns
		f = 320 Hz	50	—	—	ns
		f = 3200 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz,	—	0.8	1.0	ps
		50 kHz to 80 MHz,	—	0.25	0.3	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz,	—	6.1	10.0	ps
		50 kHz to 80 MHz,	—	3.0	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 3200 Hz	—	3200	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 3200 Hz	—	0.05	0.1	dB
Wander/Jitter at 3200 Hz Bandwidth (BWSEL[1:0] = 00 and BWBOOST= 0; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 32 Hz	1000	—	—	ns
		f = 320 Hz	100	—	—	ns
		f = 3200 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.9	1.1	ps
		50 kHz to 80 MHz	—	0.3	0.4	ps
CLKOUT RMS Jitter Generation FEC[2:0] = 001, 010, 100,101, 110, 111	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.85	1.1	ps
		50 kHz to 80 MHz	—	0.3	0.4	ps

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5321-XC5 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±5%, TA = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.1	10.0	ps
		50 kHz to 80 MHz	—	3.2	5.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 001, 010, 100,101, 110, 111	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.6	11.0	ps
		50 kHz to 80 MHz	—	3.2	5.5	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 3200 Hz	—	3200	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 3200 Hz	—	0.05	0.1	dB
Wander/Jitter at 6400 Hz Bandwidth (BWSEL[1:0] = 00 and BWBOOST = 1; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)		f = 64 Hz	500	—	—	ns
		f = 640 Hz	50	—	—	ns
		f = 6400 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.75	0.95	ps
		50 kHz to 80 MHz	—	0.27	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.1	10.0	ps
		50 kHz to 80 MHz	—	3.1	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 6400 Hz	—	6400	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 6400 Hz	—	0.05	0.1	dB
Wander/Jitter at 6400 Hz Bandwidth (BWSEL[1:0] = 11 and BWBOOST = 0; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 64 Hz	1000	—	—	ns
		f = 640 Hz	100	—	—	ns
		f = 6400 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	1.0	1.3	ps
		50 kHz to 80 MHz	—	0.4	.55	ps
CLKOUT RMS Jitter Generation FEC[2:0] = 001, 010, 100,101, 110, 111	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	1.0	1.5	ps
		50 kHz to 80 MHz	—	.45	0.7	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	9.3	13.0	ps
		50 kHz to 80 MHz	—	4.1	6.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 001, 010, 100,101, 110, 111	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	8.0	20.0	ps
		50 kHz to 80 MHz	—	4.0	7.5	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 6400 Hz	—	6400	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 6400 Hz	—	0.05	0.1	dB

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5321-XC5 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±5%, TA = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 12800 Hz Bandwidth (BWSEL[1:0] = 11 and BWBOOST = 1; FXDDELAY = 1)						
Jitter Tolerance (see Figure 8)		f = 128 Hz	500	—	—	ns
		f = 1280 Hz	50	—	—	ns
		f = 12800 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[2:0] = 000	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	.85	1.2	ps
		50 kHz to 80 MHz	—	.35	.55	ps
CLKOUT Peak-Peak Jitter Generation FEC[2:0] = 000	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.8	11.0	ps
		50 kHz to 80 MHz	—	3.4	5.5	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 12,800 Hz	—	12800	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 12,800 Hz	—	0.05	.1	dB
Acquisition Time	T_{AQ}	RSTN/CAL high to CAL_ACTV low, with valid clock input and VALTIME = 0	—	300	350	ms
Clock Output Wander with Temperature Gradient [1,2]	C_{CO_TG}	Stable Input Clock; Temperature Gradient <10 °C/min; 800 Hz Loop BW	—	—	45	ps/ °C/ min
Initial Frequency Accuracy in Digital Hold Mode (first 100 ms with voltage and temperature held constant)	C_{DH_FA}	Stable Input Clock Selected until entering Digital Hold	—	—	5.5	ppm
Clock Output Frequency Accuracy Over Temperature in Digital Hold Mode	C_{DH_T}	Constant Supply Voltage	—	17.2	30	ppm /°C
Clock Output Frequency Accuracy Over Supply Voltage in Digital Hold Mode	C_{DH_V33}	Constant Temperature	—	—	600	ppm /V
Clock Output Phase Step[3](See Figure 9)	t_{PT_MTIE}	When hitlessly recovering from Digital Hold mode	–200	0	200	ps
Clock Output Phase Step Slope[3] (See Figure 9)	m_{PT}	When hitlessly recovering from Digital Hold mode				
BWSEL[1:0] = 11, BWBOOST = 0		6400 Hz, No Scaling	—	—	10	ps/ µs
BWSEL[1:0] = 00, BWBOOST = 0		3200 Hz, No Scaling	—	—	5	
BWSEL[1:0] = 01, BWBOOST = 0		1600 Hz, No Scaling	—	—	2.5	
BWSEL[1:0] = 10, BWBOOST = 0		800 Hz, No Scaling	—	—	1.25	

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/µs unit is used here since the maximum phase transient magnitude for the Si5321-XC5 (tPT_MTIE) never reaches one nanosecond.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
3.3 V DC Supply Voltage	V_{DD33}	–0.5 to 3.6	V
LVTTL Input Voltage	V_{DIG}	–0.3 to (V_{DD33} + 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1.0	kV

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	46	°C/W

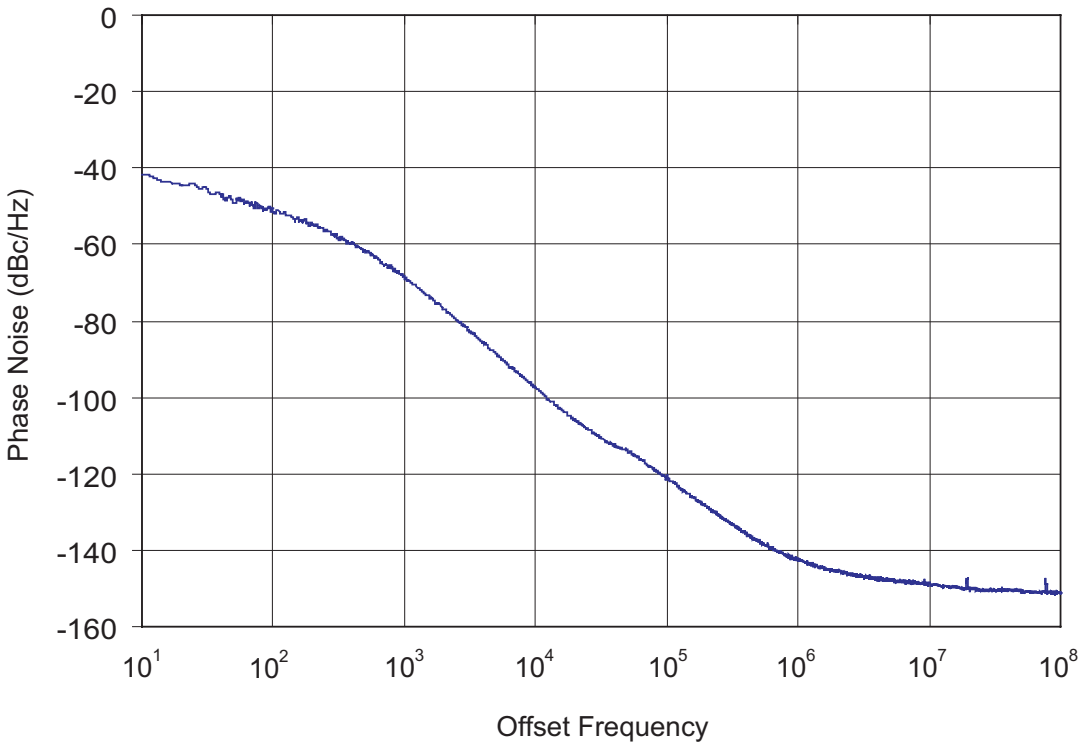
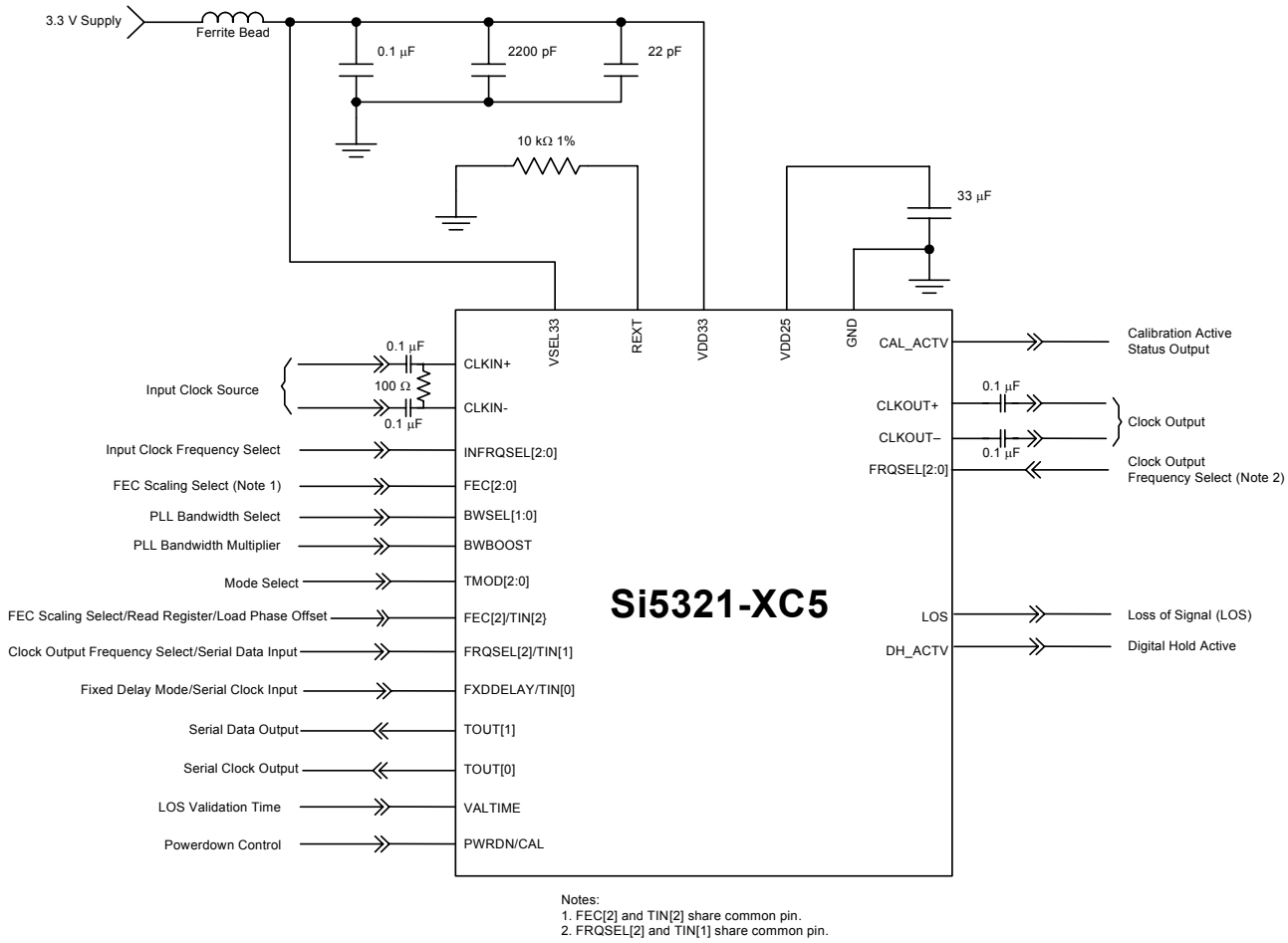


Figure 5. Typical Si5321-XC5 Phase Noise (CLKIN = 155.52 MHz, CLKOUT = 622.08 MHz, and Loop BW = 800 Hz)



Notes:
1. FEC[2] and TIN[2] share common pin.
2. FRQSEL[2] and TIN[1] share common pin.

Figure 6. Si5321-XC5 Typical Application Circuit (3.3 V Supply)

2. Functional Description

The Si5321-XC5 is a high-performance precision clock multiplication and clock generation device. This device accepts a clock input in the 19, 39, 78, 155, 311, or 622 MHz range, attenuates significant amounts of jitter, and multiplies the input clock frequency to generate a clock output in the 19, 39, 78, 155, 311, 622, 1250, or 2500 MHz range. Additional forward or reverse clock rate scaling by a factor of 255/238, 255/237, or 66/64 is provided. This allows systems to easily provide clocks that are scaled for forward error correction (FEC) rates. The 255/238 and 255/237 factors support the ITU-T G.709 requirements for optical transport unit (OTU) OC-48 and OC-192 rates. The 66/64 factor allows conversion between XSBI and 10 GbE Base R rates.

Typical applications for the Si5321-XC5 in SONET/SDH systems are generation and/or cleaning of 19.44, 38.88, 77.76, 155.52, 311.04, 622.08, 1244.16, or 2488.32 MHz clocks from 19.44, 38.88, 77.76, 155.52, 311.04, or 622.08 MHz clock sources.

The Si5321-XC5 employs Silicon Laboratories DSPLL® technology to provide excellent jitter performance while minimizing the external component count and maximizing flexibility and ease of use. The Si5321-XC5 DSPLL phase locks to the input clock signal, attenuates jitter, and multiplies the clock frequency to generate the device's SONET/SDH-compliant clock output. The DSPLL loop bandwidth is user selectable, allowing Si5321-XC5 jitter performance optimization for different applications. The Si5321-XC5 can produce a clock output with jitter generation as low as 0.3 ps_{RMS} (see Table 4 on page 11), making the device an ideal solution for clock multiplication in SONET/SDH (including OC-48, OC-192, and OC768), Gigabit Ethernet, and 10 GbE systems.

The Si5321-XC5 monitors the clock input signal for loss-of-signal and provides a loss-of-signal (LOS) alarm when it detects missing pulses. The Si5321-XC5 provides a digital hold capability that allows the device to continue generation of a stable output clock when the input reference is lost.

2.1. DSPLL®

The Si5321-XC5's phase-locked loop (PLL) uses Silicon Laboratories' DSPLL technology to eliminate jitter, noise, and the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). The technology produces low phase noise clocks with less jitter than is generated using traditional methods. See Figure 5 for an example phase noise plot. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated thus making the DSPLL less susceptible to board-level noise sources. This digital technology also provides highly-stable and consistent operation over all process, temperature, and voltage variations. The benefits are smaller, lower power, cleaner, reliable, and easy-to-use clock circuits.

2.1.1. Selectable Loop Filter Bandwidth

The digital characteristics of the DSPLL loop filter allow control of the loop filter parameters without the need to change external components. The Si5321-XC5 provides the user with up to eight user-selectable loop bandwidth settings for different system requirements. The base loop bandwidth is selected using the BWSEL[1:0] pins along with BWBOOST = 0 pins. When the BWBOOST is driven high, the bandwidth selected on the BWSEL[1:0] pins is doubled. (See Table 7.)

When the BWBOOST pin is asserted, the Si5321-XC5 shows improved jitter generation performance. The BWBOOST function is defined only when hitless recovery and FEC scaling are disabled. Therefore, when BWBOOST is high, the user must also drive FXDDELAY high and FEC[1:0] to 000 for proper operation.

2.2. Clock Input and Output Rate Selection

The Si5321-XC5 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238, 238/255, 255/237, 237/255, 66/64, or 64/66 for FEC rate compatibility. Output rates vary in accordance with the input clock rate. The multiplication factor is configured by selecting the input and output clock frequency ranges for the device.

The Si5321-XC5 accepts an input clock in the 19, 38, 77, 155, 311, or 622 MHz frequency range. The input frequency range is selected using the INFRQSEL[2:0] pins. The INFRQSEL[2:0] settings and associated output clock rates are listed in Table 8.

The Si5321-XC5's DSPLL phase locks to the clock input signal to generate an internal VCO frequency that is a multiple of the input clock frequency. The internal VCO frequency is divided down to produce a clock output in the 19, 39, 78, 155, 311, 622, 1250, or 2500 MHz frequency range. The clock output range is selected using the frequency select (FRQSEL[2:0]) pins. The FRQSEL[2:0] settings and associated output clock rates are given in Table 9.

The Si5321-XC5 clock input frequencies are variable within the range specified in Table 3 on page 8. The output rates are scaled accordingly. If a 19.44 MHz input clock is used, the clock output frequency is 19.44, 38.88, 77.76, 155.52 MHz, etc.

Table 7. Loop Bandwidth and FEC Settings

External Inputs			Effective FEC Conversion Rate	Effective PLL Bandwidth (Hz)
BWBOOST	BWSEL [1:0]	FEC [2:0]		
0	00	000	1/1	3200
0	00	001	255/238	3200
0	00	010	238/255	3200
0	00	011	Reserved	—
0	00	100	255/237	3200
0	00	101	237/255	3200
0	00	110	66/64	3200
0	00	111	64/66	3200
0	10	000	1/1	800
0	10	001	255/238	800
0	10	010	238/255	800
0	10	011	Reserved	—
0	10	100	255/237	800
0	10	101	237/255	800
0	10	110	66/64	800
0	10	111	64/66	800
0	11	000	1/1	6400
0	11	001	255/238	6400
0	11	010	238/255	6400
0	11	011	Reserved	—
0	11	100	255/237	6400
0	11	101	237/255	6400
0	11	110	66/64	6400
0	11	111	64/66	6400
1	00	0xx	1/1	6400
1	10	0xx	1/1	1600
1	11	0xx	1/1	12800
1	01	0xx	1/1	3200
0	01	000	1/1	1600
0	01	001	255/238	1600
0	01	010	238/255	1600
0	01	011	Reserved	—
0	01	100	255/237	1600
0	01	101	237/255	1600
0	01	110	66/64	1600
0	01	111	64/66	1600

Table 8. Nominal Clock Input Frequencies

Input Clock Frequency Range	INFRQSEL2	INFRQSEL1	INFRQSEL0
Reserved	1	1	1
622 MHz	1	1	0
311 MHz	1	0	1
155 MHz	1	0	0
77 MHz	0	1	1
38 MHz	0	1	0
19 MHz	0	0	1
Reserved	0	0	0

Table 9. Nominal Clock Output Frequencies

Output Clock Frequency Range	FRQSEL2	FRQSEL1	FRQSEL0
2,488.32 MHz	1	1	1
1244.16 MHz	1	1	0
622.08 MHz	0	1	1
311.04 MHz	1	0	1
155.52 MHz	0	1	0
77.76 MHz	1	0	0
38.88 MHz	0	0	0
19.44 MHz	0	0	1

2.2.1. FEC Rate Conversion

The Si5321-XC5 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x clock frequency multiplication function with an option for additional forward or reverse frequency scaling by a factor of 255/238 (15/14), 255/237 (85/79), or 66/64 (33/32) for FEC rate conversion applications. The 255/237 and the 66/64 rate conversions requires the input clock rate to be in the 155 MHz or higher ranges. The multiplication factor is configured by selecting the input and output clock frequency ranges for the device. The additional frequency scaling for FEC rate conversion is selected using the FEC[2:0] control inputs.

For example, a 622.08 MHz output clock (a non-FEC rate) can be generated from a 19.44 MHz input clock (a non-FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL[2:0] = 011 (32x multiplication) and setting FEC[2:0] = 000 (no FEC scaling). A 666.51 MHz output clock (an FEC rate) can be generated from a 19.44 MHz input clock (a non-FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL[2:0] = 011 (32x multiplication)

and setting FEC[2:0] = 001 (255/238 FEC scaling).

Finally, a 622.08 MHz output clock (a non-FEC rate) can be generated from a 20.83 MHz input clock (an FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL[2:0] = 011 (32x multiplication) and setting FEC[2:0] = 010 (238/255 FEC scaling).

2.3. PLL Performance

The Si5321-XC5 PLL provides extremely low jitter generation, high jitter tolerance, and a well-controlled jitter transfer function with low peaking and a high degree of jitter attenuation.

2.3.1. Jitter Generation

Jitter generation is defined as the amount of jitter produced at the output of the device with a jitter free input clock. Generated jitter arises from sources within the VCO and other PLL components. Jitter generation is a function of the PLL bandwidth setting. Higher loop bandwidth settings may result in lower jitter generation but may also result in less attenuation of jitter than might be present on the input clock signal.

2.3.2. Jitter Transfer

Jitter transfer is defined as the ratio of output signal jitter to input signal jitter for a specified jitter frequency. The jitter transfer characteristic determines the amount of input clock jitter that passes to the outputs. The DSPLL technology used in the Si5321-XC5 provides tightly-controlled jitter transfer curves because the PLL gain parameters are determined by digital circuits that do not vary over supply voltage, process, and temperature. In a system application, a well-controlled transfer curve minimizes the output clock jitter variation from board to board and provides more consistent system level jitter performance.

The jitter transfer characteristic is a function of the BWSEL[1:0] setting. Lower bandwidth settings result in more jitter attenuation of the incoming clock but may result in higher jitter generation. Table 4 on page 11 gives the 3 dB bandwidth and peaking values for specified BWSEL settings. Figure 7 shows the jitter transfer curve mask.

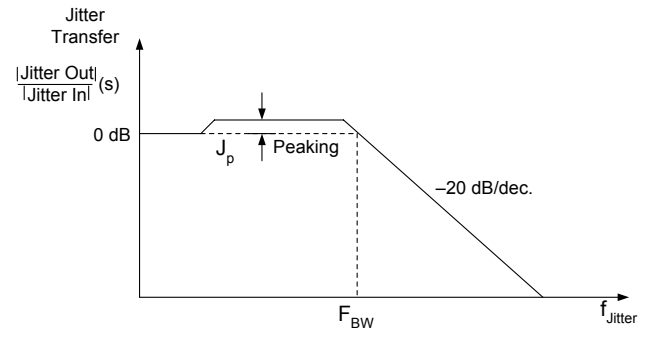


Figure 7. PLL Jitter Transfer Mask/Template

2.3.3. Jitter Tolerance

Jitter tolerance for the Si5321-XC5 is defined as the maximum peak-to-peak sinusoidal jitter that can be present on the incoming clock. The tolerance is a function of the jitter frequency because tolerance improves for lower input jitter frequency.

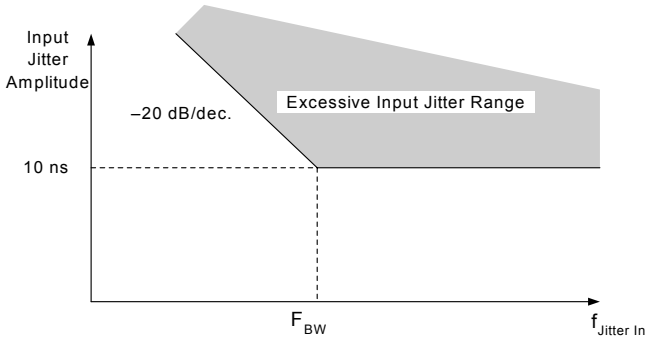


Figure 8. Jitter Tolerance Mask/Template

2.4. Loss-of-Signal Alarm

The Si5321-XC5 has loss-of-signal (LOS) circuitry that constantly monitors the CLKIN input clock for missing pulses. The LOS circuitry sets a LOS output alarm signal when missing pulses are detected.

The LOS circuitry operates as follows. Regardless of the selected input clock frequency range, the LOS circuitry divides down the input clock into the 19 MHz range. The LOS circuitry then over-samples this divided down input clock to search for extended periods of time without input clock transitions. If the LOS circuitry detects four consecutive samples of the divided down input clock that are the same state (i.e., 1111 or 0000), a LOS condition is declared; the Si5321-XC5 goes into digital hold mode, and the LOS output alarm signal is set high. The LOS sampling circuitry runs at a frequency of f_{O_78}, where f_{O_78} is the output clock frequency when the FRQSEL[2:0] pins are set to 100. Figure 3 on page 5 and Table 3 on page 8 list the minimum and maximum transitionless time periods required for declaring a LOS on the input clock (t_{LOS}).

Once the LOS alarm is asserted, it is held high until the input clock is validated over a time period designated by the VALTIME pin. When VALTIME is low, the validation time period is about 1 ms. When VALTIME is high, the validation time period is about 100 ms. If another LOS condition is detected on the input clock during the validation time (i.e., if another set of 1111 or 0000 samples are detected), the LOS alarm remains asserted and the validation time starts over. When the LOS alarm is finally released, the Si5321-XC5 exits digital hold mode and locks to the input clock. The LOS alarm is

automatically set high at power-on and at every low-to-high transition of the RSTN/CAL pin. In these cases, the Si5321-XC5 undergoes a self-calibration before releasing the LOS alarm and locking to the input clock.

The Si5321-XC5 also provides an output indicating the digital hold status of the device, DH_ACTV. The Si5321-XC5 only enters the digital hold mode upon the loss of the input clock. When this occurs, the LOS alarm will also be active. Therefore, applications that require monitoring of the status of the Si5321-XC5 need only monitor the CAL_ACTV and either the LOS or DH_ACTV outputs to know the state of the device.

2.5. Digital Hold of the PLL

When no valid input clock is available, the Si5321-XC5 digitally holds the internal oscillator to its last frequency value. This provides a stable clock to the system until an input clock is valid again. This clock maintains stable operation in the presence of constant voltage and temperature. The frequency accuracy specifications for digital hold mode are given in Table 4 on page 11.

2.6. Hitless Recovery from Digital Hold

When the Si5321-XC5 device is locked to a valid input clock, a loss of the input clock switches the device to digital hold mode. When the input clock signal returns, the device performs a hitless transition from digital hold mode back to the selected input clock. That is, the device executes “phase build-out” to absorb the phase difference between the internal VCO clock operating in digital hold mode and the new/returned input clock. The maximum phase step seen at the clock output during this transition, and the maximum slope of this step, is specified in Table 4 on page 11.

Asserting the Fixed Delay (FXDDELAY) pin disables this feature and the output clock phase and frequency locks with a known phase relationship to the input clock. Consequently, abrupt phase change on the input clock propagates through the device and the output slews at the loop bandwidth until the phase relationship is restored.

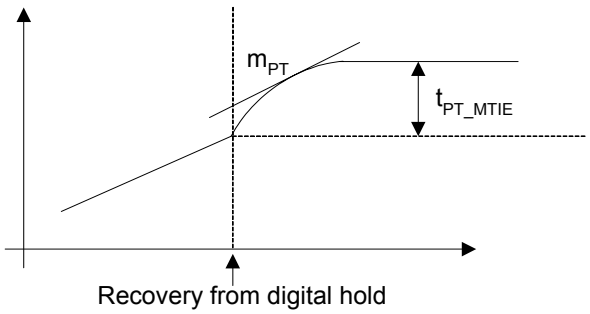


Figure 9. Recovery from Digital Hold

2.7. Clock Output Phase Adjust

2.7.1. Introduction

The Si5321 can be placed in a special mode to manually increment or decrement the device output clock phase. The Si5321 has two output phase adjust options: coarse phase adjust and fine phase adjust. Coarse phase adjust allows the clock output phase to be incremented or decremented in approximately 3.22 ns steps by forcing the PLL feedback divider circuitry to spit or swallow clock cycles. Fine phase adjust is done by externally setting the value of the offset DAC in the phase detector. Fine phase adjust allows the clock output phase to be incremented or decremented in approximately 100 ps steps. Coarse phase adjust and fine phase adjust can be used together or separately.
Both coarse and fine phase adjust are available through a 5-pin management interface. This interface can be used to directly write to internal device registers that control the clock output phase of the Si5321. The following section describes the Si5321 phase adjust capabilities via the 5-pin interface.

2.7.2. Clock Output Phase Adjust

The TMOD[2:0] pins are used to select the device mode of operation. Table 1 lists the device control pins and associated functions when the device is in output phase adjust mode.

Table 10. Output Phase Adjust Control Pins

Device Pin	I/O	Location	Normal Operation	Register Read Out	Output Phase INC/DEC
TMOD[2]	I	B6	0	1	0
TMOD[1]	I	B7	0	1	0
TMOD[0]	I	C8	0	0	1
FEC[2]/TIN[2]	I	B2	FEC[2]	READ	LOAD
FRQSEL[2]/TIN[1]	I	B3	FRQSEL[2]	N/A	SDI
FXDDELAY/TIN[0]	I	B4	FXDDELAY	ENVSEL	SCLKI
TOUT[1]/DEVID[1]	O	A5	0	SDO	N/A
TOUT[0]/DEVID[0]	O	A6	0	SCLKO	N/A

In the output phase adjust mode, the state of FEC[2], FRQSEL[2], and FXDDELAY cannot be changed. Instead, the device remembers the last valid state of these pins and uses these settings for the entire time the device is in output phase adjust mode. For example, if FXDDELAY is tied low when the device enters output phase adjust mode, hitless recovery from digital hold is enabled during output phase adjust mode. If FXDDELAY is tied high when the device enters output phase adjust mode, hitless recovery from digital hold is disabled during output phase adjust mode. Similarly, the device retains the last valid state of FEC[2] and FRQSEL[2] while the device is in the output phase adjust mode, thereby retaining the pin-selected frequency plan.

In the fine phase adjust mode, it takes two steps to manually adjust the device output clock phase. The first step, Register Read Out, is used to acquire the current phase detector value. The second step, Output Phase Increment/Decrement, is used to manually increment or decrement the DAC value, and write it back to the Si5321 to achieve the desired phase adjust. The TMOD[2:0] pins determine whether the device is being used to read the phase detector DAC value or increment/decrement the output phase.

2.7.3. Register Read Out

To read the phase detector DAC value, the TMOD[2:0] pins must be set to 110. When configured to read this register value, the device operates normally except that a high level on the READ input signal causes the values of many of the internal digital registers to be periodically copied into parallel shadow registers. After a brief delay, the values in the shadow registers are serially shifted out through the serial data output pin, SDO, and synchronized to the serial clock output, SCLKO. The register read envelope is bounded by a four-bit preamble 0101. As long as READ remains high, the internal registers are resampled and shifted out once every 254 cycles of SCLKO. The complete I/O data format and timing for register readout is shown on page 6. During register read out, the SCLKO and SDO pins drive out a low value except when driving out the register read envelope. Once a readout sequence commences, the entire register read envelope is shifted out, regardless of any changes on READ. The ENVSEL signal should be set high to read the phase detector DAC value.

The 119-bit READ register chain is defined as follows:

Reserved[21:0]	pdDAC[6:0]	Reserved[89:0]

The data contents of the register read envelope are shifted out from left to right.

2.7.4. Output Phase Increment/Decrement

TMOD[2:0] pins are set to 001 to write back the desired DAC codes. Serial clock and data inputs (SCLKI and SDI) are used to serially program a 9-bit chain of phase adjust registers. A parallel load signal (LOAD) is then used to drive the serially-programmed values into the phase offset (auto-zeroing) DAC and into the pulse spitting/swallowing circuitry. This allows external control of the phase offset DAC for fine output phase adjust and external control of the pulse spitting/swallowing circuitry for coarse phase adjust of the Si5321 output phase. Timing constraints for programming the Si5321 phase adjust registers and for loading in the new values are shown on page 6. The 9-bit phase adjust register chain is defined as follows:

pdDAC[6:0]	spit	swallow

The device has a special production test mode entered when the mode select lines are set to TMOD[2:0] = 111. If this happens during operation, the part is not guaranteed to meet data sheet specifications. Furthermore, because no application can guarantee

that the state of all three mode select lines will switch simultaneously, the mode select lines should be changed one bit at a time. This process will ensure that the device never enters the state TMOD[2:0] = 111. Because the Si5321 samples the state of the mode select lines approximately every 210 ns, a delay of approximately 500 ns between states is recommended to ensure the device samples each state correctly. An example of how this might be done is as follows:

- To change from normal operation to the register read mode, the following sequence should be used: TMOD[2:0] = 000, 100, 110.
- To change from register read to the register write mode, use this sequence: TMOD[2:0] = 110, 100, 000, 001.

While it is unlikely for any problems caused by this timing to occur, it is possible to inadvertently enter the mode 111 unless this procedure is followed.

2.7.5. Output Phase Decrement Example

1. Read the current device phase detector DAC values by setting TMOD[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register.
2. Perform a coarse phase decrement on the device clock outputs. Set TMOD[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain: 1000000_1_0

   Note: This example assumes the previous value of the phase detector DAC is 1000000. The value actually written here should be the same as the DAC value read in step 1.

   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5321 phase detector to remove a fixed delay from the device clock outputs. The amount of delay removed from the clock outputs is approximately equal to 3.22 ns.
3. Read the current device phase detector DAC values by setting TMOD[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register.
4. Perform a fine phase decrement on the device clock outputs. Set TMOD[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain: 1000001_0_0

   Note: This example assumes the previous value of the phase detector DAC is 1000000. The value actually written here should be the same as the DAC value read in step 3 plus one count.

   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5321 phase detector to remove a fixed amount of delay from the device clock outputs. The amount of delay removed from the clock outputs is approximately equal to 100 ps.

2.7.6. Output Phase Increment Example

1. Read the current device phase detector DAC values by setting TMOD[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register.
2. Perform a coarse phase increment on the device clock outputs. Set TMOD[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain: 1000000_0_1

   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5321 phase detector to add a fixed amount of delay to the device clock outputs. The amount of delay added to the clock outputs is approximately equal to 3.22 ns.

   Note: This example assumes the previous value of the phase detector DAC is 1000000. The value actually written here should be the same as the DAC value read in step 1.
3. Read the current device phase detector DAC values by setting TMOD[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register. The following example assumes the phase detector DAC value is 1000000.
4. Perform a fine phase increment on the device clock outputs. Set TMOD[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain: 0111111_0_0

   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5321 phase detector to add a fixed delay to the device clock outputs. The amount of delay added to the clock outputs is approximately equal to 100 ps.

   Note: This example assumes the previous value of the phase detector DAC is 1000000. The value actually written here should be the same as the DAC value read in step 3 minus one count.

For a coarse phase increment or decrement, the amount of delay time added or subtracted to the clock output is based on the VCO frequency. Regardless of the input or output frequency selections, the VCO is always running at a nominal 2.48832 GHz. However, the VCO is phase locked to the input clock. Therefore, its frequency will ultimately be determined by the frequency of the input clock. The resulting effect is that if

the input clock is not exactly equal to the nominal frequency for that selection, the VCO frequency will also be off by the same relative amount. Thus the step sizes resulting from these manipulations will also be off by that same relative amount. The frequency of the VCO is also scaled according to the setting of the FEC[2:0] pins.

When the phase of the Si5321 clock output is adjusted using the output phase adjust mode, the output clock will typically begin to move within 2 µs. However, it will move to its new phase setting at a rate of change that is determined by the setting of the BWSEL[1:0] pins.

2.8. Reset

The Si5321-XC5 provides a Reset/Calibration pin (RSTN/CAL) that resets the device and disables all of the device outputs. When the RSTN/CAL pin is driven low, the internal circuitry enters reset mode and all LVTTL outputs are forced into a high-impedance state. Also, the CLKOUT+ and CLKOUT– pins are connected to V_{DD25} through 100 Ω on-chip resistors. This feature is useful for applications that employ redundant clock sources and for in-circuit test applications. A low-to-high transition on RSTN/CAL initializes all digital logic to a known condition and initiates self-calibration of the DSPLL. At the completion of self-calibration, the DSPLL begins to lock to the clock input signal.

2.9. PLL Self-Calibration

The Si5321-XC5 achieves optimal jitter performance by using self-calibration circuitry to set the VCO center frequency and loop gain parameters within the DSPLL. Internal circuitry generates self calibration automatically on powerup or after a loss-of-power condition. Self-calibration also can be manually initiated by a low-to-high transition on the RSTN/CAL input.

A self-calibration should be initiated after changing the state of the FEC[2:0] inputs. Whether manually initiated or automatically initiated at powerup, the self-calibration process requires the presence of a valid input clock.

If the self-calibration is initiated without a valid input clock, the device waits for a valid input clock before executing the self-calibration. The Si5321-XC5 does not provide an output clock while waiting for a valid input clock or while executing its self-calibration. When the input clock is validated, the calibration procedure executes to completion; the device locks to the input clock, and the output clock turns on. Subsequent losses of the input clock do not require self-calibration. If the input clock is lost following self-calibration, the device enters digital hold mode with the output clock frequency held to its last value before the LOS condition was detected. When the input clock returns and is validated, the device exits digital hold mode by re-locking to the input clock without executing another self-calibration.

2.10. Bias Generation Circuitry

The Si5321-XC5 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents, which significantly reduces power consumption and variation as compared with traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

2.11. Differential Input Circuitry

The Si5321-XC5 provides a differential input for the clock input, CLKIN. This input is internally-biased to a voltage of V_{ICM} (see Table 2 on page 7) and may be driven by a differential or single-ended driver circuit. For transmission line termination, the termination resistor is connected externally as shown.

2.12. Differential Output Circuitry

The Si5321-XC5 utilizes a current mode logic (CML) architecture to drive the differential clock output, CLKOUT.

For single-ended output operation simply connect to either CLKOUT+ or CLKOUT– and leave the unused signal unconnected.

2.13. Power Supply Connections

The Si5321-XC5 incorporates an on-chip voltage regulator to power the device from a 3.3 V supply. The voltage regulator requires an external compensation circuit of one resistor and one capacitor to ensure stability over all operating conditions.

Internally, the Si5321-XC5 V_{DD33} pins are connected to the on-chip voltage regulator input and to the device's LVTTL I/O circuitry. The V_{DD25} pins supply power to the core DSPLL circuitry, and are also used for connection of the external compensation circuit.

The regulator's compensation circuit is a resistor and a capacitor in series between the V_{DD25} node and ground. Typically, the resistor is incorporated into the capacitor's equivalent series resistance (ESR). The target RC time constant for this combination is 15 to 50 µs. The capacitor used in the Si5321-XC5 evaluation board is a 33 µF tantalum capacitor with an ESR of 0.8 Ω. This gives an RC time constant of 26.4 µs. The Venkel part number TA6R3TCR336KBR is an example of a capacitor that meets these specifications. (See Figure 6.)

To get optimal performance from the Si5321-XC5 device, the power supply noise spectrum must comply with the plot in Figure 10. This plot shows the power

supply noise tolerance mask for the Si5321-XC5. The customer should provide a 3.3 V supply that does not have noise density in excess of the amount shown in the diagram. However, the diagram cannot be used as spur criteria for a power supply that contains single tone noise.

2.14. Design and Layout Guidelines

Precision clock circuits are susceptible to board noise and EMI. To take precautions against unacceptable levels of board noise and EMI affecting performance of the Si5321-XC5, consider the following:

- Power the device from 3.3 V since the internal regulator provides >40 dB of isolation to the V_{DD25} pins (which power the PLL circuitry).
- When powering the device from 3.3 V, use an isolated, local plane to connect the V_{DD25} pins. Avoid running signal traces over or below this plane without a ground plane in between.
- Route all I/O traces between ground planes as much as possible
- Maintain an input clock amplitude in the 200 mV_{PP} to 500 mV_{PP} differential range.
- Excessive high-frequency harmonics of the input clock should be minimized. The use of filters on the input clock signal can be used to remove high-frequency harmonics.

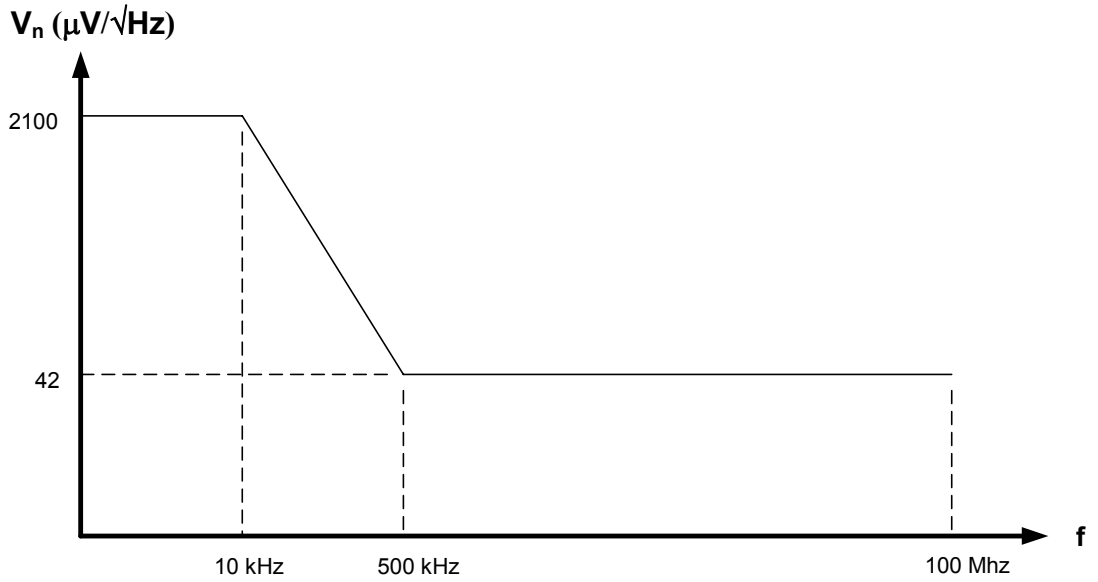
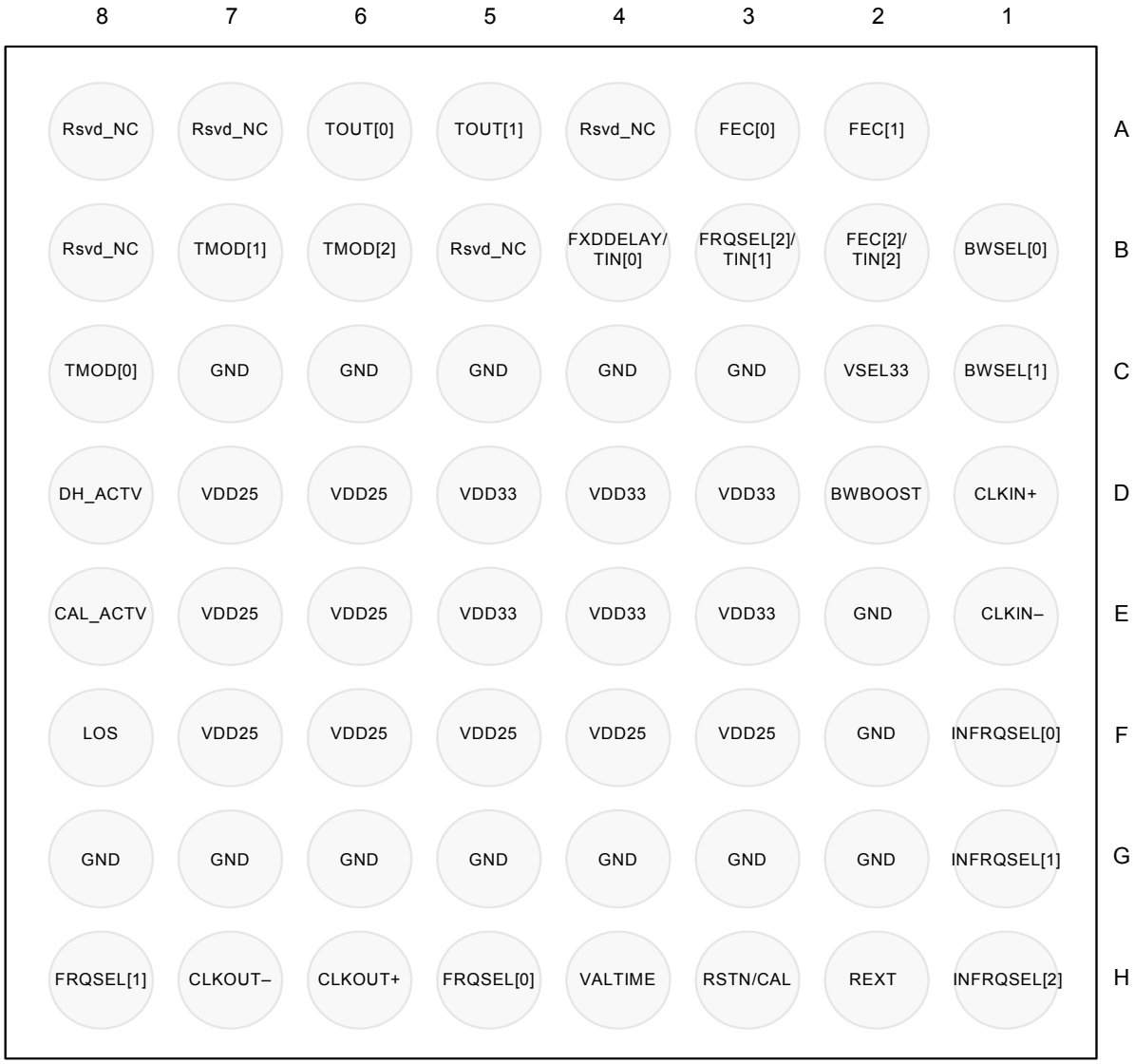


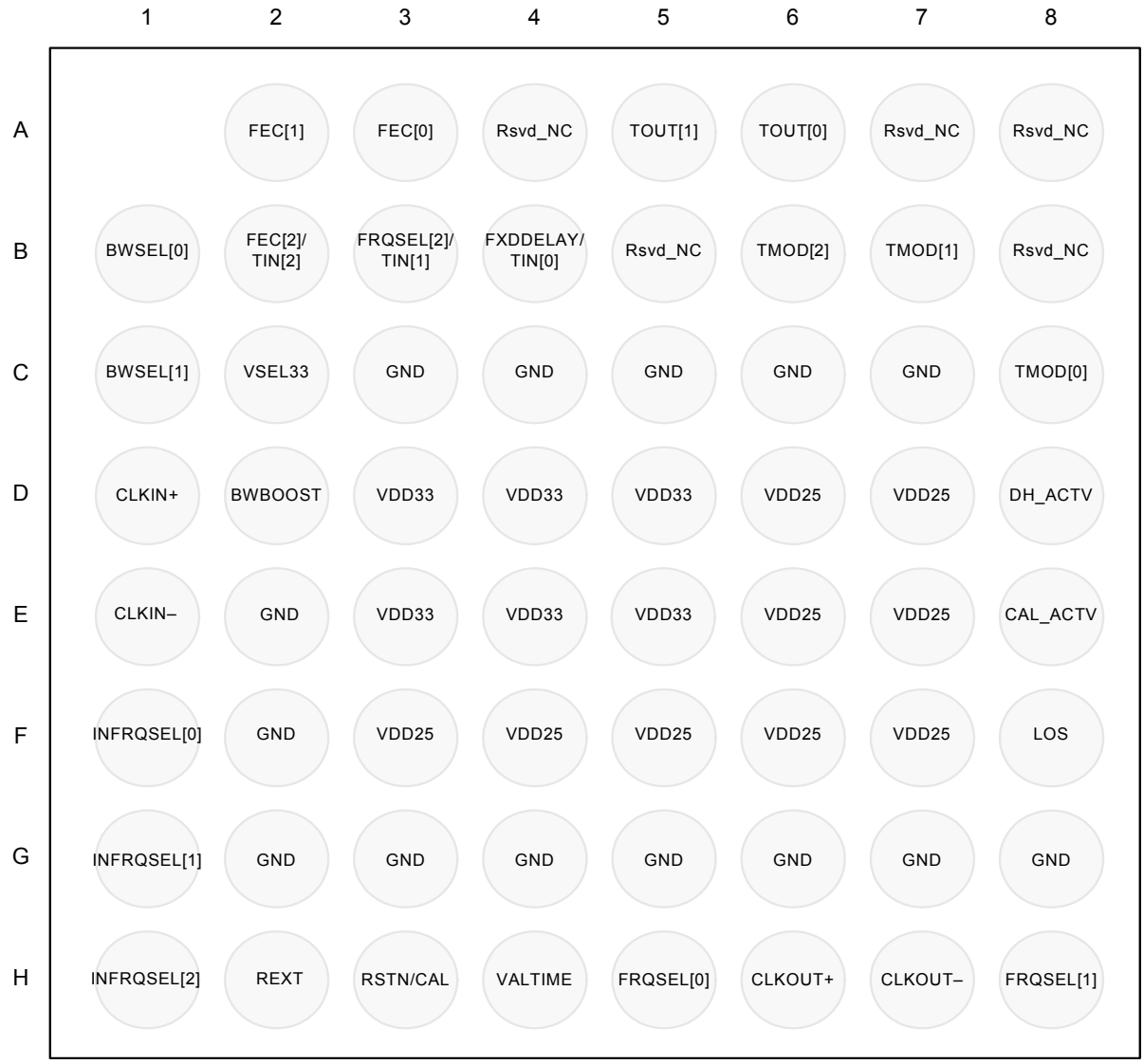
Figure 10. Power Supply Noise Tolerance Mask

3. Pin Descriptions: Si5321-XC5



Bottom View

Figure 11. Si5321-XC5 Pin Configuration (Bottom View)



Top View

Figure 12. Si5321-XC5 Pin Configuration (Transparent Top View)

Table 11. Si5321-XC5 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
D1 E1	CLKIN+ CLKIN–	I	AC Coupled 200–500 mV_{PPD} (See Table 2)	**System Clock Input.** Clock input to the DSPLL circuitry. The frequency of the CLKIN signal is multiplied by the DSPLL to generate the CLKOUT clock output. The input-to-output frequency multiplication factor is set by selecting the clock input range and the clock output range. The frequency of the CLKIN clock input can be in the 19, 38, 77, 155, 311, or 622 MHz range (nominally 19.44, 38.88, 77.76, 155.52, 311.04, or 622.08 MHz) as indicated in Table 3 on page 8. The clock input frequency is selected using the INFRQSEL[2:0] pins. The clock output frequency is selected using the FRQSEL[1:0] pins. An additional scaling factor may be selected for FEC operation using the FEC[2:0] control pins.
F1 G1 H1	INFRQSEL[0] INFRQSEL[1] INFRQSEL[2]	I*	LVTTL*	**Input Frequency Range Select.** Pins(INFRQSEL[2:0]) select the frequency range for the input clock, CLKIN. (See Table 3 on page 8.) 000 = Reserved. 001 = 19 MHz range. 010 = 38 MHz range. 011 = 77 MHz range. 100 = 155 MHz range. 101 = 311 MHz range. 110 = 622 MHz range. 111 = Reserved.
H6 H7	CLKOUT+ CLKOUT–	O	CML	**Differential Clock Output.** High-frequency clock output. The frequency of the CLKOUT output is a multiple of the frequency of the CLKIN input. The input-to-output frequency multiplication factor is set by selecting the clock input range and the clock output range. The frequency of the CLKOUT clock output can be in the 19, 38, 77, 155, 311, 622, 1244 or 2488 MHz range as indicated in Table 3 on page 8. The clock output frequency is selected using the FRQSEL[2:0] pins. The clock input frequency is selected using the INFRQSEL[2:0] pins. An additional scaling factor may be selected for FEC operation using the FEC[2:0] control pins.
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

Table 11. Si5321-XC5 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
H5 H8 B3	FRQSEL[0] FRQSEL[1] FRQSEL[2]	I*	LVTTL*	**Clock Output Frequency Range Select.** Select the frequency range of the clock output, CLKOUT. (See Table 3 on page 8.) 001 = 19 MHz Frequency Range. 000 = 39 MHz Frequency Range. 100 = 78 MHz Frequency Range. 010 = 155 MHz Frequency Range. 101 = 311 MHz Frequency Range. 011 = 622 MHz Frequency Range. 110 = 1.25 GHz Frequency Range. 111 = 2.5 GHz Frequency Range.
B3	TIN[1]	I	LVTTL	**Serial Data Input (Output Phase Inc/Dec).** Input pin for transferring data into the phase adjust registers.
A3 A2 B2	FEC[0] FEC[1] FEC[2]	I*	LVTTL*	**FEC Selection.** Enables or disables scaling of the input-to-output frequency multiplication factor for FEC clock rate compatibility. The frequency of the CLKOUT output is a multiple of the frequency of the CLKIN input. Selecting the clock input range, the clock output range, and the FEC scaling factor sets the input-to-output frequency multiplication factor. The clock output frequency is selected using the FRQSEL[2:0] pins. The clock input frequency is selected using the INFRQSEL[2:0] pins. Scaling factors of 255/238, 238/255, 255/237, 237/255, 66/64, or 64/66 may be selected for FEC operation using the FEC[2:0] control pins as indicated below. Scaling factors of 255/237, 237/255, 66/64, or 64/66 require that the input clock rate be in the 155 MHz or higher range. 000 = No FEC scaling. 001 = 255/238 FEC scaling. 010 = 238/255 FEC scaling. 011 = Reserved. 100 = 255/237 FEC scaling (155 MHz or higher input clock range required). 101 = 237/255 FEC scaling (155 MHz or higher input clock range required). 110 = 66/64 FEC scaling (155 MHz or higher input clock range required). 111 = 64/66 FEC scaling (155 MHz or higher input clock range required).
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

Table 11. Si5321-XC5 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B2	TIN[2]	I	LVTTL	**Read Register (Register Read Out).** This pin must be held high to shift the phase detector DAC values out of the device. **Load Phase Offset (Output Phase Inc/Dec).** A rising edge on this pin loads data from the phase adjust registers into the phase offset circuitry.
B1 C1	BWSEL[0] BWSEL[1]	I*	LVTTL*	**Bandwidth Select.** BWSEL[1:0] pins set the bandwidth of the loop filter within the DSPLL to 6400, 3200, 1600, or 800 Hz as indicated below. 00 = 3200 Hz 01 = 1600 Hz 10 = 800 Hz 11 = 6400 Hz **Note:** The loop filter bandwidth is twice the value indicated here when BWBOOST is set high.
D2	BWBOOST	I*	LVTTL*	**Bandwidth Boost.** Active high input to boost the selected bandwidth 2x. When this pin is high the loop filter bandwidth selected on BWSEL[1:0] is doubled. When this pin is high, FXDDELAY must also be high and FEC[2:0] must be 000.
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

Table 11. Si5321-XC5 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B4	FXDDELAY	I*	LVTTL*	**Fixed Delay Mode.** Set high to disable hitless recovery from digital hold mode. This configuration is useful in applications that require a known or constant input-to-output phase relationship. When this pin is high, hitless switching from digital hold mode back to a valid clock input is disabled. When switching from digital hold mode to a valid clock input with FXDDELAY high, the clock output changes as necessary to re-establish the initial/ default input-to-output phase relationship that is established after powerup or reset. The rate of change is determined by the setting of BWSEL[1:0]. When this pin is low, hitless switching from Digital Hold mode back to a valid clock input is enabled. When switching from digital hold mode to a valid clock input with FXDDELAY low, the device enables "phase build out" to absorb the phase difference between the clock output and the clock input so that the phase change at the clock output is minimized. In this case, the input-to-output phase relationship following the transition out of digital hold mode is determined by the phase relationship at the time that switching occurs. **Note:** FXDDELAY should remain at a static high or static low level during normal operation. Transitions on this pin are allowed only when the RSTN/CAL pin is low. FXDDELAY must be set high when BWBOOST is set high.
B4	TIN[0]	I	LVTTL	**Envelope Select (Register Read Out).** This pin must be held high to read the value of the phase detector DAC. **Serial Clock Input (Output Phase Inc/Dec).** A rising edge on this pin drives serial data from TIN[1] into the phase adjust registers.
H4	VALTIME	I*	LVTTL*	**Clock Validation Time for LOS.** VALTIME sets the clock validation times for recovery from an LOS alarm condition. When VALTIME is high, the validation time is approximately 100 ms. When VALTIME is low, the validation time is approximately 2 ms.
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

Table 11. Si5321-XC5 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
H3	RSTN/CAL	I*	LVTTL*	**Reset/Calibrate.** When low, all LVTTL outputs are forced into a high impedance state, the DSPLL is forced out-of-lock, and the device control logic is reset. A low-to-high transition on RSTN/CAL initializes all digital logic to a known condition and initiates self-calibration of the DSPLL. At the completion of self-calibration, the DSPLL begins to lock to the selected clock input signal and begins to drive out the output clock signal onto the CLKOUT pins.
F8	LOS	O	LVTTL	**Loss-of-Signal (LOS) Alarm for CLKIN.** Active high output indicates that the Si5321-XC5 has detected missing pulses on the input clock signal. The LOS alarm is cleared after either 100 ms or 13 s of a valid CLKIN clock input, depending on the setting of the VALTIME input.
D8	DH_ACTV	O	LVTTL	**Digital Hold Mode Active.** Active high output indicates that the DSPLL is in digital hold mode. Digital hold mode locks the current state of the DSPLL and forces the DSPLL to continue generation of the output clock with no additional phase or frequency information from the input clock.
E8	CAL_ACTV	O	LVTTL	**Calibration Mode Active.** This output is driven high during the DSPLL self-calibration and the subsequent initial lock acquisition period.
C2	VSEL33	I*	LVTTL*	**Reserved.** This pin must be tied to VDD33 directly for normal operation.
D3–D5, E3–E5	V_{DD33}	V_{DD}	Supply	**3.3 V Supply.** 3.3 V power is applied to the V_{DD33} pins. Typical supply bypassing/decoupling for this configuration is indicated in the typical application diagram for 3.3 V supply operation.
D6, D7, E6, E7, F3–F7	V_{DD25}	V_{DD}	Supply	**2.5 V Compensation Network.** These pins provide a means of connecting the compensation network for the on-chip regulator.
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

Table 11. Si5321-XC5 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
C3–C7, E2, F2, G2–G8	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of the device.
H2	REXT	I	Analog	**External Biasing Resistor.** Used by on-chip circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
A4, A7, B5, B8	RSVD_NC		LVTTL	**Reserved—No Connect.** This pin must be left unconnected for normal operation.
B6 B7 C8	TMOD[2] TMOD[1] TMOD[0]	I	LVTTL	**Mode Select.** Used to enable clock output phase adjust mode.
A6	TOUT[0]	O	LVTTL	**Serial Clock Output (Register Read Out).** A rising edge on this pin shifts data from the device registers to the serial data output pin (TOUT[1]).
A5	TOUT[1]	O	LVTTL	**Serial Data Output (Register Read Out).** Output pin for transferring data out of the device registers.
***Note:** The LVTTL inputs on the Si5321-XC5 device have an internal pulldown mechanism that causes the input to default to a logic low state if the input is not driven from an external source.				

4. Ordering Guide

Part Number	Package	Temperature Range
Si5321-G-XC5	63-Ball CBGA (Prior Revision) RoHS-5	–20 to 85 °C
Si5321-H-XL5	63-Ball PBGA (Current Revision) RoHS-5	–20 to 85 °C
Si5321-H-ZL5	63-Ball PBGA (Current Revision) RoHS-6	–20 to 85 °C

5. Package Outline

Figure 13 illustrates the package details for the Si5321-XC5. Table 12 lists the values for the dimensions shown in the illustration.

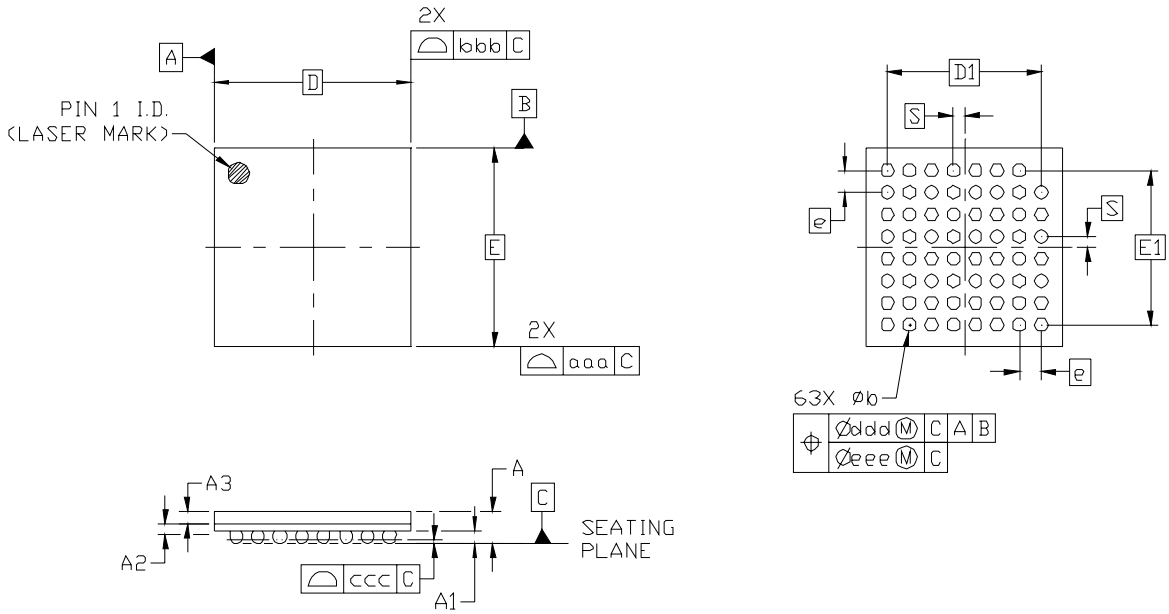


Figure 13. 63-Ball Plastic Ball Grid Array (PBGA)

Table 12. Package Diagram Dimensions (mm)

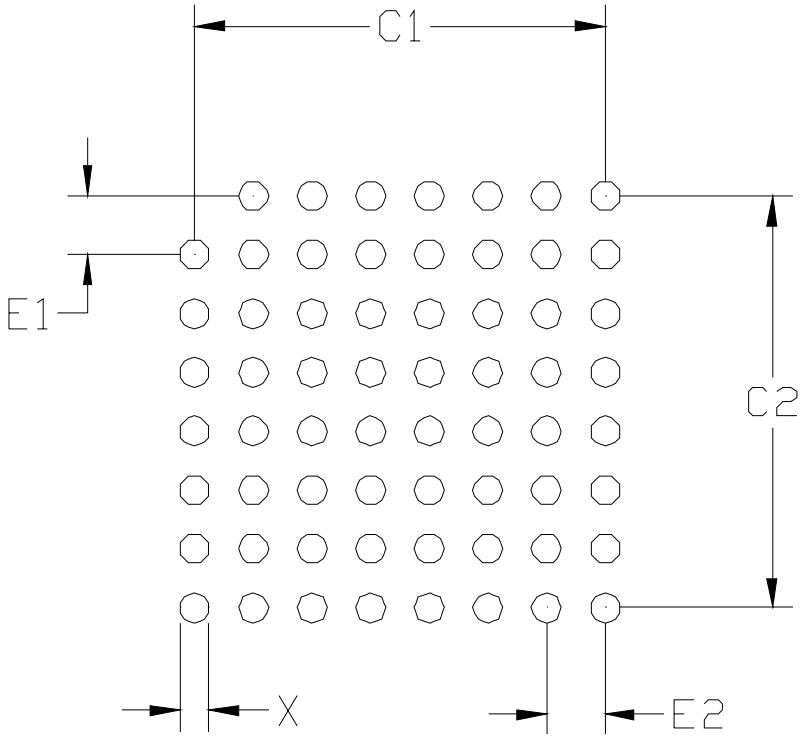
Symbol	Min	Nom	Max
A	1.24	1.41	1.58
A1	0.40	0.50	0.60
A2	0.34	0.38	0.42
A3	0.50	0.53	0.56
b	0.50	0.60	0.70
D	9.00 BSC		
E	9.00 BSC		
D1	7.00 BSC		

Symbol	Min	Nom	Max
E1	7.00 BSC		
e	1.00 BSC		
S	0.50 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.12		
ddd	0.15		
eee	0.08		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-192, variation AAB-1.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. 9x9 mm PBGA Card Layout



Symbol	Min	Nom	Max
X	0.40	0.45	0.50
C1		7.00	
C2		7.00	
E1		1.00	
E2		1.00	

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST:

Revision 1.0 to Revision 1.1

- Updated number of cycles from 256 to 254 in Figure 4, “Output Phase Adjust Timing Diagrams,” on page 6.
- Updated number of cycles from 256 to 254 in "2.7.3. Register Read Out" on page 21.

Revision 1.1 to Revision 1.2

- Device Revision G to H Transition.
- Updated test condition for differential output voltage swing, input clock frequency, clock output rise/fall time, and jitter specifications.
- Updated "3. Pin Descriptions: Si5321-XC5" on page 25.
- Updated "5. Package Outline" on page 34.
- Updated "6. 9x9 mm PBGA Card Layout" on page 35.

NOTES:

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