VTC Inc.
Value the Customer™

VM5200

10, 14 OR 20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

970801

August, 1997

FEATURES

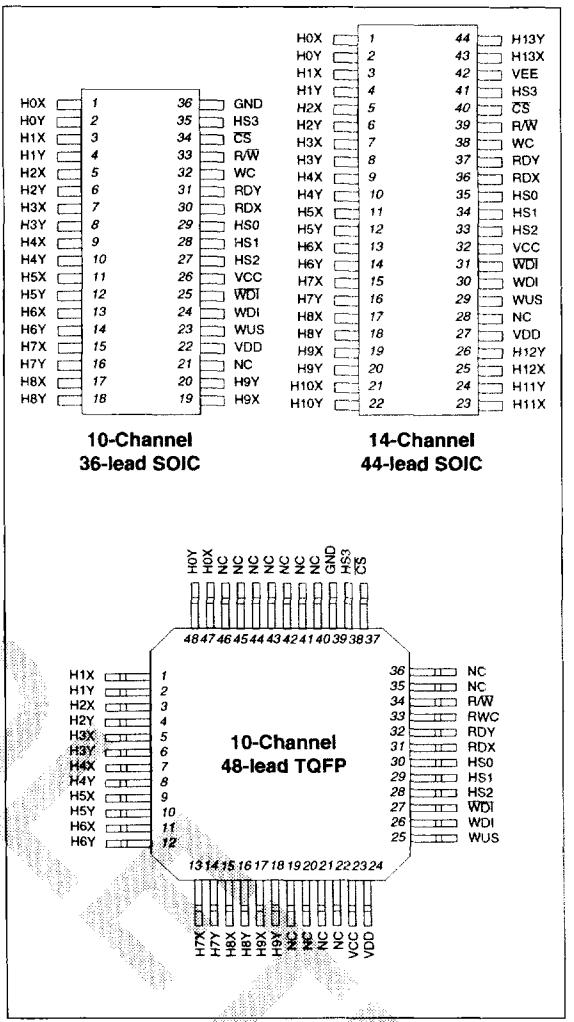
- High Performance
  - Rise/Fall Times = 6.5 ns Typical into 1 µH Head
  - Input Capacitance = 15 pF Typical
  - Input Noise = 0.52 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 µH
  - Voltage Gain = 150 V/V - Other Options Available
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- Options Available
  - WDFF on the Write Data Inputs Connected or Disconnected
- Available With up to 20-Channels, Consult VTC for Other Options

DESCRIPTION

The VM5200 is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address up to 20-channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

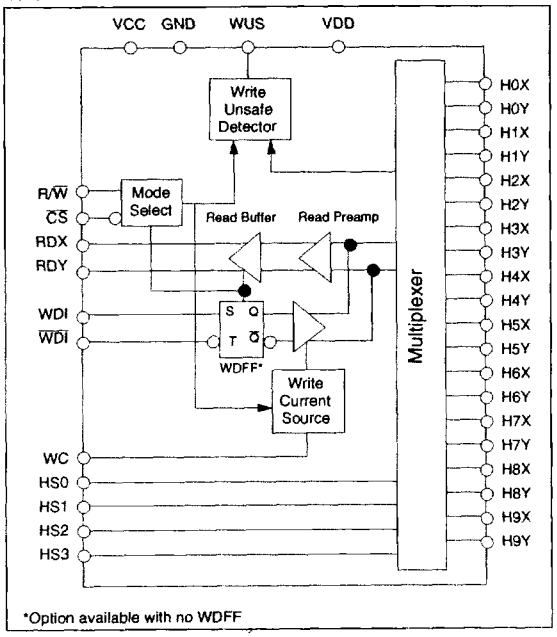
The VM5200 is available in a variety package options. Please consult VTC for package availability.

CONNECTION DIAGRAMS



For additional connection diagrams see the last page of this data sheet.

BLOCK DIAGRAM



*Option available with no WDFF

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:	
V_{DD}	-0.3V to +13.5V
V_{CC}	-0.3V to +7V
Write Current (I_W)	100mA
Input Voltages:	
Digital Input Voltage V_{IN}	-0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H	-0.3V to (V_{CC} + 0.3)V
WUS Pin Voltage Range V_{WUS}	-0.3V to +13.5V
Output Current:	
RDX, RDY: I_O	-10mA
WUS: I_{WUS}	+12mA
Junction Temperature,	150°C
Storage Temperature Range	-65° to 150°C
Thermal Characteristics, Θ_{JA}:	
36-lead SOIC	80°C/W
44-lead SOIC	70°C/W
48-lead TQFP	80°C/W
64-lead TQFP	60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:	
V_{DD}	12V ± 10%
V_{CC}	5V ± 10%
Junction Temperature	0°C to 125°C

CIRCUIT OPERATION

The VM5200 addresses up to 20 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Table 1. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM5200 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the Write Data Flip-Flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM5200 because the internal 380Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM5200 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load.

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There is also a mask option to make RDX and RDY open collector outputs. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

$R/\overline{W}$	$\overline{CS}$	MODE
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	HS1	HS2	HS3	HS4	HEAD
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	I_{CC}	Read Mode		47	60	mA
		Write Mode		26	35	
		Idle Mode		1.1	2.5	
VDD Supply Current	I_{DD}	Read Mode		0.6	1.5	mA
		Write Mode		18 + I_W	32 + I_W	
		Idle Mode		0.8	1.5	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		242	350	mW
		Write Mode: I_W = 20mA		586	850	
		Idle Mode		12.7	35	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} < 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Read/Idle Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	40	50**		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	50	75**		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.52	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz	12	15	18	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	260	750		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	8		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	60	80		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	55	80		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45	55		dB
Output Offset Voltage	| V_{OS} |	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.2	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.2	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		17	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

** The bandwidth is head dependent due to the capacitive cancellation circuitry. When the preamplifier is used with a head the bandwidth is dominated by the inductance of the head and the input capacitance of the preamplifier even if the LC pole is beyond the amplifier bandwidth as given above.

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			15	18	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		400		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.6			MHz
Write Current Range	I_W	1430Ω< R_{WC} < 5kΩ	10		35	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.72	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time	t_r/t_f	(L_H = 1µH)		6.5	9	ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		2	5	ns

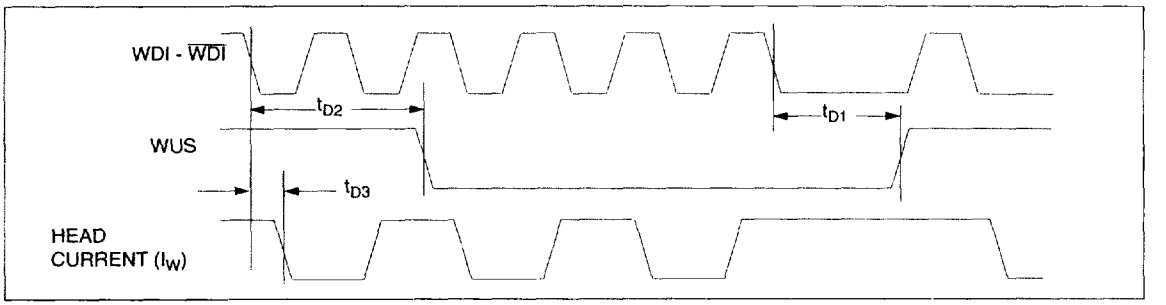

Figure 1: Write Mode Timing Diagram

ADDITIONAL CONNECTION DIAGRAMS