timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT.	TMS4C1025-80		TMS4C1025-10		TMS4C1025-12		UNIT
		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	175		210		255		ns
$t_{c(N)}$	Nibble-mode read or write cycle time	t_{NC}	40		45		50		ns
$t_{c(rdW)N}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	65		75		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	25	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		25		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		25		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	t_{RRH}	0		0		10		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		ALT. SYMBOL	TMS4C1025-80		TMS4C1025-10		TMS4C1025-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Notes 11 and 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		25		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		25		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		120		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		55		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.