ABRIDGED VERSION

SSI 32P4746/4746A

Read Channel with 1,7 ENDEC, 4-burst Servo

silicon systems®
A TDK Group Company

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4

DESCRIPTION

The SSI 32P4746/4746A devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 16 to 48 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor. For reduced clocking speeds, the 32P4746/4746A employs a dual-bit parallel interface to the controller.

Programmable functions of the SSI 32P4746/4746A devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4746/4746A utilize an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL:

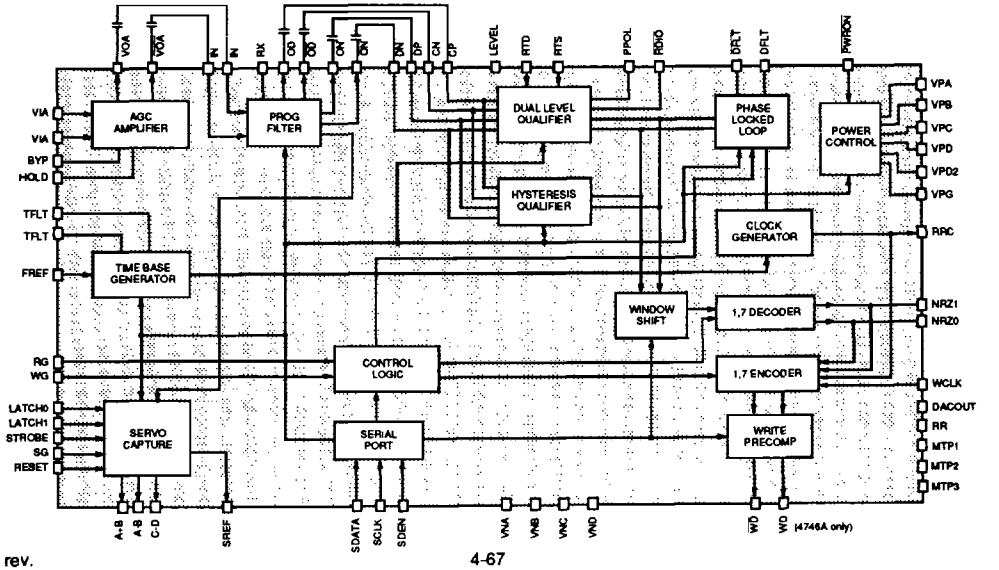
- **DAC controlled programmable data rates from 16 to 48 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation < 500 mW typical at 5V**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <1 mA)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR:

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Dual mode pulse qualification circuitry (user selectable)**
- **CMOS $\overline{\text{RDIO}}$ signal output for servo timing support**
- **Internal LOW-Z and fast decay timing**
- **0.8 ns max. pulse pairing at 48 Mbit/s using a 18 MHz sine wave input**

(continued)

BLOCK DIAGRAM



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FEATURES (continued)

SERVO CAPTURE:
- 4-burst servo capture with A-B, C-D and A+B outputs
- Internal hold capacitors
- Separate registers for *fc* and VTH during servo mode
- 4-bit DAC for servo AGC level control (0.75 to 1.0 Vp-p)

PROGRAMMABLE FILTER:
- Programmable cutoff frequency of 6 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% *fc* accuracy
- ± 2% maximum group delay variation to *fc*
- Less than 1.5% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:
- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:
- Fast acquisition phase lock loop with zero phase restart technique
- Dual-bit NRZ interface
- Integrated 1,7 RLL Encoder/Decoder
- Programmable decode window symmetry control via serial port
  - Window shift control TBD (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- TTL write data output - 32P4746
- Differential PECL write data output - 32P4746A
- Hard sector operation
- VCO and Synchronized Read Data test points

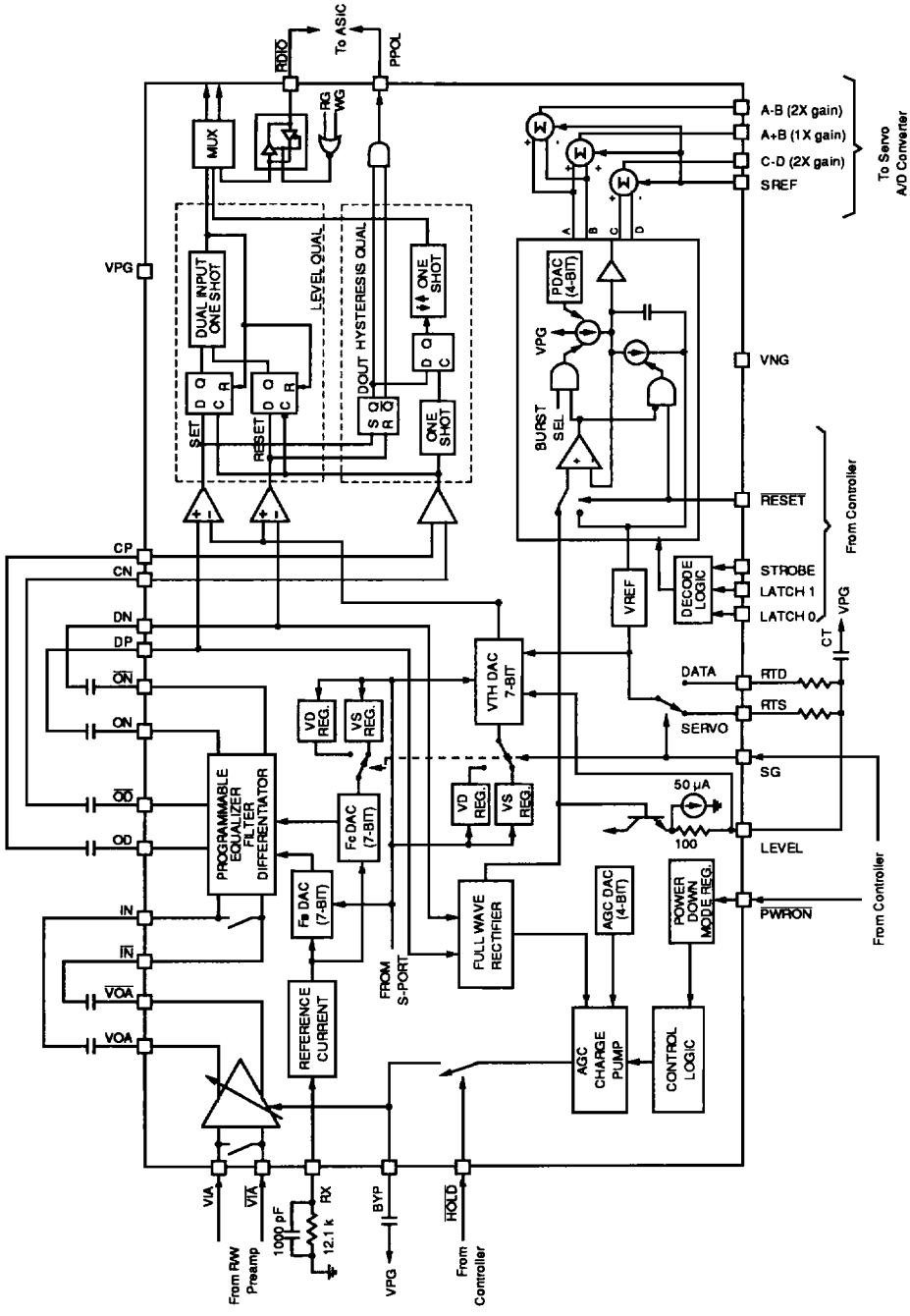


FIGURE 1: 32P4746/32P4746A Application Diagram

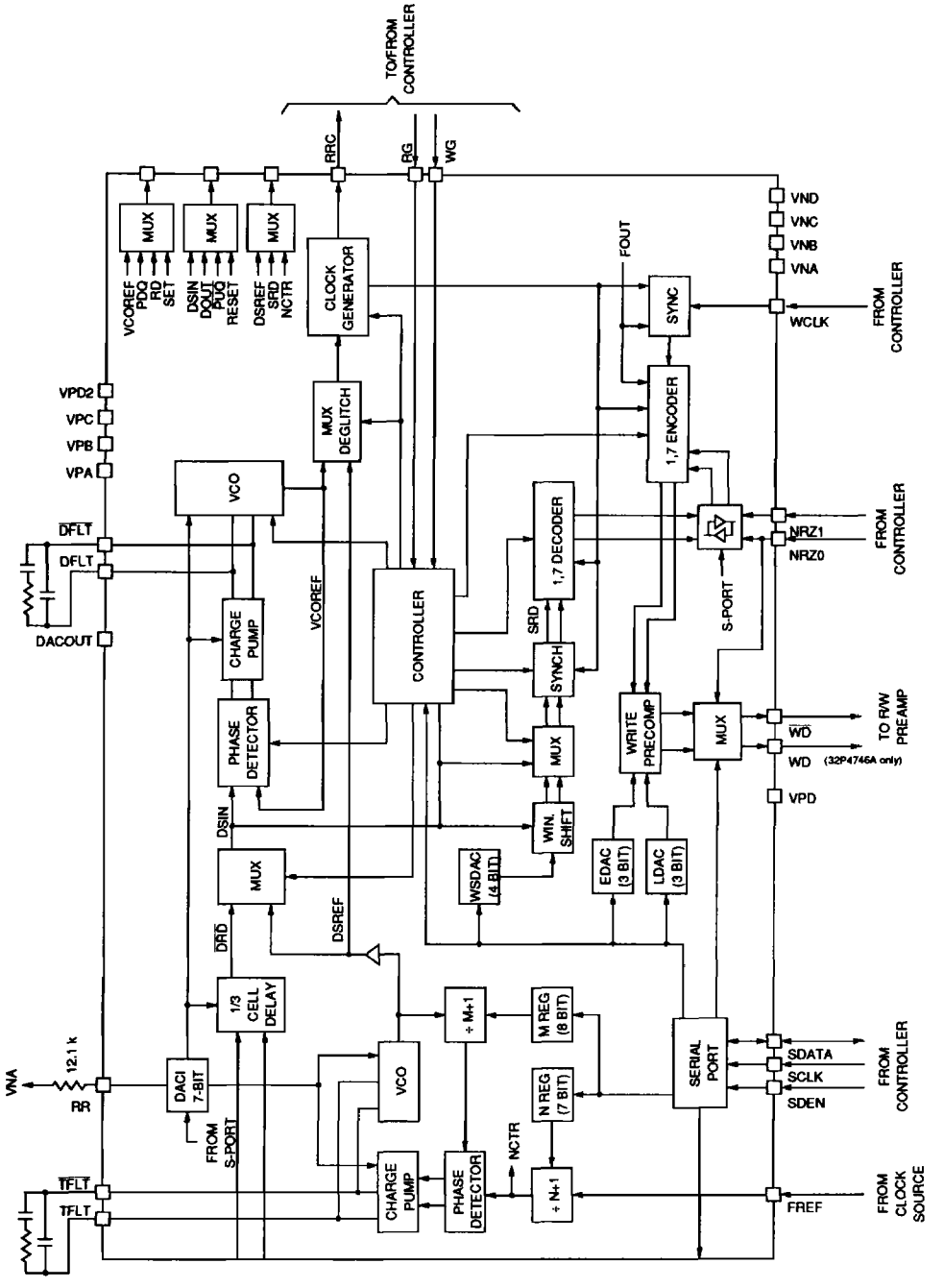
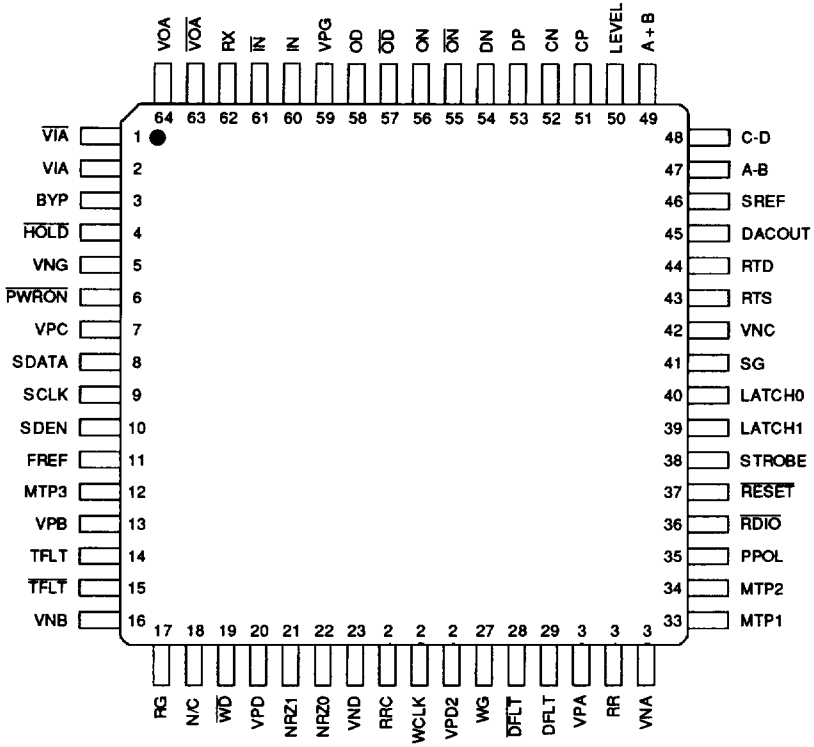


FIGURE 2: 32P4746/4746A Application Diagram

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



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64-Lead TQFP

4

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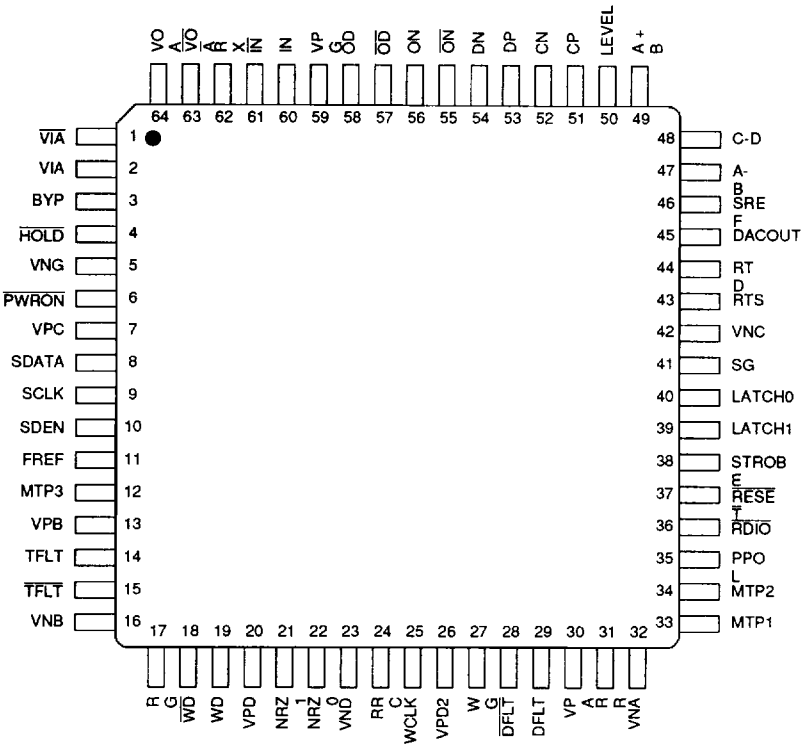

32P4746A
64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P4746	64-Lead TQFP	32P4746-CGT	32P4746-CGT
SSI 32P4746A	64-Lead TQFP	32P4746A-CGT	32P4746A-CGT

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