TELEDYNE PHILBRICK

Fast Settling FET Input Operational Amplifier

1430

The 1430 is a high speed, precision, hybrid operational amplifier that combines fast settling times, low bias currents, high slew rate, wide bandwidth, and good phase margin. A guaranteed settling time of 200nsec (for a full 10V step settling to ± 1mV) and a design particularly suited for inverting applications make the 1430 an ideal output amplifier for fast 12 bit D/A converters. Other applications include sample-hold amplifiers and radar pulse amplifiers. The standard 1430 is fully specified for − 25°C to + 85°C operation. With a 20°C/Watt heat sink, the 1430 is specified for − 55°C to + 125°C operation. For military/aerospace applications, the 1430-83 is screened to the high reliability requirements of MIL-STD-883, Method 5008.

The 1430 was carefully designed so its output settling time would not vary appreciably with closed loop gain (see Figure 1 below). This is particularly important for applications as a current to voltage converter with a high speed current-output DAC (see Figure 3). Although designed primarily for inverting applications, the 1430 will accept up to ± 3V dc at its noninverting input for applications requiring an offset. For applications requiring ultra high speed noninverting operation, we recommend the Teledyne Philbrick 1435. The 1430 requires only a feedback capacitor for stability at closed-loop gains of unity and above. In applications where the low ± 2mV initial offset voltage must be trimmed, an external 1kΩ potentiometer may be used as shown in Figure 4.

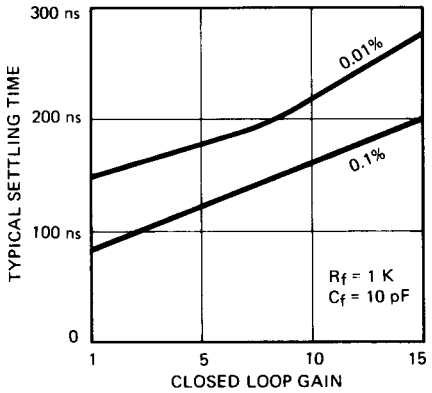
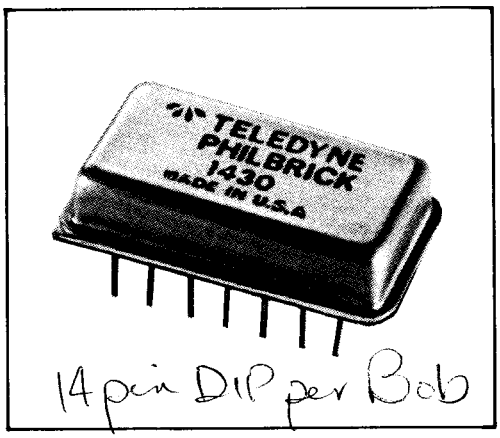


Figure 1. Settling Time vs Closed Loop Gain



14 pin DIP per Bob

FEATURES

- 200nsec Maximum Settling Time 10V Step to ± 0.01%
- 100MHz Gain Bandwidth Product
- 500V/μsec Slew Rate
- ± 50mA Output Current
- − 55°C to + 125°C Operation
- Optional MIL-STD-883 Screening

APPLICATIONS

- Voltage-Output DAC's
- Sample-Hold Amplifiers
- Pulse Amplifiers
- Wideband Amplifiers

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SPECIFICATIONS Inverting circuits only, V_{CC} = ±15 V unless otherwise stated
(Operation above +85 °C requires 20 °C/watt heat sink)

	@ +25 °C Typical	@ +25 °C Guaranteed	@ -55 °C to +125 °C Typical
OUTPUT RANGE			
Voltage (Peak)	---	±10 V	±9 V
Current	---	±50 mA	±25 mA
VOLTAGE GAIN (dc, Open Loop)			
Rated Load	114 dB	106 dB	100 dB
FREQUENCY RESPONSE (Inverting Only)			
Small Signal (Gain-Bandwidth Product) ①	100 MHz	80 MHz	50 MHz
Small Signal (Unity Gain Open Loop)	60 MHz	---	---
Max Sine Power Out (3 to 5% distortion)	---	5 MHz	2.5 MHz
Max Peak to Peak Out (Triangle Wave)	---	8 MHz	4.0 MHz
Slew Rate	500 V/μsec	---	500 V/μsec
Settling Time ②			
10 V Step to within 100 mV (1%)	70 nsec	---	---
10 mV (0.1%)	100 nsec	---	---
1 mV (0.01%)	---	200 nsec	300 nsec
5 V Step to within 50 mV (1%)	70 nsec	---	---
5 mV (0.1%)	100 nsec	---	---
0.5 mV (0.01%)	180 nsec	---	---
2 V Step to within 20 mV (1%)	80 nsec	---	---
2 mV (0.1%)	100 nsec	---	---
0.2 mV (0.01%)	240 nsec	---	---
Overload Recovery Time (10 V Step Input)	10 μsec	---	---
Max Capacitive Load without Oscillation	---	100 pF	50 pF
INPUT VOLTAGE RANGE			
Common Mode for DC Linear Operation	±3 V	---	---
Common Mode Fault	---	±18 V	---
Differential (Between Inputs)	---	36 V	---
INPUT OFFSET VOLTAGE			
Initial (without external trim) @ 25 °C	±0.5 mV	±2 mV	---
Zero Adjustment (Optional)	---	1 kΩ pot	---
Vs. Temperature (Avg. -25 °C to +85 °C)	25 μV/°C	75 μV/°C	100 μV/°C
Power Supply Rejection Ratio	---	3 mV/V	---
INPUT BIAS CURRENT			
Initial @ 25 °C	-150 pA	-500 pA	---
Vs. Temperature (Avg. -55 °C to 125 °C) ③ ④	Doubles each 10 °C		---
INPUT IMPEDANCE @ dc			
Differential	$10^{11}\ \Omega \parallel 3$ pF	---	---
NOISE (Referred to Input)			
Flicker (0.016 to 1.6 Hz)			
Voltage (peak-to-peak)	10 μV	---	---
Current (peak-to-peak)	3 pA	---	---
Midband (1.6 to 160 Hz)			
Voltage (rms)	2.5 μV	---	---
Current (rms)	2 pA	---	---
Highband (160 Hz to 16 kHz)			
Voltage (rms)	2 μV	---	---
Wideband (1.6 Hz to 1.6 MHz)			
Voltage (rms)	9 μV	---	---
POWER REQUIREMENTS			
Nominal Supply Voltage	---	±15 V	---
Voltage Range	±10 to ±18 V	---	---
Current: Quiescent	---	±25 mA	±30 mA
Current: Full Load	---	±75 mA	---
TEMPERATURE RANGE			
Operating ④	---	-55 °C to +125 °C	---
Storage	---	-65 °C to +150 °C	---
MTBF @ 85 °C ⑤	≥ 694,000 hrs		

① @ 1 MHz
② $R_i = R_f$ = 1 kΩ
C_f = 15 pF for 0.01%, 10 pF for 0.1%
R_L = 250 Ω C_L = 10 pF
③ Bias Current @ +85 °C is 10 nA, typ.
Bias Current @ +125 °C is 1 μA, typ.
④ With 20 °C/watt heat sink above 85 °C
⑤ Ground Benign Per Mil Handbook 217B

The input circuits of these units are protected to ±V_{CC}. Output circuits are short-circuit protected to ground.

Recommended Power Supply: Teledyne Philbrick Model 2211

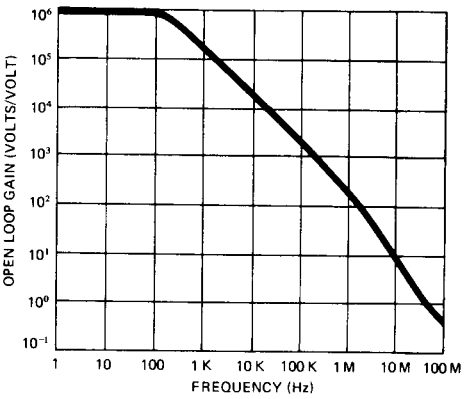


Figure 2. Open Loop Gain vs. Frequency

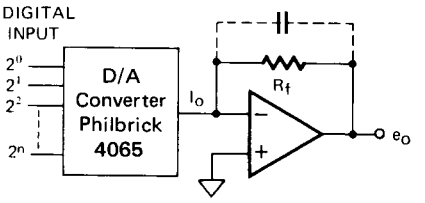


Figure 3. Output Amplifier for D/A Converter

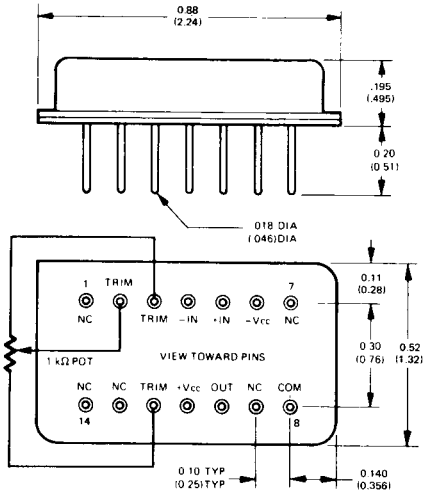


Figure 4. Mechanical Configuration

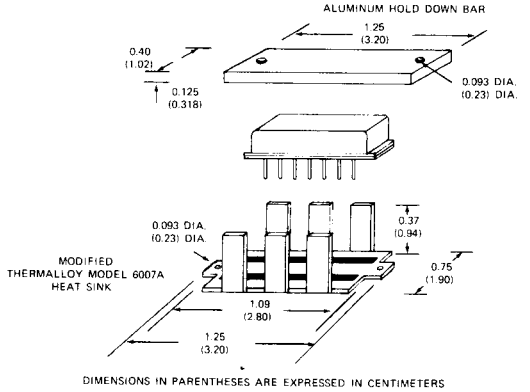


Figure 5. 1430/1430-83 Heat Sink Assembly

SETTLING TIME – DEFINED

Settling Time is the important specification when handling fast (sub-microsecond rise time), precision (0.1% or better amplitude accuracy) pulses.

Settling Time is defined as the total time required after application of an input step (of voltage or current) for a circuit's output to stay within a specified error band relative to the final value of the output. (See Figure 6).

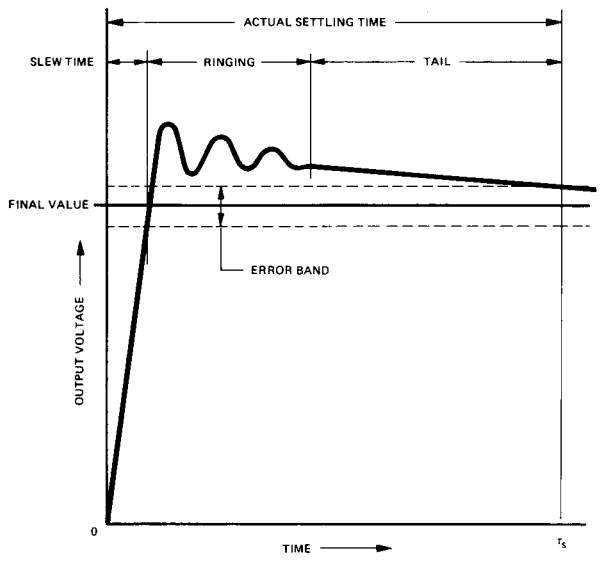


Figure 6. The Composition of Settling Time

Settling time cannot be predicted from bandwidth and/or slewing rate since a step input, when applied to the amplifier, will cause the output to slew at its maximum rate toward the final value. The output will usually overshoot slightly and "ring" as it settles toward the final value.

Settling time, therefore, includes not only the slew rate, but the ringing time as well. The error band is generally expressed as a percentage of the desired output level, i.e., 0.01% or 1 mV for a 10 volt amplifier.

When observing settling time on an oscilloscope the amplifier may appear to have settled (ringing has ceased) but the value is still outside the error band. It may take a few seconds for this to drift within the error band. This phenomenon is called a "long tail" and is often a source of error. The long tails make it virtually impossible to calculate settling time by using slew rate, and ringing characteristics as the sole factors. It should also be realized that knowing the settling time to a given accuracy (say 0.1%) is in no way helpful in extrapolating the settling time to a higher accuracy such as 0.01% and vice-versa.

If settling time cannot be extrapolated, calculated, guessed, or ignored, it must be measured. This can be a difficult and misleading task if the proper procedures are not followed precisely. Figure 7 illustrates the settling characteristics of the 1430 using the test circuit given in Figure 8A.

SETTLING TIME – MEASURED

It is not possible to look for 0.1% or 0.01% accuracy directly from an oscilloscope just by looking at the output waveform. At high sensitivity (for resolution), a 10 volt full scale signal will greatly overdrive the scope's input amplifier to the point that its recovery time will probably be much worse than the settling time of interest.

The test circuit shown in Figure 8 is an excellent method for fast settling time measurements. In this circuit R_{in} and R_f are matched to R_{in}' and R_f'. When the AUT* has settled to ±0.01% of a 20 V step (±2 mV) the settling point (see Figure 8) will have settled to ±1 mV. To minimize capacitance at the settling point an FET follower with less than 1 pF input capacitance (3N128) is used. The two Schottky Diodes on the settling point act as limiters without storing a charge and also have little capacitive loading effect. Thus the lag due to capacitance (3 pF) in combination with $R_f = R_i = 1\ k\Omega$ can be as low as 1.5 nanoseconds.

The diode gate and R1, R2 network forms an ideal square wave source for testing since a square wave with significant ripple can cause (unfairly) an amplifier to look bad. Resistors R1 and R2 can be trimmed for desired output.

This scheme permits you to look quite directly at the true AUT output, yet avoids most of the drawbacks usually entailed because the output signal is subtracted from the input signal.

*AUT – Amplifier Under Test

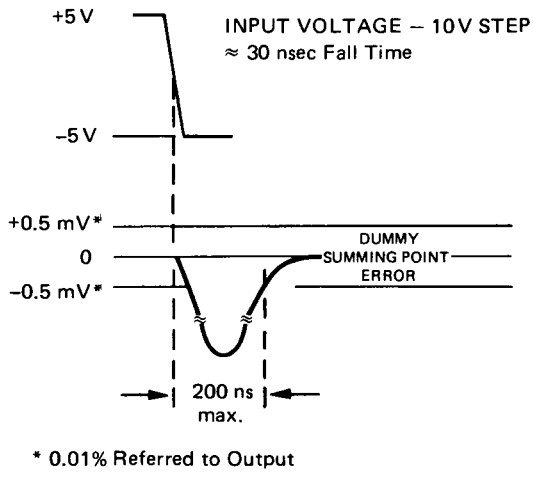
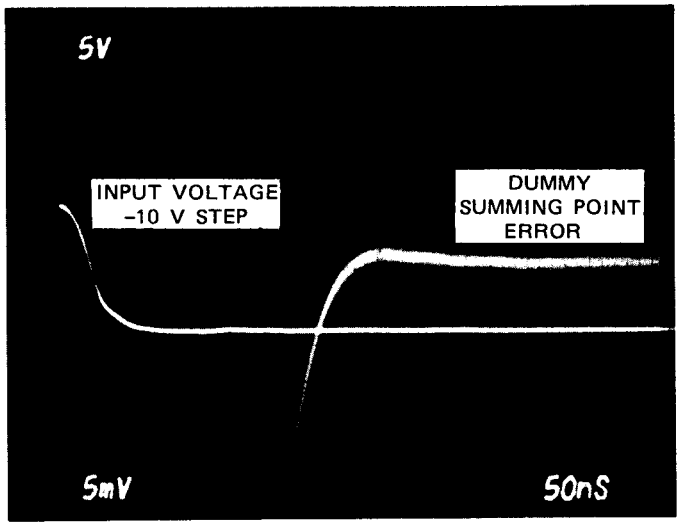


Figure 7. Settling Time of Model 1430/1430-83



See Figure 8 – Test Circuit and Clipping Amplifier. Since the Clipping Amplifier has a gain of 5, 5 mV/division = 1 mV/division on dummy junction. The dummy summing junction has a gain of 1/2, thus settling to 1/2 mV equals 1 mV (0.01%).

Measuring settling time to 0.01% requires a clipping amplifier to prevent overloading the oscilloscope's input. The circuit shown in Figure 8B is excellent for this purpose.

A good question here might be: Why can't you just connect the 3N128 buffer to the summing point and watch that point settle? There are two good reasons; the feedback capacitance C_f and the input capacitance C_{in}. Many fast settling amplifiers give best results when some finite amount of feedback capacitance is used. The effect of this can be seen at the settling point, but not at the summing point. Also, some good amplifiers have significant input capacitance due to "Miller capacitance" or to feedforward capacitors. If this is the case, it is possible to see the true settling only at the settling point. So you can test for settling at the summing point so long as the answer is the same as that at the settling point; but if the answer isn't the same, you shouldn't.

An amplifier is of little use for precision work if its output for a 400 nanosecond pulse rises in 10 nanoseconds (1000 V/μsec slew for 10 V output step), overshoots 20%, rings for 100 nanoseconds, and due to a tail won't arrive permanently within 0.01% of its final value for another 600 nanoseconds. A 1430 will be within 0.01% of final value within 200 nanoseconds.

125 °C OPERATION

In order to operate the 1430/1430-83 from +85 to +125 °C, it must be used with a 20 °C per watt heat sink. A suggested device is the Thermalloy Model 6007A*, modified as shown in Figure 8 by removing the two fins at each end and adding the aluminum "hold down bar". Heat sink compound must be used between the 1430/1430-83 and the heat sink.

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Dallas, Texas 75234

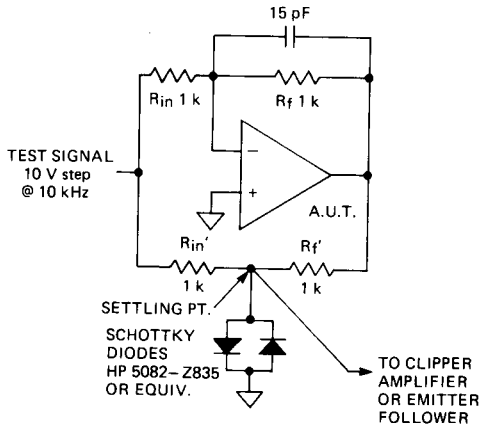

Figure 8A. Test Circuit

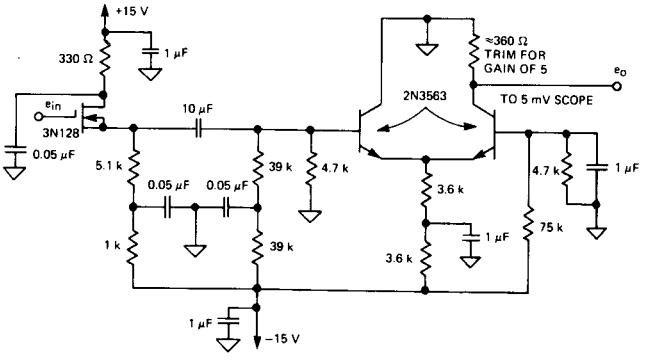

Figure 8B. Clipping Amplifier

SCREENING ACCORDING TO MIL-STD-883 METHOD 5008		
Test	**Methods and Conditions**	**Purpose**
Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
Stabilization Bake	Method 1008, Condition C 24 hours at 150 °C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
Constant Acceleration	Method 2001, Condition B Y_1 Axis, 10,000 g	Removes potential failures due to weak wire or chip bonding.
Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hr. at 30 psi; Leak Rate $< 5 \times 10^{-7}$ cc/sec; Gross Leak, Condition C_1, no bubbles	Verifies Integrity of hermetic package
Burn In	Method 1015 Condition B 160 hours at 125 °C	Reduces infant mortality rate
Temperature Cycling	Method 1010, Condition B 10 cycles from $-55\,^{\circ}C\ ^{+0\,^{\circ}C}_{-5\,^{\circ}C}$ to $+125\,^{\circ}C\ ^{+3\,^{\circ}C}_{-0\,^{\circ}C}$	Removes potential failures due to weak wire or chip bonding.
External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.