| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Added footnotes 14/, 15/, and 16/ to table I. Made changes to footnote 12/ in table I. Corrected pin name on pin 66 in figure 2. Corrected pin number in figure 5. Made editorial changes throughout. - LTG | 00-10-23 | Thomas M. Hess |
| B | Update boilerplate to MIL-PRF-38535 requirements. - LTG | 01-03-28 | Thomas M. Hess |
| C | Add appendix A to document. - LTG | 01-06-14 | Thomas M. Hess |
| D | Add device type 02. - LTG | 02-07-18 | Thomas M. Hess |
| E | Update boilerplate to current MIL-PRF-38535 requirements, to include updating the RHA boilerplate paragraphs. Correct title to accurately describe device function. - CFS | 07-07-30 | Thomas M. Hess |

| REV | E | E | E | E | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | 35 | 36 | 37 | 38 | | | | | | | | | | | | | | | | |
| REV | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |

| REV STATUS | REV | E | E | E | E | E | E | E | E | E | E | E | E | E |
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| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

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**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
99-03-05

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, RADIATION HARDENED MICROPROCESSOR, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-98583** |

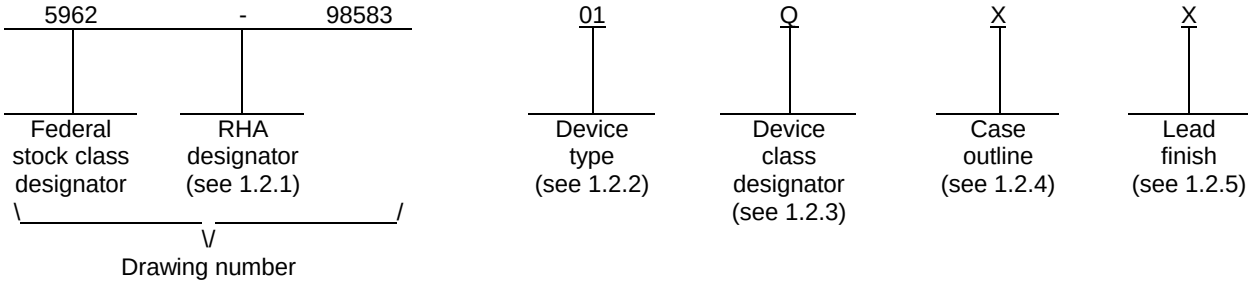
SHEET 1 OF 38

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | | Circuit function |
|---|---|---|---|
| 01 | UT80C196KD or UT80CRH196KD | 1/ | Mil-Temp, MCS-96 Based Microcontroller |
| 02 | UT80C196KD or UT80CRH196KD | 1/ | Extended Industrial Temp, MCS-96 Based Microcontroller |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | See figure 1 | 68 | Quad flatpack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

---

1/ The RH in the Generic number signifies the radiation hardened version of the device.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| DC supply voltage ($V_{DD}$) | -0.3 V to +6.0 V |
| Voltage on any pin ($V_{I/O}$) | -0.3 V to $V_{DD}$ +0.3 V |
| DC input current ($I_I$) | ±10 mA |
| Storage temperature ($T_{STG}$) | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 4 W |
| Maximum junction temperature ($T_J$) | +175°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | 2°C/W 2/ |

1.4 Recommended operating conditions.

| | |
|---|---|
| DC supply voltage ($V_{DD}$) | 4.5 V to 5.5 V |
| Temperature range ($T_C$) | -55°C to +125°C (Device type 01) |
| Temperature range ($T_C$) | -40°C to +125°C (Device type 02) |
| DC input voltage ($V_{IN}$) | 0 V to $V_{DD}$ |
| High level input voltage (XTAL1) ($V_{IH}$) | 0.7$V_{DD}$ |
| Low level input voltage (XTAL1) ($V_{IL}$) | 0.3$V_{DD}$ |
| Min high level input voltage ($V_{IH}$) | 2.2 V 3/ |
| Max low level input voltage ($V_{IL}$) | 0.8 V 3/ |

1.5 Radiation features.

| | |
|---|---|
| Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) | 100 Krads(Si) |
| Single event phenomenon | |
| effective linear energy threshold, (LET) no upset | 25 MeV-cm$^2$/mg 4/ |
| Neutron fluence | 1.0E14 n/cm$^2$ 4/ |

1.6 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | 95 percent |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Per MIL-STD-883, method 1012.
3/ Except XTAL1 and $\overline{\text{RESET}}$.
4/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Load circuit and waveforms. The load circuit and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Low level input voltage (except XTAL1, RESET) | $V_{IL}$ | | 1, 2, 3 | All | | 0.8 | V |
| High level input voltage (except XTAL1, RESET) | $V_{IH}$ | | 1, 2, 3 | All | 2.2 | | V |
| High level input voltage (XTAL1) | $V_{IH1}$ | | 1, 2, 3 | All | $.7V_{DD}$ | | V |
| Low level input voltage (XTAL1) | $V_{IL1}$ | | 1, 2, 3 | All | | $.3V_{DD}$ | V |
| High level output voltage (Standard outputs) 3/ | $V_{OH}$ | $I_{OH}$ = -200 µA (CMOS) 4/ | 1, 2, 3 | All | $V_{DD}$-.3 | | V |
| | | $I_{OH}$ = -4.0 mA (TTL) | | | 3.8 | | |
| High level output current (Open drain outputs with pullups) 5/ | $I_{OH}$ | $V_{OH} = V_{DD}$ - .3 4/ | 1, 2, 3 | All | -20 | | µA |
| | | $V_{OH} = V_{DD}$ - .9 | | | -60 | | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 200 µA (CMOS) 4/ | 1, 2, 3 | All | | 0.3 | V |
| | | $I_{OL}$ = 4.0 mA (TTL) | | | | 0.4 | |
| Positive going threshold RESET | $V_{T+}$ | | 1, 2, 3 | All | $.5V_{DD}$ | $.7V_{DD}$ | V |
| Negative going threshold RESET | $V_{T-}$ | | 1, 2, 3 | All | $.2V_{DD}$ | $.4V_{DD}$ | V |
| Typical range of Hysteresis RESET 4/ | $V_H$ | | 1, 2, 3 | All | .9 | | V |
| Pullups on ADV, RD, RESET, Port 1, Port 2.0, 2.6, 2.7, AD0-15, WR, WRL, BHE, ALE, CLKOUT 4/ | $R_{PU}$ | $V_{CC}$ = 5.5 V, $V_{IN} = V_{SS}$ | 1, 2, 3 | All | 6.9 | 36.7 | KΩ |
| Pulldown on INST, NMI, HSO.0-HSO.3, P2.5 4/ | $R_{PD}$ | $V_{CC}$ = 5.5 V, $V_{IN} = V_{DD}$ | 1, 2, 3 | All | 3.7 | 27.5 | KΩ |
| Logical 0 input current (Test mode entry) 6/ | $I_{IL}$ | $V_{IN} = V_{IH}$ | 1, 2, 3 | All | -550 | -120 | µA |
| I/O leakage current, standard inputs and outputs | $I_{LI}$ | $V_{IN} = V_{SS}$ or $V_{DD}$ | 1, 2, 3 | All | -5 | +5 | µA |
| I/O leakage current, with pullups 7/ | $I_{LI1}$ | $V_{IN} = V_{SS}$ | 1, 2, 3 | All | -800 | -150 | µA |
| I/O leakage current, with pulldowns 8/ | $I_{LI2}$ | $V_{IN} = V_{DD}$ | 1, 2, 3 | All | 200 | 1500 | µA |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Power supply current in reset | $I_{DDRESET}$ | CLK @ 20 MHz, $\overline{RESET} \le V_{IL}$ | 1, 2, 3 | All | | 65 | mA |
| Active power supply current | $AI_{DD}$ | CLK @ 20 MHz, typical Program flow | 1, 2, 3 | All | | 110 | mA |
| Quiescent power supply current | $QI_{DD}$ | | 1, 3 | All | | 20 | µA |
| | | | 2 | All | | 1000 | µA |
| | | M, D, P, L, and R | 1 | All | | 1000 | µA |
| Power supply current in power down | $I_{DDPD}$ | CLK @ 20MHz, no active I/O | 1, 2, 3 | All | | 6 | mA |
| Power supply current in idle mode | $I_{DDIDLE}$ | CLK @ 20 MHz, no active I/O | 1, 2, 3 | All | | 55 | mA |
| Pin capacitance | $C_{I/O}$ | @ 1 MHz, 25°C 4/ See 4.4.1b | 4 | All | | 15 | pF |
| Short circuit output current, except for pins noted in Note 10 | $I_{OS}$ | $V_{DD}$ = 5.5 V 4/ 9/ | 1, 2, 3 | All | -100 | 130 | mA |
| Short circuit output current, for pins noted in Note 10 | $I_{OS1}$ | $V_{DD}$ = 5.5 V 4/ 9/ 10/ | 1, 2, 3 | All | -200 | 250 | mA |
| Functional tests | | See 4.4.1c | 7, 8 | All | | | |
| Address VALID to READY setup 4/ | $t_{AVYV}$ | See figure 4. | 9, 10, 11 | All | | $2T_{OSC}$ -30 | ns |
| Non-READY time 4/ | $t_{YLYH}$ | | 9, 10, 11 | All | No upper limit | | ns |
| READY hold after CLKOUT low 4/ 11/ | $t_{CLYX}$ | | 9, 10, 11 | All | 0 | $2T_{OSC}$ -20 | ns |
| READY hold after ALE low 4/ 11/ | $t_{LLYX}$ | | 9, 10, 11 | All | $T_{OSC}$ | $3T_{OSC}$ -20 | ns |
| Address valid to BUSWIDTH setup 4/ | $t_{AVGV}$ | | 9, 10, 11 | All | | $2T_{OSC}$ -30 | ns |
| BUSWIDTH hold after CLKOUT low 4/ | $t_{CLGX}$ | | 9, 10, 11 | All | 0 | | ns |
| Address valid to input data valid 4/ 12/ | $t_{AVDV}$ | | 9, 10, 11 | All | | $3T_{OSC}$ -29 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $\overline{RD}$ Active to input data valid 12/ | $t_{RLDV}$ | See figure 4. | 9, 10, 11 | All | 5 4/ | $T_{OSC}$-26 | ns |
| CLKOUT low to input data valid 4/ | $t_{CLDV}$ | | 9, 10, 11 | All | 5 | $T_{OSC}$-26 | ns |
| End of $\overline{RD}$ to input data float 4/ | $t_{RHDZ}$ | | 9, 10, 11 | All | 0 | $T_{OSC}$-10 | ns |
| Data hold after $\overline{RD}$ inactive 4/ | $t_{RXDX}$ | | 9, 10, 11 | All | 0 | $T_{OSC}$-10 | ns |
| Frequency on XTAL1 4/ | $f_{OSC}$ | | 9, 10, 11 | All | 1 13/ | 20 14/ | MHz |
| XTAL1 period ($1/f_{OSC}$) 4/ | $T_{OSC}$ | | 9, 10, 11 | All | 50 14/ | 1000 13/ | ns |
| XTAL1 high to CLKOUT high or low | $t_{XHCH}$ | | 9, 10, 11 | All | 0 | 25 | ns |
| CLKOUT cycle time 14/ | $t_{CLCL}$ | | 9, 10, 11 | All | $2T_{OSC}$ | | ns |
| CLKOUT high period 4/ | $t_{CHCL}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| CLKOUT falling edge to ALE rising | $t_{CLLH}$ | | 9, 10, 11 | All | -5 | +15 | ns |
| ALE falling edge to CLKOUT rising 4/ | $t_{LLCH}$ | | 9, 10, 11 | All | -10 | +10 | ns |
| ALE cycle time 12/ 14/ | $t_{LHLH}$ | | 9, 10, 11 | All | $4T_{OSC}$ | | ns |
| ALE high period 4/ | $t_{LHLL}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+15 | ns |
| Address setup to ALE falling edge 4/ | $t_{AVLL}$ | | 9, 10, 11 | All | $T_{OSC}$-15 | | ns |
| Address hold after ALE falling edge | $t_{LLAX}$ | | 9, 10, 11 | All | $T_{OSC}$-20 | $T_{OSC}$+5 | ns |
| ALE falling edge to $\overline{RD}$ falling edge | $t_{LLRL}$ | | 9, 10, 11 | All | $T_{OSC}$-5 | $T_{OSC}$+10 | ns |
| $\overline{RD}$ low to CLKOUT falling edge | $t_{RLCL}$ | | 9, 10, 11 | All | -5 | +10 | ns |
| $\overline{RD}$ low period 12/ | $t_{RLRH}$ | | 9, 10, 11 | All | $T_{OSC}$-5 | | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $\overline{RD}$ rising edge to ALE rising edge 4/ 15/ | $t_{RHLH}$ | See figure 4. | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| $\overline{RD}$ low to address float 4/ | $t_{RLAZ}$ | | 9, 10, 11 | All | -5 | +5 | ns |
| ALE falling edge to $\overline{WR}$ falling edge 4/ | $t_{LLWL}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| CLKOUT low to $\overline{WR}$ falling edge | $t_{CLWL}$ | | 9, 10, 11 | All | -5 | +10 | ns |
| Data stable to $\overline{WR}$ rising edge 12/ | $t_{QVWH}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| CLKOUT high to $\overline{WR}$ rising edge 4/ | $t_{CHWH}$ | | 9, 10, 11 | All | -10 | +15 | ns |
| $\overline{WR}$ low period 4/ 12/ | $t_{WLWH}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | | ns |
| Data hold after $\overline{WR}$ rising edge 4/ | $t_{WHQX}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| $\overline{WR}$ rising edge to ALE rising edge 4/ 15/ | $t_{WHLH}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| $\overline{BHE}$, INST after $\overline{WR}$ rising edge 4/ | $t_{WHBX}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| AD8-15 HOLD after $\overline{WR}$ rising 4/ 16/ | $t_{WHAX}$ | | 9, 10, 11 | All | $T_{OSC}$-25 | | ns |
| $\overline{BHE}$, INST after $\overline{RD}$ rising edge 4/ | $t_{RHBX}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| AD8-15 HOLD after $\overline{RD}$ rising 4/ 16/ | $t_{RHAX}$ | | 9, 10, 11 | All | $T_{OSC}$-25 | | ns |
| Address valid to $\overline{EDACEN}$ valid 4/ | $t_{AVENV}$ | | 9, 10, 11 | All | | $2T_{OSC}$ -30 | ns |
| $\overline{EDACEN}$ hold after ALE high 4/ | $t_{LHENX}$ | | 9, 10, 11 | All | 0 | | ns |
| Address valid to EDAC input valid 4/ 12/ | $t_{AVEV}$ | | 9, 10, 11 | All | | $3T_{OSC}$ -29 | ns |
| EDAC hold after $\overline{RD}$ inactive 4/ | $t_{RXEX}$ | | 9, 10, 11 | All | 0 | $T_{OSC}$-10 | ns |
| EDAC output stable to $\overline{WR}$ rising 4/ 12/ | $t_{EVWH}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |
| EDAC output hold after $\overline{WR}$ rising 4/ | $t_{WHEX}$ | | 9, 10, 11 | All | $T_{OSC}$-10 | $T_{OSC}$+10 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS | | | | | | | |
| Oscillator Frequency | $f_{osc}$ | See figure 4. | 9, 10, 11 | All | 1 4/ | 20 | MHz |
| Oscillator Period ($1/f_{osc}$) | $T_{OSC}$ | | 9, 10, 11 | All | 50 | 1000 4/ | ns |
| High time 4/ | $t_{OSCH}$ | | 9, 10, 11 | All | 17 | | ns |
| Low time 4/ | $t_{OSCL}$ | | 9, 10, 11 | All | 17 | | ns |
| Rise time 17/ | $t_{OSCR}$ | | 9, 10, 11 | All | | 10 | ns |
| Fall time 17/ | $t_{OSCF}$ | | 9, 10, 11 | All | | 10 | ns |
| $\overline{HOLD}$/$\overline{HLDA}$ TIMINGS | | | | | | | |
| $\overline{HOLD}$ setup 4/ | $t_{HVCH}$ | See figure 4. | 9, 10, 11 | All | 25 | | ns |
| CLKOUT low to $\overline{HLDA}$ low 4/ | $t_{CLHAL}$ | | 9, 10, 11 | All | -15 | 15 | ns |
| CLKOUT low to $\overline{BREQ}$ low 4/ | $t_{CLBRL}$ | | 9, 10, 11 | All | -15 | 15 | ns |
| $\overline{HLDA}$ low to address float 4/ | $t_{HALAZ}$ | | 9, 10, 11 | All | | 10 | ns |
| $\overline{HLDA}$ low to BHE, INST, RD, WR driven weakly 4/ | $t_{HALBZ}$ | | 9, 10, 11 | All | | 15 | ns |
| CLKOUT low to $\overline{HLDA}$ high 4/ | $t_{CLHAH}$ | | 9, 10, 11 | All | -15 | 15 | ns |
| CLKOUT low to $\overline{BREQ}$ high 4/ | $t_{CLBRH}$ | | 9, 10, 11 | All | -15 | 15 | ns |
| $\overline{HLDA}$ high to address no longer float 4/ | $t_{HAHAX}$ | | 9, 10, 11 | All | -15 | | ns |
| $\overline{HLDA}$ high to BHE, INST, RD, WR valid 4/ | $t_{HAHBV}$ | | 9, 10, 11 | All | -10 | | ns |
| CLKOUT low to ALE high 4/ | $t_{CLLH}$ | | 9, 10, 11 | All | -5 | 15 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| SERIAL PORT TIMING | | | | | | | |
| Serial port clock period (BRR = 8002H) 14/ | $t_{XLXL}$ | See figure 4. | 9, 10, 11 | All | $6T_{OSC}$ | | ns |
| Serial port clock falling edge to rising edge (BRR = 8002H) 4/ | $t_{XLXH}$ | | 9, 10, 11 | All | $4T_{OSC}$ -50 | $4T_{OSC}$ +50 | ns |
| Serial port clock period (BRR = 8001H) 14/ | $t_{XLXL}$ | | 9, 10, 11 | All | $4T_{OSC}$ | | ns |
| Serial port clock falling edge to rising edge (BRR = 8001H) 4/ | $t_{XLXH}$ | | 9, 10, 11 | All | $2T_{OSC}$ -50 | $2T_{OSC}$ +50 | ns |
| Output data valid to clock rising edge 4/ | $t_{QVXH}$ | | 9, 10, 11 | All | $2T_{OSC}$ -50 | | ns |
| Output data hold after clock rising edge 4/ | $t_{XHQX}$ | | 9, 10, 11 | All | $2T_{OSC}$ -50 | | ns |
| Next output data valid after clock rising edge 4/ | $t_{XHQV}$ | | 9, 10, 11 | All | | $2T_{OSC}$ +50 | ns |
| Input data setup to clock rising edge 4/ | $t_{DVXH}$ | | 9, 10, 11 | All | $T_{OSC}$+50 | | ns |
| Input data hold after clock rising edge 4/ | $t_{XHDX}$ | | 9, 10, 11 | All | 0 | | ns |
| Last clock rising to output float 4/ | $t_{XHQZ}$ | | 9, 10, 11 | All | $2T_{OSC}$ -10 | $2T_{OSC}$ +10 | ns |

1/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.

2/ Unless otherwise specified, the temperature conditions for device type 01 is -55°C to +125°C, and the temperature conditions for device type 02 is -40°C to +125°C.

3/ For standard outputs not covered by the $I_{OH}$ specification.

4/ Tested only at initial qualification, and after any design or process changes which may affect this characteristic.

5/ Open-drain outputs include Port 1, P2.6 and P2.7.

6/ Test modes are entered at the $\overline{\text{RESET}}$ rising edge by applying $V_{IL}$ to one or more of the following pins TXD, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and HLDA. To avoid entering a test mode, ensure that these pins remain above $V_{IH}$ during the rising edge of RESET.

7/ Inputs/outputs with pullup resistors include: $\overline{\text{RESET}}$, Port 1, Port 2.0, P2.6, P2.7, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, AD0-15, $\overline{\text{RD}}$, ALE, and CLKOUT.

8/ Inputs/outputs with pulldown resistors include: NMI, HSO.0- HSO.3, P2.5, and INST.

TABLE IA. Electrical performance characteristics - Continued.

9/ Not more than one output may be shorted at a time for maximum duration of one second.

10/ The $I_{OS1}$ specification applies to pins $\overline{RESET}$, $\overline{BHE}$, $\overline{RD}$, and CLKOUT.

11/ If maximum is exceeded, additional wait state occurs.

12/ If wait states are used, add 2 $T_{OSC}$ *N, where N = number of wait states.

13/ Low speed tests performed at 5 MHz. 1 MHz operation is guaranteed by design.

14/ These specifications are verified using functional vectors (strobed) only.

15/ Assuming back-to-back bus cycles.

16/ 8-bit only.

17/ Supplied as a design limit but not guaranteed or tested.

TABLE IB. SEP test limits. 1/ 2/

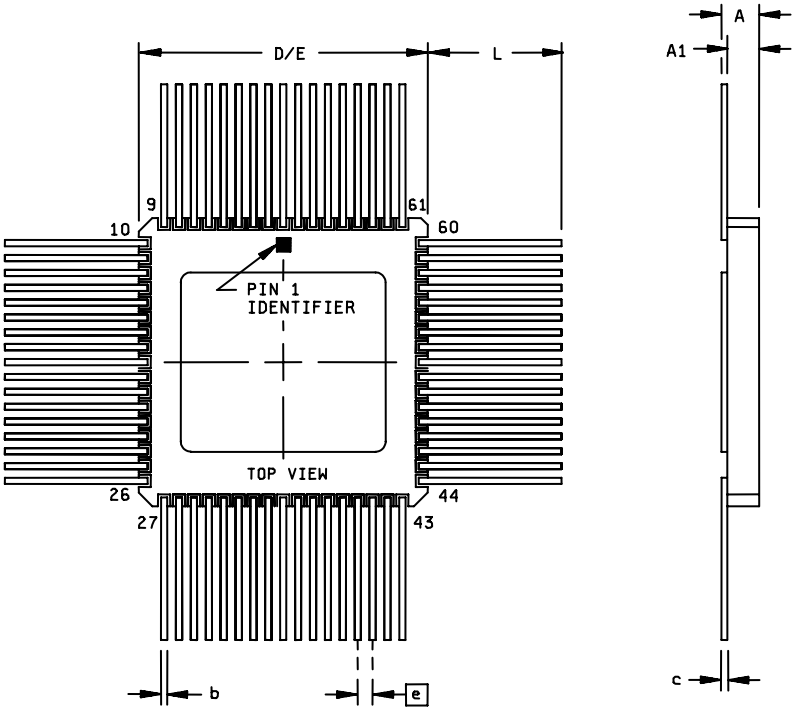
| Device Type | $T_A$ = Temperature ±10°C 3/ | $V_{DD}$ = 4.5 V | | $V_{DD}$ = 5.5 V |
|---|---|---|---|---|
| | | Effective LET no Upsets [MeV-cm$^2$/mg)] | Maximum device cross section (Cm$^2$) (LET = 80) | Effective LET no Latchup 3/ [MeV-cm$^2$/mg) |
| All | +25°C | = 25 | 3.0 x 10$^{-3}$ | > 128 |

1/ Devices that contain cross coupled resistance must be tested at the maximum rated $T_A$. For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature $T_A$ = +125°C.

Weibull and Device Parameters for Error-Rate Calculation

| Shape Parameter | Width Parameter | Structural Cross-Section | Onset LET | Depletion Depth | Funnel Depth |
|---|---|---|---|---|---|
| 1 | 14 | 3.66E-7cm$^2$/bit | 14.4MeV-cm$^2$/mg | 0.8μm | 1.45μm |

Case X




| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | --- | 2.74 | --- | .108 |
| A1 | 1.83 | 2.24 | .072 | .088 |
| b | 0.35 | 0.46 | .014 | .018 |
| c | 0.18 | 0.24 | .007 | .0095 |
| L | 6.35 | --- | .250 | --- |
| D | 21.6 | 24.50 | .850 | .965 |
| E | 21.6 | 24.50 | .850 | .965 |
| e | 1.27 TYP | 1.27 TYP | .050 TYP | .050 TYP |
| N | 68 | 68 | 68 | 68 |

NOTES:
1. The U. S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. All leads increase max limit by 0.003 inches measured at the center of the flat when lead finish A is applied.
3. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outline.

| Device types: | | All | |
|---|---|---|---|
| Case outline: | | X | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | $V_{DD}$ | 35 | HSO.3 |
| 2 | ECB5 | 36 | $V_{SS}$ |
| 3 | NMI | 37 | $\overline{\text{EDACEN}}$ |
| 4 | P0.3/ECB4 | 38 | T2CAPTURE/P2.7 |
| 5 | P0.1/ECB3 | 39 | PWM0/P2.5 |
| 6 | P0.0/ECB2 | 40 | $\overline{\text{WRL}}/\overline{\text{WR}}$ |
| 7 | P0.2/ECB1 | 41 | $\overline{\text{WRH}}/\overline{\text{BHE}}$ |
| 8 | P0.6/ECB0 | 42 | T2RST/P2.4 |
| 9 | P0.7/EXTINT | 43 | READY |
| 10 | P0.5 | 44 | P2.3/T2CLK |
| 11 | P0.4 | 45 | AD15 |
| 12 | $V_{SS}$ | 46 | AD14 |
| 13 | $V_{DD}$ | 47 | AD13 |
| 14 | $V_{SS}$ | 48 | AD12 |
| 15 | EXTINT/P2.2 | 49 | AD11 |
| 16 | $\overline{\text{RESET}}$ | 50 | AD10 |
| 17 | RXD/P2.1 | 51 | AD9 |
| 18 | TXD/P2.0 | 52 | AD8 |
| 19 | P1.0 | 53 | AD7 |
| 20 | P1.1 | 54 | AD6 |
| 21 | P1.2 | 55 | AD5 |
| 22 | PWM1/P1.3 | 56 | AD4 |
| 23 | PWM2/P1.4 | 57 | AD3 |
| 24 | T2RST/HSI.0 | 58 | AD2 |
| 25 | T2CLK/HSI.1 | 59 | AD1 |
| 26 | HSI.2/HSO.4 | 60 | AD0 |
| 27 | HSI.3/HSO.5 | 61 | $\overline{\text{RD}}$ |
| 28 | HSO.0 | 62 | ALE/$\overline{\text{ADV}}$ |
| 29 | HSO.1 | 63 | INST |
| 30 | $\overline{\text{BREQ}}$/P1.5 | 64 | BUSWIDTH |
| 31 | $\overline{\text{HLDA}}$/P1.6 | 65 | CLKOUT |
| 32 | $\overline{\text{HOLD}}$/P1.7 | 66 | $V_{SS}$ |
| 33 | T2UP-DN/P2.6 | 67 | XTAL1 |
| 34 | HSO.2 | 68 | $V_{SS}$ |

FIGURE 2. Terminal connections.

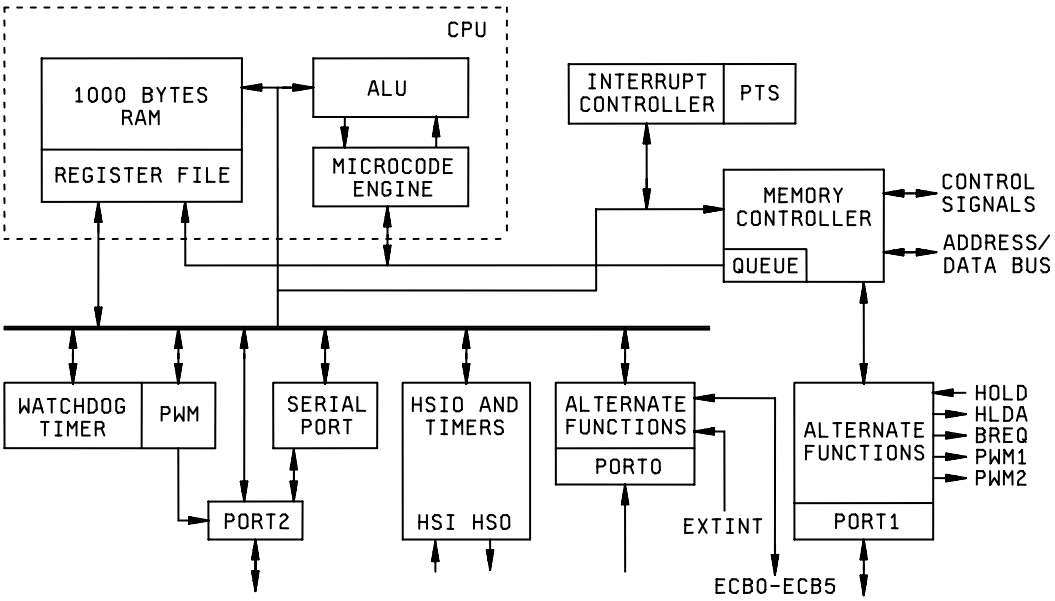



FIGURE 3. Functional block diagram.

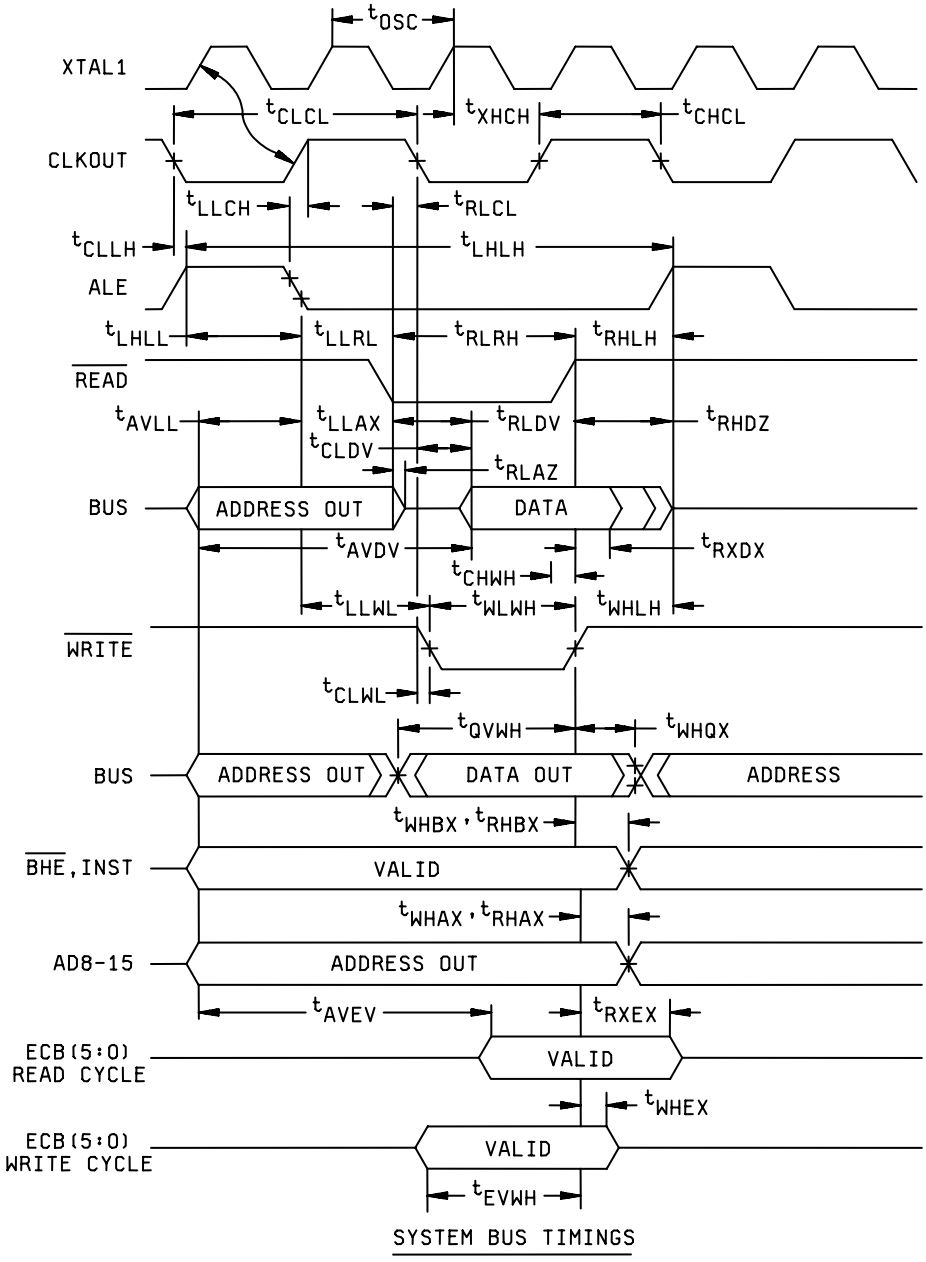
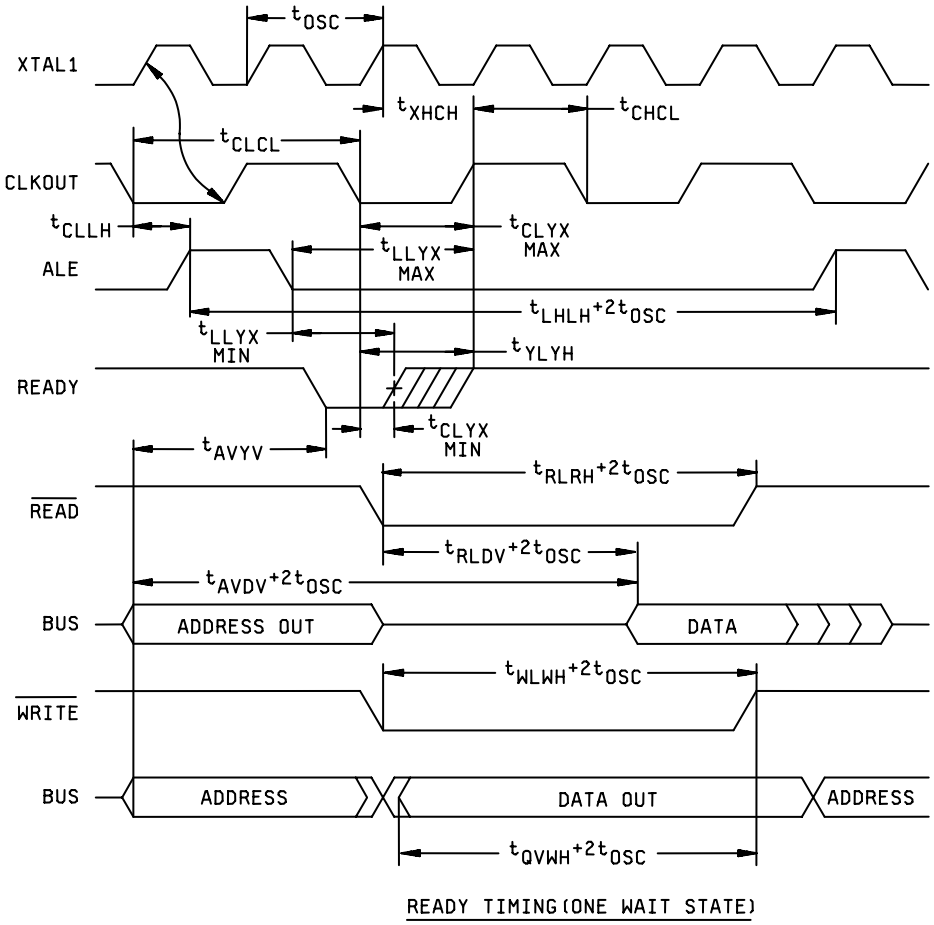
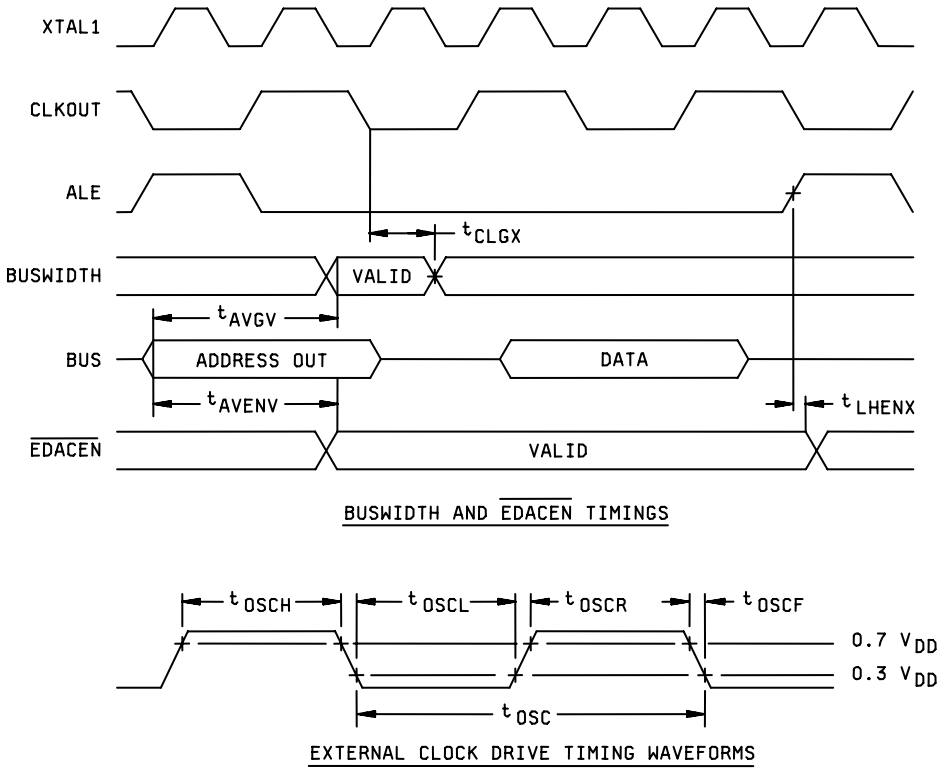



FIGURE 4. Load circuit and waveforms.




READY TIMING(ONE WAIT STATE)

FIGURE 4. Load circuit and waveforms - Continued.

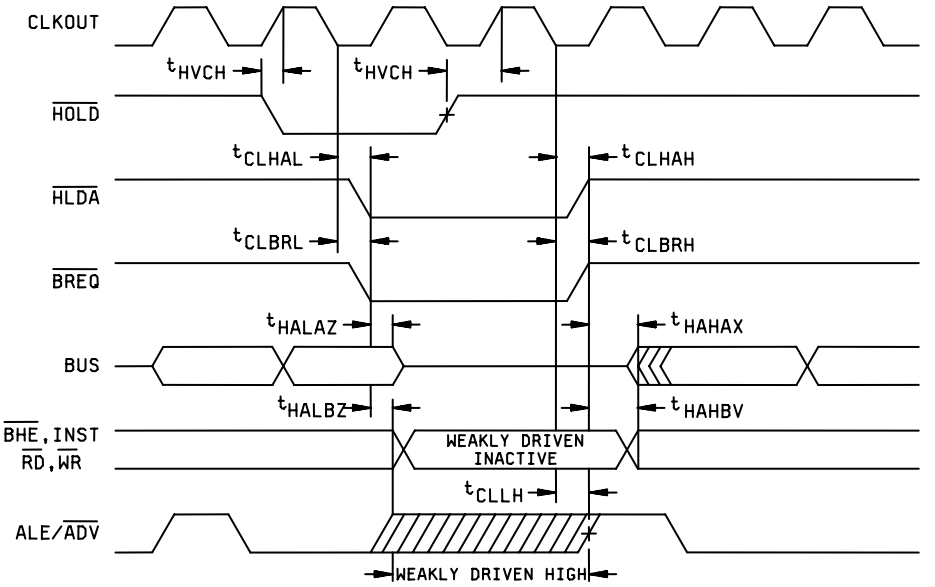



BUSWIDTH AND $\overline{EDACEN}$ TIMINGS




EXTERNAL CLOCK DRIVE TIMING WAVEFORMS

FIGURE 4. Load circuit and waveforms - Continued.



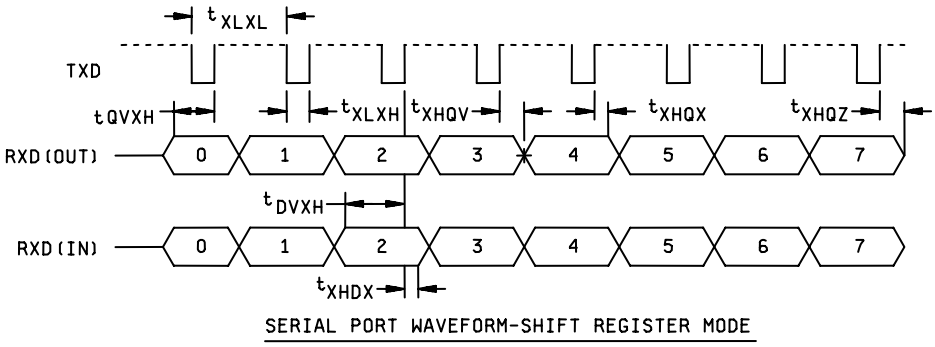
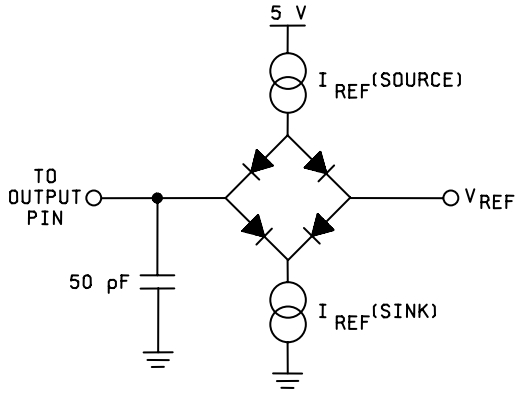
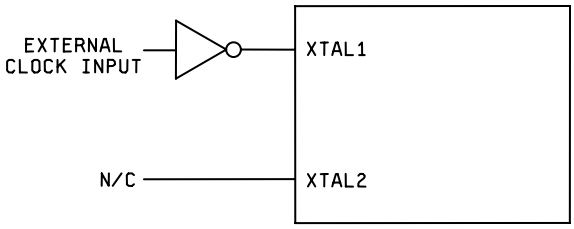




FIGURE 4. Load circuit and waveforms - Continued.

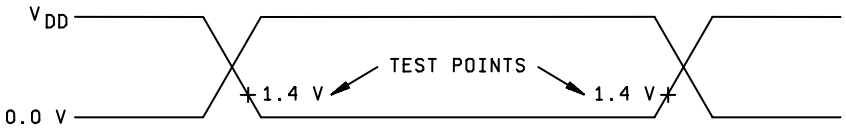



OUTPUT LOADING

NOTE: 50 pF INCLUDES SCOPE PROBE AND TEST SOCKET



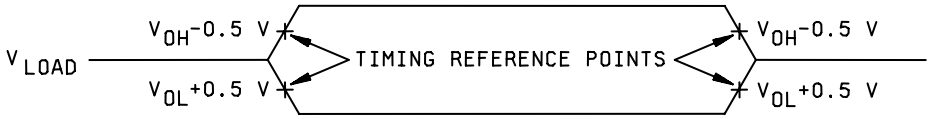

EXTERNAL CLOCK CONNECTIONS




NOTE: AC testing inputs are driven at $V_{DD}$ for a logic “1” and 0.0 V for a logic “0”. Timing measurements on outputs are made at 1.4 V

AC Testing Input, Output Waveforms.

FIGURE 4. Load circuit and waveforms - Continued.




NOTE: For timing purposes a port pin is no longer floating when it changes to a voltage outside reference points shown, and begins to float when it changes to voltage inside the reference points shown; $I_{OL}$ = 4 mA, $I_{OH}$ = -4 mA.

Float Waveforms.

FIGURE 4. Load circuit and waveforms - Continued.

| Open | $V_{DD}$ = 5 V ±0.5V | GND | $V_{DD}$ External Pin | GND External Pin |
|---|---|---|---|---|
| 2,4-8, 17-23, 26-35, 38-41, 45-63, 65 | 9, 11, 16, 24, 37, 43, 64 | 3, 10, 15, 25, 42, 44, 66, 67 | 1, 13 | 12, 14, 36, 68 |

NOTE: Each pin except those labeled "$V_{DD}$ External Pin" and "GND External Pin" will have a resistor of 2.49KΩ ±5% for irradiation.

FIGURE 5. Radiation exposure circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroup 4 ($C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect input/output capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.6 herein).

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | --- | --- | --- |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 7, 8A | 1, 2, 7, 8A | 3/ 1, 2, 7, 8A |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 7, 8A | 1, 2, 7, 8A | 1, 2, 7, 8A |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

| Parameter | Condition | Limits |
|---|---|---|
| $Q_{IDD}$ | $T_A$ = +25°C | ±10% of measured value or 20 μA, whichever is greater. |

NOTE: If device is tested at or below 20 μA, no deltas are required. Deltas' are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classed must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A$ = +25°C ±5°C after an exposure of 2 x $10^{12}$ neutrons/$cm^2$ (minimum).

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ $10^7$ ions/$cm^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/$cm^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C, and the latchup test temperature shall be the maximum rated operating temperature ±10°C.

f. Bias conditions shall be $V_{DD}$ = 4.5 V dc for the upset measurements and $V_{DD}$ = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

TABLE III. Pin descriptions.

| Pin Name | Description |
|---|---|
| $V_{DD}$ | +5 V supply voltage |
| $V_{SS}$ | Circuit ground |
| PORT 0 (P0.0-P0.7) | Port 0 is an 8-bit input only port when used in its default mode. When configured for their alternate function, five of the bits are bi-directional EDAC check bits as shown in Table A herein. |
| PORT 1 (P1.0-P1.7) | Port 1 is an 8-bit quasi-bidirectional, I/O port. All pins are quasi-bidirectional unless the alternate function is selected per Table B herein. When the pins are configured for their alternate functions, they act as standard I/O, not quasi-bidirectional. |
| PORT 2 (P2.0-P2.7) | Port 2 is an 8-bit, bidirectional, I/O port. These pins are shared with timer 2 functions, serial data I/O and PWMO output, per Table C herein. |
| AD0-AD7 | The lower 8-bits of the multiplexed address/data bus. The pins on this port are bidirectional during the data phase of the bus cycle. |
| AD8-AD15 | The upper 8-bits of the multiplexed address/data bus. The pins on this port are bidirectional during the data phase of the 16 bit bus cycle. When running in 8-bit bus width, these pins are non-multiplexed, dedicated upper address bit outputs. |
| XTAL1 | CMOS level input of the oscillator inverter. |
| CLKOUT | Output of the internal clock generator. The frequency of CLKOUT is one-half the oscillator frequency. |
| RESET | Active low reset input and open drain output. |
| BUSWIDTH | Input for the BUSWIDTH selection. If the Chip Configuration Register (CCR) bit 1 is a logic high, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If the BUSWIDTH is a 0, an 8-bit cycle occurs. If the CCR bit 1 is a logic low, then the bus is always an 8-bit bus. |
| NMI | A positive transition causes a non-maskable interrupt vector through 203EH. |
| INST | Output high during an external memory read indicates the read is a "fetch instruction". INST is valid throughout the bus cycle. INST is only activated during external memory access and output low for a data fetch. |
| EDACEN | EDACEN is an enable input for the error detection and correction functions. |
| ALE/ADV | Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address /data bus. When the pin is ADV, it goes inactive, high at the end of the bus cycle. ALE/ADV Is only activated during external memory accesses. |
| RD | Read signal output to external memory. RD is only activated during external memory reads. |
| WR/WRL | Write and Write Low output to external memory, as selected by the CCR. When selected by the CCR, WR will go low for every external write. However WRL will go low only for external writes where an even byte is being written. WR/WRL is only selected for external memory writes. |
| BHE/WRH | Byte High Enable or Write High output to external memory, as selected by the CCR. When the BHE is selected, a logic low value selects the bank of memory that is connected to the high byte of the data bus, when the WRH function is selected, the pin will go low if the bus cycle is writing to an odd memory location. When the CCR selects 8-bit BUSWIDTH mode, WRH is asserted for writes to all external memory locations. |
| READY | READY is the input used to lengthen external memory cycles for interfacing to slow memory. A logic low value will place wait states in the memory cycle. |
| HSI | Inputs to the High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI2 and HSI3. Two of these pins (HSI.2 and HSI.3) are shared with the HSO Unit. Two of these pins (HSI.0 and HSI.1) have alternate functions for Timer 2. |
| HSO | Outputs from the High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Pins HSO.4 and HSO.5 are shared with pins HSI.2 and HSI.3 of the HSI Unit respectively. |

TABLE A. PORT 0 ALTERNATE FUNCTIONS

| Port pin | Alternate Name | Alternate Function |
|---|---|---|
| P0.0-P0.3, P0.6 | ECB0-ECB4 | Error detection and correction check bits. |
| P0.4, P0.5 | P0.4, P0.5 | Input port pin. |
| P0.7 | EXTINT | Setting IOC1.1 = 1 will allow P0.7 to be used for EXTINT (INT07). |

TABLE B. PORT 1 ALTERNATE FUNCTIONS

| | | |
|---|---|---|
| P1.0 | P1.0 | I/O Pin |
| P1.1 | P1.1 | I/O Pin |
| P1.2 | P1.2 | I/O Pin |
| P1.3 | PWM1 | Setting IOC3.2 = 1enables P1.3 as the Pulse Width Modulator (PWM1) output pin. |
| P1.4 | PWM2 | Setting IOC3.3 = 1enables P1.4 as the Pulse Width Modulator (PWM2) output pin. |
| P1.5 | $\overline{\text{BREQ}}$ | Bus Request, output activated when the bus controller has a pending external memory cycle. |
| P1.6 | $\overline{\text{HLDA}}$ | Bus Hold Acknowledge, output indicating the release of the bus. |
| P1.7 | $\overline{\text{HOLD}}$ | Bus Hold, input requesting control of the bus. |

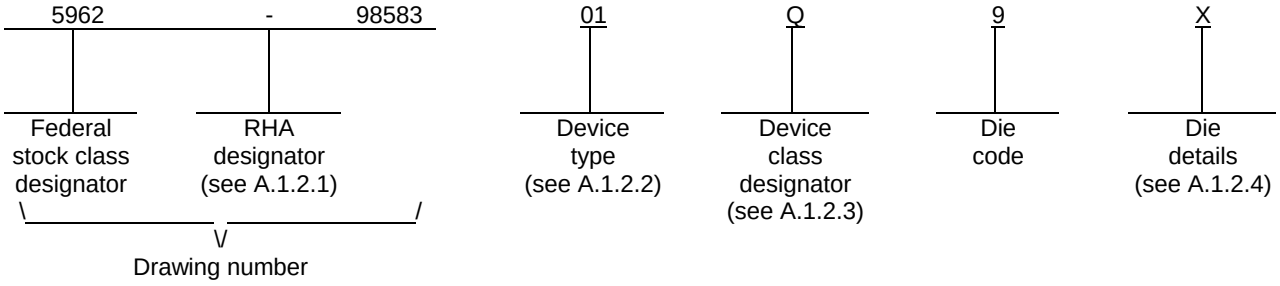
TABLE C. PORT 2 ALTERNATE FUNCTIONS

| Port Pin | Alternate Name | Alternate Function |
|---|---|---|
| P2.0 | TXD | Transmit Serial Data. |
| P2.1 | RXD | Receive Serial Data. |
| P2.2 | EXTINT | External interrupt, Clearing IOC1.1 will allow P2.2 to be used for EXTINT (INT07). |
| P2.3 | T2CLK | Timer 2 clock input and Serial port baud rate generator input. |
| P2.4 | T2RST | Timer 2 Reset. |
| P2.5 | PWMO | Pulse Width Modulator output 0. |
| P2.6 | T2UP-DN | Controls the direction of the Timer 2 counter. Logic High equals count down. Logic low equals count up. |
| P2.7 | T2CAPTURE | A rising edge on P2.7 causes the value of Timer 2 to be captured into this register, and generates a Timer 2 Capture interrupt (INT11). |

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:




A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | UT80C196KD or UT80CRH196KD 1/ | MIL-TEMP, MCS-96 Based, Microcontroller |
| 02 | UT80C196KD or UT80CRH196KD 1/ | Extended Industrial Temp, MCS-96 Based, Microcontroller |

A.1.2.3 Device class designator.

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to the die requirements of MIL-PRF-38535 |

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

| Die type | Figure number |
|---|---|
| 01 | A-1 |
| 02 | A-1 |

A.1.2.4.2 Die bonding pad locations and electrical functions.

| Die type | Figure number |
|---|---|
| 01 | A-1 |
| 02 | A-1 |

A.1.2.4.3 Interface materials.

| Die type | Figure number |
|---|---|
| 01 | A-1 |
| 02 | A-1 |

A.1.2.4.4 Assembly related information.

| Die type | Figure number |
|---|---|
| 01 | A-1 |
| 02 | A-1 |

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.

| | |
|---|---|
| Die size: | 394 mils x 394 mils |
| Die thickness: | 17.5 mils ±1 mil |

Interface materials.

| | |
|---|---|
| Top metallization: | Si Al Cu 9 kÅ – 12.5 kÅ |
| Backside metallization: | None: Backgrind |

Glassivation.

| | |
|---|---|
| Type: | PSG |
| Thickness: | 10 kÅ ±2 kÅ |

Substrate: EPI on single crystal silicon

Assembly related information.

| | |
|---|---|
| Substrate potential: | Tied to $V_{SS}$ |
| Special assembly instructions: | None |

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions

| PAD | XCENTER | YCENTER |
|---|---|---|
| 1 | 165.0 | 185.9 |
| 2 | 158.7 | 185.9 |
| 3 | 152.4 | 185.9 |
| 4 | 146.1 | 185.9 |
| 5 | 139.8 | 185.9 |
| 6 | 133.5 | 185.9 |
| 7 | 127.2 | 185.9 |
| 8 | 120.9 | 185.9 |
| 9 | 114.6 | 185.9 |
| 10 | 108.3 | 185.9 |
| 11 | 102.0 | 185.9 |
| 12 | 95.7 | 185.9 |
| 13 | 89.4 | 185.9 |
| 14 | 83.1 | 185.9 |
| 15 | 76.8 | 185.9 |
| 16 | 70.5 | 185.9 |
| 17 | 64.2 | 185.9 |
| 18 | 57.9 | 185.9 |
| 19 | 51.6 | 185.9 |
| 20 | 45.3 | 185.9 |
| 21 | 39.0 | 185.9 |
| 22 | 32.7 | 185.9 |
| 23 | 26.4 | 185.9 |
| 24 | 20.1 | 185.9 |
| 25 | 13.8 | 185.9 |
| 26 | 7.5 | 185.9 |
| 27 | 1.2 | 185.9 |
| 28 | -5.1 | 185.9 |
| 29 | -11.4 | 185.9 |
| 30 | -17.7 | 185.9 |
| 31 | -24.0 | 185.9 |
| 32 | -30.3 | 185.9 |
| 33 | -36.6 | 185.9 |
| 34 | -42.9 | 185.9 |
| 35 | -49.2 | 185.9 |
| 36 | -55.5 | 185.9 |
| 37 | -61.8 | 185.9 |
| 38 | -68.1 | 185.9 |
| 39 | -74.4 | 185.9 |
| 40 | -80.7 | 185.9 |
| 41 | -87.0 | 185.9 |
| 42 | -93.3 | 185.9 |
| 43 | -99.6 | 185.9 |
| 44 | -105.9 | 185.9 |
| 45 | -112.2 | 185.9 |
| 46 | -118.5 | 185.9 |
| 47 | -124.8 | 185.9 |
| 48 | -131.1 | 185.9 |
| 49 | -137.4 | 185.9 |
| 50 | -143.7 | 185.9 |

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

Die bonding pad locations and electrical functions

| PAD | XCENTER | YCENTER |
|---|---|---|
| 51 | -150.0 | 185.9 |
| 52 | -156.3 | 185.9 |
| 53 | -162.6 | 185.9 |
| 54 | -168.9 | 185.9 |
| 55 | -184.6 | 170.2 |
| 56 | -184.6 | 163.9 |
| 57 | -184.6 | 157.4 |
| 58 | -184.6 | 151.1 |
| 59 | -184.6 | 144.8 |
| 60 | -184.6 | 138.5 |
| 61 | -184.6 | 132.2 |
| 62 | -184.6 | 125.9 |
| 63 | -184.6 | 119.6 |
| 64 | -184.6 | 113.3 |
| 65 | -184.6 | 107.1 |
| 66 | -184.6 | 100.8 |
| 67 | -184.6 | 94.5 |
| 68 | -184.6 | 88.2 |
| 69 | -184.6 | 81.9 |
| 70 | -184.6 | 75.6 |
| 71 | -184.6 | 69.3 |
| 72 | -184.6 | 63.0 |
| 73 | -184.6 | 56.7 |
| 74 | -184.6 | 50.4 |
| 75 | -184.6 | 44.1 |
| 76 | -184.6 | 37.8 |
| 77 | -184.6 | 31.5 |
| 78 | -184.6 | 25.2 |
| 79 | -184.6 | 18.9 |
| 80 | -184.6 | 12.6 |
| 81 | -184.6 | 6.3 |
| 82 | -184.6 | 0.0 |
| 83 | -184.6 | -6.3 |
| 84 | -184.6 | -12.6 |
| 85 | -184.6 | -18.9 |
| 86 | -184.6 | -25.2 |
| 87 | -184.6 | -31.5 |
| 88 | -184.6 | -37.8 |
| 89 | -184.6 | -44.1 |
| 90 | -184.6 | -50.4 |
| 91 | -184.6 | -56.7 |
| 92 | -184.6 | -63.0 |
| 93 | -184.6 | -69.3 |
| 94 | -184.6 | -75.6 |
| 95 | -184.6 | -81.9 |
| 96 | -184.6 | -88.2 |
| 97 | -184.6 | -94.5 |
| 98 | -184.6 | -100.8 |
| 99 | -184.6 | -107.1 |
| 100 | -184.6 | -113.4 |

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

Die bonding pad locations and electrical functions

| PAD | XCENTER | YCENTER |
|---|---|---|
| 101 | -184.6 | -119.7 |
| 102 | -184.6 | -126.0 |
| 103 | -184.6 | -132.3 |
| 104 | -184.6 | -138.6 |
| 105 | -184.6 | -144.9 |
| 106 | -184.6 | -151.2 |
| 107 | -184.6 | -157.5 |
| 108 | -184.6 | -164.0 |
| 109 | -184.6 | -170.3 |
| 110 | -168.9 | -186.0 |
| 111 | -162.6 | -186.0 |
| 112 | -156.3 | -186.0 |
| 113 | -150.0 | -186.0 |
| 114 | -143.7 | -186.0 |
| 115 | -137.4 | -186.0 |
| 116 | -131.1 | -186.0 |
| 117 | -124.8 | -186.0 |
| 118 | -118.5 | -186.0 |
| 119 | -112.2 | -186.0 |
| 120 | -105.9 | -186.0 |
| 121 | -99.6 | -186.0 |
| 122 | -93.3 | -186.0 |
| 123 | -87.0 | -186.0 |
| 124 | -80.7 | -186.0 |
| 125 | -74.4 | -186.0 |
| 126 | -68.1 | -186.0 |
| 127 | -61.8 | -186.0 |
| 128 | -55.5 | -186.0 |
| 129 | -49.2 | -186.0 |
| 130 | -42.9 | -186.0 |
| 131 | -36.6 | -186.0 |
| 132 | -30.3 | -186.0 |
| 133 | -24.0 | -186.0 |
| 134 | -17.7 | -186.0 |
| 135 | -11.4 | -186.0 |
| 136 | -5.1 | -186.0 |
| 137 | 1.2 | -186.0 |
| 138 | 7.5 | -186.0 |
| 139 | 13.8 | -186.0 |
| 140 | 20.1 | -186.0 |
| 141 | 26.4 | -186.0 |
| 163 | 165.0 | -186.0 |
| 143 | 39.0 | -186.0 |
| 144 | 45.3 | -186.0 |
| 145 | 51.6 | -186.0 |
| 146 | 57.9 | -186.0 |
| 147 | 64.2 | -186.0 |
| 148 | 70.5 | -186.0 |
| 149 | 76.8 | -186.0 |
| 150 | 83.1 | -186.0 |

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

Die bonding pad locations and electrical functions

| PAD | XCENTER | YCENTER |
|---|---|---|
| 151 | 89.4 | -186.0 |
| 152 | 95.7 | -186.0 |
| 153 | 102.0 | -186.0 |
| 154 | 108.3 | -186.0 |
| 155 | 114.6 | -186.0 |
| 156 | 120.9 | -186.0 |
| 157 | 127.2 | -186.0 |
| 158 | 133.5 | -186.0 |
| 159 | 139.8 | -186.0 |
| 160 | 146.1 | -186.0 |
| 161 | 152.4 | -186.0 |
| 162 | 158.7 | -186.0 |
| 163 | 165.0 | -186.0 |
| 164 | 180.7 | -170.3 |
| 165 | 180.7 | -163.8 |
| 166 | 180.7 | -157.5 |
| 167 | 180.7 | -151.2 |
| 168 | 180.7 | -144.9 |
| 169 | 180.7 | -138.6 |
| 170 | 180.7 | -132.3 |
| 171 | 180.7 | -126.0 |
| 172 | 180.7 | -119.7 |
| 173 | 180.7 | -113.4 |
| 174 | 180.7 | -107.1 |
| 175 | 180.7 | -100.8 |
| 176 | 180.7 | -94.5 |
| 177 | 180.7 | -88.2 |
| 178 | 180.7 | -81.9 |
| 179 | 180.7 | -75.6 |
| 180 | 180.7 | -69.3 |
| 181 | 180.7 | -63.0 |
| 182 | 180.7 | -56.7 |
| 183 | 180.7 | -50.4 |
| 184 | 180.7 | -44.1 |
| 185 | 180.7 | -37.8 |
| 186 | 180.7 | -31.5 |
| 187 | 180.7 | -25.2 |
| 188 | 180.7 | -18.9 |
| 189 | 180.7 | -12.6 |
| 190 | 180.7 | -6.3 |
| 191 | 180.7 | 0.0 |
| 192 | 180.7 | 6.3 |
| 193 | 180.7 | 12.6 |
| 194 | 180.7 | 18.9 |
| 195 | 180.7 | 25.2 |
| 196 | 180.7 | 31.5 |
| 197 | 180.7 | 37.8 |
| 198 | 180.7 | 44.1 |
| 199 | 180.7 | 50.4 |
| 200 | 180.7 | 56.7 |

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

Die bonding pad locations and electrical functions

| PAD | XCENTER | YCENTER |
|---|---|---|
| 201 | 180.7 | 63.0 |
| 202 | 180.7 | 69.3 |
| 203 | 180.7 | 75.6 |
| 204 | 180.7 | 81.9 |
| 205 | 180.7 | 88.2 |
| 206 | 180.7 | 94.5 |
| 207 | 180.7 | 100.8 |
| 208 | 180.7 | 107.1 |
| 209 | 180.7 | 113.4 |
| 210 | 180.7 | 119.7 |
| 211 | 180.7 | 126.0 |
| 212 | 180.7 | 132.3 |
| 213 | 180.7 | 138.6 |
| 214 | 180.7 | 144.9 |
| 215 | 180.7 | 151.2 |
| 216 | 180.7 | 157.6 |
| 217 | 180.7 | 163.9 |
| 218 | 180.7 | 170.2 |

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

Die bonding pad locations and electrical functions

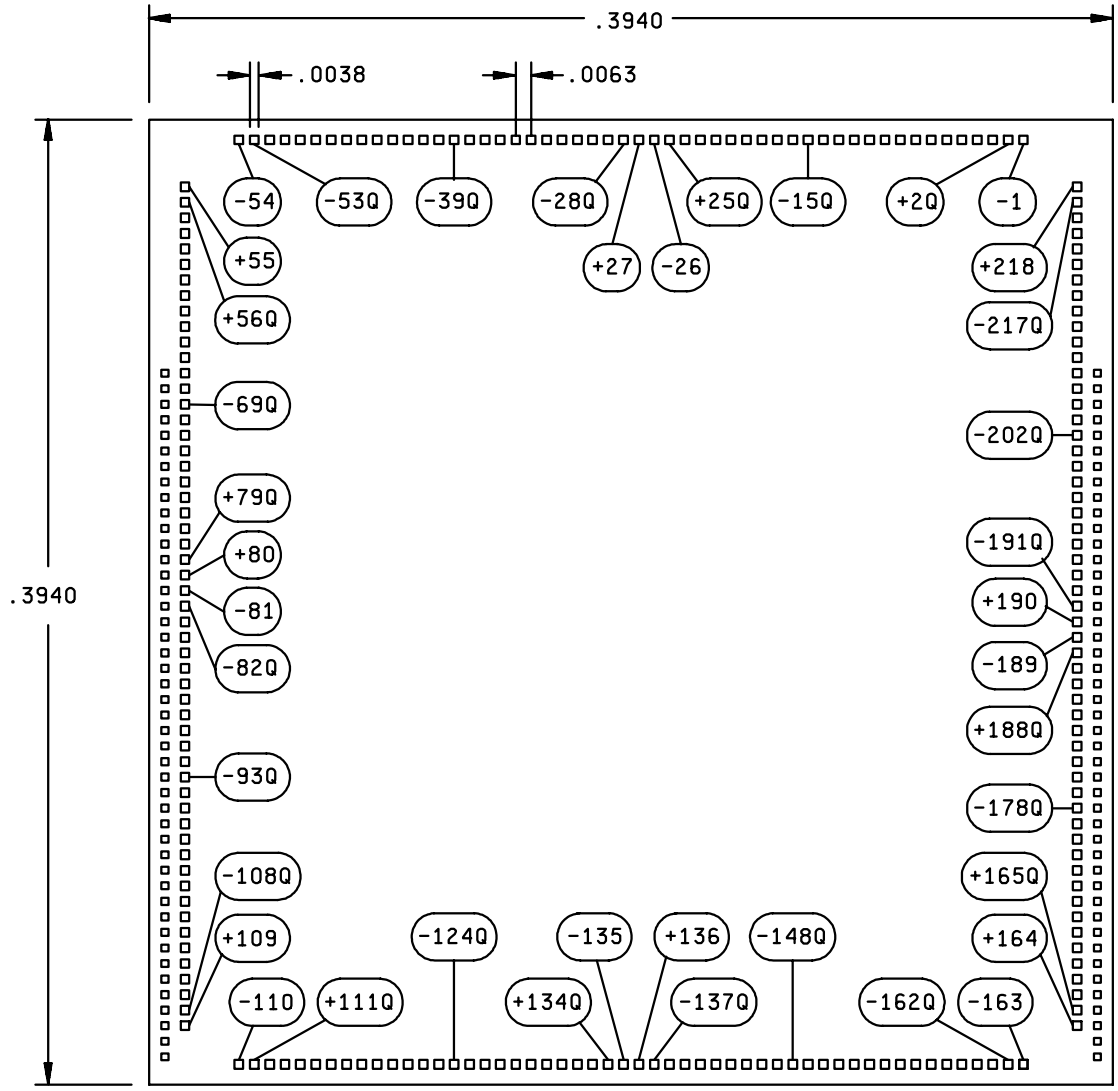



FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-07-30

Approved sources of supply for SMD 5962-98583 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9858301QXA | 65342 | UT80C196KD-WCA |
| 5962-9858301QXC | 65342 | UT80C196KD-WCC |
| 5962R9858301QXA | 65342 | UT80CRH196KD-WCA |
| 5962R9858301QXC | 65342 | UT80CRH196KD-WCC |
| 5962R9858301VXA | 65342 | UT80CRH196KD-WCA |
| 5962R9858301VXC | 65342 | UT80CRH196KD-WCC |
| 5962R9858301Q9A | 65342 | UT80CRH196KD_QCDIE |
| 5962R9858301V9A | 65342 | UT80CRH196KD_VCDIE |
| 5962-9858302QXA | 65342 | UT80C196KD-WWA |
| 5962-9858302QXC | 65342 | UT80C196KD-WWC |
| 5962R9858302QXA | 65342 | UT80CRH196KD-WWA |
| 5962R9858302QXC | 65342 | UT80CRH196KD-WWC |
| 5962R9858302VXA | 65342 | UT80CRH196KD-WWA |
| 5962R9858302VXC | 65342 | UT80CRH196KD-WWC |
| 5962R9858302Q9A | 65342 | UT80CRH196KD_QWDIE |
| 5962R9858302V9A | 65342 | UT80CRH196KD_VWDIE |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 65342 | Aeroflex Colorado Springs, Inc.<br>4350 Centennial Boulevard<br>Colorado Springs, CO 80907-3486 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.