PRELIMINARY DEVICE SPECIFICATION

AMCC

S3008/S3009 E4 Transmitter and Receiver

FEATURES

- Complies with CCITT specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 139.264 Mbit/s E4 transmission rate
- Supports Code Mark Inversion (CMI)
- Selectable reference frequencies of 17.408, 34.816, 46.421, and 69.632 MHz
- Interface to both ECL and TTL logic
- 8-bit TTL/CMOS datapath
- Bypass mode for off-chip clocking
- Local and line loopback mode
- Lock detect
- Low jitter ECL interface
- Very low power

APPLICATIONS

- E4-based transmission systems
- E4 modules
- E4 test equipment
- E4 line monitors
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

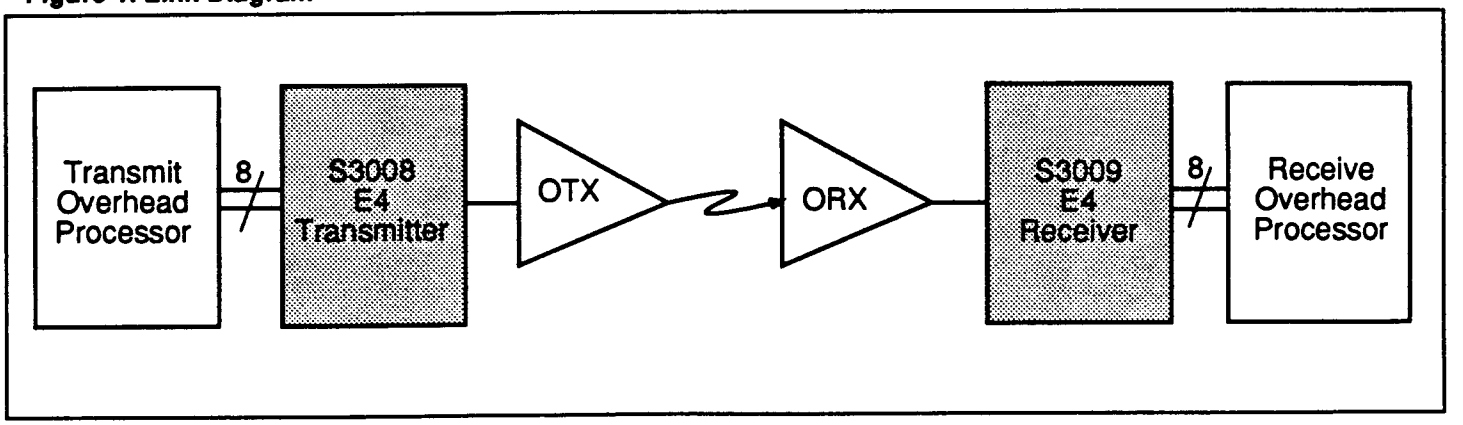
GENERAL DESCRIPTION

The S3008/S3009 E4 transmitter and receiver chips are the first fully integrated serialization/deserialization E4 139.264 Mbit/sec interface devices. With architecture developed by PMC-Sierra, the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with E4 transmission standards. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3008 transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3009 receiver chip by synchronizing its on-chip VCO with the incoming data stream. The S3008 also performs E4 frame detection. The chipset can be used with 17.408, 34.816, 46.421, and 69.632 MHz reference clocks, in support of existing system clocking schemes. On-chip code-mark-inversion (CMI) encoding and decoding is provided. If desired, both clock generation and recovery can be bypassed, allowing the use of externally generated and recovered clocks.

The very low jitter differential ECL interface guarantees compliance with the bit-error rate requirements of the CCITT standard. The S3008/S3009 chipset is packaged in a 50-mil pitch, 68-pin LDCC, offering designers a small package outline.

Figure 1. Link Diagram



S3008/S3009 OVERVIEW

The S3008 and S3009 implement E4 serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 2 and 3 show basic operation of both chips. These chips can be used to implement the front end of E4 equipment, which consists primarily of the serial transmit interface (S3008) and the serial receive interface (S3009). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing, which includes management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3008/S3009 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. CMI encoding
4. Serial output

Receiver

1. Clock and data recovery from serial input
2. CMI decoding
3. Frame detection
4. Serial-to-parallel conversion
5. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 12. On-chip clock generation can be bypassed and an externally generated clock used in its place, providing an additional measure of design flexibility.

A lock detect feature is provided on both chips, which indicates that the PLL is locked (synchronized) to the data stream.

Figure 2. S3008 E4 Transmitter

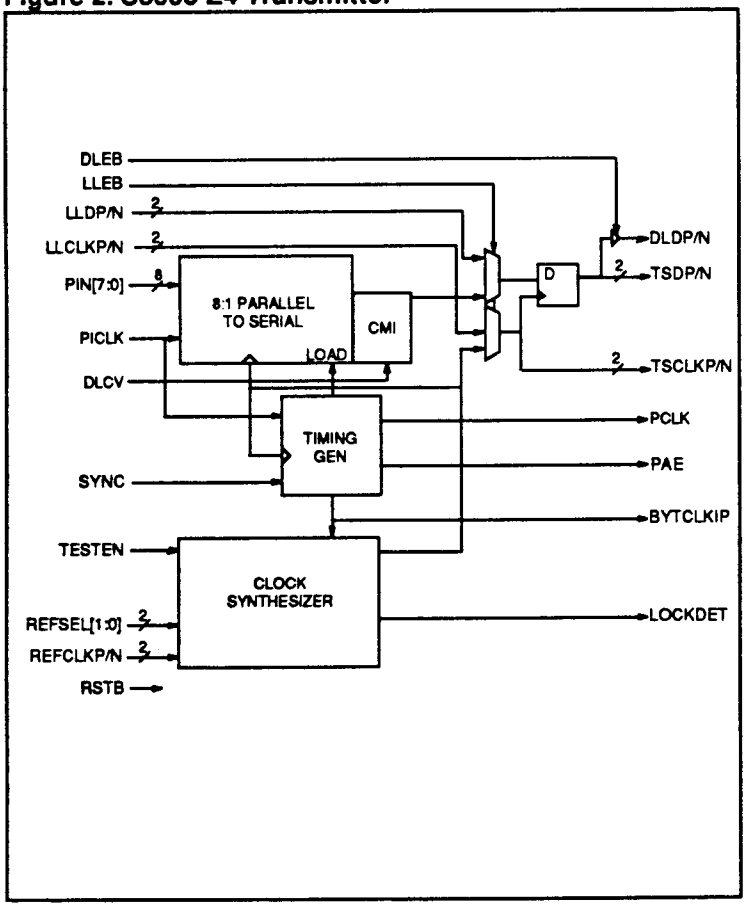
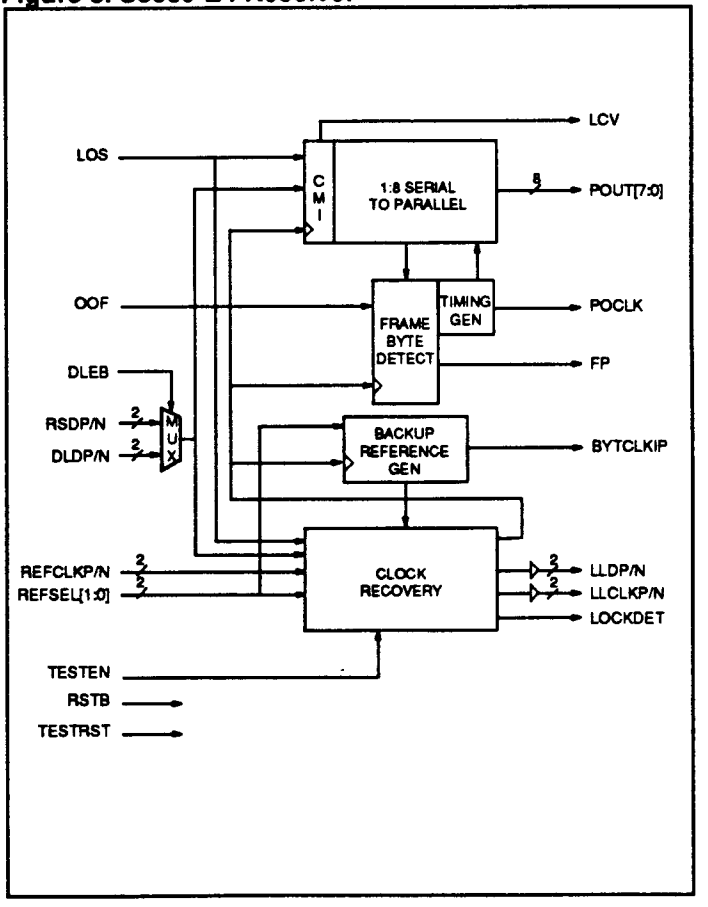


Figure 3. S3009 E4 Receiver



S3008 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3008 transmitter chip performs the serializing stage in the processing of a transmit E4 bit serial data stream. It converts the byte serial 17.408 Mbyte/sec data stream to bit serial format at 139.264 Mbit/sec and encodes the data using a Coded-Mark-Inversion (CMI) encoder.

A high-frequency bit clock can be generated from a variety of lower frequency references by using an integral frequency synthesizer consisting of a phase-locked loop circuit with an adjustable divider in the loop. For applications that provide a high-frequency bit clock externally, the internal synthesizer may be bypassed. Reference frequencies of 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz are selectable by two reference select input pins (See Table 1).

Loopback modes are provided for diagnostic loopback (transmitter to receiver), or line loopback (receiver to transmitter) when used with the compatible S3009. (See Other Operating Modes on page 8.)

Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLK). The output clock frequency is synthesizable from any of four selectable reference frequencies.

The REFSEL[1:0] inputs select the ratio between the output clock frequency and the reference input frequency, as shown in Table 1.

The REFCLK input must be generated from a differential ECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the same accuracy required for operation in an E4 system.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. The loop filter's corner frequency is optimized to minimize output phase jitter. The loop filter capacitor is included on the package.

Table 1. Reference Frequency Options

REFSEL [1:0]	REFERENCE CLOCK FREQUENCY
00	17.408 MHz
01	34.816 MHz
10	46.421 MHz
11	69.632 MHz

1 Noise on REFCLK should be less than 14.1 ps rms in a jitter frequency band from 12kHz to 1 MHz.

Timing Generator

The Timing Generation function, seen in Figure 2, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of TSCLK. For CMI coded E4, its frequency is 17.408 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3008 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLK. Although the frequency of PICLK and the internally generated byte clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present.

The Timing Generator also produces a feedback reference clock to the Clock Synthesizer. A counter divides

the synthesized clock down to the same frequency as the reference clock REFCLK. The PLL in the Clock Synthesizer maintains the stability of the synthesized clock by comparing the phase of the feedback clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 2 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

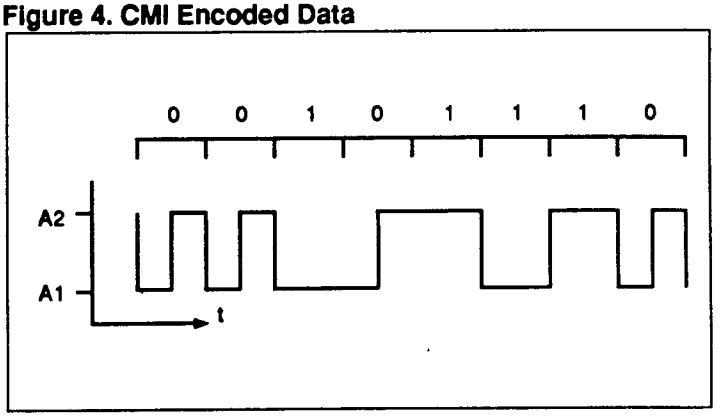
An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data shifts out of the second register and into the output selection logic at the TSCLK/2 rate.

CMI Encoding

Coded Mark Inversion format (CMI) ensures at least one data transition per bit period, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the next bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 4 shows an example of CMI-encoded data. The E4 interface is specified to have CMI-encoded data.

The CMI encoder on the S3008 accepts serial data from the Parallel to Serial converter block at 139.264 Mbit/sec, one-half the TSCLK rate. The data is then encoded into CMI format, and the result is shifted out into the output selection logic at the 278.528 Mbaud rate of TSCLK. A single CMI violation can be inserted for diagnostic purposes by applying a low-to-high transition on DLCV. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

Figure 4. CMI Encoded Data



S3008 TRANSMITTER PIN DESCRIPTIONS

Input Signals

Parallel Data Input [PIN]<7:0>. TTL. A 17.408 Mbyte/sec word, aligned to the PICLK parallel input clock. PIN<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN<0:7> is sampled on the rising edge of PICLK.

Parallel Input Clock [PICLK]. TTL. A 17.408 MHz nominally 50% duty cycle input clock, to which PIN<0:7> is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN<7:0>.

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests. (See Table 2.)

Synchronization Enable [SYNC]. TTL. Active high input that enables the timing generator to invert the internal byte transfer clock if transfers from the PIN<7:0> input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input.

Reference Clock [REFCLKP/N]. Differential ECL. Input used as the reference for the internal bit clock frequency synthesizer, or used as an externally provided bit clock. (See Table 1.)

Reference Select [REFSEL]<1:0>. TTL. Input used to select the reference frequency for the internal clock synthesizer (17.408, 34.816, 46.421, 69.632 MHz). (See Table 1.)

Line Loopback Data [LLDP/N]. Differential ECL. Used to implement a line loopback, in which the received bit serial data and clock signals are regenerated and passed through the S3008 transmitter. An internal 100-Ω resistor terminates LLDP to LLDN.

Line Loopback Clock [LLCLKP/N]. Differential ECL. Inputs normally provided from a companion S3009 device. Used to implement a line loopback, in which received bit serial data and clock signals are regenerated and passed through the S3008 transmitter. An internal 100-Ω resistor terminates LLCLKP to LLCLKN.

Diagnostic Line Code Violation [DLCV]. TTL. A rising edge causes a CMI code violation in the serial output data. DLCV is an asynchronous input.

Diagnostic Loopback Enable [DLEB]. TTL. Enables the DLD output when low. When DLEB is high, the DLD output is held in the inactive state to prevent interference between the transmit and receive devices.

Line Loopback Enable [LLEB]. TTL. When low, the LLD and LLCLK inputs are connected to the TSD and TSCLK outputs to implement line loopback. When in normal mode (LLEB high), the internally generated data and clock signals are output at TSD and TSCLK.

Master Reset [RSTB]. TTL. Reset input for the device, active low.

Output Signals

Transmit Serial Data [TSDP/N]. High-speed Source-terminated Differential ECL. Serial data stream signals, normally connected to an optical transmitter module. Updated on the falling edge of TSCLK.

Diagnostic Loopback Data [DLDP/N]. High-speed Source Terminated Differential ECL. Serial data stream signals, normally connected to a companion S3009 device for diagnostic loopback purposes. The DLD outputs are updated on the falling edge of TSCLK. They are held in the inactive state, except when DLEB is low.

Transmit Serial Clock [TSCLKP/N]. High-speed Source-terminated Differential ECL. Phase-aligned with the TSD and DLD output signals. TSCLK can be a buffered version of the internal frequency synthesizer clock, of the REFCLK inputs during clock bypass (TESTEN high), or of the LLCLK inputs during line loopback (LLEB low).

Parallel Clock [PCLK]. TTL/CMOS. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3008 device.

Phase Alignment Event [PAE]. TTL/CMOS. Pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PICLK timing domains. PAE is updated on the falling edge of the PCLK output.

Reference Feedback Clock [BYTCLKIP]. TTL/CMOS. It is compared with the reference clock (REFCLK) to maintain stability of the clock synthesis PLL. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.

Lock Detect [LOCKDET]. TTL. Goes low after the PLL

S3009 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3009 receiver chip provides the first stage of digital processing of a receive E4 bit-serial stream. It converts the bit-serial 139.264 Mbit/sec data stream into a 17 Mbyte/sec byte-serial data format. A Coded Mark Inversion (CMI) decoder is enabled during operation for decoding E4 signals.

Clock recovery is performed on the incoming CMI-coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate. Reference frequencies of 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz are selected by two reference select input pins. For applications that provide a high frequency bit clock externally, the internal clock recovery circuit may be bypassed. (See Other Operating Modes on page 8.)

A loopback mode is provided for diagnostic loopback (transmitter to receiver). Signal pins are provided to allow for line loopback (receiver to transmitter) when used with the compatible S3008 device.

Clock Recovery

Clock Recovery, as shown in the block diagram in Figure 3, generates a clock that is at the same frequency as the incoming data baud rate at the RSD or DLD inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are com-

pared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost.

The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has been low continuously for 4000 to 8000 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When set high, LOS squelches the incoming data stream, and thus causes the PLL to switch its source of reference after 4000 to 8000 recovered clock periods. Loss-of-signal condition is removed when LOS is low, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

When the test clock enable (TESTEN) input is set high, the clock recovery block is disabled. The reference clock (REFCLK) is used as the bit rate clock input in place of the recovered clock. The frequency of the REFCLK should be appropriate for the desired data rate. The reference selection inputs REFSEL[1:0] have no effect when TESTEN is set high.

Backup Reference Generator

The Backup Reference Generator seen in Figure 3 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCLK. The modulus of the counter is a function of the reference clock frequency and the operating frequency. The frequency of the reference clock is selected by the REFSEL[1:0] inputs, as shown in Table 2.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for an E4 framing pattern. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial to Parallel Converter

The Serial to Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock generated by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

CMI Decoding

The CMI decoder block on the S3009 accepts serial data from the RSDP/N input at the TSCLK rate of 278.528 Mbaud. The data is then decoded from CMI to NRZ format and converted from serial to parallel at 139.264 Mbit/sec (half of the TSCLK rate).

S3009 RECEIVER PIN DESCRIPTIONS

Input Signals

Receive Serial Data [RSDP/N]. Differential ECL. Serial data stream signals normally connected to an optical receiver module. When internal clock recovery is used, clock is recovered from transitions on the RSD inputs. When external clock recovery is used, the RSD inputs are sampled on the rising edge of the reference clock (REFCLK). An internal 100-Ω termination resistor is connected across RSDP and RSDN.

Diagnostic Loopback Data [DLDP/N]. Differential ECL. Serial data stream signals, normally connected to a companion S3008 device for diagnostic loopback purposes. Clock is recovered from transitions on the DLD inputs while in diagnostic loopback. An integral 100-Ω termination resistor is connected across DLDP and DLDN.

Diagnostic Loopback Enable [DLEB]. TTL. Selects diagnostic loopback. When DLEB is high, the S3009 device uses the primary data (RSD) input. When low, the S3009 device uses the diagnostic loopback data (DLD) input.

Out of Frame [OOF]. TTL. Indicator used to enable framing pattern detection logic in the S3009. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 14 and 15.)

Loss of Signal [LOS]. ECL. A 100k single-ended ECL input that is used by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the received serial data (RSD) pins will be squelched. When LOS is low, data on the RSD pins will be processed normally.

Reference Clock [REFCLKP/N]. Differential ECL. Input normally used as the reference for the integral clock recovery PLL. (See Table 1.) When the test clock enable (TESTEN) input is set high, REFCLK replaces the bit rate recovered clock. (See Table 2.)

Reference Select [REFSEL]<1:0>. TTL. Input used to select the internal frequency synthesizer reference clock frequency (17.408, 34.816, 46.421, 69.632 MHz). See Table 1.

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests. It can also be used to enable an external clock source in bypass mode (see Table 2).

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held high for normal operation.

Master Reset [RSTB]. TTL. Input for the device, active low. After reset, frame boundary detection is disabled.

Output Signals

Line Loopback Data [LLDP/N]. High-speed Source-terminated Differential ECL. A regenerated version of either the incoming data stream (RSD) input in normal mode, or the diagnostic loopback data (DLD) input in diagnostic loopback mode (DLEB set high). LLD is updated on the rising edge of LLCLK.

Line Loopback Clock [LLCLKP/N]. High-speed Source-terminated Differential ECL. Phase aligned with the line loopback data (LLD) output signals. LLCLK can be a buffered version of the internally recovered bit clock, or the reference clock (REFCLK) input when clock recovery is bypassed (TESTEN set high).

Parallel Output [POUT]<7:0>. TTL/CMOS. Parallel data bus, a 17.408 Mbyte/sec word, aligned to the parallel output clock (POCLK). POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT<7:0> is updated on the falling edge of POCLK.

Line Code Violation [LCV]. TTL/CMOS. Set high to indicate that one or more bits of the byte currently presented on POUT<7:0> contains a CMI line code violation. LCV is updated on the falling edge of POCLK.

Frame Pulse [FP]. TTL/CMOS. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.

Parallel Output Clock [POCLK]. TTL/CMOS. A 17.408 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT<7:0> byte serial output data. POUT<7:0> and FP are updated on the falling edge of POCLK.

Reference Feedback Clock [BYTCLKIP]. TTL/CMOS. Compared with the reference clock (REFCLK) to maintain stability of the clock recovery PLL when it is in loss of signal state. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.

Lock Detect [LOCKDET]. TTL. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.

OTHER OPERATING MODES

Diagnostic Loopback

The Diagnostic Loopback consists of alternate serial data outputs (in the case of the S3008) and inputs (in the case of the S3009).

On the S3008, the differential ECL output DLD provides Diagnostic Loopback serial data. When the Diagnostic Loopback Enable (DLEB) input is low, this data output is a replica of TSD. When DLD is connected to the S3009, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When DLEB is high, DLD is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver.

On the receiver side, the differential ECL input DLD is the Diagnostic Loopback serial data input. When the Diagnostic Loopback Enable (DLEB) input is set high, the DLD input is routed in place of the normal data stream (RSD).

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. For the S3008, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the CMI Encoder block. When LLEB is low, it forces the output data multiplexor to select data and clock from the LLD and LLCLK inputs. When these inputs are connected to the Line Loop Clock (LLCLK) and Line Loop Data (LLD) outputs of a S3009 receiver, a receive-to-transmit loopback can be established at the serial data rate.

The interface diagram in Figure 5 shows both diagnostic and line loopback modes.

Test and Bypass Modes

The Test Clock Enable (TESTEN) inputs on both chips provide access to the PLL.

The PLL-generated clock source on both the S3008 and S3009 can be bypassed by setting TESTEN high. In this mode, an externally generated bit serial clock source must be applied at the REFCLK input. Table 2 lists the possible combinations allowed in bypass mode.

Figure 5. Interface Diagram

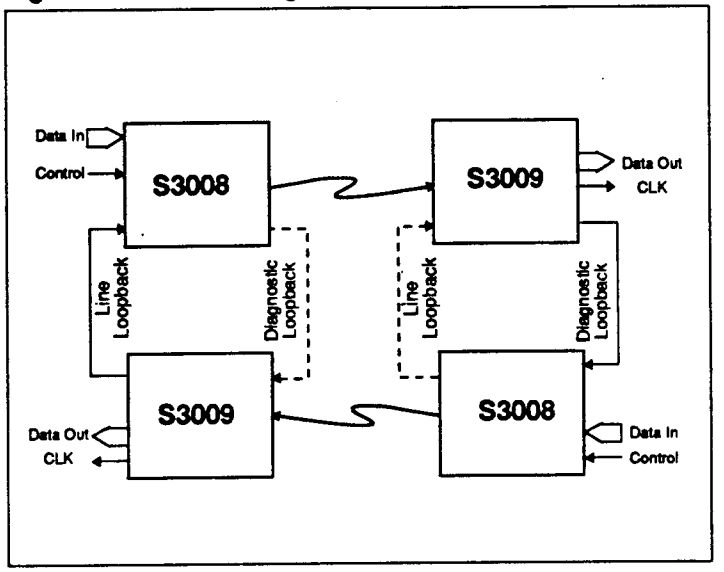


Table 2. Bypass Mode

TESTEN	Reference Clock Frequency In Bypass Mode	Serial Data Rate (Mbit/s)
0	Normal Operating Mode (See Table 1)	—
1	278.528	139.264 CMI

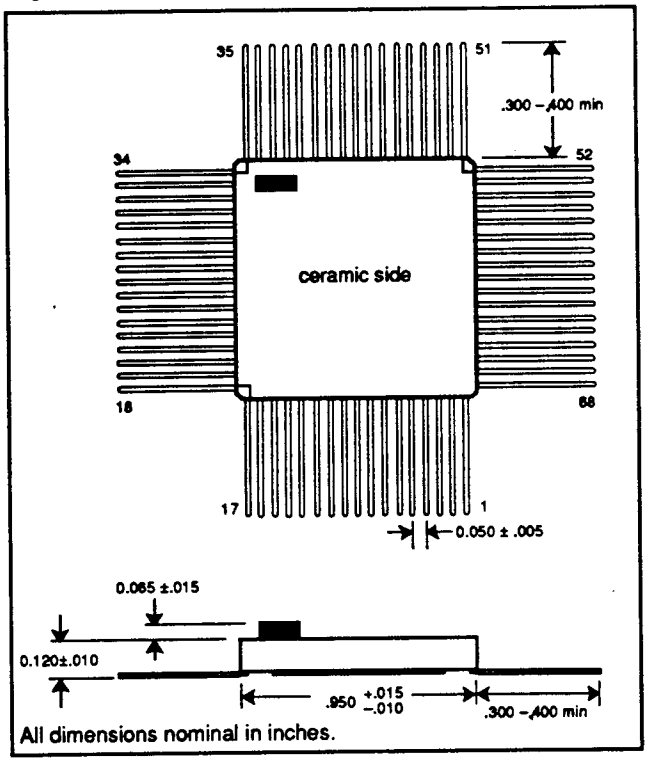
ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	–55		125	°C
Junction Temperature under Bias	–55		150	°C
Storage Temperature	–65		150	°C
Voltage on VCC with Respect to GND	–0.5		+7.0	V
Voltage on VEE with Respect to GND	+0.5		–8.0	V
Voltage on Any TTL Input Pin	–0.5		+5.5	V
Voltage on Any ECL Input Pin	0		VEE	V
TTL/CMOS Output Sink Current			20	mA
TTL/CMOS Output Source Current			10	mA
High Speed ECL Output Source or Sink Current			50	mA
Static Discharge Voltage		100		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		Min	Typ	Max	Unit
Ambient Temperature under Bias		0		+70	°C
Junction Temperature under Bias				+130	°C
Voltage on VCC with Respect to GND		4.75	5.0	5.25	V
Voltage on VEE with Respect to GND		–4.2	–4.5	–4.8	V
Voltage on Any TTL Input Pin		0		VCC	V
Voltage on Any ECL Input Pin		0		–2.0	V
TTL/CMOS Output Sink Current				8	mA
TTL/CMOS Output Source Current				1	mA
ECL Output Source Current				25	mA
High Speed ECL Output Source or Sink Current				10	mA
S3005	ICC		41	52	mA
	IEE		314	402	mA
S3006	ICC		54	69	mA
	IEE		324	414	mA

Figure 6. 68-pin LDCC Package



All dimensions nominal in inches.

TTL INPUT/OUTPUT DC CHARACTERISTICS

(T_A = -40°C to +70°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7%)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IL}	TTL Input Low Voltage		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	TTL Input High Voltage	2.0		Volts	Guaranteed Input HIGH Voltage
V_{OL}	TTL Output or Low Voltage		0.5	Volts	I_{OL} = -20 mA
V_{OH}	TTL Output or High Voltage	2.7		Volts	I_{OH} = 1 mA
V_{OL}	TTL Driving CMOS, Output Low Voltage		0.4	Volts	Guaranteed Output LOW Voltage, IOH = -100 µA
V_{OH}	TTL Driving CMOS, Output High Voltage	3.68		Volts	Guaranteed Output LOW Voltage, IOH = 100 µA

ECL INPUT DC CHARACTERISTICS[1]

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IL}	ECL Input Low Voltage	-1.950	-1.475	Volts	Guaranteed Input LOW Voltage
V_{IH}	ECL Input High Voltage	-1.145	-0.800	Volts	Guaranteed Input High Voltage

1 These conditions will be met with a 70°C ambient airflow of 400 LFPM.

S3008 TRANSMITTER PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VCC	18	ECL GND	35	NC	52	ECL GND
2	PIN[7]	19	VCC	36	REFCLK+	53	PLLVEE
3	PIN[6]	20	PAE	37	PLLGND	54	PLLGND
4	ECL GND	21	BYTCLKIP	38	REFCLK–	55	NC
5	PIN[5]	22	TTL GND	39	TSD+	56	LOCKDET
6	VEE	23	PCLK	40	PLLVEE	57	LLEB
7	VEE	24	VEE	41	TSD–	58	SYNC
8	PIN[4]	25	ECL GND	42	PLLGND	59	DLCV
9	PIN[3]	26	DLEB	43	TSCLK–	60	PICLK
10	PIN[2]	27	REFSEL[0]	44	TSCLK+	61	ECL GND
11	VEE	28	REFSEL[1]	45	LLCLK+	62	VEE
12	PIN[1]	29	RSTB	46	PLLVEE	63	VCC
13	ECL GND	30	VEE	47	LLCLK–	64	TTL GND
14	PIN[0]	31	TESTEN	48	PLLGND	65	VCC
15	DLD–	32	PLLGND	49	LLD+	66	TTL GND
16	DLD+	33	PLLVEE	50	PLLVEE	67	TTL GND
17	VCC	34	ECL GND	51	LLD–	68	ECL GND

S3009 RECEIVER PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VCC	18	ECL GND	35	NC	52	ECL GND
2	POUT[7]	19	VCC	36	REFCLK+	53	PLLVEE
3	POUT[6]	20	TESTRST	37	PLLGND	54	PLLGND
4	ECL GND	21	RSTB	38	REFCLK–	55	NC
5	POUT[5]	22	TTL GND	39	LLD–	56	LOCKDET
6	VEE	23	LOS	40	PLLVEE	57	DLEB
7	VEE	24	VEE	41	LLD+	58	OOF
8	POUT[4]	25	ECL GND	42	PLLGND	59	TTL GND
9	POUT[3]	26	REFSEL[1]	43	LLCLK–	60	POCLK
10	POUT[2]	27	REFSEL[0]	44	LLCLK+	61	ECL GND
11	VEE	28	VCC	45	DLD–	62	VEE
12	POUT[1]	29	VCC	46	PLLVEE	63	BYTCLKIP
13	ECL GND	30	VEE	47	DLD+	64	TTL GND
14	POUT[0]	31	TESTEN	48	PLLGND	65	LCV
15	TTL GND	32	PLLGND	49	RSD–	66	VCC
16	FP	33	PLLVEE	50	PLLVEE	67	TTL GND
17	VCC	34	ECL GND	51	RSD+	68	ECL GND

Power Supply Connections:

VCC	+5V
VEE	–5.2V
TTL GND	0V
ECL GND	0V
PLLGND	0V
PLLVEE	–5.2V

Table 3. S3008 AC Timing Characteristics (T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7%)

Symbol	Description	Min	Max	Units
	TSCLK Frequency (nom. 155, 311, or 622 MHz)		640	MHz
	TSCLK Duty Cycle	33	67	%
	PICLK Duty Cycle	33	67	%
tS_{PIN}	PIN [7.0] Set-up Time to PICLK	2000		ps
tH_{PIN}	PIN [7.0] Hold Time to PICLK	1000		ps
tS_{LLD}	LLD Set-Up Time to LLCLK	300		ps
tH_{LLD}	LLD Hold Time to LLCLK	100		ps
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay		440	ps
tP_{PAE1}	PCLK Low to PAE Valid Propagation Delay		3000	ps

Figure 7. PIN AC Input Timing

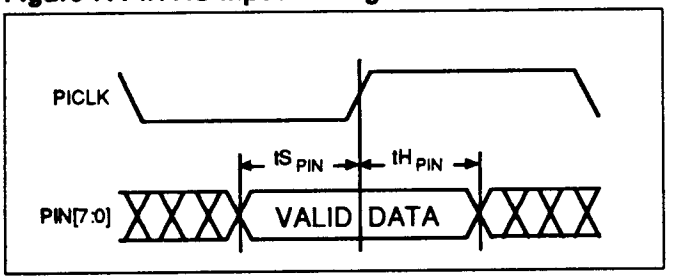
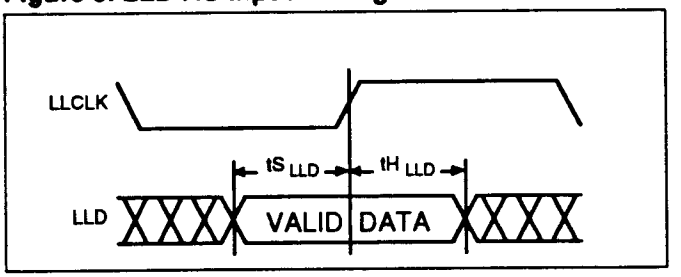
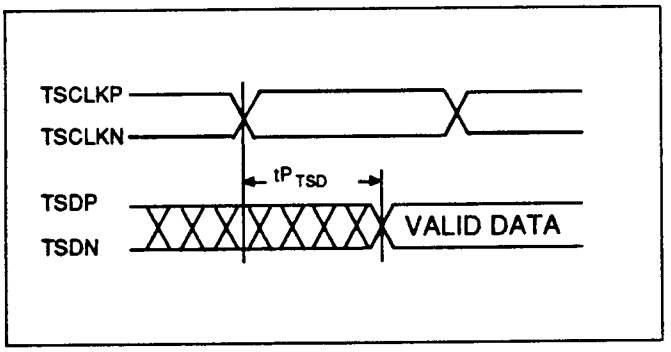


Figure 8. LLD AC Input Timing



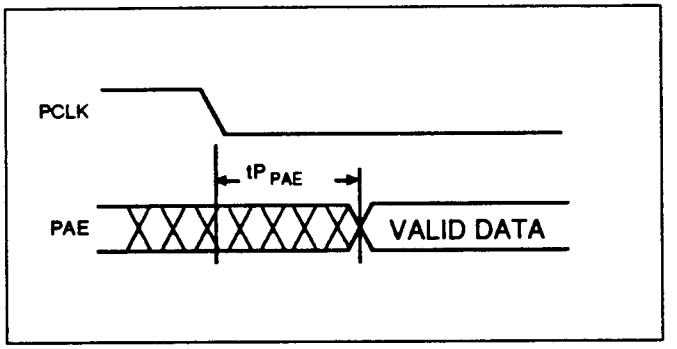
1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in picoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.
3. When a set-up time is specified on differential ECL signals between an input and a clock, the set-up time is the time in picoseconds from the cross-over point of the input to the cross-over point of the clock.
4. When a hold time is specified on differential ECL signals between an input and a clock, the hold time is the time in picoseconds from the cross-over point of the clock to the cross-over point of the input.

Figure 9. Output Timing



Notes on High-Speed PECL Output Timing
1. Output propagation delay time is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 10. PAE Output Timing



Notes on TTL Output Timing
1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 15-pF load on the outputs.

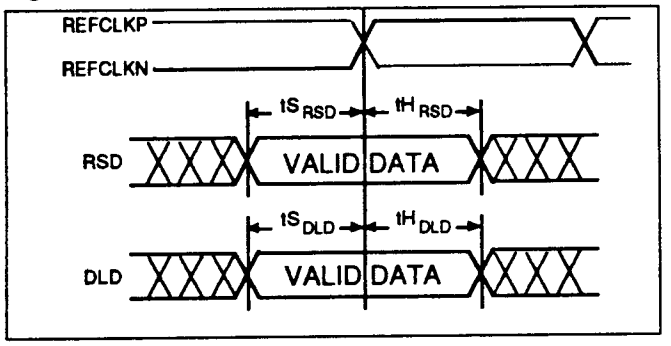
Table 4. S3008 External Clock Mode Timing

Description	Min	Max	Units
REFCLK in Bypass Mode (nom. 278 MHz)		285	MHz
REFCLK in Bypass Mode duty cycle	33	67	%

Table 5. S3008 AC Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle	45	55	%
tP_{POUT}	POCLK Low to POUT[7:0] Valid Prop. Delay	0	1500	ps
tP_{FP}	POCLK Low to FP Valid Propagation Delay	0	1500	ps
	LLCLK Frequency		640	MHz
	LLCLK Duty Cycle	45	55	%
tP_{LLD}	LLCLK Low to LLD Valid Propagation Delay	–500	+500	ps
	RSD Minimum Pulse Width	400		ps

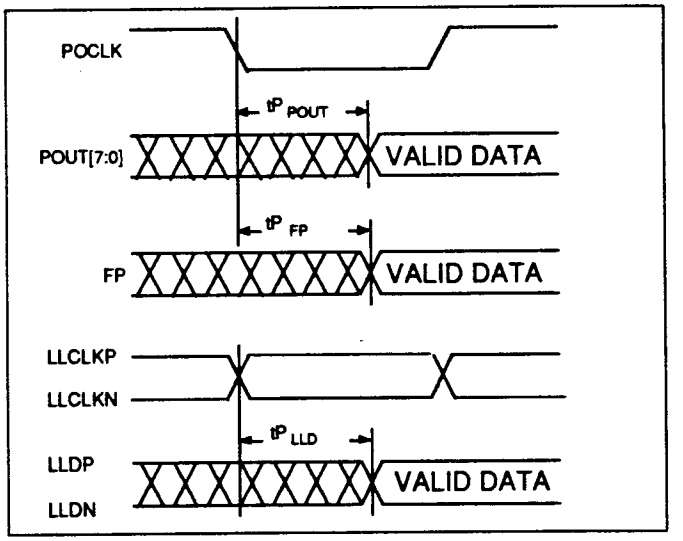
Figure 11. Input Timing - External Clock Mode



Notes on Input Timing:

1. When a set-up time is specified between a data input and a clock input, the set-up time is the time in picoseconds from the crossover point of the differential data input to the crossover point of the differential clock input.
2. When a hold time is specified between a data input and a clock input, the hold time is the time in picoseconds from the crossover point of the differential clock input to the crossover point of the differential data input.

Figure 12. Output Timing Diagram



Notes on Output Timing:

1. Output propagation delay time of TTL outputs is the time in picoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays of TTL outputs are measured with a 15 pF load on the outputs.
3. Output propagation delay time of high speed ECL outputs is the time in picoseconds from the cross-over point of the reference signal to the cross-over point of the output.
4. Maximum output propagation delays of TTL outputs are measured with a 50Ω transmission line on the outputs.

Table 6. S3009 External Clock Mode Timing

Symbol	Description	Min	Max	Units
	REFCLK Freq.		285	MHz
	REFCLK Duty Cycle	33	67	%
tS_{RSD}	RSD to REFCLK Set-up Time	300		ps
tH_{RSD}	REFCLK to RSD Hold Time	100		ps
tS_{DLD}	DLD to REFCLK Set-Up Time	300		ps
tH_{DLD}	REFCLK to DLD Hold Time	100		ps

RECEIVER FRAMING

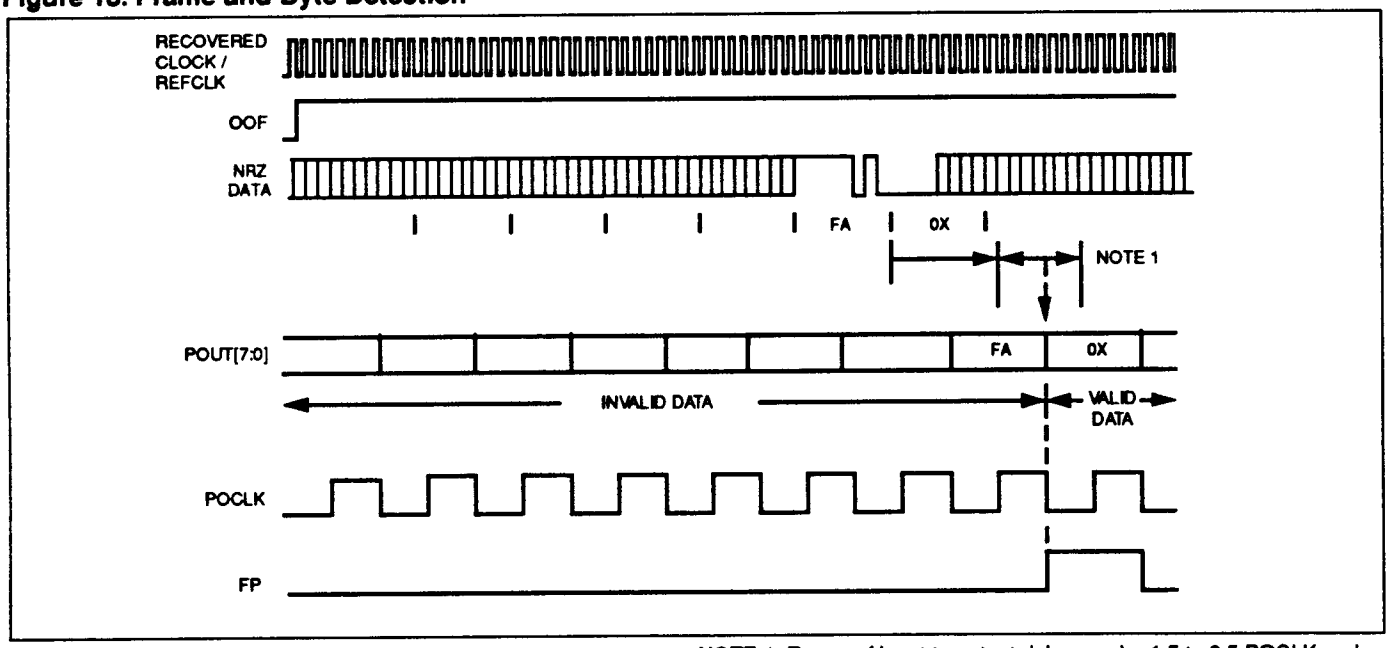
Figure 13 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. The boundary is recognized upon receipt of the 12-bit E4 frame alignment code $(FA0X)_{16}$. The first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]) will be the 0X code. Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 14. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 14 shows a typical OOF timing pattern which occurs when the S3009 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 15 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 13. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 14. OOF Operation Timing

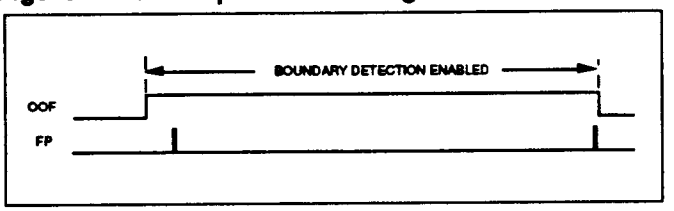
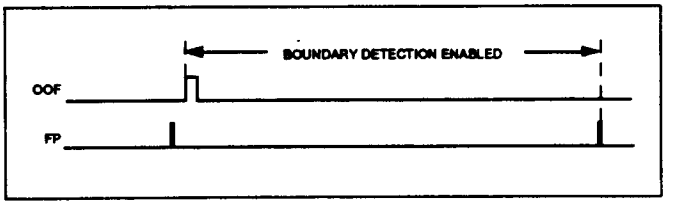
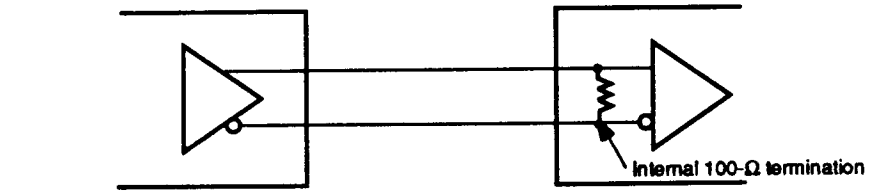


Figure 15. Alternate OOF Timing

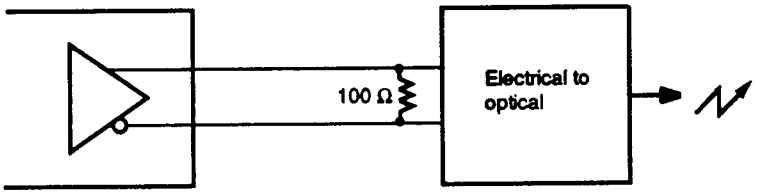


DIFFERENTIAL ECL I/O APPLICATIONS

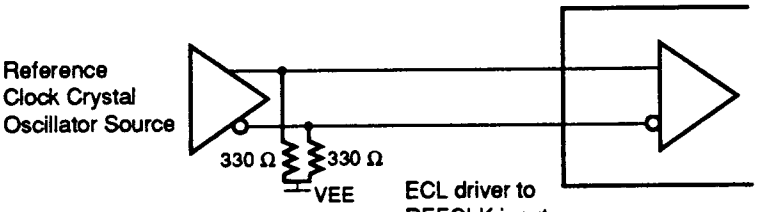
Figure 16. Differential ECL Input and Output Applications

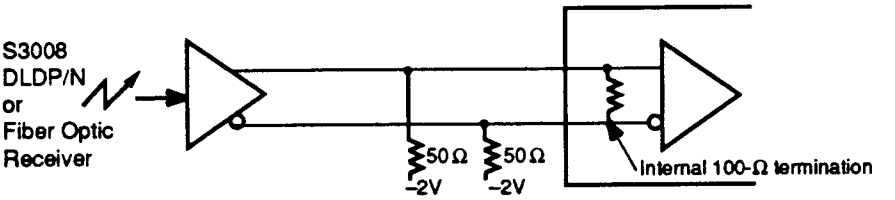


High-speed source-terminated differential ECL output
to high-speed source-terminated differential ECL input

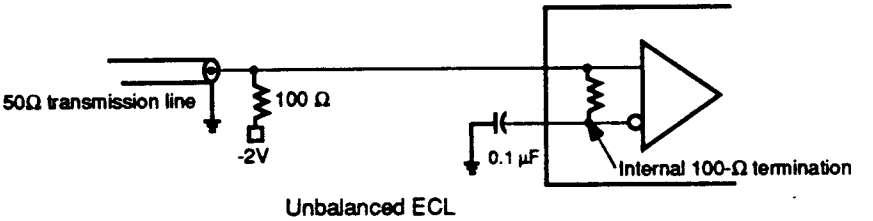


High-speed source-terminated differential ECL output
to ECL-compatible input





ECL-compatible
output to receiver
differential input



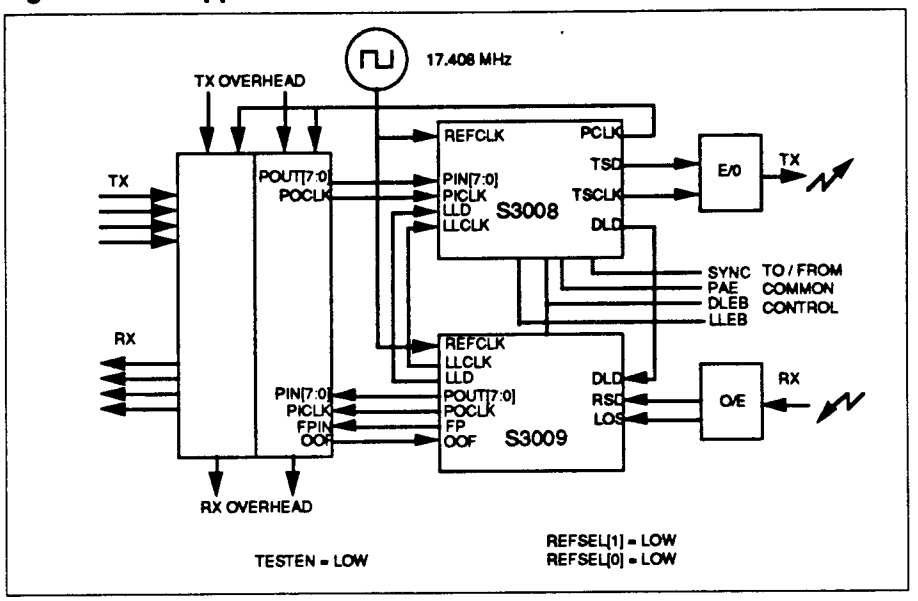
Unbalanced ECL
signal to internally terminated
differential input

Note: Applies to these signals: TSDP/N, LLDP/N, LLCLKP/N, RSDP/N, DLDP/N

E4 OPTICAL INTERFACE

The S3008 and S3009 devices are designed to interface seamlessly to make an E4 transceiver. Figure 17 shows these two devices connected together with receive and transmit overhead processors on the equipment side and electrical-to-optical converters on the line side to realize the core of a typical E4 transceiver.

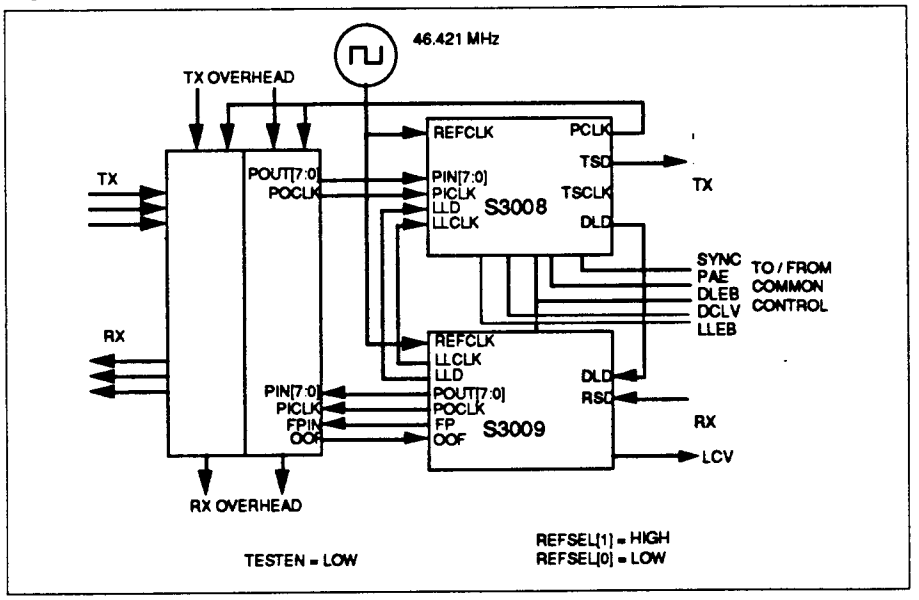
Figure 17. E4 Application



E4 ELECTRICAL INTERFACE

With the S3008 and S3009 devices, an electrical E4 transceiver can be implemented as shown in Figure 18. In this case, a clock reference of 46.421 MHz was selected. TSD would be coupled through a line driver and transformer to a coaxial cable for short span applications.

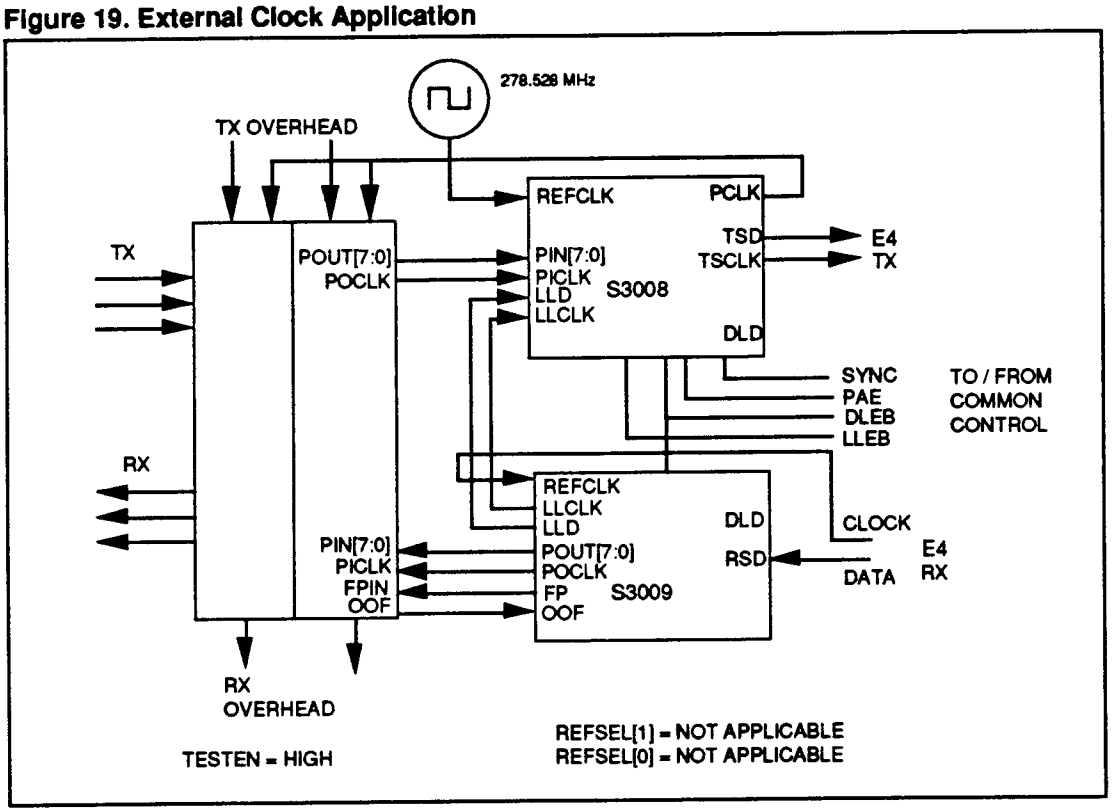
Figure 18. E4 Electrical Interface



EXTERNAL CLOCK APPLICATION

The S3009 can receive data at E4 or other standard data rates by bypassing the internal clock recovery PLL and supplying the appropriate clock to the RSCLK input. Figure 19 shows an application for E4 with external clock recovery on the receive side, and an external transmit clock connected to REFCLK of the S3008 device.

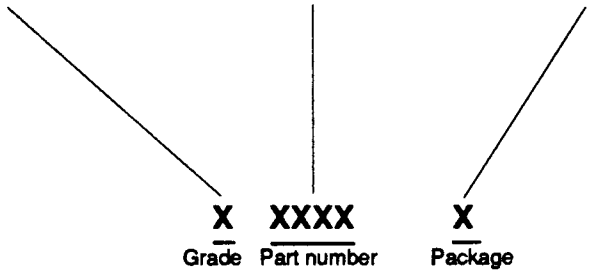
Figure 19. External Clock Application



Ordering Information

GRADE	TRANSMITTER	PACKAGE
S—commercial	3008	A—68 LDCC

GRADE	RECEIVER	PACKAGE
S—commercial	3009	A—68 LDCC



NOTES

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