54F/74F674

16-Bit Serial/Parallel-In, Serial-Out Shift Register

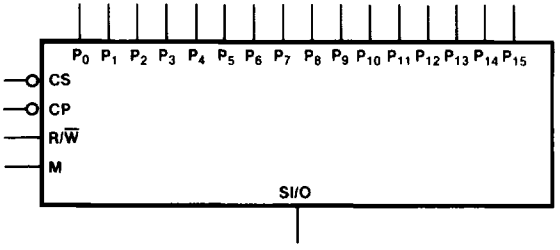
Description

The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-state serial output. In the serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

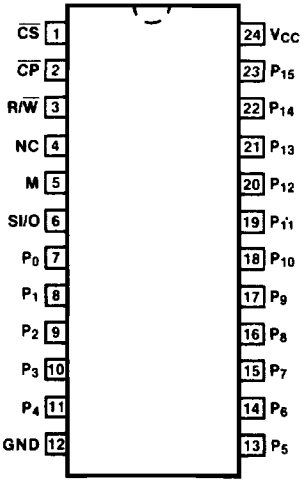
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-In, Serial-Out Converter**
- **Recirculating Serial Shifting**
- **Common Serial Data I/O Pin**
- ***Slim 24 Lead Package***

Ordering Code: See Section 5

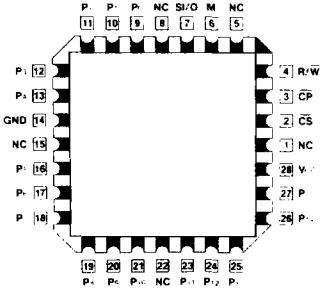
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_{15}	Parallel Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active LOW)	0.5/0.375
M	Mode Select Input	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SI/O	3-State Serial Data Input or 3-State Serial Output	1.75/0.375 75/15 (12.5)

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state.

Serial Load—data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output—the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-state buffer is active and represents the Q_{15} output.

To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

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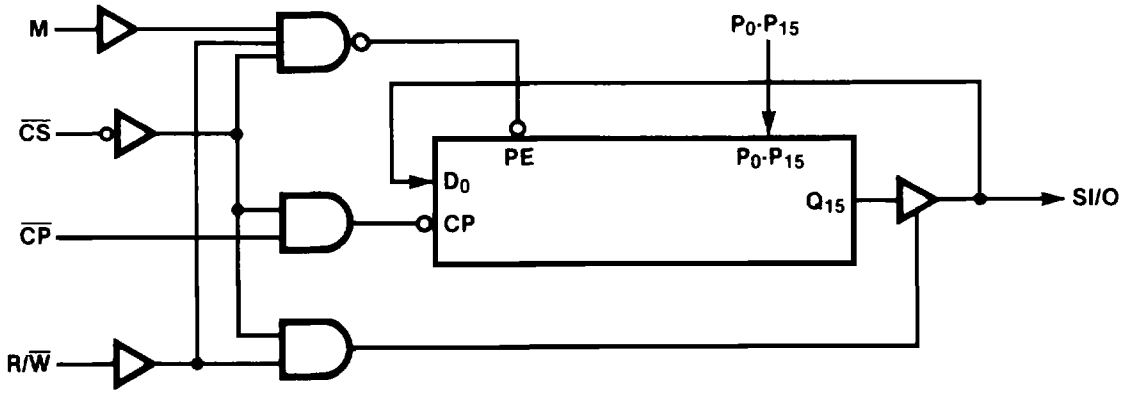
Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{M}$	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data In	Serial Load
L	H	L	↓	Data Out	Serial Output with Recirculation
L	H	H	↓	Active	Parallel Load; No Shifting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		53	80	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to SI/O		11.0 12.5						ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O		7.0 7.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O		7.0 7.0							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI/O to $\overline{CP}$	7.0 7.0							ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI/O to $\overline{CP}$	0 0								
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{CP}$	3.0 3.0							ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{CP}$	0 0								
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	5.0 5.0							ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	0 0								
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.0 5.0							ns	3-8