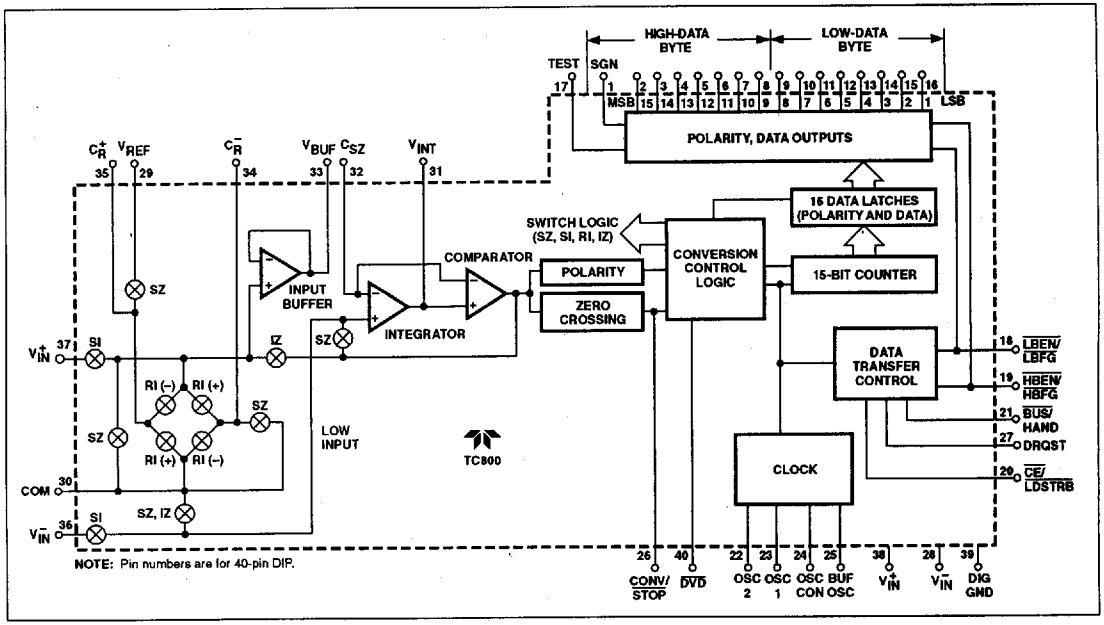
TELEDYNE COMPONENTS

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 15-Bit Resolution Plus Sign Bit
- Dynamic Range ..... 96 dB
- Integrating Dual-Slope Converter
  - — Monotonic
  - — Eliminates 50/60 Hz 'Line' Interference
  - — High-Noise Immunity
  - — Auto-Zero Cycle Eliminates Trimming
  - — Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three-State Data Bit/Sign Outputs
  - — 8-Bit or 16-Bit Parallel Data Transfer to µProcessor Bus
- UART Control Signals
  - — Serial Data Transmission
  - — 'Handshake' Data Transfer
  - — Distributed Control Systems
  - — Fiber-Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - — Data Valid Output Signal
  - — Continuous or Convert-on-Command Operation
- High-Impedance Differential Input
  - — Maximum Input Current ..... 15 pA
- Low Input Noise ..... 15 μV_{P-P}
- On-Chip Crystal Oscillator for 2.5 Conversions/Sec
  - — f_{XTAL} = 2.4576 MHz
  - — Integration Period (Rejects 50, 60, 400 Hz Interference Signals) ..... 100 ms
- Supply Operation ..... ±5V
  - — Low Power Dissipation ..... 20 mW
- Static-Discharge Protected Inputs
- Available in 60-Pin Flat Package

FUNCTIONAL DIAGRAM

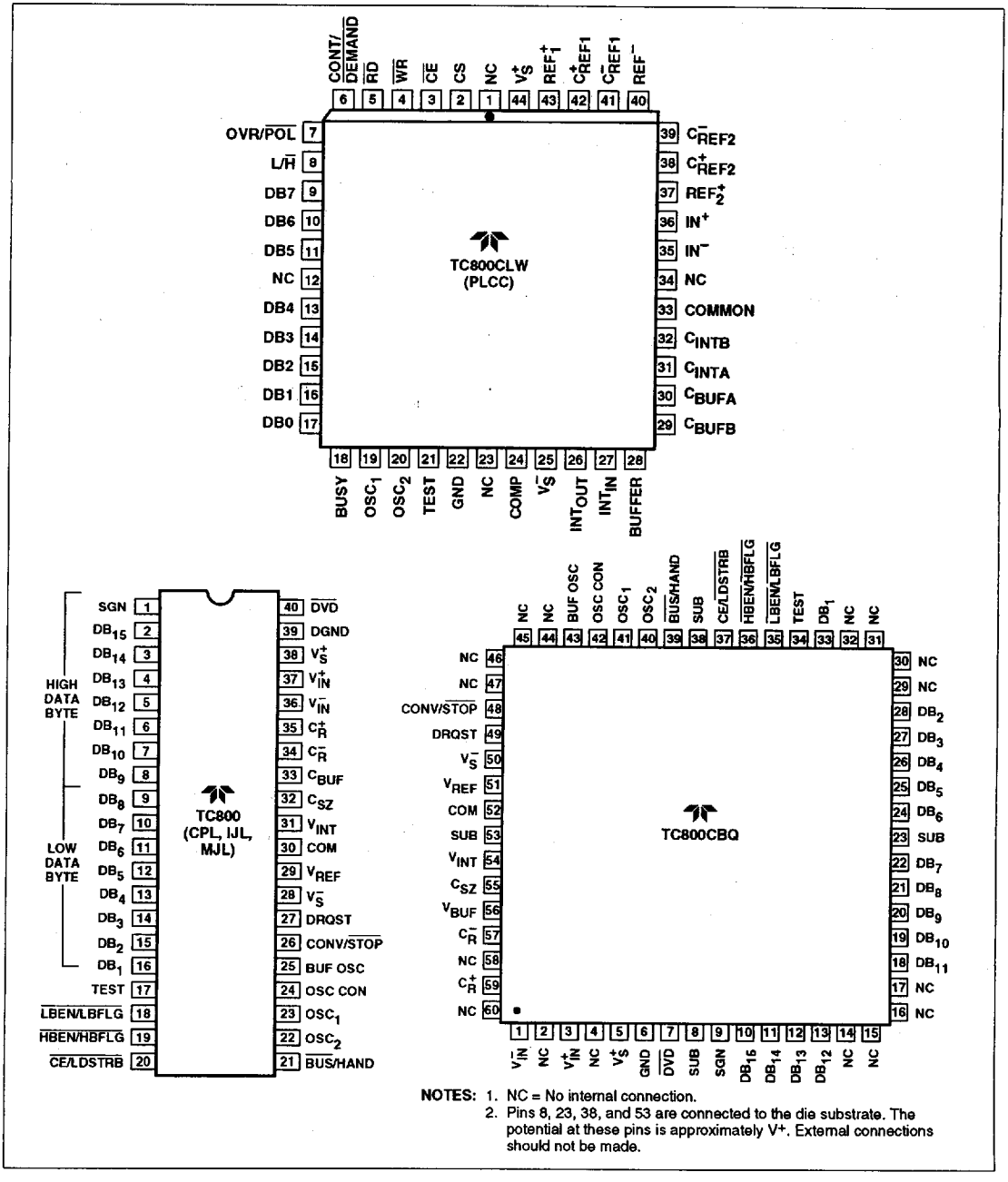


1814 D-03

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

PIN CONFIGURATIONS



NOTES: 1. NC = No internal connection.
2. Pins 8, 23, 38, and 53 are connected to the die substrate. The potential at these pins is approximately V+. External connections should not be made.

1815 D-04

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

GENERAL DESCRIPTION

The TC800 is a 15-bit plus sign, integrating analog-to-digital converter (ADC). It improves conventional two-cycle, dual-slope conversion by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to noise spikes that introduce conversion errors in successive approximation converters.

The externally-adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz, for maximum power-line noise rejection. Using the 2.4576 MHz crystal oscillator mode (2.5 conversions/sec), 50 Hz, 60 Hz, and 400 Hz signals are rejected.

Microprocessor interface signals support 1-byte (16-bit) or 2-byte (8-bit) parallel data transfers. A 'handshake' operating mode supports serial data transmission via a UART. A serial count output is derived by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber-optic transmission systems.

The high-impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range, and interface control signals make the high-resolution TC800 the ideal analog-to-digital converter for process control, data logging and 'intelligent' measurement systems.

See TC850 data sheet for applications requiring fast conversion rates.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC800CPL	40-Pin Plastic DIP	0°C to +70°C
TC800IJL	40-Pin CerDIP	–25°C to +85°C
TC800MJL	40-Pin CerDIP	–55°C to +125°C
TC800CLW	44-Pin Plastic Leaded Chip Carrier	0°C to +70°C
TC800CBQ	60-Pin Plastic Flat (Formed Leads)	0°C to +70°C

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_S^+ to GND) ..... +6.2V
Negative Supply Voltage (V_S^- to GND) ..... –9V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) ..... V_S^+ to V_S^-
Voltage Reference Input (V_{REF}) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ +0.3V to GND –0.3V
Package Power Dissipation
CerDIP ..... 1W @ +85°C
Plastic Packages ..... 0.5W @ +70°C
Ambient Operating Temperature Range
Plastic DIP (CPL, CBQ) ..... 0°C to +70°C
PLCC (CLW) ..... 0°C to +70°C
CerDIP (IJL) ..... –25°C to +85°C
(MJL) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, Conversion Rate = 2.5 Conversion/sec, Crystal Frequency = 2.4576 MHz, T_A = +25°C, Full-Scale Voltage = 3.2768V (Notes 1 and 3).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Input						
Zero-Scale Error		V_{IN} = 0V	—	—	±0.5	LSB
NL	Nonlinearity	Best Straight Line — Full Scale ≤ V_{IN} ≤ +Full Scale	—	1.3	2	LSB
		End Point — Full Scale≤ V_{IN} ≤ +Full Scale	—	2.8	—	LSB
DNL	Differential Nonlinearity		—	—	±0.5	LSB
I_{IN}	Input Current	V_{IN} = 0V, T_A = +25°C	—	5	15	pA
		0°C ≤ T_A ≤ +70°C	—	25	125	pA
		–25°C ≤ T_A ≤ +85°C	—	70	175	pA
		–55°C ≤ T_A ≤ +125°C	—	2.5	7.5	nA
V_{CMR}	Common-Mode Input Range	Over Operating Temperature Range	V_S^-+1.5	—	V_S^+–1	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = 0V, V_{CM} = ±1V	—	80	—	µV/V
	Full-Scale Gain Temperature Coefficient	External Ref Temperature Coefficient = 0 ppm/°C 0°C ≤ T_A ≤ +70°C	—	1.5	5	ppm/°C
	Zero-Scale Error Temperature Coefficient	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C	—	0.8	2	µV/°C
	Full-Scale Magnitude Symmetry Error	V_{IN} = 3.27V	—	—	2	LSB
e_N	Input Noise	Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
Conversion Speed			—	2.5	—	Conv/sec
V_{OH}	Output High Voltage	I_O = 100 µA	3.5	4.4	—	V
V_{OL}	Output Low Voltage	I_O = 1.6 mA (Note 2)	—	0.18	0.4	V
I_{OP}	Output Leakage Current	High-Impedance State	—	0.1	1	µA
I_{CP}	Control Pin Pull-Up Current	Pins 18, 19, 20; I_O = 750 µA Pin 21 = 0V, V_O = 2V	—	5	—	µA
V_{IH}	Input High Voltage	Pins 18–21, 26, 27	2.5	—	—	V
V_{IL}	Input Low Voltage	Pins 18–21, 26, 27	—	—	1	V

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

T-51-10-90

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Digital (Cont.)						
I_{IP}	Input Pin Pull-Up Current	Pins 26, 27; V = 2V	—	5	—	µA
		Pins 17, 24; V = 2V	—	25	—	µA
I_{ID}	Input Pin Pull-Down Current	Pin 21, V = 3V	—	5	—	µA
I_{OSC1}	Oscillator Output Current	V_O = 2.5V	—	1	—	mA
I_{BUFOSC}	Buffered Oscillator	V_O = 2.5V Output Current	—	5	—	mA
C_{IN}	Input Capacitance	Pins 18, 19	—	—	50	pF
t_{PW}	$\overline{BUS}$/ HAND Control Pin Minimum Pulse Width	Pin 21	70	—	—	ns
t_{WBE}	Byte-Enable Pulse Width	Note 1	350	200	—	ns
t_{WCE}	Chip-Enable Pulse Width	Note 1	400	250	—	ns
t_{ABE}	Byte-Enable Access Time	Note 1	—	200	350	ns
t_{ACE}	Chip-Enable Access Time	Note 1	—	250	400	ns
t_{DHB}	Data Hold From	Note 1 Byte-Enable Change	—	140	300	ns
t_{DHC}	Data Hold From	Note 1 Chip-Enable Change	—	240	400	ns
Power						
I_S^+	Positive Supply Current		—	2	3.5	mA
I_S^-	Negative Supply Current		—	2	3.5	mA

NOTES: 1. Parallel data transfer ($\overline{BUS}$/HAND = 0). See Figures 8 and 9.
2. For pins 18–20, I_O = 750 µA.
3. Crystal source (2.4576 MHz): DIGI-KEY Corp., Highway 32 South, P.O. Box 677, Thief River Falls, MN 56701-9988, Phone 1-800-344-4539, Part No. X047.

PIN DESCRIPTION

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
1	9	SGN	Sign Bit: 1 = positive input. The input signal polarity is determined at the end of the signal-integrate phase.
2	10	DB_{15}	Data Bit 15 (MSB)
3	11	DB_{14}	Data Bit 14
4	12	DB_{13}	Data Bit 13
5	13	DB_{12}	Data Bit 12
6	18	DB_{11}	Data Bit 11
7	19	DB_{10}	Data Bit 10
8	20	DB_9	Data Bit 9
9	21	DB_8	Data Bit 8
10	22	DB_7	Data Bit 7
11	24	DB_6	Data Bit 6
12	25	DB_5	Data Bit 5
13	26	DB_4	Data Bit 4
14	27	DB_3	Data Bit 3
15	28	DB_2	Data Bit 2
16	33	DB_1	Data Bit 1 (LSB)

Three-State Output Data Bits

NOTE: DB_{15}–DB_1 are at logic '1' for an overrange conversion.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
17	34	TEST	Test = 0V; Data outputs forced to logic '1' and clock is disabled. Test = V^+; Counter latches enabled.
18	35	$\overline{LBEN}$ / $\overline{LBFLG}$ (Input/Output)	A low data byte enable input or flag output, depending on $\overline{BUS}$/ HAND (pin 21) status. (1) $\overline{BUS}$/ HAND = 0: With pin 21 low and $\overline{CE}$/ $\overline{LDSTRB}$ = 0 (pin 20), data bits 8 through 1 (pins 9–16) are output when $\overline{LBEN}$ = 0. (2) $\overline{BUS}$/ HAND = 1: Valid data on pins 9–16 is indicated by flag output, LBFLG = 0.
19	36	$\overline{HBEN}$/ $\overline{HBFLG}$ (Input/Output)	A high data byte enable input or flag output, depending on $\overline{BUS}$/ HAND (pin 21) status. (1) $\overline{BUS}$/ HAND = 0: With pin 21 low and $\overline{CE}$/ $\overline{LDSTRB}$ = 0 (pin 20), the high data byte (sign bit plus data bits 15–9) are output when $\overline{HBEN}$ = 0. (2) $\overline{BUS}$/ HAND = 1: Valid data on pins 1–8 is indicated by flag output, HBLFG = 0.
20	37	$\overline{CE}$/ $\overline{LDSTRB}$ (Input/Output)	(1) $\overline{BUS}$/ HAND = 0: $\overline{CE}$ is master chip enable. With $\overline{CE}$ = 1, sign bit plus data bits 15–1 are disabled (high-impedance state). $\overline{CE}$ = 0 enables outputs and data is transferred under control of $\overline{LBEN}$ and $\overline{HBEN}$.

$\overline{CE}$	$\overline{LBEN}$	$\overline{HBEN}$	Function
0	0	1	Low Data Byte Output
0	1	0	High Data Byte Output
0	0	0	Low + High Data Byte Output
0	1	1	High-Impedance State

(2) $\overline{BUS}$/ HAND = 1: $\overline{LDSTRB}$ is a load strobe output sign. In the handshake mode, $\overline{LDSTRB}$ = 0 instructs the receiving device to accept data.

21	39	$\overline{BUS}$/ HAND	(1) $\overline{BUS}$ = 0: Parallel output data mode, where $\overline{CE}$, $\overline{HBEN}$, and $\overline{LBEN}$ directly control the 16 data bits. (2) HAND = 1: $\overline{LDSTRB}$, $\overline{LBFLG}$, $\overline{HBFLG}$ are used in the handshake data transfer mode. (3) HAND = ⎍ (pulsed high): Causes entry into handshake mode for UART interfacing.
22	40	OSC_2	Oscillator input.
23	41	OSC_1	Oscillator output.
24	42	OSC CON	Selects internal oscillator structure. (1) OSC CON = 1: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC. (2) OSC CON = 0: Crystal oscillator. Internal clock frequency is frequency at BUF OSC 415.
25	43	BUF OSC	Buffered oscillator output
26	48	CONVERT / $\overline{STOP}$	CONVERT = 1: Conversions performed continuously. $\overline{STOP}$ = 0: Conversion process stops 7 counts before entering signal-integrate phase. The conversion in progress when $\overline{STOP}$ = 0 is completed.
27	49	DRQST	Data request signal. Used in handshake mode to indicate an external device is ready to accept data. If DRQST is not used, connect to V_S^+.
28	50	V_S^-	Negative power supply.
29	51	V_{REF}	Voltage reference input.
30	52	COM	Analog common. The TC800 is auto-zeroed to the analog common potential.
31	54	V_{INT}	Integrator output.
32	55	C_{SZ}	System-zero capacitor.
33	56	V_{BUF}	Output of input signal buffer.
34	57	C_R^-	Negative Reference capacitor.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
35	59	C_R^+	Positive Reference capacitor.
36	1	V_{IN}^-	Negative differential analog input.
37	3	V_{IN}^+	Positive differential analog input.
38	5	V_S^+	Positive power supply
39	6	GND	Digital ground. Ground return point for digital logic.
40	7	DVC	Data valid signal. DVC = 1 during signal-integrate and reference-integrate phases until data is latched. DVC = 0 when in auto-zero phase; data does not change.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC800 is a dual-slope, integrating ADC. An understanding of the dual-slope conversion technique will aid in following the detailed operation theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration).

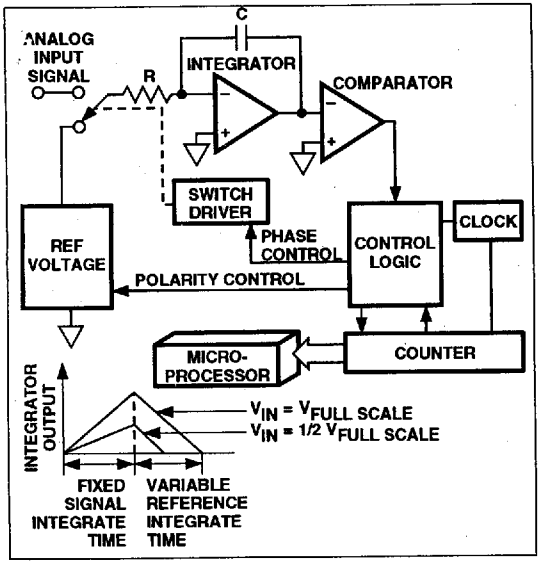


Figure 1 Basic Dual-Slope Converter

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity, constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter (Figure 1), a complete conversion requires the integrator output to 'ramp-up' and 'ramp-down.'

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation related the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} v_{IN}(t)\,dt = \frac{V_R t_{RI}}{RC}$$

where: V_R = Reference voltage
t_{SI} = Signal integration time
t_{RI} = Reference voltage integration time (variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right]$$

ANALOG SECTION DESCRIPTION

System-Zero Phase

During system-zero phase (Figure 2), errors due to buffer, integrator, and comparator offset voltages are compensated for by charging system-zero capacitor (C_{SZ}) with a compensating error voltage. With zero input voltage, the integrator output remains at zero.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

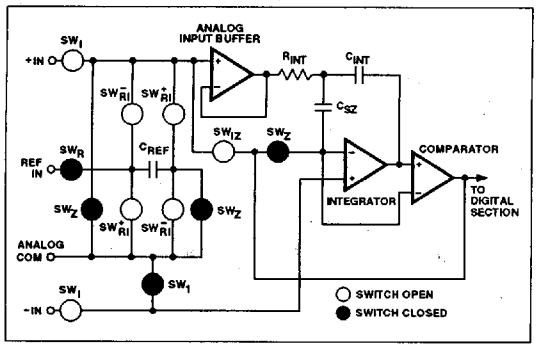


Figure 2 System-Zero Phase

The external input signal is disconnected from internal circuitry by opening two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges C_{SZ} with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages.

Input Signal-Integration Phase

The TC800 integrates differential voltage between the (+) and (–) inputs (Figure 3). The differential voltage must be within the device common-mode range; 1V from either supply rail, typically. The input signal is integrated for 16,384 clock cycles.

The input signal polarity is determined at the end of the phase.

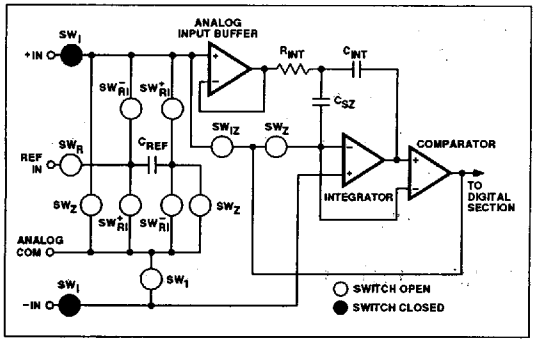


Figure 3 Input Signal Integration Phase

Reference Voltage Integration Phase

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. The phase lasts for a maximum of 32,768 clock periods. (See Figure 4.)

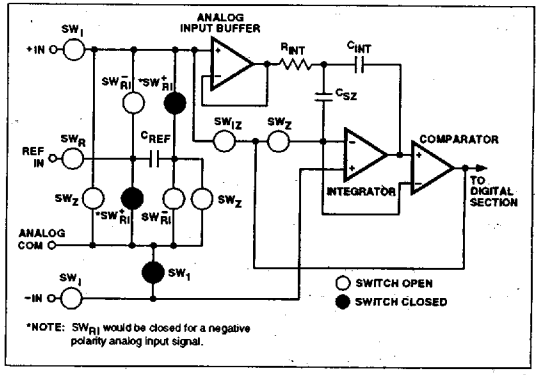


Figure 4 Reference Voltage Integration Phase

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system-zero phase is entered and that true system offset voltages are compensated for. This phase normally lasts 4096 clock cycles. (See Figure 5.)

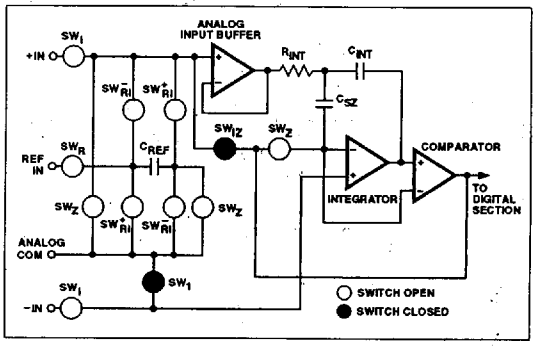


Figure 5 Integrator Output Zero Phase

Differential Inputs V_{IN}^+ (Pin 37) and V_{IN}^- (Pin 36)

The TC800 operates with differential voltages within the input amplifier common-mode range, extending from 1V below V_{IN}^+ to 1V above V_{IN}^-. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used by the positive common-mode voltage. For these critical applications, the integrator output swing can be reduced to within 0.4V of either supply without loss of linearity.

Analog Common

Analog common (COM, pin 30) is used as the V_{IN}^- return during system-zero and reference-integrate phases. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, V_{IN}^- will be set at a fixed, known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

DIGITAL SECTION DESCRIPTION

Digital Control Signals

$\overline{\text{BUS}}$ / HAND

The $\overline{\text{BUS}}$ / HAND input (pin 21) selects parallel bus data transfer mode or handshake transfer mode. An internal pull-down resistor guarantees parallel mode operation when the input pin is open. The handshake mode allows serial data transmission with a UART. In parallel mode, the TC800 outputs data under control of the $\overline{\text{HBEN}}$ (pin 19), $\overline{\text{LBEN}}$ (pin 18), and $\overline{\text{CE}}$ (pin 20) signals. In the handshake mode, the TC800 output signals communicate with peripheral devices to control data transmission.

For $\overline{\text{BUS}}$ = 0, $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$, and $\overline{\text{CE}}$ input signals control data transmission. Figures 8 and 9 show typical timing relationships and operation. The $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$, and $\overline{\text{CE}}$ signals are asynchronous to the internal conversion clock. Output data is immediately accessed. To avoid accessing data as updates are occurring, the data valid ($\overline{\text{DVD}}$, pin 40) signal can be used as an enable signal. Data will not change if $\overline{\text{DVD}}$ = 0.

In handshake mode, two data transfer methods are possible. If HAND is pulsed high (HAND = ⎍) for a minimum of 70 ns, the TC800 enters the handshake mode. If HAND = 1 continuously, the parallel mode is not re-entered, and a handshake data transfer will occur at the end of each conversion cycle.

The $\overline{\text{BUS}}$ / HAND input configures dual-purpose pins 18, 19, and 20 as inputs or outputs. In conjunction with the data request input signal, handshake data transfer is controlled by output signals $\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$, and $\overline{\text{LDSTRB}}$. (See Table I.)

Data Request Input

The data request (DRQST, pin 27) input is used only in the handshake data transfer mode. DRQST = 1 indicates an external receiving device is ready to accept data from the TC800. It serves as a send data command. When $\overline{\text{BUS}}$ / HAND = 0, DRQST should be tied to V_S^+.

Table I (Pin designations refer to 40-Pin DIP)

	Pin Description		
Operating Mode	**$\overline{\text{LBEN}}$ / $\overline{\text{LBFLG}}$ (Pin 18)**	**$\overline{\text{HBEN}}$ / $\overline{\text{HBFLG}}$ (Pin 19)**	**$\overline{\text{CE}}$ / $\overline{\text{LDSTRB}}$ (Pin 20)**
Bus Transfer Mode $\overline{\text{BUS}}$ / HAND = 0	$\overline{\text{LBEN}}$: Low data byte enable input. Logic '0' activates low-order data (DB_8–DB_1) if $\overline{\text{CE}}$ = 0.	$\overline{\text{HBEN}}$: High data byte enable input. Logic '0' activates the high order data (SGN, DB_{15}–DB_9) if $\overline{\text{CE}}$ = 0.	$\overline{\text{CE}}$: Master output enable input. When $\overline{\text{CE}}$ = 1 outputs SGN, DB_{15}–DB_1 are disabled and in a high-impedance state
Handshake Transfer Mode $\overline{\text{BUS}}$ / HAND = 1 or ⎍	$\overline{\text{LBFLG}}$: Low data byte flag output. Indicates output data is DB_8–DB_1.	$\overline{\text{HBFLG}}$: High data byte flag output. Indicates output data is DB_{15}–DB_9.	$\overline{\text{LDSTRB}}$: Load strobe output signal. A logic '0' or falling edge indicates valid data is present at the output.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

CONV / $\overline{\text{STOP}}$ Input

The CONV / $\overline{\text{STOP}}$ input (pin 26) is pulled high through an internal pull-up resistor. If CONV / $\overline{\text{STOP}}$ = 1, or is left open, the TC800 continuously performs conversions. Each measurement cycle is 65,536 counts long. The measurement cycle time for one conversion is:

$$\text{Time Conversion (ms)} = \frac{65{,}536}{f_{CLK}\ (\text{kHz})},$$

where f_{CLK} = internal clock frequency.

If CONV / $\overline{\text{STOP}}$ = 0 during reference-integrate phase and after zero-crossing has been detected, the integrator-zero phase is immediately entered and completed. This eliminates the time spent in the reference-integrate phase after the output data latches are updated.

If CONV / $\overline{\text{STOP}}$ remains low, the TC800 will wait in the system-zero phase. The signal-integrate phase begins 7 clock counts after a CONV = 1 signal is detected. The CONV / $\overline{\text{STOP}}$ signal is detected synchronously with the internal clock. The system-zero phase should last a minimum of 70 ms. (See Figures 6 and 7 for CONV / $\overline{\text{STOP}}$ conversion timing diagrams.)

If CONV / $\overline{\text{STOP}}$ goes low and remains low during the system-zero phase, the TC800 will stop at the end of the phase and wait for CONV = 1. The signal-integrate phase will start 7 clock counts after CONV = 1 is detected.

TEST Input

When TEST (pin 17) = 1, the counter data latches are enabled. When TEST = 0, the counter outputs are forced to a logic '1' state and the internal clock is disabled. When TEST is returned to logic '1' and one clock pulse is applied, all counter outputs are clocked low.

Data Valid

Data valid ($\overline{\text{DVD}}$, pin 40) = 1 at the start of signal integrate and $\overline{\text{DVD}}$ = 0 one-half clock period after new data is stored in the data latches. Since $\overline{\text{DVD}}$ is always low when data is not changing, the signal may be used as a 'Data Valid Flag.' (See Figures 6 and 7 for timing relationships.)

DATA OUTPUT DESCRIPTION

Parallel Mode Data Interface

With $\overline{\text{BUS}}$ / HAND = 0, the sign and data bits are controlled by the $\overline{\text{CE}}$, $\overline{\text{LBEN}}$, and $\overline{\text{HBEN}}$ inputs. All three have internal pull-up resistors. Inactive data bits are in a high-impedance state.

The $\overline{\text{HBEN}}$ signal controls the most significant data bytes (SGN, DB_{15}–DB_9). $\overline{\text{LBEN}}$ controls the least significant data bytes (DB_8–DB_1).

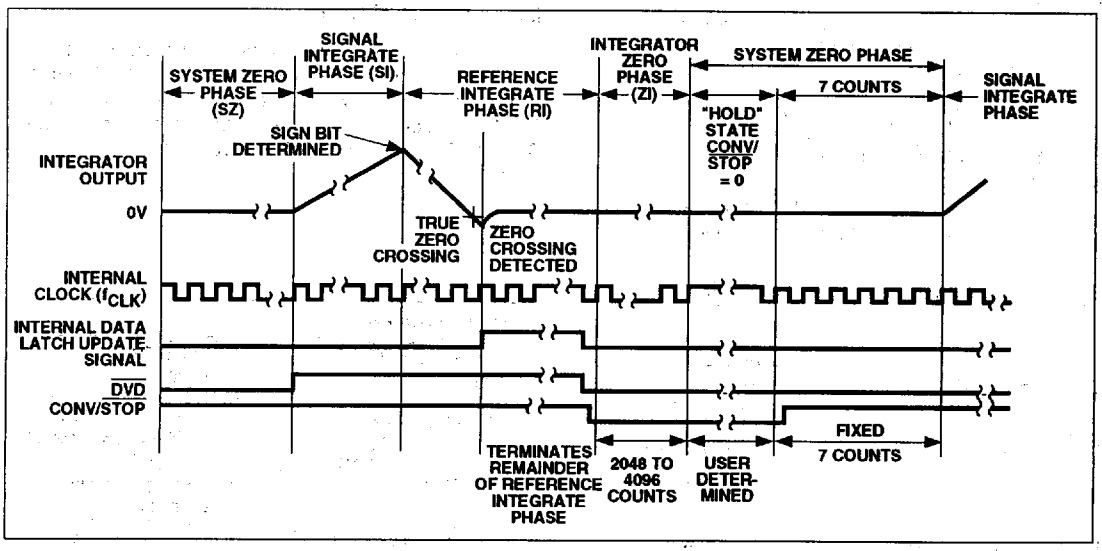


Figure 6 **Convert-on-Command Operation** (CONV / $\overline{\text{STOP}}$ = 0 After Zero Crossing Detected)

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

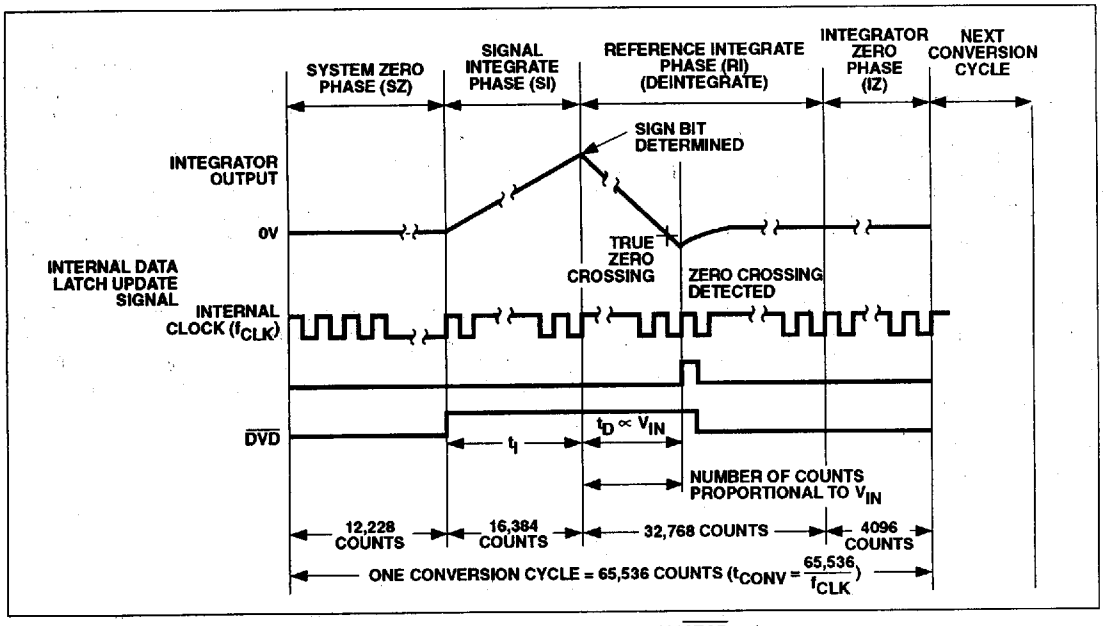


Figure 7 Continuous Conversion (CONV / $\overline{STOP}$ = 1)

Table II

CE	$\overline{HBEN}$	$\overline{LBEN}$	High Data Byte (SGN, DB_{15}–DB_9)	Low Data Byte (DB_8–DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive High Z State)

NOTE: X = 1 or 0.

The $\overline{HBEN}$, $\overline{LBEN}$, and $\overline{CE}$ inputs are asynchronous with the internal conversion clock. Output data is immediately available. To avoid accessing data as updates occur, the $\overline{DVD}$ input can control data access. Data will not change if DVD = 0.

Handshake Mode Data Transfer

The TC800 actively controls data transfer to peripherals through the handshake data transfer mode. In the handshake mode, pins 18, 19, and 20 (LBFLG, HBFLG, and $\overline{LDSTRB}$) are TTL-compatible outputs. The $\overline{LDSTRB}$ signal indicates valid data is available for the peripheral. The LBFLG and HBFLG signals indicate which data byte is being transferred. The data request signal (DRQST, pin 27) informs the TC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

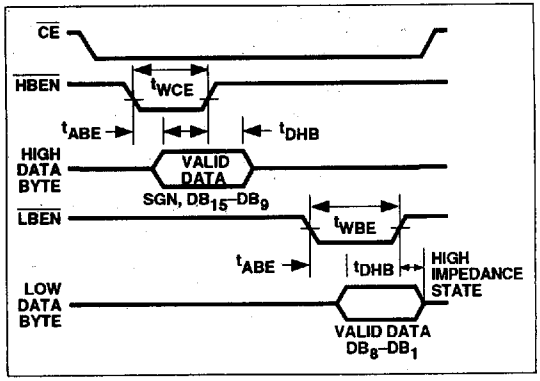


Figure 8 Parallel Data Transfer (Two 8-Bit Bytes)

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

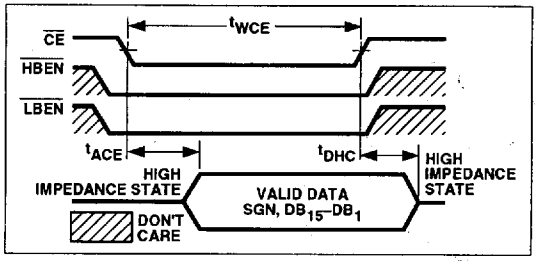


Figure 9 Parallel Data Transfer (16-Bit Bytes)

The $\overline{BUS}$ / HAND signal is ignored after the handshake mode is entered. Conversions continue, but data latch updating is inhibited until the TC800 transfers two data bytes and clears the internal mode latch.

The handshake mode is entered in two ways:

(1) Set $\overline{BUS}$ / HAND = 1

(2) Pulse $\overline{BUS}$ / HAND High (_┌┐_)

$\overline{BUS}$ / HAND = 1

With $\overline{BUS}$ / HAND = 1, the TC800 enters the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch signal is set, the $\overline{BUS}$ / HAND signal is ignored. The DRQST signal controls data transfer to the external requesting peripheral. Figure 10 shows the timing diagram for the data transfer with $\overline{BUS}$ / HAND = 1 (throughout the transfer). Note that DRQST = 1 throughout the transfer. The data transfer rate is set by the TC800 internal clock. A complete data transfer occurs in 4 clock periods after a DRQST = 1 is detected on a high-to-low internal clock-edge transition.

For peripherals that cannot accept data at the TC800 clock rate, the DRQST input can be used to delay the transmit sequence. This mode is useful in interfacing to UARTs. Figure 11 shows a typical UART interface.

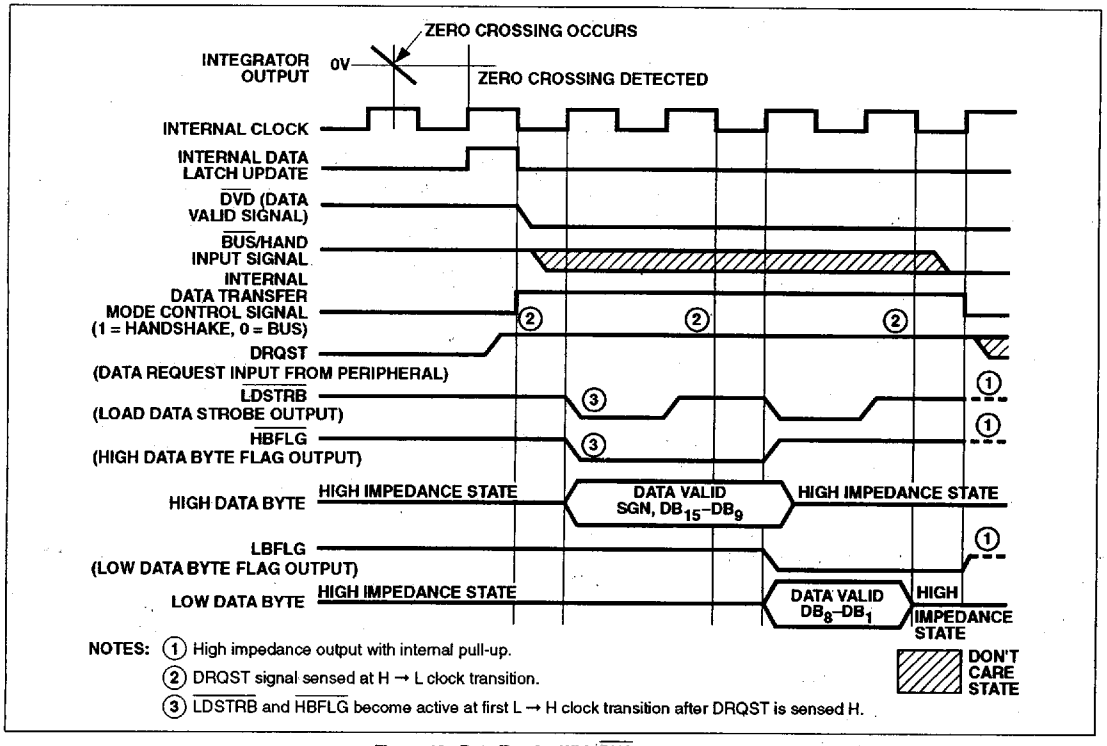


Figure 10 Data Trasfer With $\overline{BUS}$ / HAND = 1

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

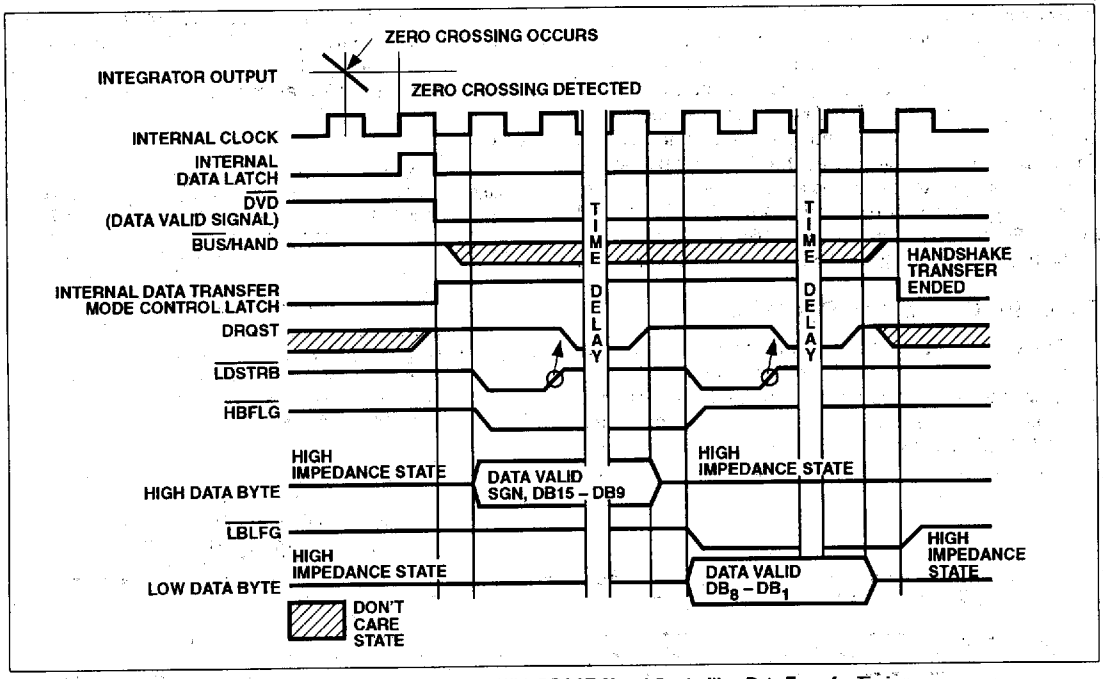
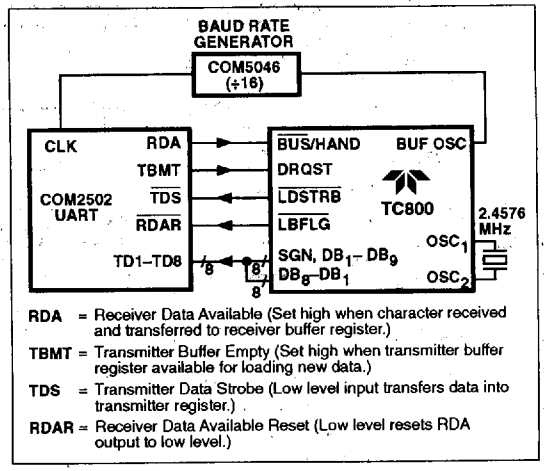


Figure 11A Typical UART Interface Timing With DRQST Signal Controlling Data Transfer Timing

The UART data transfer sequence begins with DRQST = 1, indicating the UART transmitter buffer register is empty (TBMT = 1). LDSTRB and HBFLG become active when DRQST is sensed synchronously. The high-order data byte is stored in the UART transmitter buffer register when LDSTRB = 1. This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low, halting the cycle with the SGN and DBN_{15}–DB_9 data bits active. After the UART transfers the received data to the transmitter register, DRQST (TBMT) goes high. On the first high-to-low internal clock transition, the high data byte is disabled and one-half clock period later HBFLG = 1. Concurrently, LDSTRB = 0 and DB_8–DB_1 become active. One clock period later, LDSTRB = 1 and the low data byte is clocked into the UART transmitter buffer register; DRQST goes low. When DRQST returns high, it is sensed on the first TC800 internal clock high-to-low edge transition, thus causing all outputs to be disabled. One-half clock period later the internal handshake mode latch is cleared and LDSTRB = HBFLG = LBFLG = 1. The outputs remain active as long as BUS / HAND = 1.



RDA = Receiver Data Available (Set high when character received and transferred to receiver buffer register.)

TBMT = Transmitter Buffer Empty (Set high when transmitter buffer register available for loading new data.)

TDS = Transmitter Data Strobe (Low level input transfers data into transmitter register.)

RDAR = Receiver Data Available Reset (Low level resets RDA output to low level.)

Figure 11B Typical UART to TC800 Connection

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

$\overline{BUS}$ / HAND = ⎍⎍ (Pulse High)

The TC800 outputs every conversion (except those completed during a handshake transfer) with BUS / HAND held high. Handshake output sequences on demand are possible by triggering the BUS / HAND control input with a low-to-high edge. Figure 12 shows a typical data transfer. The output cycle is controlled by the DRQST input signal. The complete 2-byte data transfer can take any length of time. Conversions are made, and the DVD and CONV / $\overline{STOP}$ inputs function normally, but new data will not be latched until the handshake mode is terminated.

Oscillator Control and Operation

The OSC CON input (pin 24) configures the internal oscillator as a crystal or RC oscillator. OSC CON = 1 establishes the RC oscillator; R should be 50 kW or larger. The internal clock matches the frequency and phase of the BUF OSC (pin 25) signal. In the crystal oscillator mode (OSC CON = 0), a 415 is between the buffered oscillator output and the internal clock. The internal oscillator may be overdriven by driving OSC_1 (pin 23). The OSC CON pin controls whether the internal clock is 415. (See Table III.)

Table III

Oscillator Type	OSC CON (Pin 24)	Internal Clock Frequency	Signal Integration Time	Conversion Cycle Time
RC	V_S^+ or Open	0.45/RC	$16{,}384\left(\frac{RC}{0.45}\right)$	$\frac{RC}{0.45}(65{,}536)$
Crystal	Ground	f_{XTAL} 415	$16{,}384\left(\frac{15}{f_{XTAL}}\right)$	$\frac{15}{f_{XTAL}}(65{,}536)$

NOTES: 1. f_{XTAL} = crystal frequency (2.4576 MHz)
2. Internal clock frequency = 163.8 kHz
3. Signal integration time = 1000 ms
4. Conversion cycle time = 400 ms (2.5 conversions/sec)

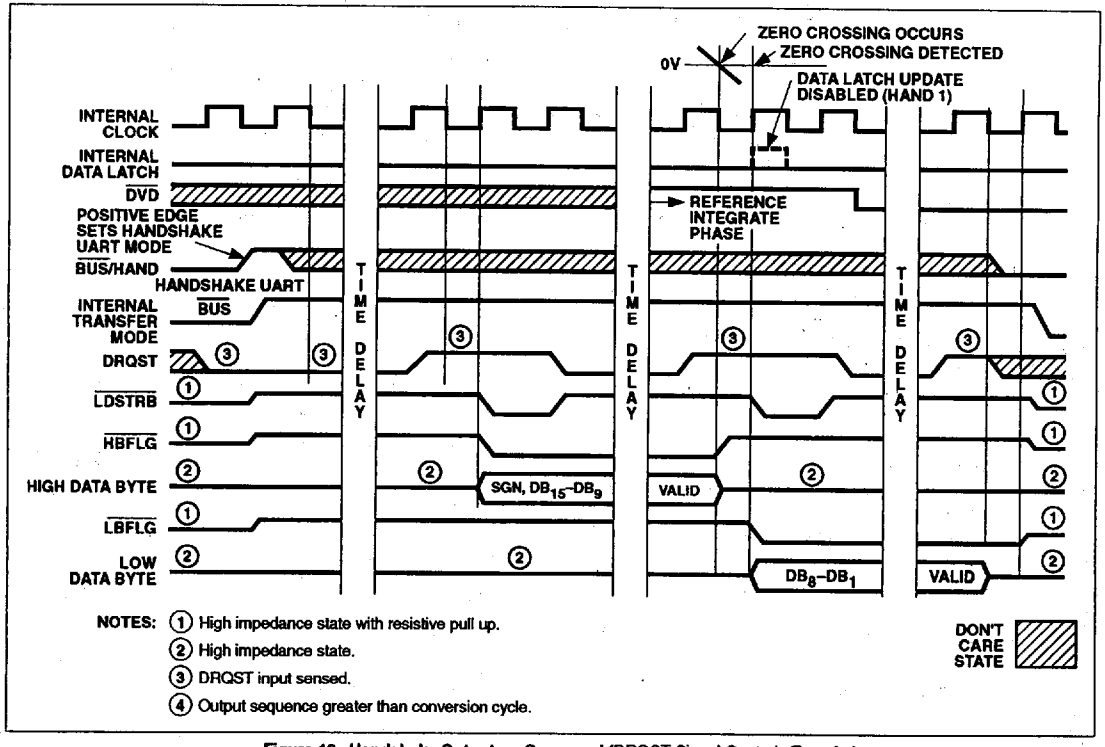


Figure 12 Handshake Output on Command (DRQST Signal Controls Transfer)

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

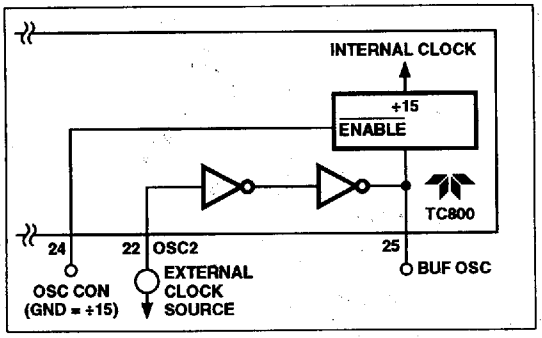


Figure 13 External Oscillator Control

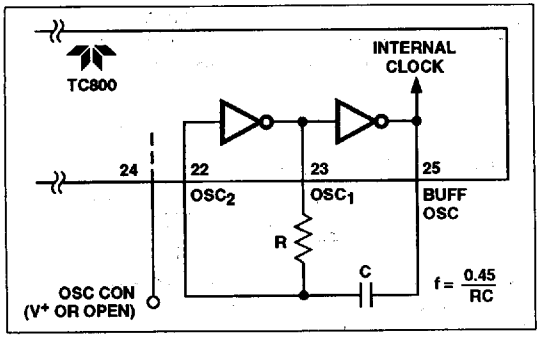


Figure 14 Internal RC Oscillator Configuration

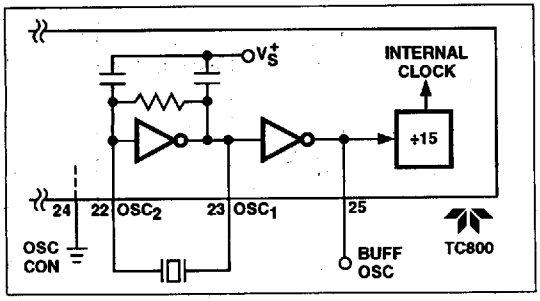


Figure 15 Internal Crystal Oscillator Configuration

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal Class A output stage amplifiers supply a 20 µA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 µA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Full-Scale Input Voltage (V_{FS})	R_{INT}
3.2768	160 kW
4.0000	200 kW

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4V of V_S^+ or V_S^- without saturating. With ±5V power supplies and analog common connected to supply ground, a 3.5V to 4.3V swing is adequate.

Using the suggested 20 µA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT}\ (\mu F) = \frac{16{,}384\left(\frac{1}{f_{CLK}\,(kHz)}\right)20\ \mu A}{\text{Integrator Output Voltage Swing (V)}},$$

where f_{CLK} = Internal clock frequency.

For 2.5 conv/sec, the internal clock frequency is 163.8 kHz. The TC800 operates at 2.5 conv/sec with an external crystal equal to 2.4576 MHz. A 0.47 µF capacitor is recommended.

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested. The outer foil of C_{INT} should be connected to pin 31.

System Zero Capacitor (C_{SZ})

A 1 µF polypropylene capacitor is suggested. The inner foil should be connected to C_{SZ} (pin 32).

Reference Capacitor (C_{REF})

A 1 µF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene or Teflon® should be used.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

T-51-10-90

TC800

Reference Voltage

The analog input required to generate the 32,768 full-scale count is $V_{IN} = 2\ V_{REF}$. The reference voltage source should be selected for temperature stability. The TC800 provides 30 ppm resolution. With a 5 ppm/°C reference, a 6° change will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed.

The reference voltage input must be a positive voltage with respect to analog common. Reference voltage circuits are shown in Figure 16.

Delay Resistor (R_S)

The R_S, C_{INT} combination compensates for comparator delay time. With a 0.47 µF integrating capacitor, a 20W series resistor is suggested.

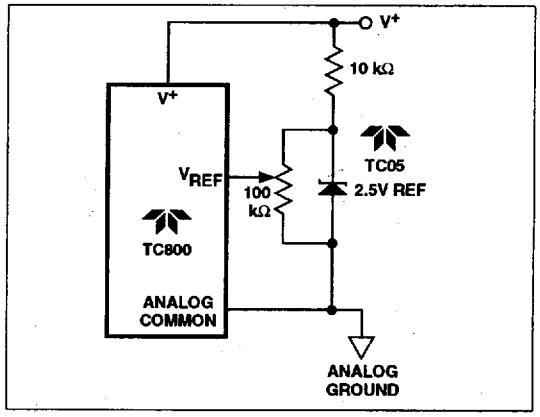
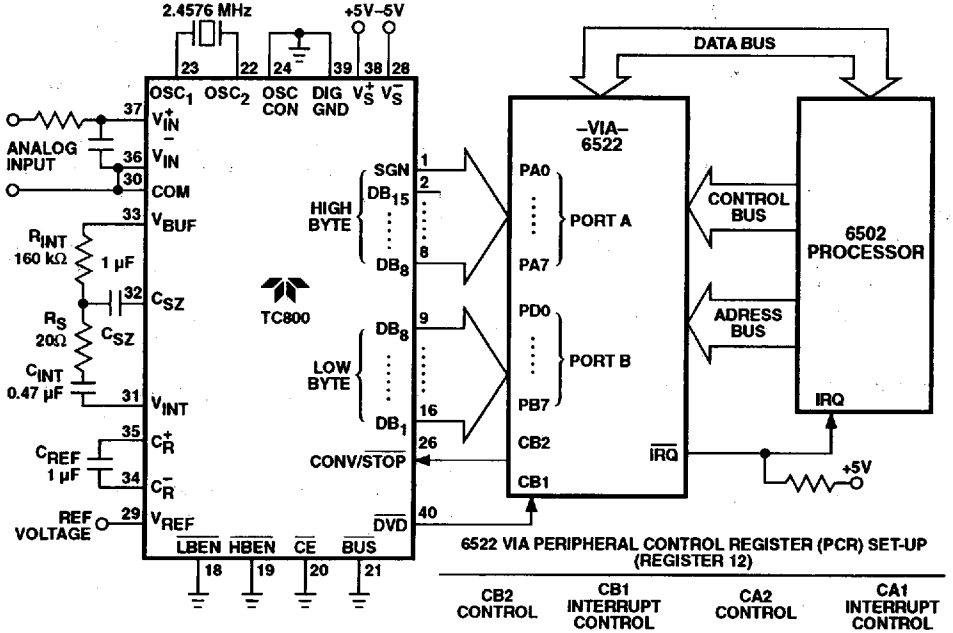


Figure 16 Reference Voltage Circuits

TYPICAL APPLICATIONS

TC800 Parallel Interface to 6522 Versatile Interface Adapter



6522 VIA PERIPHERAL CONTROL REGISTER (PCR) SET-UP (REGISTER 12)

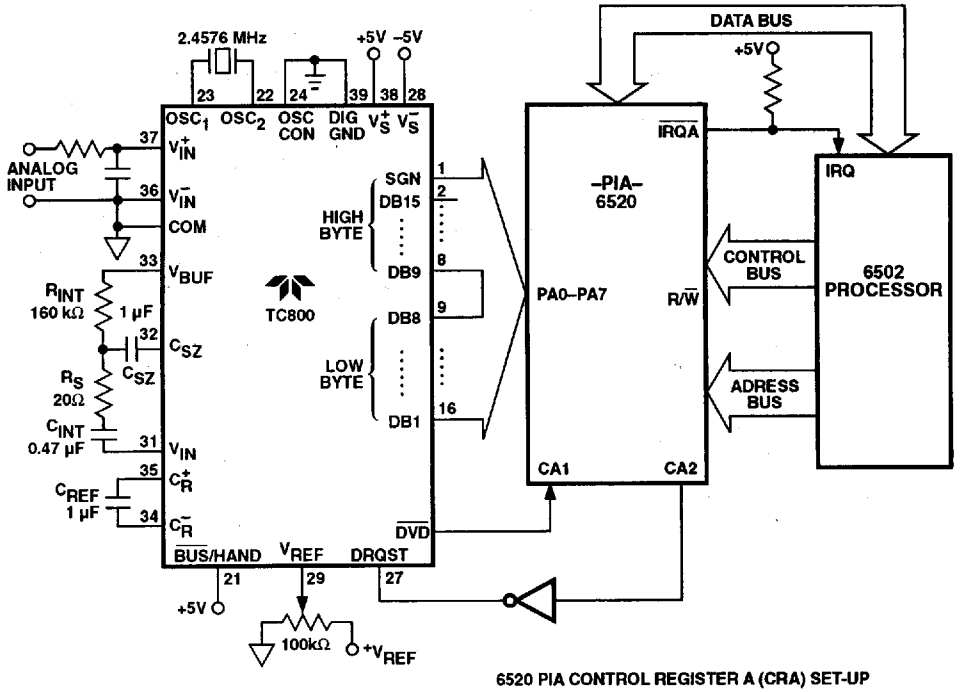
CB2 CONTROL		CB1 INTERRUPT CONTROL		CA2 CONTROL			CA1 INTERRUPT CONTROL
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0/1*	–	–	–	–	–

*NOTE: May be programmed for convert on command or continuous conversions.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TYPICAL APPLICATIONS (Cont.)

TC800 Interface to 6520 VIA



6520 PIA CONTROL REGISTER A (CRA) SET-UP

IRQA1	IRQA2	CA2 CONTROL			DDRA ACCESS	CA1 CONTROL	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	1	0	0	0	0	1

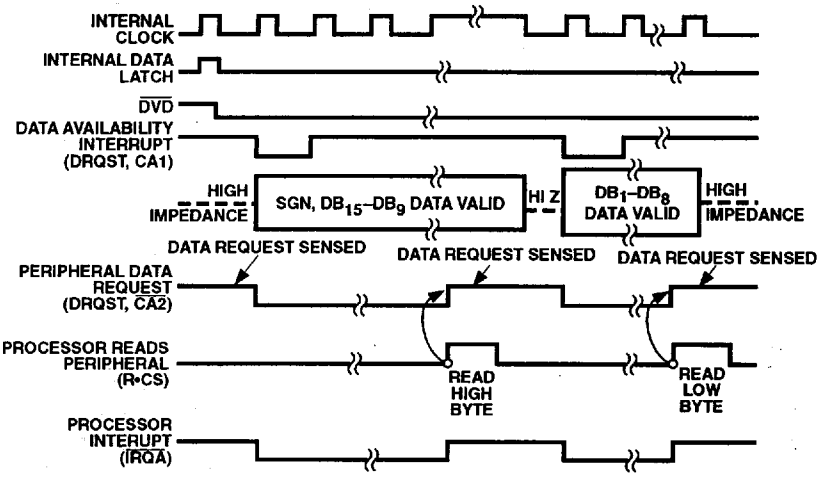
- Set by a negative CA1 transmission. reset by a read port A operation.
- CA2 is set high on negative CA1 transmission. A port A read operation sets CA2 low.
- Port A conf-gured as input.
- IRQA output enabled — goes low when Bit 7 in CRA is set by negative transition of signal on CA1.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

TC800

TYPICAL APPLICATIONS (Cont.)

TC800 to 6520 Peripheral Interface Adapter Handshake Timing Diagram



NOTE: Data from every conversion is transmitted in 2 bytes. (Data read cycle is less than conversion time.)