54F/74F269

8-Bit Bidirectional Binary Counter

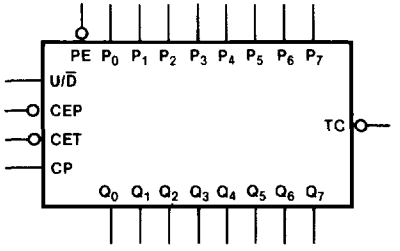
Description

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

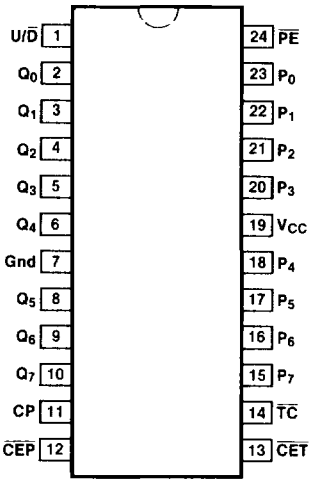
- **Synchronous Counting and Loading**
- **Built-In Lookahead Carry Capability**
- **Count Frequency 100 MHz Typ**
- **Supply Current 80 mA Typ**
- **300 mil Slimline Package**

Ordering Code: See Section 5

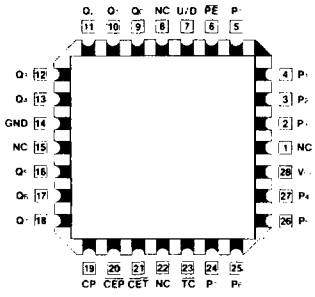
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

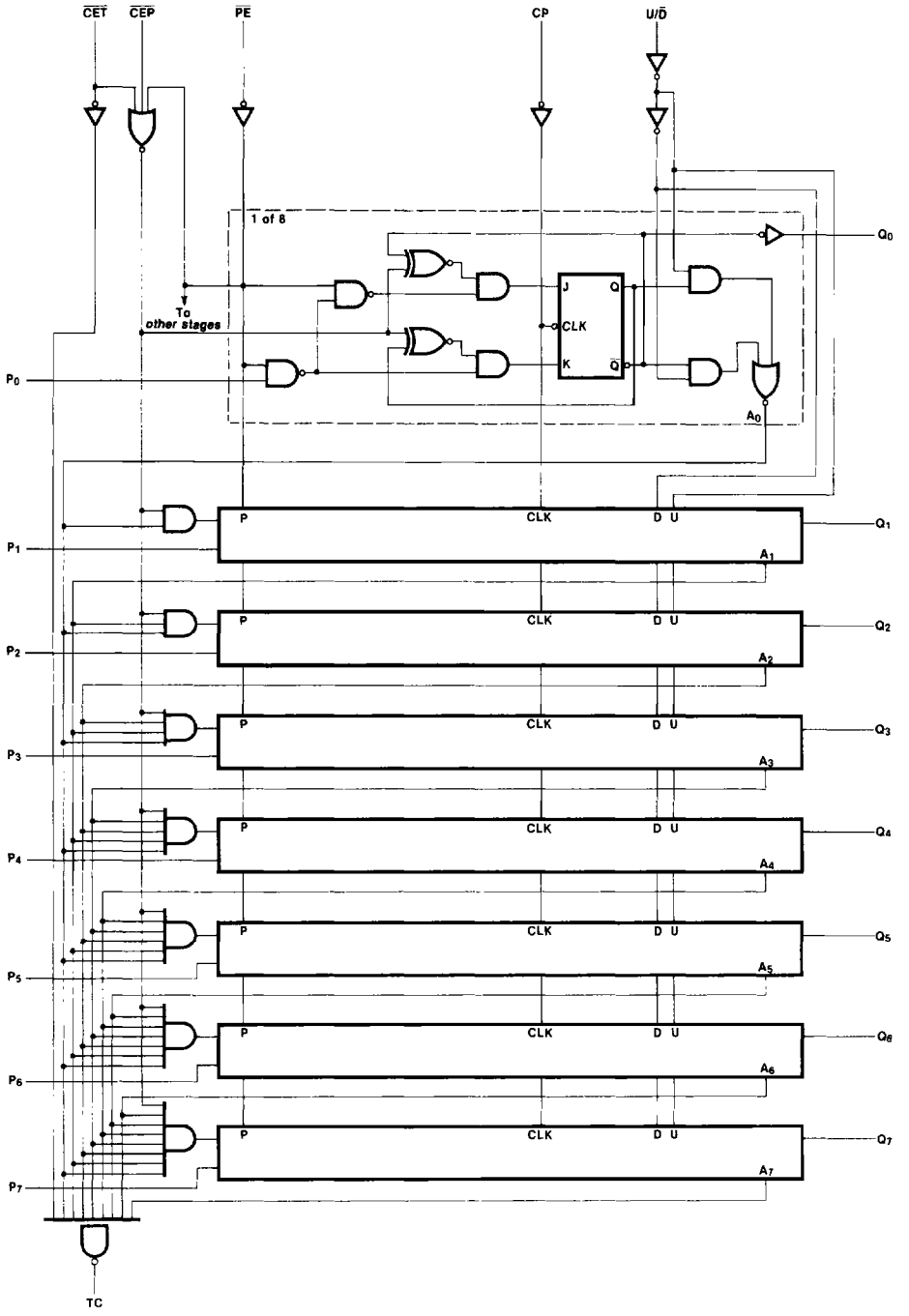


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_7	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.375
CP	Clock Input	0.5/0.375
$\overline{TC}$	Terminal Count Output (Active LOW)	0.5/0.375
Q_0-Q_7	Flip-Flop Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	Function
L	X	X	X	↑	Parallel Load all Flip-Flops
H	H	X	X	↑	Hold
H	X	H	X	↑	Hold ($\overline{TC}$ held HIGH)
H	L	L	H	↑	Count Up
H	L	L	L	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = Transition LOW-to-HIGH

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		50	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			80	100		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n			10.0 10.0					ns	3-1 3-7
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$			15.0					ns	3-1 3-2
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$			15.0					ns	3-1 3-2
t_{PHL}	Propagation Delay CP to $\overline{TC}$			15.0					ns	3-1 3-2

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	5.0 5.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	12.0 12.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	10.0 10.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	0 0				
$t_w(H)$	Clock Pulse Width, HIGH	5.0			ns	3-7

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