DEVICES INCORPORATED

L2330
Coordinate Transformer

FEATURES

- ❑ Rectangular-to-Polar or Polar-to-Rectangular at 50 MHz
- ❑ 24-Bit Polar Phase Angle Accuracy
- ❑ Replaces Fairchild TMC2330A
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Package Styles Available:
  - 120-pin Plastic Quad Flatpack
  - 120-pin Ceramic PGA

DESCRIPTION

The **L2330** is a coordinate transformer that converts bidirectionally between Rectangular and Polar coordinates.

When in Rectangular-to-Polar mode, the L2330 is able to retrieve phase and magnitude information or backward map from a rectangular raster display to a radial data set.

When in Polar-to-Rectangular mode, the L2330 is able to execute direct digital waveform synthesis and modulation. Real-time image-space conversions are achieved from radially-generated images, such as RADAR, SONAR, and ultrasound to raster display formats.

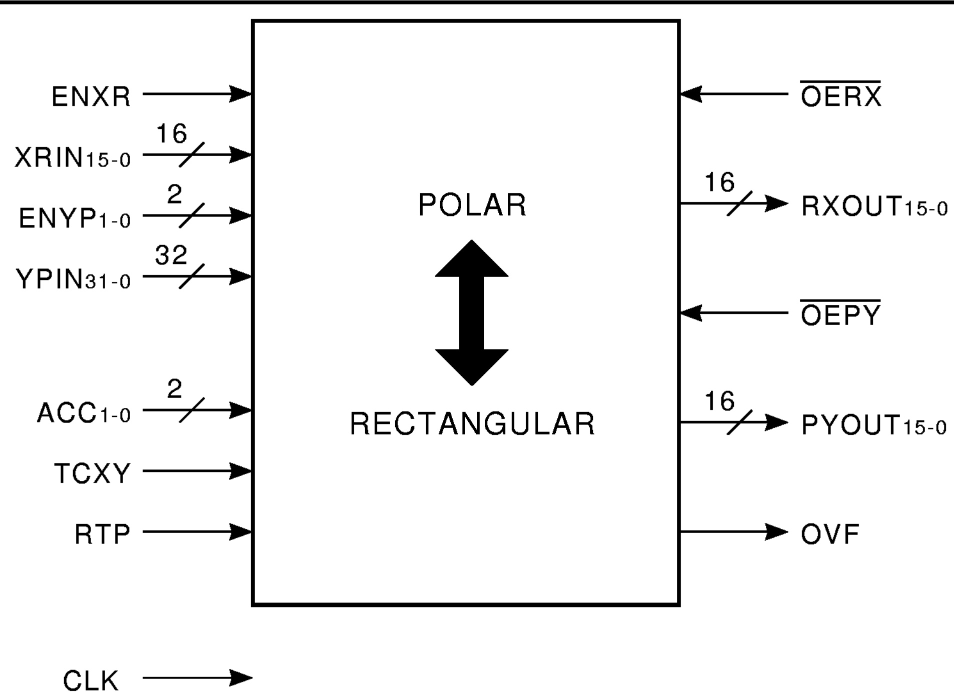
Functional Description

The L2330 converts bidirectionally between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinates. The user selects the numeric format. A valid transformed result is seen at the output after 22 clock cycles and will continue upon every clock cycle thereafter.

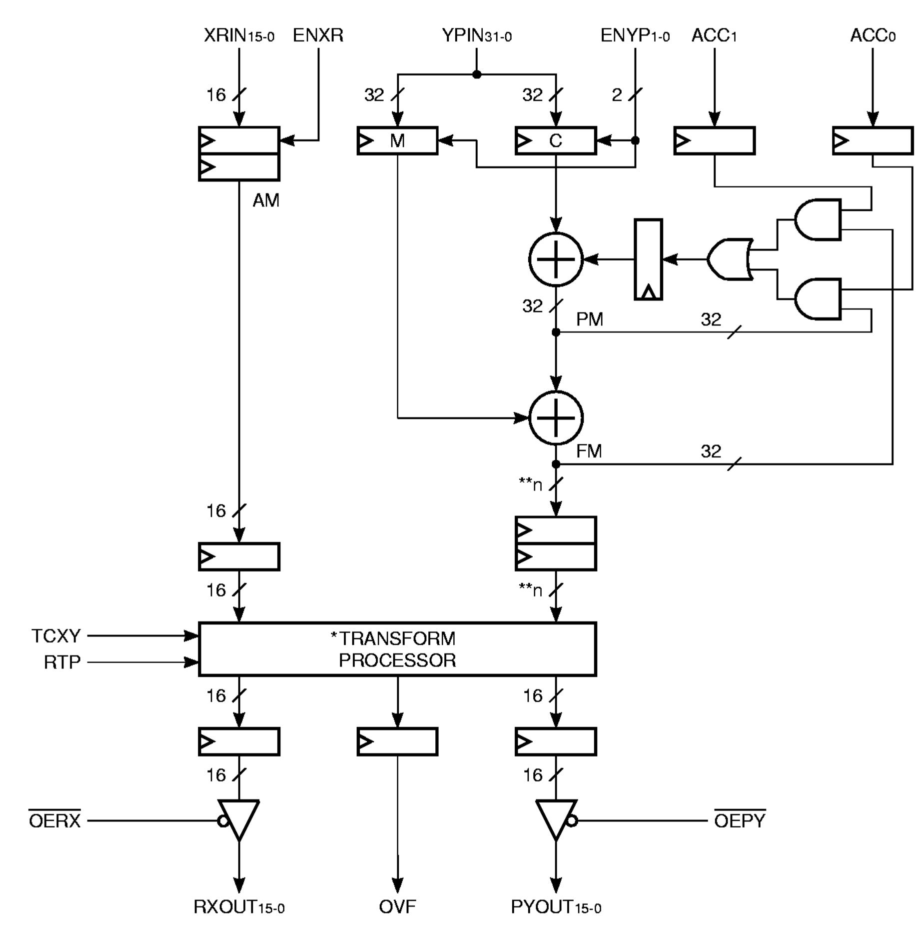
When in Rectangular-to-Polar mode, the user inputs a 16-bit Rectangular coordinate and the output generates a Polar transformation with 16-bit magnitude and 16-bit phase. The user may select the data format to be either two's complement or sign-and-magnitude Cartesian data format. Polar Magnitude data is always in magnitude format only. Polar Phase Angle data is modulo 2π so it may be regarded as either unsigned or two's complement format.

When in Polar-to-Rectangular mode, the user inputs 16-bit Polar Magnitude and 32-bit Phase data and the output generates a 16-bit Rectangular coordinate. The use may select the data format to be either two's complement or sign-and-magnitude Cartesian data format.

L2330 Block Diagram



L2330 Functional Block Diagram



* REQUIRES 18 CYCLES TO COMPLETE AND IS FULLY PIPELINED
** WHEN RTP IS HIGH 'n' IS 16-BITS, WHEN RTP IS LOW 'n' IS 24-BITS

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

$XRIN_{15-0}$ — x-coordinate/Magnitude Data Input

$XRIN_{15-0}$ is the 16-bit Cartesian x-coordinate/Polar Magnitude Data input port. $XRIN_{15-0}$ is latched on the rising edge of CLK.

$YPIN_{31-0}$ — y-coordinate/Phase Angle Data Input

$YPIN_{31-0}$ is the 32-bit Cartesian y-coordinate/Polar Phase Angle Data input port. When RTP is HIGH, the input accumulators should not be used. When ACC is LOW, the upper 16 bits of YPIN are the input port and the lower 16 bits become "don't cares". $YPIN_{31-0}$ is latched on the rising edge of CLK.

Outputs

$RXOUT_{15-0}$ — x-coordinate/Magnitude Data Output

$RXOUT_{15-0}$ is the 16-bit Cartesian x-coordinate/Polar Magnitude Data output port. When $\overline{OERX}$ is HIGH, $RXOUT_{15-0}$ is forced into the high-impedance state.

$PYOUT_{15-0}$ — y-coordinate/Phase Angle Data Output

$PYOUT_{15-0}$ is the 16-bit Cartesian y-coordinate/Polar Phase Angle Data output port. When $\overline{OEPY}$ is HIGH, $PYOUT_{15-0}$ is forced into the high-impedance state.

Controls

ENXR — x-coordinate/Magnitude Data Input Enable

When ENXR is HIGH, XRIN is latched into the input register on the rising edge of clock. When ENXR is LOW, the value stored in the register is unchanged.

$ENYP_{1-0}$ — y-coordinate/Phase Angle Data Input Control

$ENYP_{1-0}$ is the 2-bit y-coordinate/ Phase Angle Data Input Control that determines four modes as shown in

Table 1. Register Operation

$ENYP_{1-0}$	M	C
0 0	Hold	Hold
0 1	Load	Hold
1 0	Hold	Load
1 1	Clear	Load

Table 2. Accumulator Control

ACC_{1-0}	Configuration
0 0	No accumulation (normal operation)
0 1	PM accumulator path enabled
1 0	FM accumulator path enabled
1 1	Logical OR of PM and FM (Nonsensical)

Table 1. 'M' is the Modulation Register and 'C' is the Carrier Register as shown in the Functional Block Diagram.

RTP — Rectangular-to-Polar

When RTP is HIGH, Rectangular-to-Polar conversion mode is selected. When RTP is LOW, Polar-to-Rectangular conversion mode is selected.

ACC1-0 — Accumulator Control

ACC1-0 is the 2-bit accumulator control that determines four modes as shown in Table 2. Changing of the internal phase Accumulator structure is very useful when RTP is LOW allowing for waveform synthesis and modulation. ACC1-0 set to '00' is most commonly used when RTP is HIGH unless performing backward mapping from Cartesian to Polar coordinates.

TCXY — Data Input/Output Format Select

When TCXY is HIGH, two's complement format is selected. When TCXY is LOW, sign-and-magnitude format is selected.

FIGURE 1A. INPUT FORMATS

XRIN / **YPIN**

(RTP = 0)

XRIN — Integer Unsigned Magnitude

15	14	13	…	2	1	0
2^{15}	2^{14}	2^{13}		2^{2}	2^{1}	2^{0}

YPIN — Fract. Unsigned Mag./Two's Comp.

31	30	29	…	2	1	0
$*\pm2^{0}$	2^{-1}	2^{-2}		2^{-29}	2^{-30}	2^{-31}

Integer Signed Magnitude (RTP = 1, TCXY = 0)

15	14	13	…	2	1	0
NS	2^{14}	2^{13}		2^{2}	2^{1}	2^{0}

31	30	29	…	18	17	16
NS	2^{14}	2^{13}		2^{2}	2^{1}	2^{0}

Integer Two's Complement (RTP = 1, TCXY = 1)

15	14	13	…	2	1	0
-2^{15}	2^{14}	2^{13}		2^{2}	2^{1}	2^{0}

31	30	29	…	18	17	16
-2^{15}	2^{14}	2^{13}		2^{2}	2^{1}	2^{0}

(RTP = 0)

XRIN — Fractional Unsigned Magnitude

15	14	13	…	2	1	0
2^{0}	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

YPIN — Fract. Unsigned Mag./Two's Comp.

31	30	29	…	2	1	0
$*\pm2^{0}$	2^{-1}	2^{-2}		2^{-29}	2^{-30}	2^{-31}

Fractional Signed Magnitude (RTP = 1, TCXY = 0)

15	14	13	…	2	1	0
NS	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

31	30	29	…	18	17	16
NS	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

Fractional Two's Complement (RTP = 1, TCXY = 1)

15	14	13	…	2	1	0
-2^{0}	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

31	30	29	…	18	17	16
-2^{0}	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

$*\pm2^{0}$ denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.
NS denotes negative sign. (i.e. '1' negates the number)

OVF — Overflow Flag

OVF will go HIGH on the clock the magnitude of either of the current Cartesian coordinate outputs exceed the maximum range. OVF will return LOW on the clock that the Cartesian output value(s) return within range. An overflow condition can only occur when RTP is LOW.

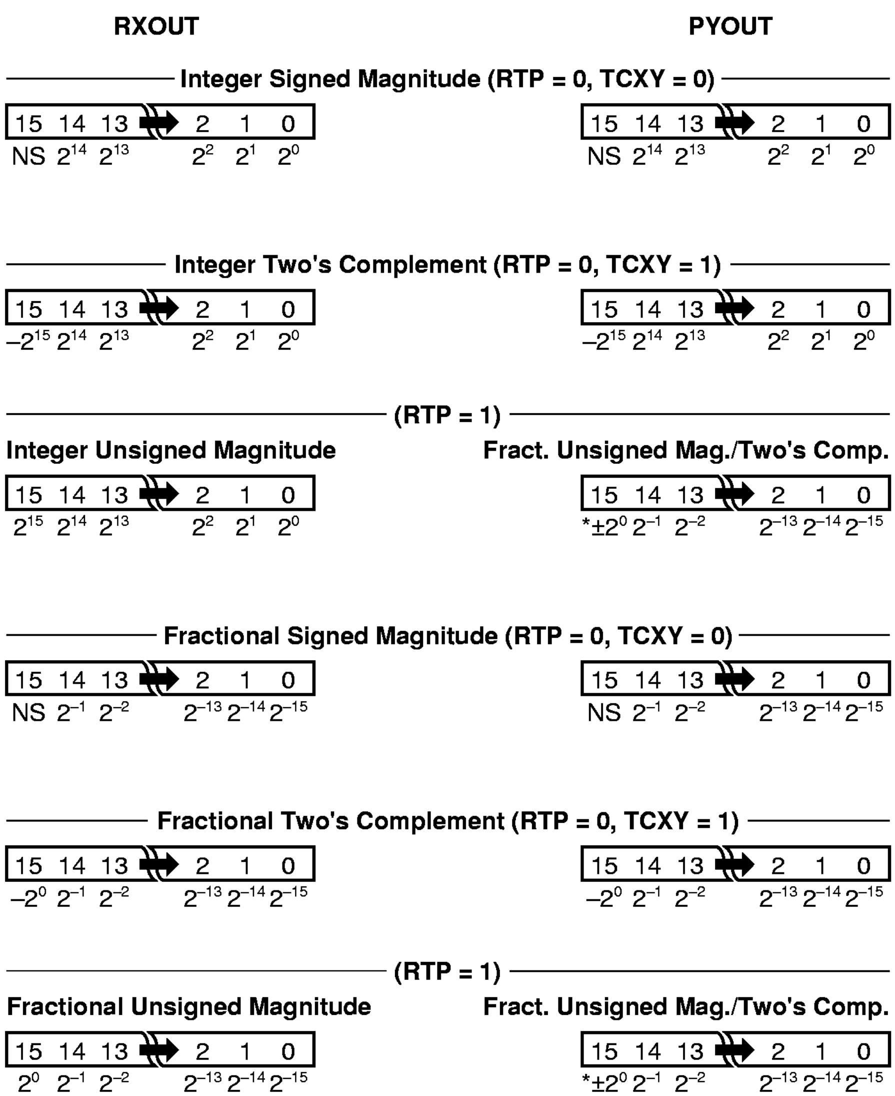
$\overline{\text{OERX}}$ — x-coordinate/Magnitude Data Output Enable

When $\overline{\text{OERX}}$ is LOW, $RXOUT_{15-0}$ is enabled for output. When $\overline{\text{OERX}}$ is HIGH, $RXOUT_{15-0}$ is placed in a high-impedance state.

$\overline{\text{OEPY}}$ — y-coordinate/Phase Angle Data Output Enable

When $\overline{\text{OEPY}}$ is LOW, $PYOUT_{15-0}$ is enabled for output. When $\overline{\text{OEPY}}$ is HIGH, $PYOUT_{15-0}$ is placed in a high-impedance state.

FIGURE 1B. OUTPUT FORMATS



*$\pm 2^0$ denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.

NS denotes negative sign. (i.e. '1' negates the number)

Conversion Ranges

The L2330 supports 16-bit unsigned radii and 16-bit signed Cartesian coordinates. Since the 16-bit rectangular coordinate space does not completely cover the polar space defined by 16-bit radii, certain values of "r" will not map correctly. This condition is indicated by the overflow (OVF) flag.

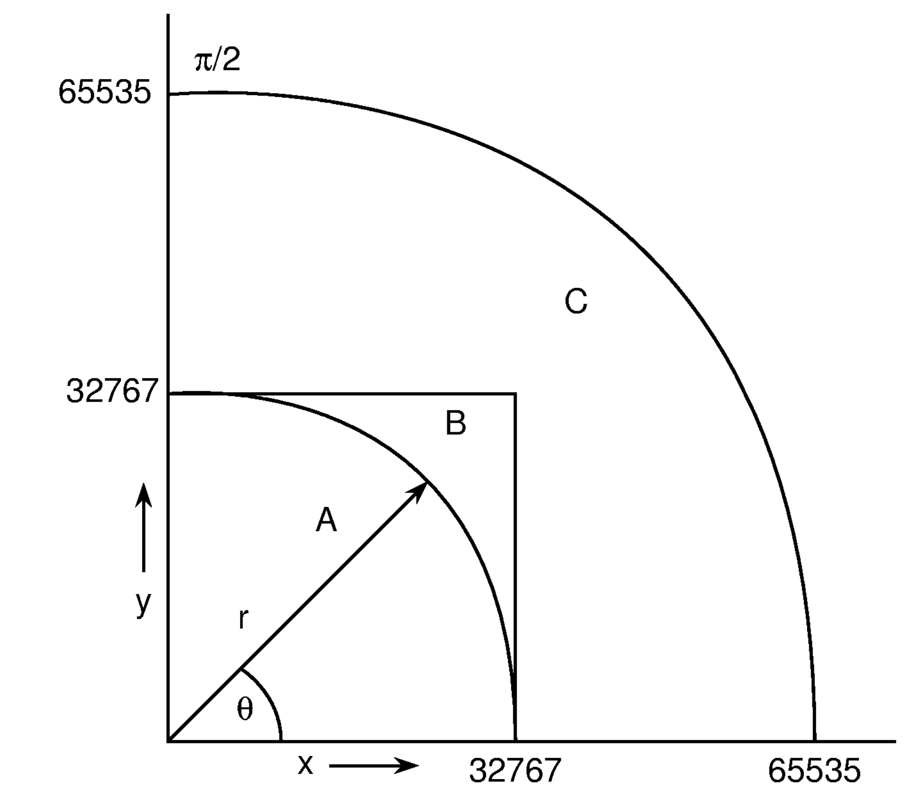
In Polar-to-Rectangular conversions, no overflow occurs for r ≤ 32767 (7FFFH). Overflow will always occur when r > 46341 (B505H). Note that in signed magnitude mode r = 46340 (B504H) will also cause an overflow. For 32767 ≤ r ≤ 46340, overflow may occur depending on the exact values of r and θ. Figure 2 shows, for the first quadrant, these three regions: A = no overflow (correct conversion), B = possible overflow, C = overflow. The other quadrants are mapped in a similar manner.

When in signed magnitude mode, the overflows on the other three quadrants are the same as in the first. This occurs because the signed magnitude number system is symmetric about zero. For example, if a given r and angle θ cause an overflow, the same r will cause an overflow for the angles -θ, π+θ , π-θ.

However, when in two's complement mode, the overflows aren't quite the same. This occurs because the two's complement number system is not symmetric about zero. For example, if the X or Y component of the input is –32768 (8000H), no overflow occurs. But if the X or Y component of the input is +32768, overflow does occur.

When converting from Rectangular-to-Polar, if both inputs are zero the radius is zero but the angle is not defined. The L2330 will output 4707H in this case. Since the angle is not defined for a zero length vector, this is not an error.

FIGURE 2. CONVERSION RANGES



Internal Precision

When performing a coordinate transformation, inaccuracies are introduced by a combination of quantization and approximation errors. The accuracy of a coordinate transformer is dependent on the word length used for the input variables, the word length used for internal calculations, as well as the number of iterations or steps performed. Truncation errors are due to the finite word length, and approximation errors are due to the finite number of iterations. For example, in the case of performing a polar-to-rectangular transformation, the accuracy of the rotation will be determined by how closely the input rotation angle was approximated by the summation of sub-rotation angles.

In this study, we examine the effectiveness of 16-bit internal precision versus 24-bit internal precision. 10,000 random Rectangular coordinates were converted to Polar and back to Rectangular. The resulting Rectangular coordinates from this double conversion were then compared to the original Rectangular coordinates input to the device. These vectors, with maximum word width of 16-bits, were sent through a 16-bit internal processor versus a 24-bit internal processor. The Rectangular coordinates were limited to the following conditions:

$$-32769 < x < 32768$$
$$-32769 < y < 32768$$

Using the 16-bit internal processor, the resulting Rectangular coordinates were compared to the original Rectangular coordinates (see Table 3). Using the 24-bit internal processor, the resulting Rectangular coordinates were compared to the original Rectangular coordinates (see Table 3). By way of comparison between the 16-bit internal processor and the 24-bit internal processor, we find that the 24-bit internal processor is significantly more accurate. This accuracy is due to internal word length. During coordinate transformation, the number of bits truncated within a 24-bit internal processor are much smaller than in a 16-bit internal processor resulting in smaller error.

TABLE 3. DOUBLE CONVERSION ERROR

Error	Internal 16-bit	Internal 24-bit
Mean Error (X)	0.0216	–0.0118
Mean Error (Y)	–0.0036	–0.0028
Mean Absolute Error (X)	1.5736	0.5116
Mean Absolute Error (Y)	1.0756	0.5160
Root Mean Square Error (X)	2.0168	0.7664
Root Mean Square Error (Y)	1.4356	0.7738
Max Error (X)	6.0/–7.0	3.0/–3.0
Max Error (Y)	5.0/–5.0	3.0/–3.0
Standard Deviation of Error (X)	2.0168	0.7664
Standard Deviation of Error (Y)	1.4357	0.7739

Circle Test

When performing a polar-to-rectangular transformation, a 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor.

In this study, we compare how accurately a coordinate transformer with a 16-bit internal processor versus a 24-bit internal processor can calculate all the coordinates of a circle. By setting the radius to 7FFFH (maximum before overflow), θ is incremented using the accumulator of the L2330 in steps of 0000 4000H until all the points of a full circle are calculated into rectangular coordinates.

The resulting rectangular coordinates were plotted and graphed. A graphical representation of the resulting vectors for both 16-bit and 24-bit internal processors are compared near 45°. Theoretically, a perfect circle is the desired output but when the resulting vectors from a coordinate transformer with 16-bit internal processor are graphed and displayed as shown in Figure 3, we see significant errors due to the inherent properties of a digital coordinate transformation system. In comparison, the 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor due to minimization of truncation errors. In many applications, this margin of error is of great significance especially when being used in applications such as medical ultrasound or modulation techniques.

Data values for Figure 3 and Figure 4 are shown in Table 4. By looking at these values, we observe the step resolution on a 16-bit internal processor is not 1 unit in the x and y. In most cases, the minimum step resolution is 2 units in the x and y. On the other hand, step resolution on a 24-bit internal processor is 1 unit in the x and y thus resulting in greater accuracy.

The minimum theoretical angle resolution that could be produced is 0.00175° when x = 7FFFH and y = 1H. A 16-bit internal processor can produce a minimum angle resolution of only 0.00549° and will not be able to properly calculate the theoretical minimum angle resolution. On the other hand, a 24-bit internal processor can produce a minimum angle resolution of 0.00002° and could therefore properly calculate the theoretical minimum angle resolution.

FIGURE 3. CIRCLE TEST RESULT NEAR 45° (16-BIT INTERNAL PROCESSOR)

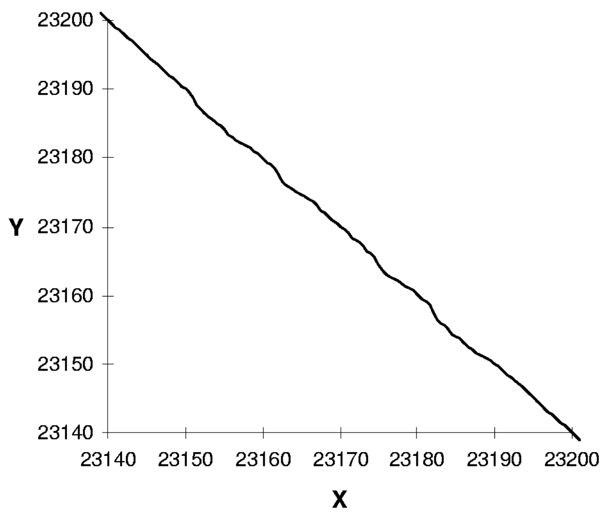


FIGURE 4. CIRCLE TEST RESULT NEAR 45° (24-BIT INTERNAL PROCESSOR)

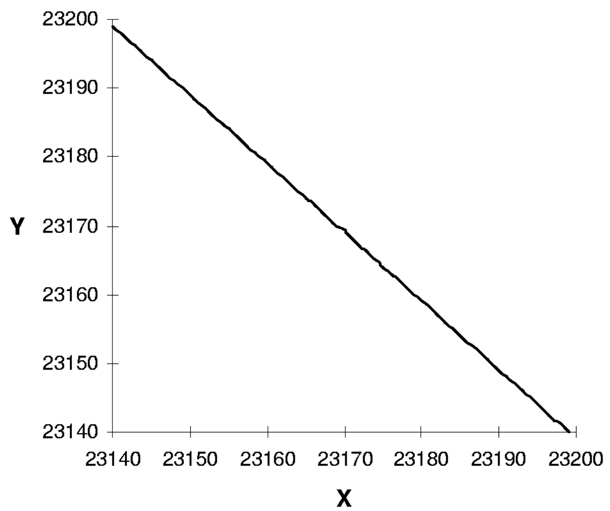


TABLE 4. RESULTANT DATA VALUES OF CIRCLE TEST NEAR 45°							
16-bit Internal Processor				24-bit Internal Processor			
x	x (HEX)	y	y (HEX)	x	x (HEX)	y	y (HEX)
23201	5AA1	23139	5A63	23199	5A9F	23140	5A64
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23195	5A9B	23144	5A68
23197	5A9D	23143	5A67	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23193	5A99	23146	5A6A
23195	5A9B	23145	5A69	23192	5A98	23147	5A6B
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	03148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23190	5A96	23149	5A6D
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23188	5A94	23151	5A6F
23187	5A93	23152	5A70	23187	5A93	23152	5A70
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23185	5A91	23154	5A72	23185	5A91	23154	5A72
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23183	5A8F	23156	5A74	23183	5A8F	23156	5A74

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			95	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

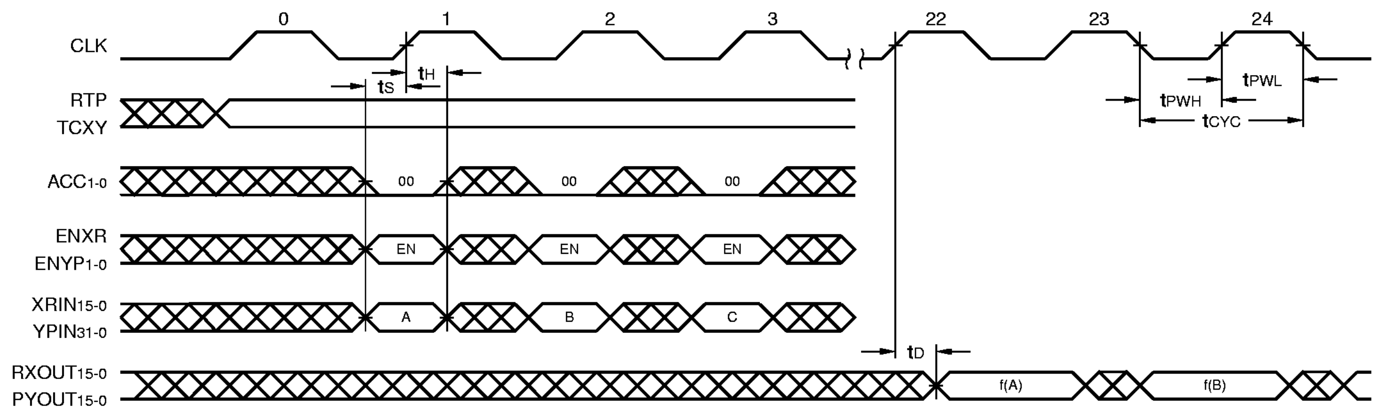
		L2330–					
		50*		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	10		8		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	12		7		6	
t_H	Input Hold Time	1		0		0	
t_D	Output Delay		22		18		16
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		13		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

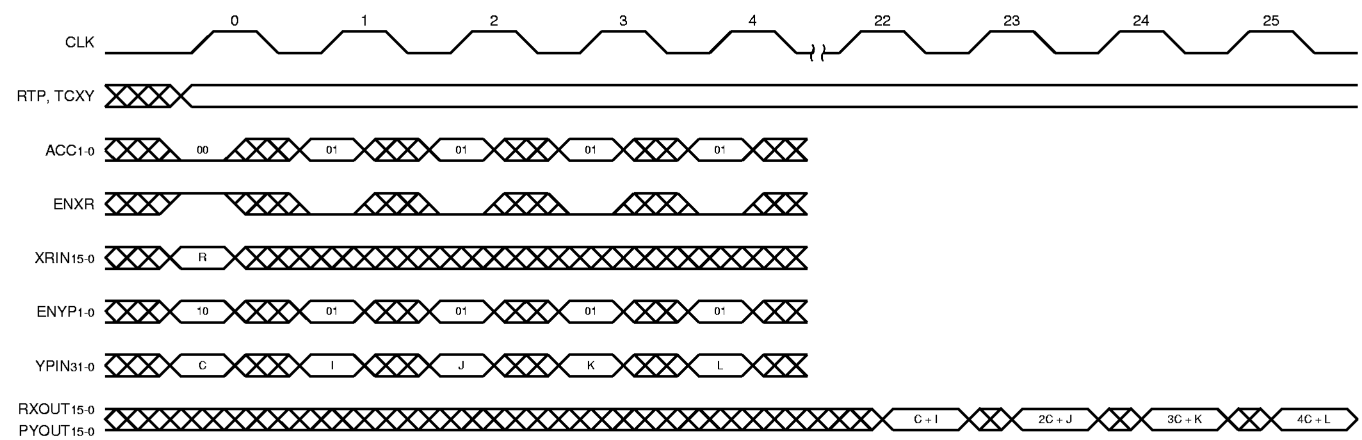
		L2330–					
		50*		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	11		9		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	13		7		6	
t_H	Input Hold Time	2		2		1	
t_D	Output Delay		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		14		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		14		13

*DISCONTINUED SPEED GRADE

Switching Waveforms: No Accumulation



Switching Waveforms: Phase Modulation



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Figure A. Output Loading Circuit

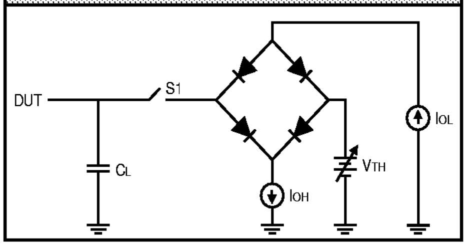
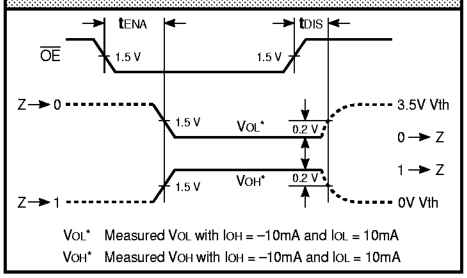
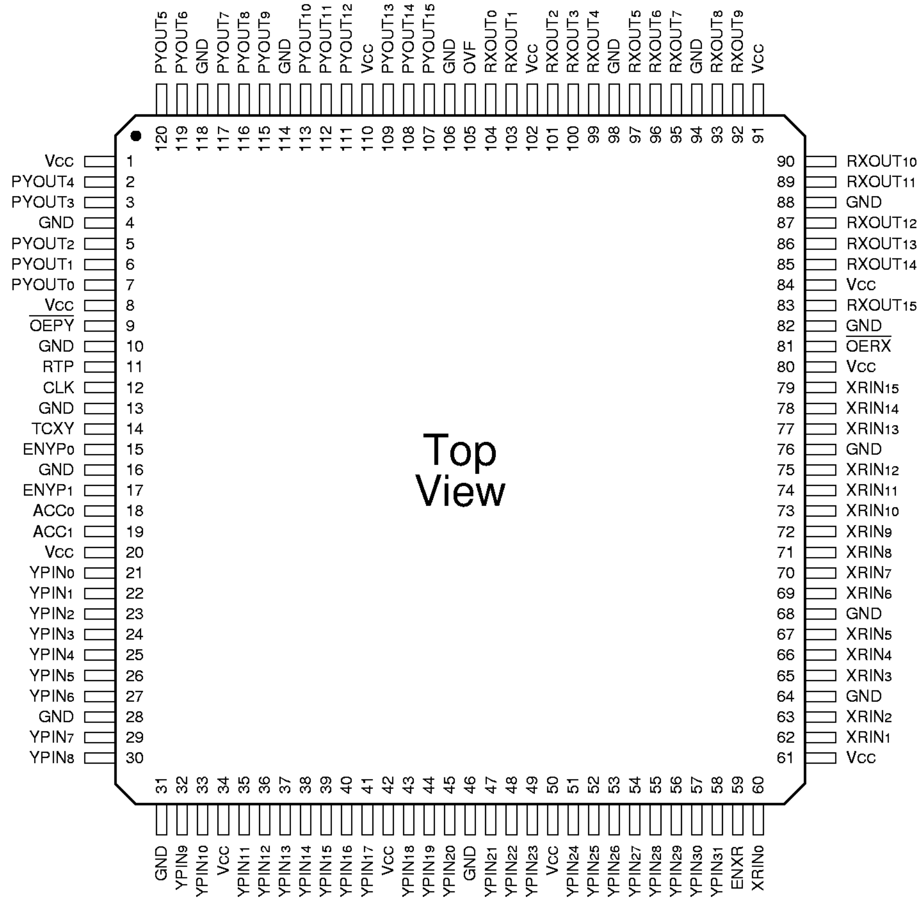


Figure B. Threshold Levels



ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — Commercial Screening
25 ns	L2330QC25
20 ns	L2330QC20

ORDERING INFORMATION

120-pin

Top View Through Package (i.e., Component Side Pinout)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PYO5	PYO7	PYO8	PYO10	PYO12	PYO14	PYO15	RXO0	RXO2	RXO4	RXO6	RXO8	RXO10
B	PYO3	PYO4	PYO6	PYO9	PYO11	PYO13	OVF	RXO1	RXO3	RXO5	RXO7	RXO9	RXO12
C	PYO1	PYO2	VCC	GND	GND	VCC	GND	VCC	GND	GND	VCC	RXO11	RXO13
D	$\overline{OEPY}$	PYO0	GND	KEY							GND	RXO14	RXO15
E	RTP	GND	VCC								VCC	GND	$\overline{OERX}$
F	TCXY	GND	CLK								VCC	XRI15	XRI14
G	ENYP1	ENYP0	GND								GND	XRI12	XRI13
H	ACC0	ACC1	VCC								XRI9	XRI10	XRI11
J	YPI0	YPI1	YPI3								GND	XRI7	XRI8
K	YPI2	YPI4	GND								GND	XRI5	XRI6
L	YPI5	YPI7	GND	VCC	YPI14	VCC	GND	VCC	YPI27	YPI31	VCC	XRI3	XRI4
M	YPI6	YPI9	YPI11	YPI13	YPI16	YPI18	YPI20	YPI23	YPI25	YPI28	ENXR	XRI1	XRI2
N	YPI8	YPI10	YPI12	YPI15	YPI17	YPI19	YPI21	YPI22	YPI24	YPI26	YPI29	YPI30	XRI0

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
25 ns	L2330GC25
20 ns	L2330GC20
	–55°C to +125°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT
25 ns	L2330GMB25
20 ns	L2330GMB20