

DESCRIPTION

The HYM532120 is a 1M x 32-bit Fast page mode CMOS DRAM module consisting of two HY5118160 in 42/42 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM.

The HYM532120W/SLW/TW/SLTW are Tin-Lead plated and HYM532120WG/SLWG /TWG/SLTWG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

FEATURES

- Low power dissipation
 - Max. self-refresh 5.50mW (SL-part)
 - Max. battery back-up 6.60mW (SL-part)
 - Max. CMOS standby 4.40mW (SL-part)
 - 11.0mW
 - Max. TTL standby 22.0mW
 - Max. operating

Speed	Power
70	1.76W
80	1.54W
100	1.10W

- Single power supply of 5V \pm 10%
- TTL compatible inputs and outputs
- Fast access time

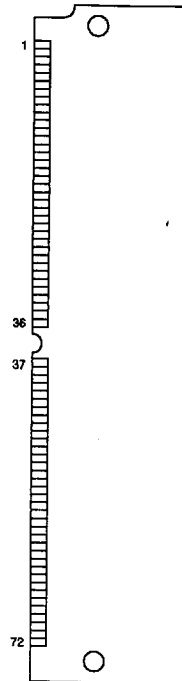
Speed	tRAC	tCAC	tPC
70	70ns	20ns	45ns
80	80ns	20ns	50ns
100	100ns	25ns	60ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh, Self-refresh
- 1024 refresh cycles / 256ms (SL-part)
- 1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A9	Address Input
DQ0-DQ34	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

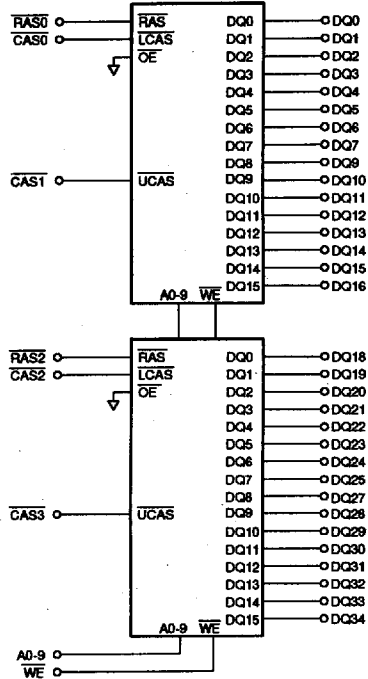
PIN CONNECTION



PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	Vss
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	NC
10	Vcc	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-70	-80	-100
PD1	Vss	Vss	Vss
PD2	Vss	Vss	Vss
PD3	Vss	NC	Vss
PD4	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	2.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pin)	V _{SS} ≤ V _{IN} ; V _{CC} + 1.0, All other pins not under test= V _{SS}		-20	20	μA	
I _{LO}	Output Leakage Current (High Impedance State)	V _{SS} ≤ V _{OUT} ≤ V _{CC} , RAS & CAS at V _{IH}		-10	10	μA	
I _{CC1}	V _{CC} Supply Current, Operating	t _{RC} = t _{RC} (min.)	70 80 100	- - -	320 280 240	mA	1,2,3
I _{CC2}	V _{CC} Supply Current, TTL Standby	RAS & CAS at V _{IH} , other inputs ≥ V _{SS}		-	4	mA	
I _{CC3}	V _{CC} Supply Current, RAS-only refresh	t _{RC} = t _{RC} (min.)	70 80 100	- - -	320 280 240	mA	1,3
I _{CC4}	V _{CC} Supply Current, Fast Page mode	t _{PC} = t _{PC} (min.)	70 80 100	- - -	240 220 200	mA	1,2,3
I _{CC5}	V _{CC} Supply Current, CMOS Standby	RAS & CAS ≥ V _{CC} -0.2V	SL-part	- -	2 0.8	mA	5
I _{CC6}	V _{CC} Supply Current, CAS-before-RAS refresh	t _{RC} = t _{RC} (min.)	70 80 100	- - -	320 280 240	mA	1,3
I _{CC7}	V _{CC} Supply Current, Battery Back Up (SL-part only)	t _{RC} = 250μs, CAS= CBR cycling or 0.2V WE= V _{CC} -0.2V A0-A9= V _{CC} -0.2V or 0.2V DQ0-DQ31= V _{CC} -0.2V, 0.2V, or open	t _{RAS} ≤ 300ns t _{RAS} ≤ 1μs	- -	9 1.2	mA	1,4,5
I _{CC8}	V _{CC} Supply Current, Self Refresh (SL-Part only)	RAS & CAS ≤0.2v other pins same as I _{CC7}			1.0	mA	
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA		-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -5mA		2.4	-	V	

NOTE :

- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
- I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
- I_{CC} is specified as average current. for I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while RAS= V_{IL}. for I_{CC4}, address can be changed maximum once while CAS= V_{IH}.
- Only t_{RAS}(max.)= 1μs is applied to refresh of battery backup but t_{RAS}(max.)= 10μs is applied to normal functional operation.
- I_{CC5}(max.)= 2mA, I_{CC7} and I_{CC8} are applied to SL-part only (HYM532120SLW/SLTW/SLWG/SLTWG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532120W-Series						UNIT	NOTE	
			-70		-90		-100				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
1	trc	Random Read or Write Cycle Time	130	-	150	-	180	-	ns		
2	trPC	RAS to CAS Precharge Time	0	-	0	-	245	-	ns		
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns		
4	trHCP	RAS Hold Time from CAS Precharge	45	-	45	-	125	-	ns		
5	trAC	Access Time from RAS	-	70	-	80	-	100	ns	5,10,11	
6	tCAC	Access Time from CAS	-	20	-	20	-	25	ns	5,10	
7	tAA	Access Time from Column Address	-	35	-	40	-	50	ns	5,11	
8	tCPA	Access Time from CAS Precharge	-	40	-	45	-	55	ns	5	
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	5	
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	15	ns	6	
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4	
12	trP	RAS Precharge Time	50	-	60	-	70	-	ns		
13	trAS	RAS Pulse Width	70	10K	80	10K	100	10K	ns		
14	trASP	RAS Pulse Width (Fast Page Mode)	70	100K	80	100K	100	100K	ns		
15	trSH	RAS Hold Time	20	-	20	-	25	-	ns		
16	tCSH	CAS Hold Time	70	-	80	-	100	-	ns		
17	tCAS	CAS Pulse Width	20	10K	20	10K	25	10K	ns		
18	trCD	RAS to CAS Delay	20	50	20	60	25	75	ns	10	
19	trAD	RAS to Column Address Delay Time	15	35	15	40	20	50	ns	11	
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	10	-	ns		
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns		
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns		
23	trAH	Row Address Hold Time	10	-	10	-	15	-	ns		
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns		
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns		
26	tAR	Column Address Hold Time from RAS	55	-	60	-	75	-	ns		
27	trAL	Column Address to RAS Lead Time	35	-	40	-	50	-	ns		
28	trCS	Read Command Set-up Time	0	-	0	-	0	-	ns		
29	trCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	7	
30	trRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	7	
31	twCH	Write Command Hold Time	15	-	15	-	20	-	ns		
32	twCR	Write Command Hold Time from RAS	55	-	60	-	75	-	ns		
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns		
34	trWL	Write Command to RAS Lead Time	20	-	20	-	25	-	ns		
35	tcWL	Write Command to CAS Lead Time	20	-	20	-	25	-	ns		
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	8	
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	8	
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	75	-	ns		
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms		
40	twCS	Write Command Set-up Time	SL-part	-	256	-	256	-	256	ms	12
				-	0	-	0	-	0	ns	9

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532120W-Series						UNIT	NOTE
			-70		-80		-100			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	15	-	15	-	20	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	50	-	ns	
44	tRPS	RAS Precharge Time (Self Refresh Cycle)	130	-	150	-	180	-	ns	
45	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
46	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
47	tRPS	RAS Precharge Time (Self Refresh Cycle)	130	-	130	-	130	-	ns	
48	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM532120 could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
4. Refer to the HY5118160 data sheet for detailed information.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. toFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to CAS leading edge in early write cycles.
9. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS \geq twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)= 256ms is applied to SL-part only (HYM532120SLW/SLTW/SLWG/SLTWG).

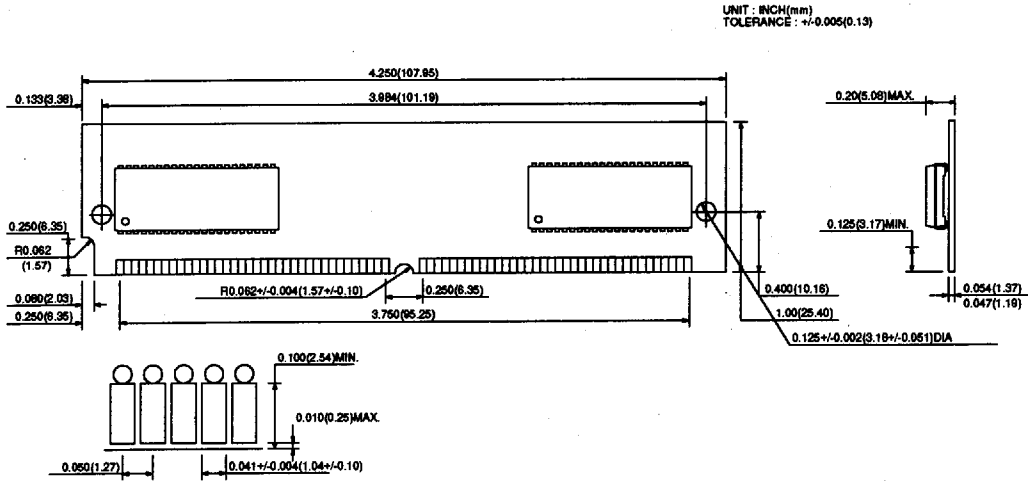
CAPACITANCE

(TA= 25°C, VCC= 5V \pm 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

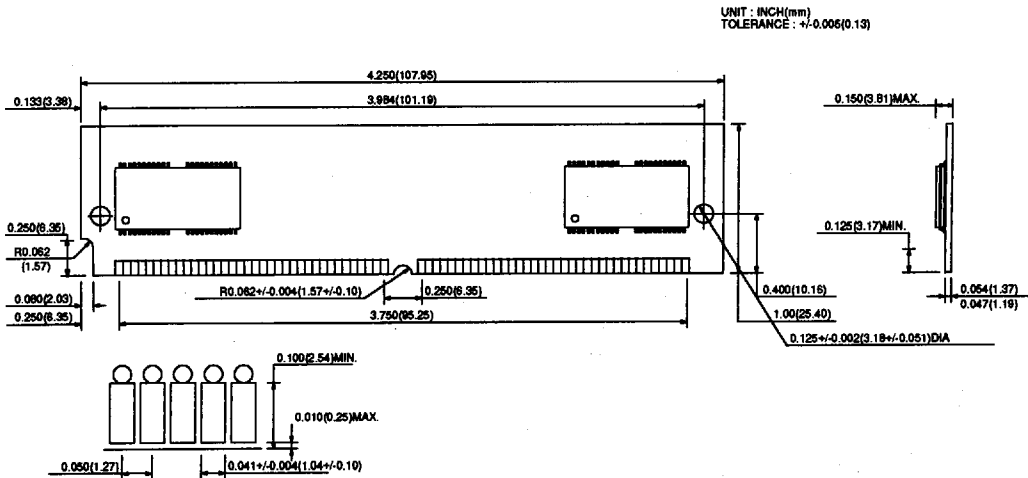
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	25	pF
CIN2	Input Capacitance (WE)	-	25	PF
CIN3	Input Capacitance (RAS0-RAS2)	-	20	pF
CIN4	Input Capacitance (CAS0-CAS3)	-	20	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ31)	-	15	pF

PACKAGE INFORMATION

72 pin Single In-line Memory Module (W; Tin-Lead plated, WG; Gold plated)
HYM532120/SL (SOJ Mounted)



HYM532120T/SLT (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532120W	70/80/100		SIMM	Tin-Lead
HYM532120SLW	70/80/100	SL-part	SIMM	Tin-Lead
HYM532120TW	70/80/100		SIMM	Tin-Lead
HYM532120SLTW	70/80/100	SL-part	SIMM	Tin-Lead
HYM532120WG	70/80/100		SIMM	Gold
HYM532120SLWG	70/80/100	SL-part	SIMM	Gold
HYM532120TWG	70/80/100		SIMM	Gold
HYM532120SLTWG	70/80/100	SL-part	SIMM	Gold

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