SF229
LOW CURRENT SECURITY ASIC

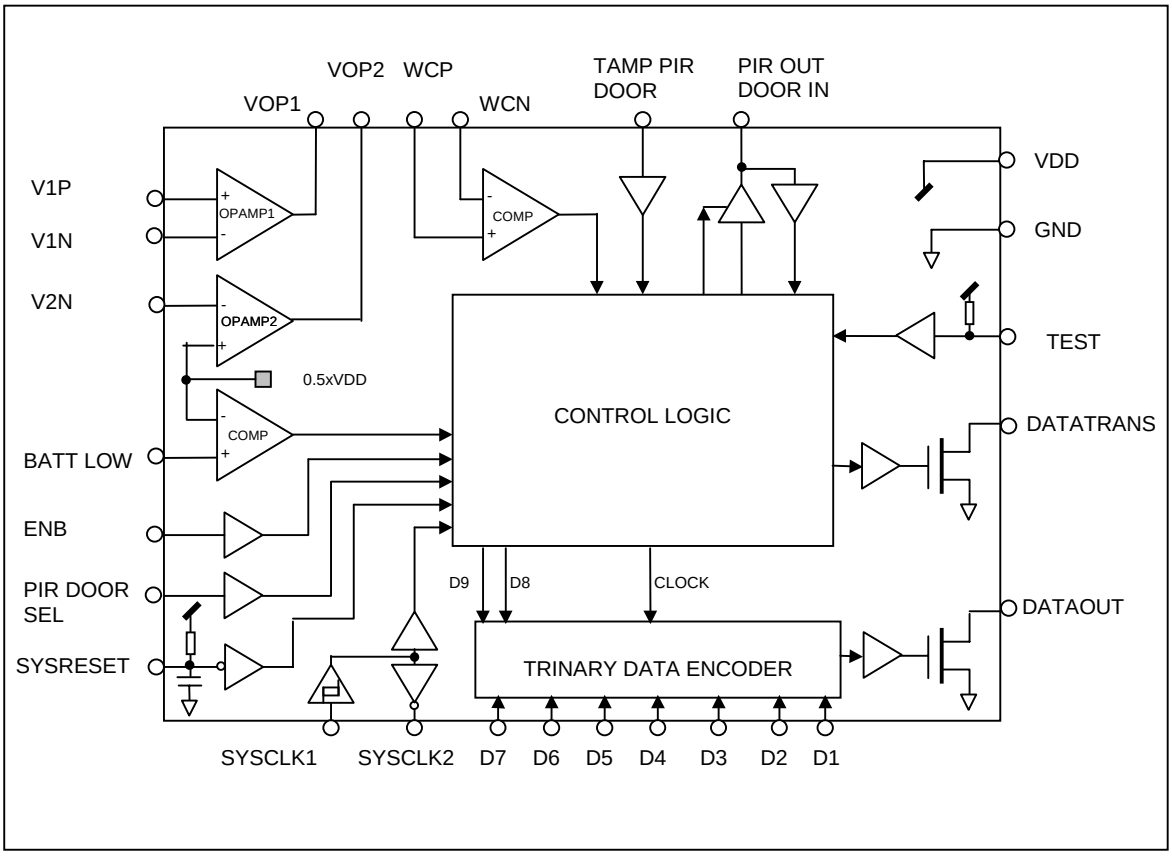
DESCRIPTION

The SF229 is a low power CMOS mixed signal ASIC designed for battery powered security applications that are either hard wired or RF linked. The ASIC may be configured in one of 2 modes:- Analogue or digital input device. In the case of analogue sensors such as PIR, Smoke, Level etc, the trigger threshold is set via external resistors. The device transmits detector alarm status and identification information.

The current consumption is very low, typically 40 µA in the inactive state and 85 µA in the alarm state, therefore ensuring maximum battery life.

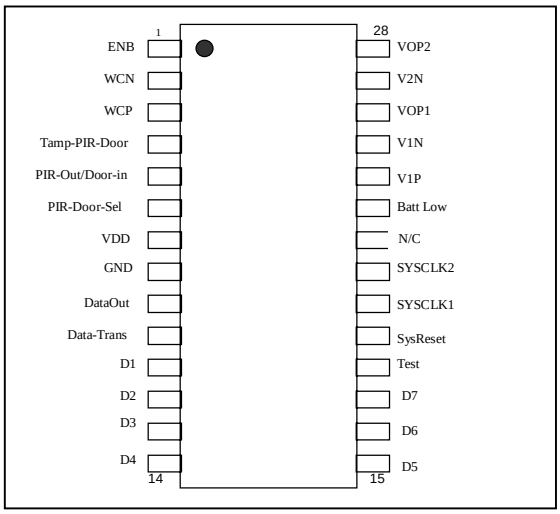
The ASIC offers direct interfacing to a PIR sensor and an RF transmitter with a minimum of support components in order to provide a reliable and cost effective solution in many security applications.

1.0 BLOCK DIAGRAM



2.0 PIN CONFIGURATION

These devices have been designed to withstand up to 1kV of electrostatic discharge between pin pairs. As such, precautions must be taken to ensure that the device is not damaged during handling and transportation.



2.1 PIN DESCRIPTION for 28 SOIC

NAME	PIN	TYPE	FUNCTION
ENB	1	Digital Input, trinary	Select number of PIR events required.
WCP	2	Analogue Input	Positive input of window comparator
WCN	3	Analogue Input	Negative input of window comparator
TAMP_PIR_DOOR	4	Digital Input	Tamper sensor input
PIR_OUT_DOOR-IN	5	Digital I/O	PIR status o/p or DOOR sensor i/p
PIR_DOOR_SEL	6	Digital Input	Select PIR or DOOR mode
VDD	7	Supply	Positive power supply
GND	8	Supply	Ground
DATAOUT	9	Digital Output	Serial data output
DATA_TRANS	10	Digital Output	On/off control for transmitter
D1	11	Digital Input, trinary	LSB input to encoder
D2	12	Digital Input, trinary	Bit 2 input to encoder
D3	13	Digital Input, trinary	Bit 3 input to encoder
D4	14	Digital Input, trinary	Bit 4 input to encoder
D5	15	Digital Input, trinary	Bit 5 input to encoder
D6	16	Digital Input, trinary	Bit 6 input to encoder
D7	17	Digital Input, trinary	Bit 7 input to encoder
TEST	18	Digital Input	Control input for test mode
SYSRESET	19	Digital Input	System reset
SYSCLK1	20	Analogue Input	Input to oscillator
SYSCLK2	21	Digital Output	Feedback from oscillator
N/C	22	-	No Connection
BATT_LOW	23	Analogue Input	Input to low battery comparator
V1P	24	Analogue Input	Non-inverting input to opamp1
V1N	25	Analogue Input	Inverting input to opamp1
VOP1	26	Analogue Output	Output of opamp1
V2N	27	Analogue Input	Inverting input to opamp2
VOP2	28	Analogue Output	Output of opamp2

3.0 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply voltage V_{DD}	8.00	V
Input pins	Vdd + 0.4 to GND –0.4	V
Output pins DATOUT and DATA TRANS	VDD+0.4 to –0.4with respect to GND	V
Operating Temperature, T_O	0 to 70	°C
Storage Temperature, T_S	-40 - +150	°C
Soldering Temperature	300 to ? secs	°C

4.0 ELECTRICAL SPECIFICATION

Test conditions V_{DD} = 5.0V, T_{amb} = 25°C unless otherwise stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage		4.5	5.0	5.5	V
$I_{DD,}$ Active in PIR mode	D1to D7 & ENB=V_{DD}		80		µA
$I_{DD,}$ Quiescent in PIR mode	As above		40		µA
$I_{DD,}$ Active in DOOR mode	D1to D7 & ENB=V_{DD}		55		µA
$I_{DD,}$ Quiescent in DOOR mode	As above		25		µA
Opamps 1&2					
$V_{OS,}$ input offset voltage		-10	+/-5	+10	mV
$I_{BIAS,}$ Input bias current		-100		+100	pA
CMR, Input Common Mode Range		Vss		Vdd-0.3	V
Z_{in}, input impedance			>1		Mohm
Opamp 1					
A_{OL}, Open Loop Gain			43		dB
A_{OL}, Open Loop Gain			93		dB
Input related noise	Bandwidth 0.1 to 20Hz		1.2		µV rms
Input related noise	Mid band value		55		nV/root Hz
GBW, Gain Bandwidth Product			230		KHz
Phase Margin			28		degrees
V_{OUTPUT} Output Voltage Range		GND		3.5	V
Opamp 2					
A_{OL}, Open Loop Gain			93		dB
GBW, Gain Bandwidth Product			1.35		KHz
Phase Margin			86		degrees
Non inverting input bias voltage	Internal node		$0.5V_{DD}$		
V_{OUTPUT} Output Voltage Range		GND		3.8	V
Comparator					
$V_{OS,}$ input offset voltage		-10	+/-5	+10	mV
$I_{BIAS,}$ Input bias current		-100		+100	pA
A_{OL}, Open Loop Gain			85		dB
CMR, Input Common Mode Range		Vss+0.5		Vdd-0.5	V
Z_{in}, input impedance			1		Mohm

Oscillator					
Clock Frequency (F=1/1.36CR)	R=2.2M, C=470pF		698		Hz
Low Battery detector comparator					
Voltage threshold			$0.5V_{DD}$		V
Input current			+/-1		nA

4.1 DIGITAL PARAMETERS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
D1 to D7 and ENB inputs					
VIN_{HI}		V_{DD}		V_{DD}	
VIN_{LO}		GND		GND	
VIN_{OPEN}			Open circuit		
IIN_{HI}	During Output DATA TRANS Active only			-2.8	µA
IIN_{LO}	As above			1.7	µA
IIN_{OPEN}	As above			100	pA
Door PIR Sel and Tamp PIR Door inputs					
VIN_{HI}					
VIN_{LO}					
IIN_{HI}					µA
IIN_{LO}					µA
PIR_OUT_DOOR-IN pin					
	Input mode				
PIR_OUT_DOOR-IN pin					
Output source current	O/P mode, Voltage=Vdd-0.?	-8			mA
Data Out					
Output sink current	Voltage= 0.?	4			mA
Output leakage current	Voltage= 9V			?	µA
Data Trans					
Output sink current	Voltage= 0.?	4			mA
Output leakage current	Voltage= 9V			?	µA

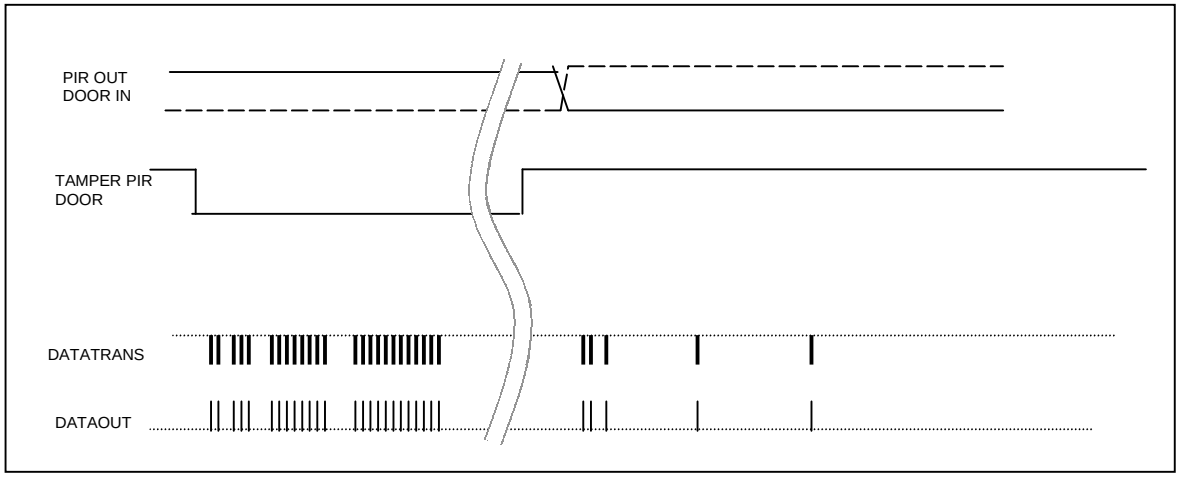
4.2 TIMING PARAMETERS

Timing parameters. Based on a clock frequency of ?Hz at SYSCLK2

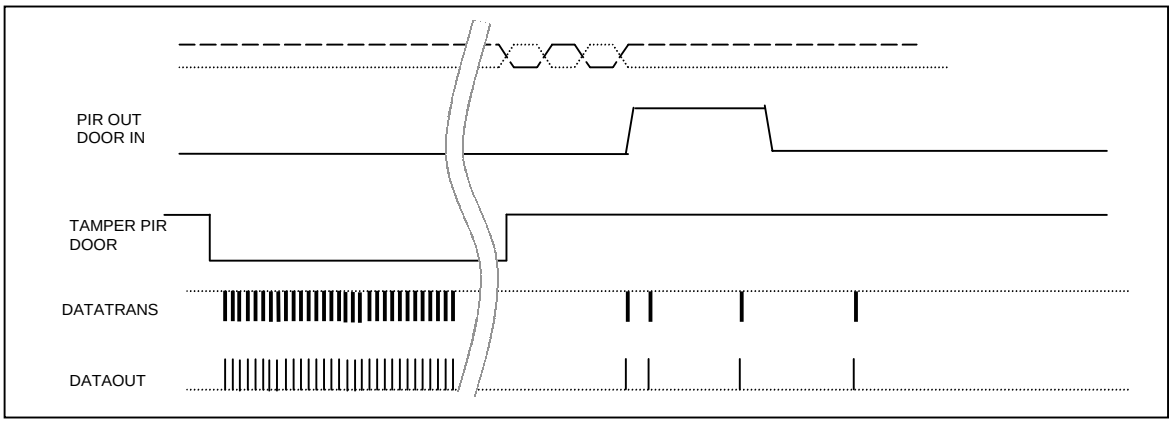
PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
T_{DE}, Activation delay	Door mode	?		?	mSecs
T_{DE}, Activation delay	PIR mode	?		?	mSecs
T_{DTO}, Delay DATATRANS to DATAOUT					mSecs
T_{DOFF}, Delay DATAOUT to DATATRANS					mSecs

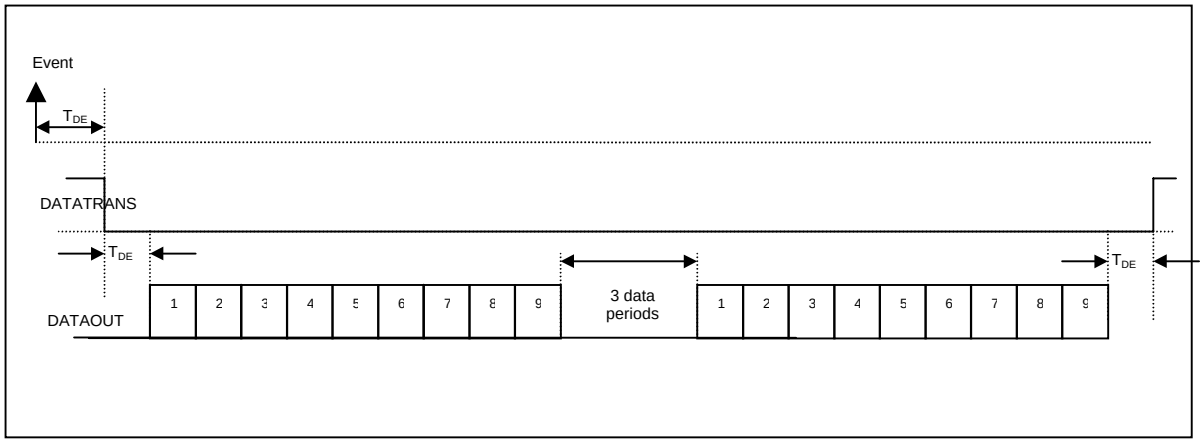
4.3 TIMING DIAGRAM

Activation sequence DOOR Mode

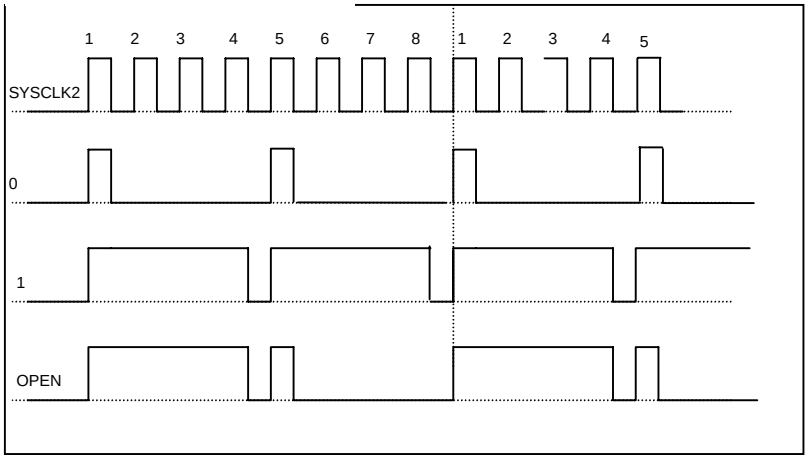


Activation sequence PIR Mode





Data Encoding



5.0 GENERAL DESCRIPTION

The SF229 ASIC forms the key semiconductor component needed to create a sensor in a security or safety system. The ASIC incorporates design techniques that result in very low operating currents making the product very suitable for battery-powered applications.
Two types of event can be detected, an analogue event or a digital event. The detection mode is selected using the PIR DOOR SEL pin.
The output from the ASIC is presented on the DATAOUT pin in the form of a 9 bit serial data stream. The first 7 bits reflect the conditions on the D1 to D7 inputs, which are location or address information and bit D8 reflects the status of the WCN/WCP, BATT LOW and TAMP PIR DOOR inputs. Bit D9 reflect the status of DOOR IN PIR OUT pin when the ASIC is in digital detect mode. Data for all 9 bits is coded to represent the hi, lo and open conditions used in a trinary logic convention.
Data is output as a series of packets, each packet comprising of 9 data bits, 3 blank data periods followed by 9 data bits. The total number of data packets output during an alarm sequence and the duration of the alarm sequence period depend on the mode in which the ASIC is set and the input which activates it. Some settings produce alarm periods that can be over 3 minutes long. Timing and protocol details are shown later in this specification.

A trinary logic scheme offers an address range of 0 to 2186 compared to conventional binary coding which would offer a range of 0 to 127. Small systems may only need to use a binary coded address field.

In the Door mode, the alarm sequence is activated by an event detected on the DOOR IN PIR OUT or TAMP PIR DOOR pins. Typical digital sensors could be contacts fitted to a door or window detector on DOOR IN PIR OUT pin and a micro switch on the security device cover on the TAMP PIR DOOR pin.
Activation is triggered by a change of state of the DOOR IN PIR OUT pin rather than a level. The transmission sequence is different depending on which input is activated. During a transmission sequence, activity on both input pins is monitored continuously and their status presented in every data packet.

In the analogue or PIR mode, events are detected using a window comparator on input pins WCP and WCN, or TAMP PIR DOOR pins. Here again the alarm sequence is dependent on the input that was activated.
Two on-chip opamps are included in the ASIC to process the analogue signal for amplitude and frequency characteristics. Typical analogue sensors would be PIR, optical, temperature or fluid level detection devices, the most common being PIR. The threshold of the window comparator is set by an external resistor bridge. The configuration and design details of this are shown later in this specification.
Also included is the ability to program the number of pulses appearing on the output of the window comparator required to start a transmission sequence. The selection is made via input pin ENB, 2, 3 and 4 pulses may be selected.

5.1 Digital Circuitry

Normally the TAMP PIR DOOR pin is held Hi through a normally closed micro switch. The switch is biased so it will open if the security device cover is removed. A resistor connected to the pin will produce a logic lo condition.

ENB pin is used to select the number of pulses needed for activation on PIR mode according to:

ENB pin connection	Condition
VDD	2 PIR pulse
GND	3 PIR pulse
OPEN	4 PIR pulse

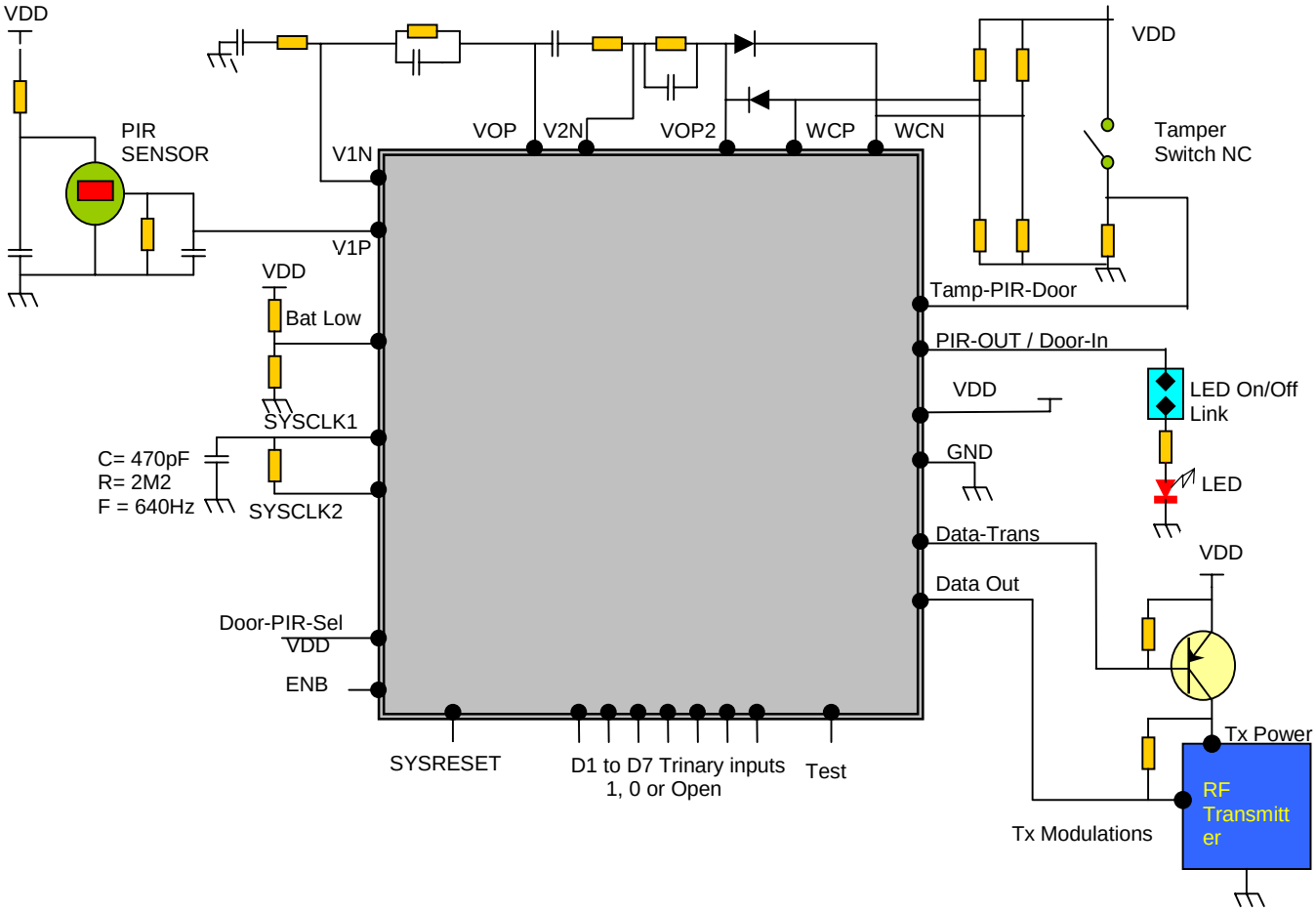
6.0 DESCRIPTION OF FUNCTION MODES

DOOR PIR SEL pin	Function	Condition	Bit 8	Bit 9
1	PIR mode	Waiting for an event	No data stream	No data stream
1	PIR mode	PIR alarm active	OPEN	0
1	PIR mode	TAMPER alarm active	1	0
1	PIR mode	Low Battery	0	0
0	Door / Window mode	Waiting for an event	No data stream	No data stream
0	Door / Window mode	PIR-OUT/DOOR IN 1 to 0 transition	X	0
0	Door / Window mode	PIR-OUT/DOOR IN 0 to 1 transition	X	1
0	Door / Window mode	Tamper alarm active	1	X
0	Door / Window mode	Low Battery	0	X

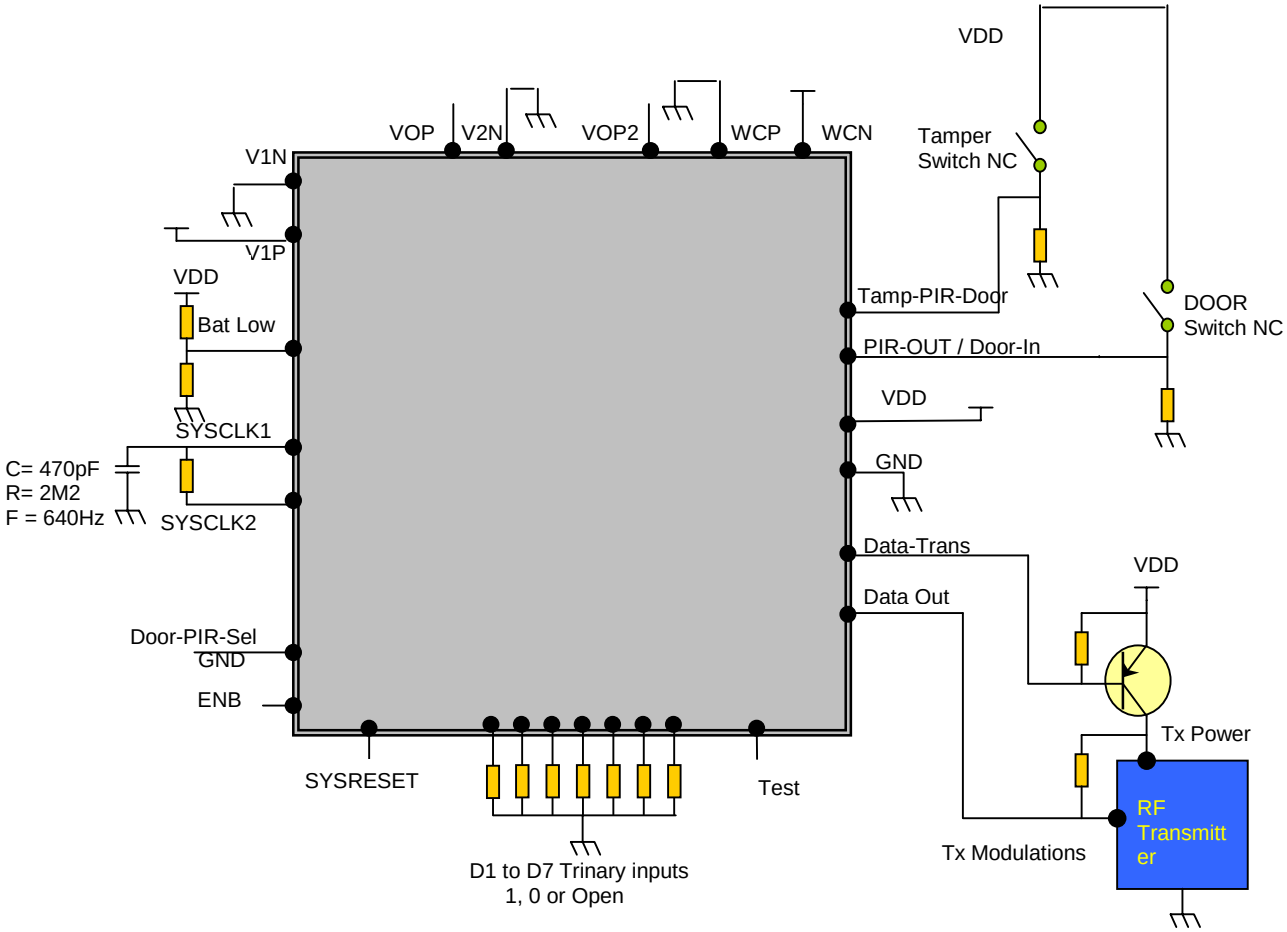
X = Don’t care condition.

7.0 APPLICATIONS INFORMATION

7.1 CIRCUIT DIAGRAM AS A PIR SENSOR



7.2 CIRCUIT DIAGRAM AS A CONTACT CLOSURE SENSOR



8.0 ORDERING INFORMATION

Order products using the following code:

SF229A DE for 28 pin SOIC package in Tubes
SF229A DE T for 28 pin SOIC package Tape & Reel.

Datasheets contain specifications current on publication date.

Preliminary datasheets contain specifications based on prototype analysis and are current on publication date.

Semefab (Scotland) Ltd. may change this specification at any time without notification.

Supply of products conforms to Semefab (Scotland) Ltd. Terms and Conditions

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