

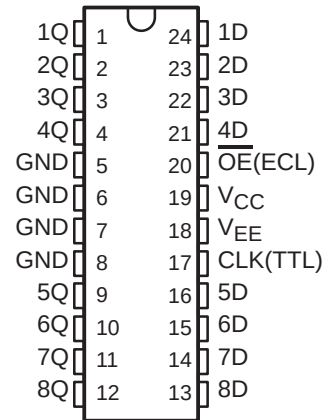
SN100KT5578

OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

SDZS13A – APRIL 1990 – REVISED OCTOBER 1990

- 100K Compatible
- TTL Clock and ECL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC} , V_{EE} , and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include “Small Outline” Packages and Standard Plastic DIPs
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015

DW OR NT PACKAGE
(TOP VIEW)



description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 100K ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

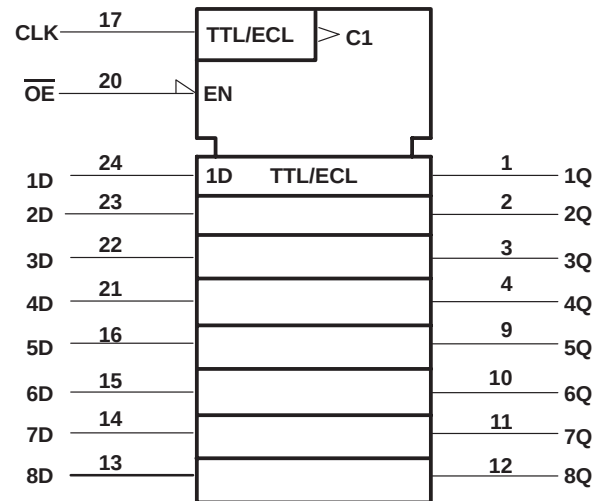
The output-control input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5578 is characterized for operation from 0°C to 85°C.

Function Table

INPUTS			OUTPUT (ECL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	L

logic symbol†

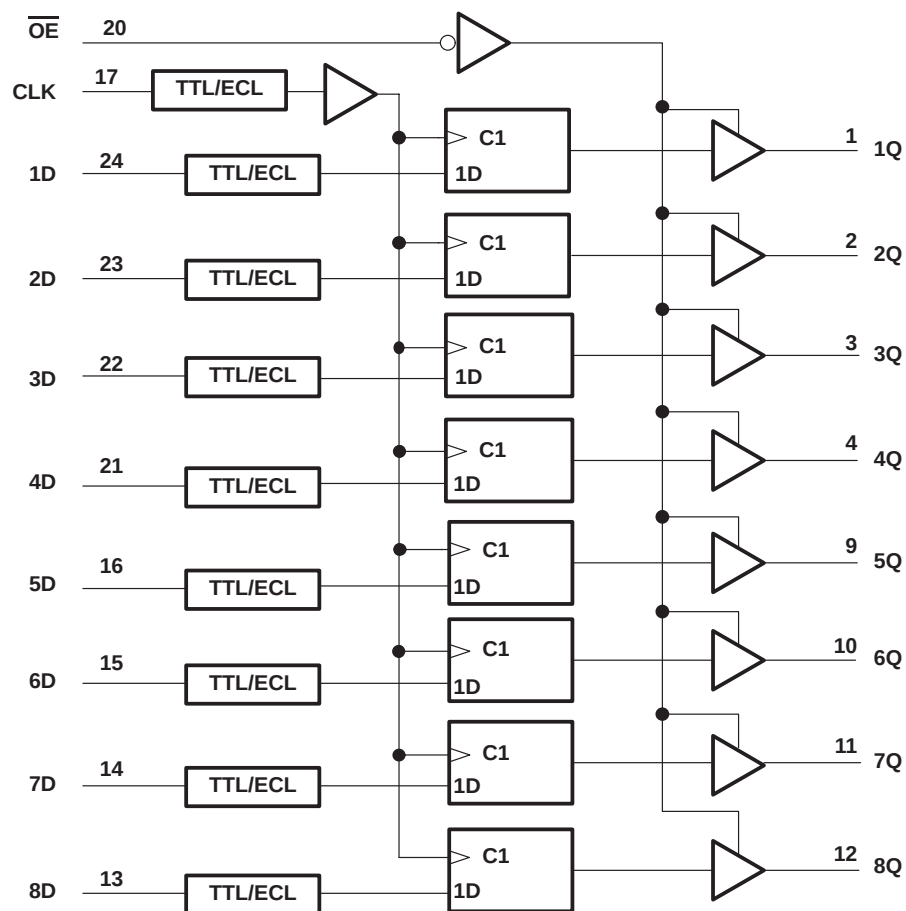


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Supply voltage range, V_{EE}	–8 V to 0 V
Input voltage range (TTL) (see Note 1)	–1.2 V to 7 V
Input voltage range (ECL)	V_{EE} to 0 V
Input current range (TTL)	–30 mA to 5 mA
Current out of any output	50 mA
Operating ambient temperature range	0°C to 85°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage	4.5	5	5.5	V
V_{EE}	ECL supply voltage	–4.2	–4.5	–4.8	V
V_{IH}	TTL high-level input voltage	2			V
V_{IL}	TTL low-level input voltage			0.8	V
I_{IK}	TTL input clamp current			–18	mA
V_{IH}	ECL high-level input voltage [‡]	–1165		–880	mV
V_{IL}	ECL low-level input voltage [‡]	–1810		–1475	mV
T_A	Operating ambient temperature (see Note 2)	0		85	°C

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			MIN	TYP [§]	MAX	UNIT
V_{IK}	D inputs and CLK	$V_{CC} = 4.5$ V,	$V_{EE} = -4.2$ V,	$I_I = -18$ mA			–1.2	V
I_I	D inputs and CLK	$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V,	$V_I = 7$ V			0.1	mA
I_{IH}	D inputs and CLK	$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V,	$V_I = 2.7$ V			20	μA
I_{IL}	D inputs and CLK	$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V,	$V_I = 0.5$ V			–0.5	mA
I_{IH}	OE only	$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V,	$V_{IH} = -880$ mV			350	μA
I_{IL}	OE only	$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V,	$V_{IL} = -1810$ mV	0.50			μA
$V_{OH}^{\ddagger}$		$V_{CC} = 4.5$ V,	$V_{EE} = -4.5$ V ± 0.3 V,	See Note 3	–1020		–880	mV
$V_{OL}^{\ddagger}$		$V_{CC} = 4.5$ V,	$V_{EE} = -4.5$ V ± 0.3 V,	See Note 3	–1810		–1620	mV
I_{CCH}		$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V			17	24	mA
I_{CCL}		$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V			14.5	21	mA
I_{EE}		$V_{CC} = 5.5$ V,	$V_{EE} = -4.8$ V			–104	–149	mA
C_i		$V_{CC} = 5$ V,	$V_{EE} = -4.5$ V,	$f = 10$ MHz		4		pF

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

[§] All typical values are at $V_{CC} = 5$ V, $V_{EE} = -4.5$ V, $T_A = 25^\circ\text{C}$.

NOTES: 2. Each 100KT series circuit has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

3. Outputs are terminated through a 50-Ω resistor to –2 V.

timing requirements

			V _{CC} = 4.5 V to 5.5 V, V _{EE} = –4.2 V to –4.8 V, T _A = MIN to MAX†		UNIT
			MIN	MAX	
f _{clock}	Clock frequency		0	180	MHz
t _w	Pulse duration, CLK	High	1.5		ns
		Low	2.5		
t _{su}	Setup time, data before CLK↑	High	4		ns
		Low	4		
t _h	Hold time, data after CLK↑	High	1		ns
		Low	1		

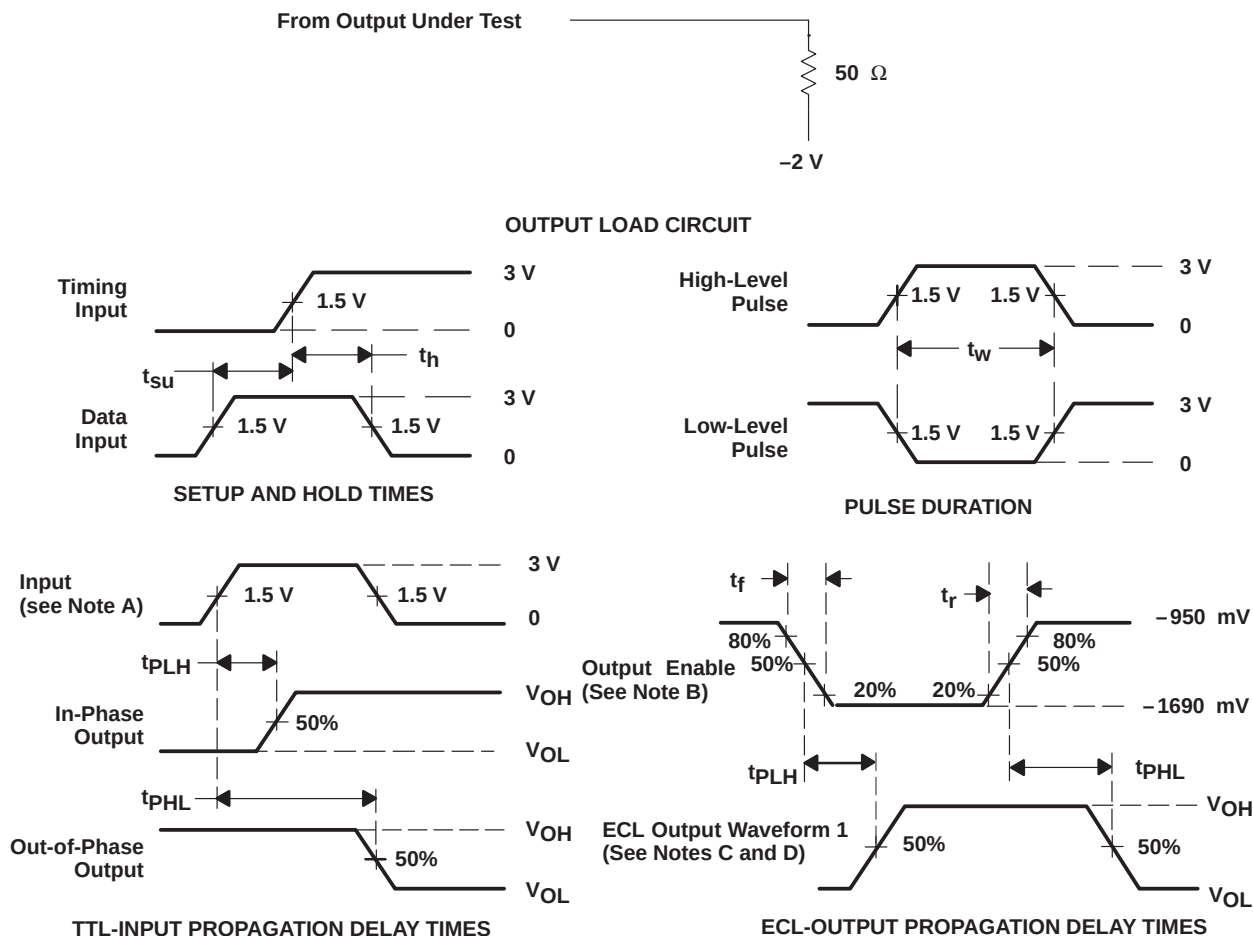
switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Figure 1)

PARAMETER	FROM (IINPUT)	TO (OUTPUT)	MIN	TYP‡	MAX	UNIT
f _{max}			180			MHz
t _{PLH}	CLK	Q	0.8	2.3	4.1	ns
t _{PHL}			0.8	2.2	3.8	
t _{PLH}	$\overline{\text{OE}}$	Q	0.5	1.4	3	ns
t _{PHL}			0.5	1.7	3.4	
t _r		Y		1.5		ns
t _f		Y		1.5		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, V_{EE} = –4.5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 2.5$ ns, $t_f = 2.5$ ns.
- B. For ECL inputs, input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r = 0.7$ ns, $t_f = 0.7$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by $\overline{OE}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN100KT5578DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN100KT5578NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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