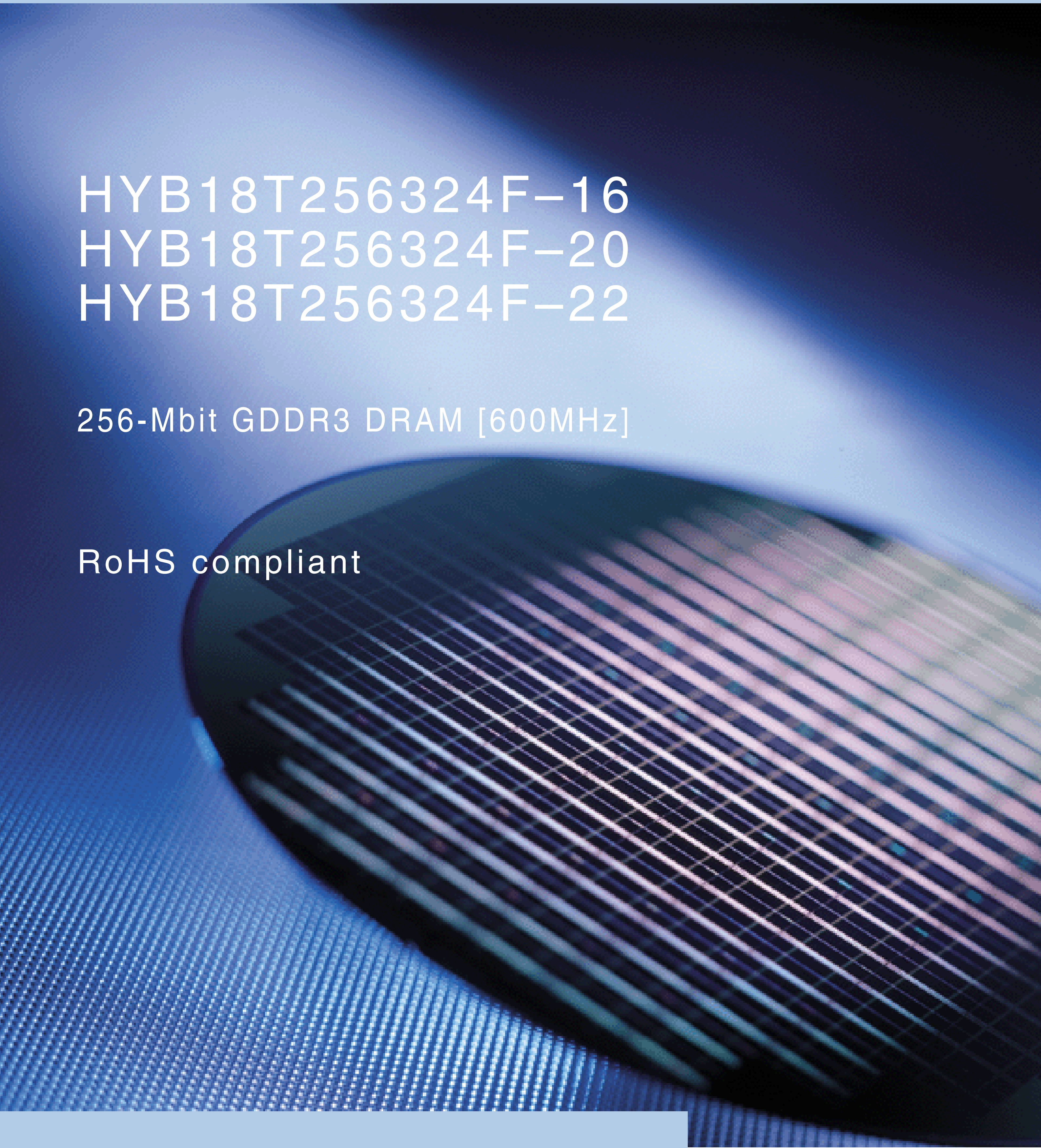
Data Sheet, Rev. 1.11, April 2005



HYB18T256324F–16
HYB18T256324F–20
HYB18T256324F–22

256-Mbit GDDR3 DRAM [600MHz]

RoHS compliant

Memory Products

Never stop thinking.

Edition 04-2005

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HYB18T256324F–16 HYB18T256324F–20 HYB18T256324F–22

Revision History:	**Rev. 1.11**	**04-2005**
Previous Revision:	Rev. 1.0	

Page	Subjects (major changes since last revision)
2	added disclaimer
30	figure 11: note 1 changed
75	table 41: added currents for -16
79	table 42-44: new values

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Table of Contents

1 Overview

1.1 Features

- Maximum clock frequency of 600 MHz
- Organization: 2048K x 32 x 4 banks
- 4096 rows and 512 columns (128 burst start locations) per bank
- Differential clock inputs (CLK and $\overline{\text{CLK}}$)
- CAS latencies of 5, 6 and 7
- Write latencies of 2, 3, 4
- Fixed burst sequence with length of 4.
- 4n prefetch
- Short RAS to CAS timing for Writes
- t_{RAS} Lockout support
- t_{WR} programmable for Writes with Auto-Precharge
- Data mask for write commands
- Single ended READ strobe (RDQS) per byte. RDQS edge-aligned with READ data
- Single ended WRITE strobe (WDQS) per byte. WDQS center-aligned with WRITE data
- DLL aligns RDQS and DQ transitions with Clock
- Programmable IO interface including on chip termination (ODT)
- Autoprecharge option with concurrent autoprecharge support
- 4K Refresh (32ms)
- Autorefresh and Self Refresh
- P-TBGA 144 package (11mm × 11mm)
- V_{DD} / V_{DDQ} Voltage (according to **Table 1**)
- Calibrated output drive. Active termination support.

Table 1 Key Timing and Power Supply Parameters

Speed Sort		**–1.6**	**- 2.0**	**- 2.2**	**Units**
Power Supply	V_{DD} / V_{DDQ}	**2.0 ± 100 mV**	**2.0 ± 100 mV**	**2.0 ± 100 mV**	**V**
CAS latency = 7	$t_{CK7\ min}$	1.6	2.0	2.2	ns
	$f_{CK7\ max}$	600	500	455	MHz
CAS latency = 6	$t_{CK6\ min}$	2.0	2.0	2.2	ns
	$f_{CK6\ max}$	500	500	455	MHz
CAS latency = 5	$t_{CK5\ min}$	—	—	2.7	ns
	$f_{CK5\ max}$	—	—	370	MHz
Access Time	t_{ACmin}	–0.4	–0.4	–0.45	ns
	t_{ACmax}	0.4	0.4	0.45	ns
RDQS-DQ Skew	t_{DQSQ}	0.225	0.225	0.25	ns

Table 2 Ordering Information

Part Number[1)]	Organisation	V_{DD} / V_{DDQ} (V)	Clock (MHz)	Package
HYB18T256324F–16	×32	2.0	600	P-TBGA 144
HYB18T256324F–20		2.0	500	
HYB18T256324F–22		2.0	455	

1) HYB: designator for memory components
256: 256-Mbit density
32: 32 bit interface
4: Die Revision
F: Green Product

1.2 General Description

The Infineon 256-Mbit GDDR3 DRAM [600MHz]is a high speed memory device, designed for high bandwidth intensive applications like PC graphics systems. The chip's quad bank architecture is optimized for high speed and achieves a peak bandwidth of 8 Gbyte/s using a 32 bit interface and a maximum system clock of 600 MHz.

HYB18T256324F–[16/20/22] uses a double data rate interface and a $4n$-prefetch architecture. The GDDR3 interface transfers two 32 bit wide data words per clock cycle to/from the I/O pins. Corresponding to the $4n$-prefetch a single write or read access consists of a 128 bit wide, one-clock-cycle data transfer at the internal memory core and four corresponding 32 bit wide, one-half-clock-cycle data transfers at the I/O pins.

Single-ended unidirectional Read and Write Data strobes are transmitted simultaneously with Read and Write data respectively in order to capture data properly at the receivers of both the Graphics SDRAM and the controller. Data strobes are organized per byte of the 32 bit wide interface. For read commands the RDQS are edge-aligned with data, and the WDQS are center-aligned with data for write commands.

The HYB18T256324F–[16/20/22] operates from a differential clock (CLK and $\overline{\text{CLK}}$). Commands (addresses and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of WDQS, and output data is referenced to both edges of RDQS.

In this document references to 'the positive edge of CLK' imply the crossing of the positive edge of CLK and the negative edge of $\overline{\text{CLK}}$. Similarly, the 'negative edge of CLK' refers to the crossing of the negative edge of CLK and the positive edge of $\overline{\text{CLK}}$. References to RDQS are to be interpreted as any or all RDQS<3:0>. WDQS, DM and DQ should be interpreted in a similar fashion.

Read and write accesses to the HYB18T256324F–[16/20/22] are burst oriented. The burst length is fixed to 4 and the two least significant bits of the burst address are 'Don't Care' and internally set to LOW. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the column location for the burst access. Each of the 4 banks consists of 4096 row locations and 512 column locations. An AUTO PRECHARGE function can be combined with READ and WRITE to provide a self-timed row precharge that is initiated at the end of the burst access. The pipelined, multibank architecture of the HYB18T256324F–[16/20/22] allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The device is supplied with 2.0 V for output drivers and core. (V_{DD} / V_{DDQ} voltages see **Table 1**)

The "On Die Termination" interface (ODT) is optimized for high frequency digital data transfers and is internally controlled. The termination resistor value can be set using an external ZQ resistor or disabled through the Extended Mode Register.

The output driver impedance can be set using the Extended Mode Register. It can either be set to ZQ / 6 (autocalibration) or to 35, 40 or 45 Ohms.

Auto Refresh and Power Down with Self Refresh operations are supported.

A standard P-TBGA 144 package is used which enables ultra high speed data transfer rates and a simple upgrade path from former DDR Graphics SDRAM products.

2 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12
A	$WDQS_0$	$RDQS_0$	V_{SSQ}	DQ_3	DQ_2	DQ_0	DQ_{31}	DQ_{29}	DQ_{28}	V_{SSQ}	$RDQS_3$	$WDQS_3$
B	DQ_4	DM_0	V_{DDQ}	V_{DDQ}	DQ_1	V_{DDQ}	V_{DDQ}	DQ_{30}	V_{DDQ}	V_{DDQ}	DM_3	DQ_{27}
C	DQ_6	DQ_5	V_{SSQ}	V_{SSQ}	V_{SSQ}	V_{DD}	V_{DD}	V_{SSQ}	V_{SSQ}	V_{SSQ}	DQ_{26}	DQ_{25}
D	DQ_7	RFU	V_{DD}	V_{SS}	V_{SSQ}	V_{SS}	V_{SS}	V_{SSQ}	V_{SS}	V_{DD}	RFU	DQ_{24}
E	DQ_{17}	DQ_{16}	V_{DDQ}	V_{SSQ}	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SSQ}	V_{DDQ}	DQ_{15}	DQ_{14}
F	DQ_{19}	DQ_{18}	V_{DDQ}	V_{SSQ}	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SSQ}	V_{DDQ}	DQ_{13}	DQ_{12}
G	$WDQS_2$	$RDQS_2$	V_{DDQ}	V_{SSQ}	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SSQ}	V_{DDQ}	$RDQS_1$	$WDQS_1$
H	DQ_{20}	DM_2	V_{DDQ}	V_{SSQ}	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SS} therm	V_{SSQ}	V_{DDQ}	DM_1	DQ_{11}
J	DQ_{21}	DQ_{22}	V_{DDQ}	V_{SSQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SSQ}	V_{DDQ}	DQ_9	DQ_{10}
K	DQ_{23}	A_3	V_{DD}	V_{SS}	RFU	V_{DD}	V_{DD}	RFU	V_{SS}	V_{DD}	A_4	DQ_8
L	V_{REF}	A_2	A_{10}	RAS#	RESET	CKE	RFU	ZQ	CS#	A_9	A_5	V_{REF}
M	A_0	A_1	A_{11}	BA_0	CAS#	CLK	CLK#	WE#	BA_1	A_8/AP	A_6	A_7

144 BALL P-TFBGA: TOP VIEW

Figure 1 Standard Ballout 256-Mbit GDDR3 DRAM [600MHz]

Note: Figure shows top view

2.1 Ball Definition and Description

Table 3 Ball description

Ball	Type	Detailed Function
CLK, $\overline{\text{CLK}}$	Input	**Clock:** CLK and $\overline{\text{CLK}}$ are differential clock inputs. Address and command inputs are latched on the positive edge of CLK. Graphics SDRAM outputs (RDQS, DQs) are referenced to CLK. CLK and $\overline{\text{CLK}}$ are not internally terminated.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock and input buffers. Taking CKE LOW provides Power Down. If all banks are precharged, this mode is called Precharge Power Down and Self Refresh mode is entered if a Autorefresh command is issued. If at least one bank is open, Active Power Down mode is entered and no Self Refresh allowed. All input receivers except CLK, $\overline{\text{CLK}}$ and CKE are disabled during Power Down. In Self Refresh mode the clock receivers are disabled too. Self Refresh Exit is performed by setting CKE asynchronously HIGH. Exit of Power Down without Self Refresh is accomplished by setting CKE HIGH with a positive edge of CLK. The value of CKE is latched asynchronously by Reset during Power On to determine the value of the termination resistor of the address and command inputs. CKE is not allowed to go LOW during a RD, a RW or a snoop BURST.
$\overline{\text{CS}}$	Input	**Chip Select:** $\overline{\text{CS}}$ enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands with the exeption of DETERNIS are ignored, but internal operations continue. $\overline{\text{CS}}$ is one of the four command balls.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	**Command Inputs:** Sampled at the positive edge of CLK, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define (together with $\overline{\text{CS}}$) the command to be executed.
DQ<0:31>	I/O	**Data Input/Output:** The DQ signals form the 32 bit data bus. During READs the balls are outputs and during WRITEs they are inputs. Data is transferred at both edges of RDQS.
DM<0:3>	Input	**Input Data Mask:** The DM signals are input mask signals for WRITE data. Data is masked when DM is sampled HIGH with the WRITE data. DM is sampled on both edges of WDQS. DM0 is for DQ<0:7>, DM1 is for DQ<8:15>, DM2 is for DQ<16:23> and DM3 is for DQ<24:31>. Although DM balls are input-only, their loading is designed to match the DQ and WDQS balls.
RDQS<0:3>	Output	**Read Data Strobes:** RDQSx are unidirectional strobe signals. During READs the RDQSx are transmitted by the Graphics SDRAM and edge-aligned with data. RDQS have preamble and postamble requirements. RDQS0 is for DQ<0:7>, RDQS1 for DQ<8:15>, RDQS2 for DQ<16:23> and RDQS3 for DQ<24:31>.
WDQS<0:3>	Input	**Write Data Strobes:** WDQS are unidirectional strobe signals. During WRITEs the WDQS are generated by the controller and center aligned with data. WDQS have preamble and postamble requirements. WDQS0 is for DQ<0:7>, WDQS1 for DQ<8:15>, WDQS2 for DQ<16:23> and WDQS3 for DQ<24:31>.
BA<0:1>	Input	**Bank Address Inputs:** BA select to which internal bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA are also used to distinguish between the MODE REGISTER SET and EXTENDED MODE REGISTER SET commands.
A<0:11>	Input	**Address Inputs:** During ACTIVATE, A0-A11 defines the row address. For READ/WRITE, A2-A7 and A9 defines the column address, and A8 defines the auto precharge bit. If A8 is HIGH, the accessed bank is precharged after execution of the column access. If A8 is LOW, AUTO PRECHARGE is disabled and the bank remains active. Sampled with PRECHARGE, A8 determines whether one bank is precharged (selected by BA<0:1>, A8 LOW) or all 4 banks are precharged (A8 HIGH). During (EXTENDED) MODE REGISTER SET the address inputs define the register settings. A<0:11> are sampled with the positive edge of CLK.
ZQ	-	**ODT Impedance Reference:** The ZQ ball is used to control the ODT impedance.

Table 3 **Ball description**

Ball	Type	Detailed Function
RES	Input	**Reset pin:** The RES pin is a V_{DDQ} CMOS input. RES is not internally terminated. The LOW to HIGH transition of the Reset signal is used to latch the CKE value during Power On in order to set the value of the termination resistors of the address and command inputs. When RES is LOW, all terminations are switched off. The LOW to HIGH transition of the RES signal must occur at the beginning of the power up sequence in order to insure functionnality.
V_{ref}	Supply	**Voltage Reference:** V_{ref} is the reference voltage input.
V_{DD}, V_{SS}	Supply	**Power Supply:** Power and Ground for the internal logic.
V_{DDQ}, V_{SSQ}	Supply	**I/O Power Supply:** Isolated Power and Ground for the output buffers to provide improved noise immunity.
NC, RFU	-	Please do not connect No Connect and Reserved for Future Use balls.

2.2 Functional Block Diagram

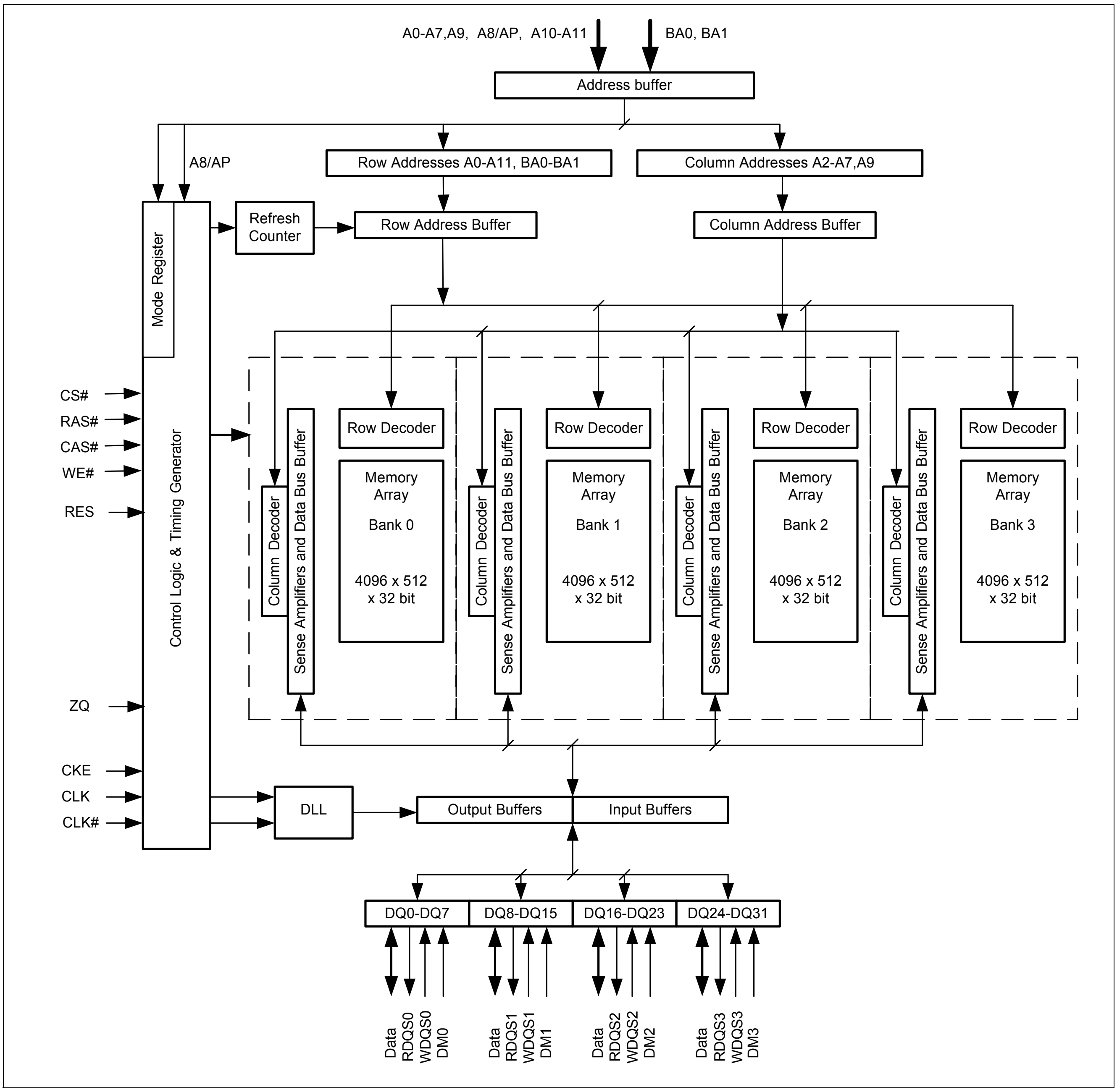

Figure 2 Functional Block Diagram

2.3 Commands

2.3.1 Command Table

In the following table CKEn refers to the positive edge of CLK corresponding to the clock cycle when the command is given to the Graphics SDRAM. CKEn-1 refers to the previous positive edge of CLK. For all command and address inputs CKEn is implied.

All input states or sequences not shown are illegal or reserved.

Table 4 Command Overview

Operation	Code	CKE n-1	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0	BA1	A8	A2-7 A9-11	Note
Device Deselect	DESEL	H	H	H	L X H	X X H	X L H	X	X	X	X	1
Data Terminator Disable	DTERDIS	H	H	H	H	L	H	X	X	X	X	1,9
No Operation	NOP	H	H	L	H	H	H	X	X	X	X	
Mode Register Set	MRS	H	H	L	L	L	L	0	0	OPCODE		
Extended Mode Register Set	EMRS	H	H	L	L	L	L	1	0	OPCODE		
Bank Activate	ACT	H	H	L	L	H	H	BA	BA	Row Address		1,2
Read	RD	H	H	L	H	L	H	BA	BA	L	Col.	1,3
Read w/ Autoprecharge	RD/A	H	H	L	H	L	H	BA	BA	H	Col.	1,3
Write	WR	H	H	L	H	L	L	BA	BA	L	Col.	1,3
Write w/ Autoprecharge	WR/A	H	H	L	H	L	L	BA	BA	H	Col.	1,3
Precharge	PRE	H	H	L	L	H	L	BA	BA	L	X	1
Precharge All	PREALL	H	H	L	L	H	L	X	X	H	X	1
Auto Refresh	AREF	H	H	L	L	L	H	X	X	X	X	1,4
Power Down Mode Entry	PWDNEN	H	L	H L	X H	X H	X H	X	X	X	X	1,5
Power Down Mode Exit	PWDNEX	L	H	X	X	X	X	X	X	X	X	1,6
Self Refresh Entry	SREFEN	H	L	L	L	L	H	X	X	X	X	1,7
Self Refresh Exit	SREFEX	L	H	X	X	X	X	X	X	X	X	1,8

1. *X represents “Don’t Care”.*
2. *BA0 and BA1 provide bank address, A0 - A11 provide the row address.*
3. *BA0 and BA1 provide bank address, A2- A7, A9 provide the column address, A8/AP controls Auto Precharge.*
4. *Auto Refresh and Self Refresh Entry differ only by the state of CKE*
5. *PWDNEN is selected by issuing a DESEL or NOP at the first positive CLK edge following the HIGH to LOW transition of CKE.*
6. *First possible valid command after t_{XPN}. During t_{XPN} only NOP or DESEL commands are allowed.*
7. *Self Refresh is selected by issuing AREF at the first positive CLK edge following the HIGH to LOW transition of CKE.*
8. *First possible valid command after t_{XSC}. During t_{XSC} only NOP or DESEL commands are allowed.*
9. *This command is invoked when a Read is issued on another DRAM rank placed on the same command bus. Cannot be in power-down or self-refresh state. The Read command will cause the data termination to be disabled. Refer to for timing.*

Abbreviations:

BA:Bank Address

Col.:Column Address

2.3.2 Description of Commands

Table 5 Description of Commands

Command	Description
DESEL	The DESEL function prevents new commands from being executed by the Graphics SDRAM. The Graphics SDRAM is effectively deselected. Operations in progress are not affected.
NOP	The NOP command is used to perform a no operation to the Graphics SDRAM, which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.
MRS	The Mode Register is loaded via address inputs A0 - A11. For more details see sections **Chapter 3.5**. The MRS command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
EMRS	The Extended Mode Register is loaded via address inputs A0 - A11. For more details see section **Chapter 3.4**. The EMRS command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
ACT	The ACT command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 and BA1 inputs selects the bank, and the address provided in inputs A0 - A11 selects the row. This row remains active (or open) for accesses until a precharge (PRE, RD/A, or WR/A command) is issued to that bank. A precharge must be issued before opening a different row in the same bank.
RD	The RD command is used to initiate a burst read access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For RD commands the value on A8 is set LOW.
RD/A	The RD/A command is used to initiate a burst read access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the read burst. The same individual-bank precharge function is performed like it is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user must not issue a new ACT command to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section **Chapter 3.10**.
WR	The WR command is used to initiate a burst write access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For WR commands the value on A8 is set LOW. Input data appearing on the DQs is written to the memory array depending on the value on the DM input appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed for that byte / column location.
WR/A	The WR/A command is used to initiate a burst write access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the write burst. The same individual-bank precharge function is performed which is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user is not allowed to issue a new ACT to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section **Chapter 3.7**. Input data appearing on the DQs is written to the memory array depending on the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed for that byte / column location.

Table 5 **Description of Commands**

Command	Description
PRE	The PRE command is used to deactivate the open row in a particular bank. The bank will be available for a subsequent row access a specified time (t_{RP}) after the PRE command is issued. Inputs BA0 and BA1 select the bank to be precharged. A8/AP is set to LOW. Once a bank has been precharged, it is in the idle state and must be activated again prior to any RD or WR commands being issued to that bank. A PRE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.
PREALL	The PREALL command is used to deactivate all open rows in the memory device. The banks will be available for a subsequent row access a specified time (t_{RP}) after the PREALL command is issued. Once the banks have been precharged, they are in the idle state and must be activated prior to any read or write commands being issued. The PREALL command will be treated as a NOP for those banks where there is no open row, or if a previously open row is already in the process of precharging. PREALL is issued by a PRE command with A8/AP set to HIGH.
AREF	The AREF is used during normal operation of the GDDR3 Graphics RAM to refresh the memory content. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AREF command. The HYB18T256324F–[16/20/22] requires AREF cycles at an average periodic interval of t_{REFI}(max)=7.8µs. To improve efficiency a maximum number of eight AREF commands can be posted to one memory device (with t_{RFC} from AREF to AREF) as described in section **Chapter 3.11**. This means that the maximum absolute interval between any AREF command is 8 x 7.8µs (62.4µs). This maximum absolute interval is to allow the GDDR3 Graphics RAM output drivers and internal terminators to recalibrate, compensating for voltage and temperature changes. All banks must be in the idle state before issuing the AREF command. They will be simultaneously refreshed and return to the idle state after AREF is completed. tRFC is the minimum required time between an AREF command and a following ACT/AREF command.
SREFEN	The Self Refresh function can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When entering the self refresh mode by issuing the SREFEN command, the GDDR3 Graphics RAM retains data without external clocking. The SREFEN command is initiated like an AREF command except CKE is disabled (LOW). The DLL is automatically disabled upon entering Self Refresh mode and automatically enabled and reset upon exiting Self Refresh. (200 cycles must then occur before a RD command can be issued) The adress, command and data terminators remain on input signals except CKE are “Don’t Care”. If two GDDR3 Graphics RAMs share the same cimmand and address bus, Self Refresh max be entered only for the two devices at the sme time.
SREFEX	The SREFEX command is used to exit the self refresh mode. The DLL is automatically enabled and resetted upon exiting. The procedure for exiting self refresh requires a sequence of commands. First CLK and $\overline{CLK}$ must be stable prior to CKE going from LOW to HIGH. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XSNR} is satisfied. This time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and output calibration is to apply NOPs for 200 cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.
PWDNEN	The PWDNEN command enables the power down mode. It is entered when CKE is set low together with a NOP/DESEL. The CKE signal is sampled at the rising edge of the clock. Once the power down mode is initiated, all of the receiver circuits except CLK and CKE are gated off to reduce power consumption. The DLL remains active (unless disabled before with EMRS). All banks can be set to idle state or stay active. During Power Down Mode, refresh operations cannot be performed; therefore the refresh conditions of the chip have to be considered and if necessary Power Down state has to be left to perform an Autorefresh cycle.

Table 5 **Description of Commands**

Command	Description
PWDNEX	A CKE HIGH value sampled at a low to high transition of CLK is required to exit power down mode. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XPN} is satisfied. After t_{XPN} any command can be issued, but it has to comply with the state in which the power down mode was entered.
DTERDIS	Data Termination Disable (Bus snooping for RD commands) : The Data Termination Disable Command is detected by the device by snooping the bus for RD commands excluding $\overline{CS}$. The GDDR3 Graphics RAM will disable its Data terminators when a RD command is detected. The terminators are disabled starting at CL - 1 clocks after the RD command is detected and the duration is 4 clocks. In a two rank system, both DRAM devices will snoop the bus for RD commands to either device and both will disable their terminators if a RD command is detected. The command and address terminators are always enabled. See **Figure 9** for an example of when the data terminators are disabled during a RD command.

Table 6 **Minimum delay from RD/A and WR/A to any other command (to another bank) with concurrent Autoprecharge**

From Command	To Command	Minimum delay to another bank (with concurrent autoprecharge)	Note
WR/A	RD or RD/A	(WL + 2) . t_{CK} + t_{WTR}	
	WR or WR/A	2 . t_{CK}	
	PRE	t_{CK}	
	ACT	t_{CK}	
RD/A	RD or RD/A	2 . t_{CK}	
	WR or WR/A	(CL + 4 - WL) . t_{CK}	
	PRE	t_{CK}	
	ACT	t_{CK}	

2.4 State Diagram and Truth Tables

2.4.1 State Diagram for One Activated Bank

The following diagram shows all possible states and transitions for one activated bank. The other three banks of the Graphics SDRAM are assumed to be in idle state.

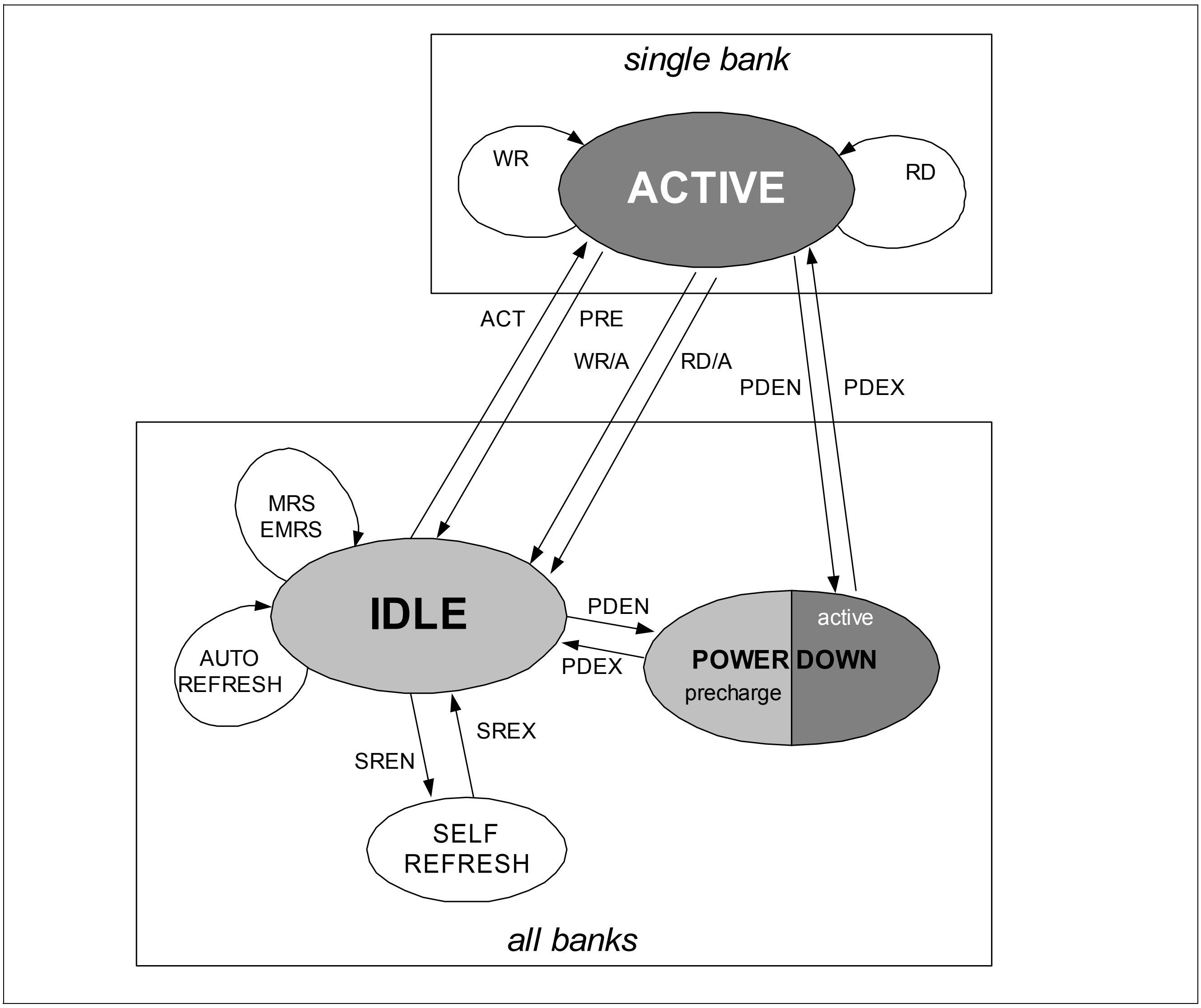

Figure 3 State diagram for one bank

Note: MRS, EMRS, AUTO REFRESH, SELF REFRESH and precharge POWER DOWN are only allowed if all four banks are idle.

2.4.2 Function Truth Table for more than one Activated Bank

If there is more than one bank activated in the Graphics SDRAM, some commands can be performed in parallel due to the chip's multibank architecture. The following table defines for which commands such a scheme is possible. All other transitions are illegal. Notes 1-11 define the start and end of the actions belonging to a submitted command. This table is based on the assumption that there are no other actions ongoing on bank n or bank m. If there are any actions ongoing on a third bank t_{RRD}, t_{RTW} and t_{WTR} have to be taken always into account.

Table 7 Function Truth Table I

Current State	ongoing action on bank n	possible action in parallel on bank m
ACTIVE	ACTIVATE [1]	ACT, PRE, WRITE, WRITE/A, READ, READ/A [12]
	WRITE [2]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[13]
	WRITE/A [3]	ACT, PRE, WRITE, WRITE/A, READ [14]
	READ [4]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[15]
	READ/A [5]	ACT, PRE, WRITE, WRITE/A, READ, READ/A [15]
	PRECHARGE [6]	ACT, PRE, WRITE, WRITE/A, READ, READ/A [12]
	PRECHARGE ALL [6]	-
	POWER DOWN ENTRY [7]	-
IDLE	ACTIVATE [1]	ACT
	POWER DOWN ENTRY [7]	-
	AUTO REFRESH [8]	-
	SELF REFRESH ENTRY [7]	-
	MODE REGISTER SET (MRS)[9]	-
	EXTENDED MRS [9]	-
POWER DOWN	POWER DOWN EXIT [10]	-
SELF REFRESH	SELF REFRESH EXIT [11]	-

1. *Action ACTIVATE starts with issuing the command and ends after t_{RCD}*
2. *Action WRITE starts with issuing the command and ends t_{WR} after the first pos. edge of CLK following the last falling WDQS edge; exept for READ, READ/A. WRITE, WRITE/A ends t_{WTR} after the first pos. edge of CLK following the last falling WDQS edge.*
3. *Action WRITE/A starts with issuing the command and ends t_{WR} after the first positive edge of CLK following the last falling WDQS edge; exept for READ, READ/A. WRITE, WRITE/A ends t_{WTR} after the first pos. edge of CLK following the last falling WDQS edge.*
4. *Action READ starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS*
5. *Action READ/A starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS*
6. *Action PRECHARGE and PRECHARGE ALL start with issuing the command and ends after t_{RP}*
7. *During POWER DOWN and SELF REFRESH only the EXIT commands are allowed*
8. *Action AUTO REFRESH starts with issuing the command and ends after t_{RFC}*
9. *Actions MODE REGISTER SET and EXTENDED MODE REGISTER SET start with issuing the command and ends after t_{MRD}*
10. *Action POWER DOWN EXIT starts with issuing the command and ends after t_{XPN}*
11. *Action SELF REFRESH EXIT starts with issuing the command and ends after t_{XSC}*
12. *During action ACTIVATE an ACT command on another bank is allowed considering t_{RRD}, a PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.*
13. *During action WRITE an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank must be separated by at least one NOP from the ongoing WRITE. RD or RD/A are not allowed before t_{WTR} is met.*

14. *During action WRITE/A an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank has to be separated by at least one NOP from the ongoing command. RD is not allowed before t_{WTR} is met. RD/A is not allowed during an ongoing WRITE/A action.*
15. *During action READ and READ/A an ACT or a PRE command on another bank is allowed any time. A new RD or RD/A command on another bank has to be separated by at least one NOP from the ongoing command. A WR or WR/A command on another bank has to meet t_{RTW}.*

2.4.3 Function Truth Table for CKE

Table 8 Function Truth Table II (CKE Table)

CKE n-1	CKE n	CURRENT STATE	COMMAND	ACTION
L	L	Power Down	X	stay in Power Down
		Self Refresh	X	stay in Self Refresh
L	H	Power Down	DESEL or NOP	Exit Power Down
		Self Refresh	DESEL or NOP	Exit Self Refresh [5]
H	L	All Banks Idle	DESEL or NOP	Entry Precharge Power Down
		Bank(s) Active	DESEL or NOP	Entry Active Power Down
		All Banks Idle	Auto Refresh	Entry Self Refresh

1. *CKE_n is the logic step at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.*
2. *Current state is the state of the GDDR3 Graphics RAM immediatly prior to clock edge n.*
3. *COMMAND is the command registered at clock edge n, and ACTION is a result of COMMAND.*
4. *All states and sequences not shown are illegal or reserved.*
5. *DESEL or NOP commands should be issued on any clock edges occuring during the t_{XSR} period. A minimum of 200 clock cycles is required before applying any other valid command.*

3 Functional Description

3.1 Clocks, CKE, Commands and Addresses

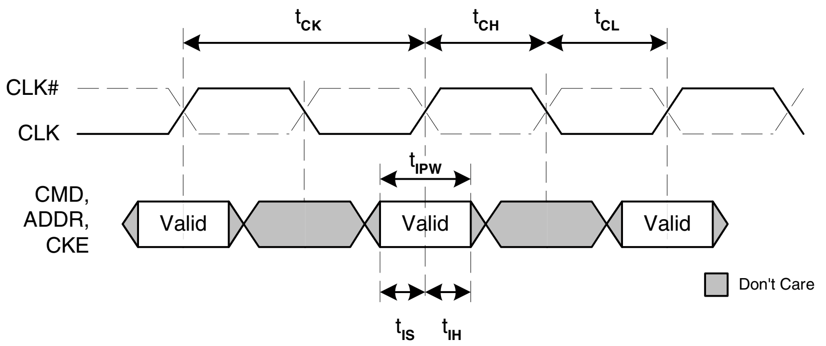

Figure 4 Clock, CKE and Command/Address Timings

Setup and Hold Timing for CKE is equal to CMD and ADDR Setup and Hold Timing. The DLL ensures the alignment of DQs and CLK. Therefore the preferred operation mode for high frequencies is DLL on. The DLL frequency range is from 600 MHz down to 250 MHz.

Table 9 General Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	CAS latency	Symbol	Limit Values						Unit
			–1.6		–2.0		–2.2		
			min	max	min	max	min	max	
Clock									
Clock Cycle Time	7	t_{CK7}	1.6	3.3	2.0	4.0	2.2	4.0	ns
	6	t_{CK6}	2.0	3.3	2.0	4.0	2.2	4.0	ns
	5	t_{CK5}	—	—	—	—	2.7	4.0	ns
System frequency	7	f_{CK7}	300	600	250	500	250	455	MHz
	6	f_{CK6}	300	500	250	500	250	455	MHz
	5	f_{CK5}	—	—	—	—	250	370	MHz
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Command, CKE and Address Setup and Hold Times									
Address/Command/CKE input setup time		t_{IS}	0.6	—	0.75	—	0.75	—	ns
Address/Command/CKE input hold time		t_{IH}	0.6	—	0.75	—	0.75	—	ns
Address/Command/CKE input pulse width		t_{IPW}	0.85	—	0.85	—	0.85	—	t_{CK}

3.2 Initialization

The HYB18T256324F–[16/20/22] must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation or permanent damage to the device.

The following sequence is highly recommended for Power-Up:

1. *Apply power (V_{DD}, V_{DDQ}, V_{REF}). Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF}. Maintain RES=L and CS=H to ensure that all the DQ ouputs will be in HiZ state, all active terminations off and the DLL off. All other pins may be undefined.*
2. *Maintain stable conditions for 200 µs minimum for the GDDR3 Graphics RAM to power up.*
3. *After clock is stable, set CKE to L. After t_{ATS} minimum set RES to high. On the rising edge of RES, the CKE value is latched to determine the address and command bus termination value. If CKE is sampled LOW the address termination value is set to ZQ / 2. If CKE is sampled HIGH, the address and command bus termination is set to ZQ.*
4. *After t_{ATH} minimum, set CKE to high.*
5. *Wait a minimum of 350 cycles to calibrate and update the address and command termination impedances. Issue DESELECT on the command bus during these 350 cycles.*
6. *Apply a PRECHARGE ALL command, followed by an Extended Mode Register command after t_{RP} is met and activate the DLL.*
7. *Issue an Mode Register Set command after tMRD is met to reset the DLL and define the operating parameters.*
8. *Wait 200 cycles of clock input to lock the DLL. No Read command can be applied during this time. Since the impedance calibration is already completed, the DLL mimic circuitry can use the actual programmed driver impedance value.*
9. *Issue a PRECHARGE ALL command or issue 4 single bank PRECHARGE commands, one to each of the 4 banks to place the chip in an idle state.*
10. *Issue two or more AUTO REFRESH commands to update the driver impedance.*

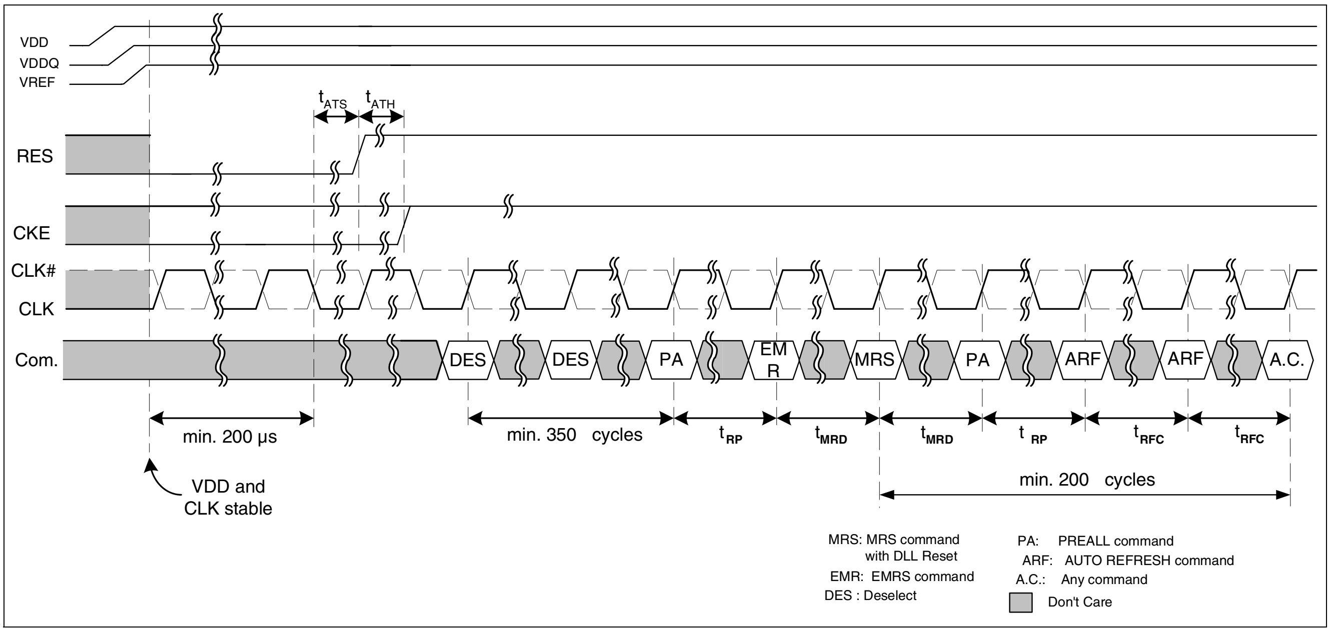

Figure 5 Power Up Sequence

Table 10 Reset Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
RES to CKE setup time	t_{ATS}	10	—	10	—	10	—	ns	
RES to CKE hold time	t_{ATH}	10	—	10	—	10	—	ns	

3.3 Programmable impedance output drivers and active terminations

3.3.1 GDDR3 IO Driver and Termination

The GDDR3 SGRAM is equipped with programmable impedance output buffers and active terminations. This allows the user to match the driver impedance to the system impedance.

To adjust the impedance of DQ<0:31> and RDQS<0:3> , an external precision resistor (ZQ) is connected between the ZQ pin and VSS. The value of the resitor must be six times the value of the desired impedance. For example, a 240Ω resistor is required for an output impedance of 40Ω. The range of ZQ is 210Ω to 270Ω, giving an output impedance range of 35Ω to 45Ω (one sixth the value of ZQ within 10%). RES, CLK and $\overline{\text{CLK}}$ are not internally terminated.

The value of ZQ is used to calibrate the internal DQ termination resistors of DQ<0:31>, WDQS<0:3> and DM<0:3>. The two termination values that are selectable using EMRS[3:2] are ZQ / 4 and ZQ / 2.

The value of ZQ is also used to calibrate the internal address command termination resistors. The inputs terminated in this manner are A<0:11>, CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$. The two termination values that are selectable upon power up (CKE latched a the LOW to HIGH transition of RES) are ZQ/2 and ZQ.

The signals RES and CLK/$\overline{\text{CLK}}$ are not internally terminated.

If no resistance is connected to ZQ, an internal default value of 240Ω will be used. In this case, no calibration will be performed.

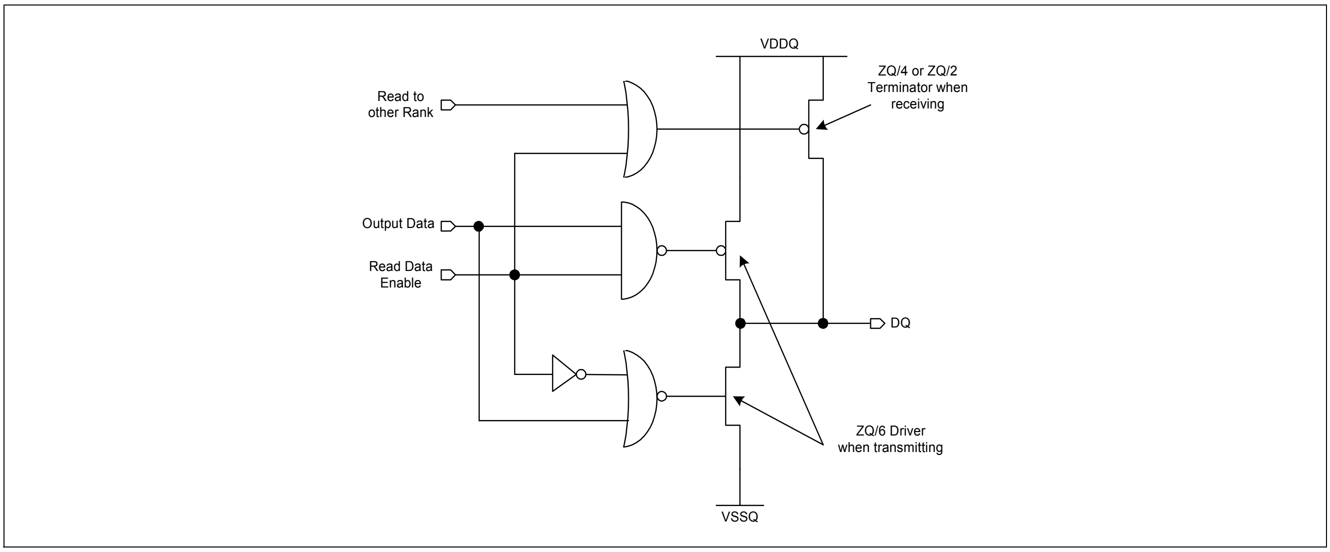

Figure 6 Output Driver simplified schematic

Table 11 Range of external resistance ZQ

Parameter	Symbol	min	nom	max	Unit	Notes
External resistance value	ZQ	210	240	270	Ω	

Table 12 Termination types and activation

Ball	Termination type	Termination activation
CLK, $\overline{\text{CLK}}$, RDQS<0:3>, ZQ, RES	No termination	
CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA<0:1>, A<0:11>	Add / CMDs	Always ON
DM<0:3>, WDQS<0:3>,	DQ	Always ON
DQ<0:31>	DQ	CMD bus snooping

3.3.2 Self Calibration for Driver and Termination

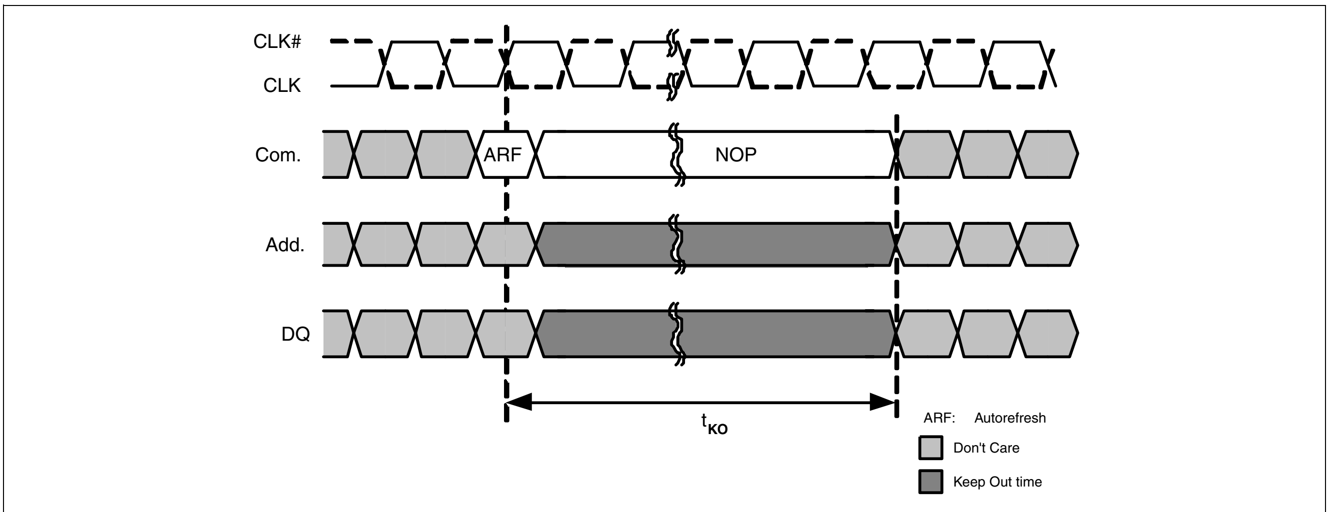

Figure 7 Termination update keep out time after Autorefresh command

Table 13 Termination update Keep Out time

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Termination update Keep Out time	t_{KO}	10	—	10	—	10	—	ns	

To guarantee optimum driver impedance after power-up, the GDDR3 SGRAM needs 350 cycles after the clock is applied and stable to calibrate the impedance upon power-up. The user can operate the part with fewer than 350 cycles, but optimal output impedance will not be guaranteed.

The GDDR3 Graphics RAM proceeds in the following manner for Self Calibration :

The PMOS device is calibrated against the external ZQ resistor value (**Figure 8**). First one PMOS leg is calibrated against ZQ. The number of legs used for the terminators (DQ and ADD/CMD) and the PMOS driver is represented in **Table 14**. Next, one NMOS leg is calibrated against the already calibrated PMOS leg. The NMOS driver uses 6 NMOS legs.

Table 14 Number of Legs used for Terminator and Driver Self Calibration

			Termination	Number of Legs	Notes
		CKE (at RES)			
Terminator	ADD / CMD	0	ZQ/2	2	
		1	ZQ	1	
		EMRS[3:2]			
	DQ	00	Disabled	0	1
		10	ZQ/4	4	
		11	ZQ/2	2	
Driver	PMOS		ZQ/6	6	
	NMOS		ZQ/6	6	

Note: EMRS[3:2] = 00 disables the ADD and CMD terminations as well.

Figure 8 represents a simplified schematic of the calibration circuits. First, the strength control bits are adjusted in such a way that the V_{DDQ} voltage is divided equaly between the PMOS device and the ZQ resistor. The best bit pattern will cause the comparator to switch the PMOS Match signal output value. In a second step, the NFET is calibrated against the already calibrated PFET. In the same manner, the best control bit combination will cause the comparator to switch the NMOS Match signal output value.

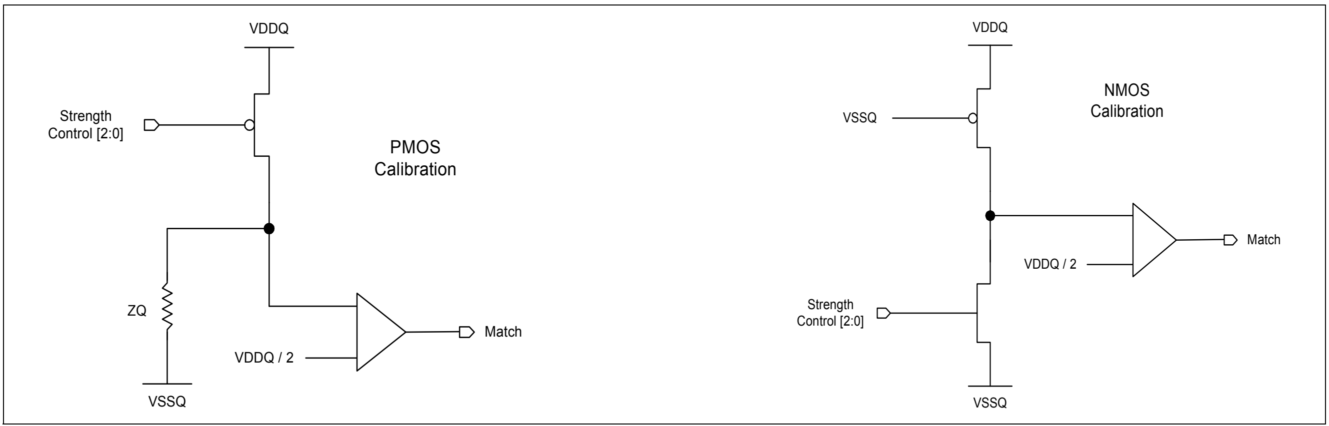

Figure 8 Self Calibration of PMOS and NMOS Legs

3.3.3 Dynamic Switching of DQ terminations

The GDDR3 Graphics RAM will disable its data terminators when a READ or DTERDIS command is detected. The terminators are disabled starting at CL - 1 Clocks after the READ / DTERDIS command is detected and the duration is 4 clocks. In a two rank system, both devices will snoop the bus for a READ / DTERDIS command to either device and both will disable their terminators if a READ / DTERDIS command is detected. The address and command terminators are always enabled.

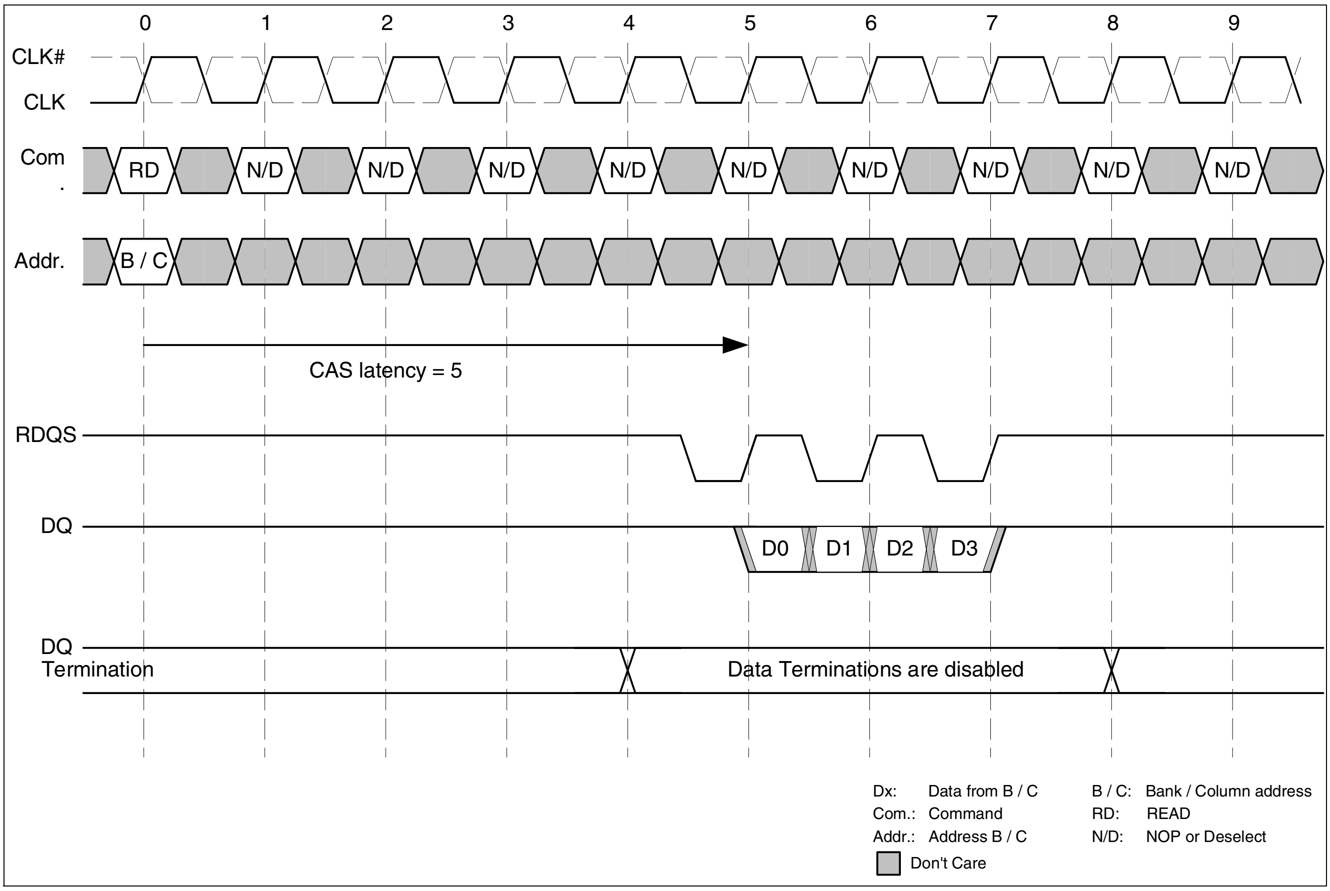

Figure 9 ODT Disable Timing during a READ command

3.3.4 Output impedance and Termination DC Electrical Characteristics

The Driver and Termination impedances are determined by applying $V_{DDQ/2}$ nominal (1.0 V) at the corresponding input / output and by measuring the current flowing into or out of the device. V_{DDQ} is set to the nominal value of 2.0 V. (see **Table 1**)

I_{OH} is the current flowing out of DQ when the Pull-Up transistor is activated and the DQ termination disabled.

I_{OL} is the current flowing into DQ when the Pull-Down transistor is activated and the DQ termination disabled.

$I_{TCAH(ZQ)}$ is the current flowing out of the Termination of Commands and Addresses for a ZQ termination value.

Table 15 DC Electrical Characteristics

Parameter		Nom.		Unit	Notes
	ZQ Value	240		Ω	
		min	max		
I_{OH}	ZQ/6	20.5	25.0	mA	1
I_{OL}	ZQ/6	20.5	25.0	mA	1
$I_{TCAH(ZQ)}$	ZQ	3.4	4.2	mA	1

*Note: 1: Measurement performed with V_{DDQ} =2.0 V (nominal see **Table 1**) and by applying $V_{DDQ/2}$ (1.0 V) at the corresponding Input / Output.*
$0°C \leq T_C \leq 85°C$.

3.4 Extended Mode Register Set Command (EMRS)

The Extended Mode Register is used to set the output driver impedance value, the termination impedance value, the Write Recovery time value for Write with Autoprecharge. It is used as well to enable/disable the DLL, to issue the Vendor ID and to enable/disable the Low Power mode. There is no default value for the Extended Mode Register. Therefore it must be written after power up to operate the GDDR3 Graphics RAM. The Extended Mode Register can be programmed by performing a normal Mode Register Set operation and setting the BA0 bit to HIGH. All other bits of the EMR register are reserved and should be set to LOW.

The Extended Mode Register must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation).

The timing of the EMRS command operation is equivalent to the timing of the MRS command operation.

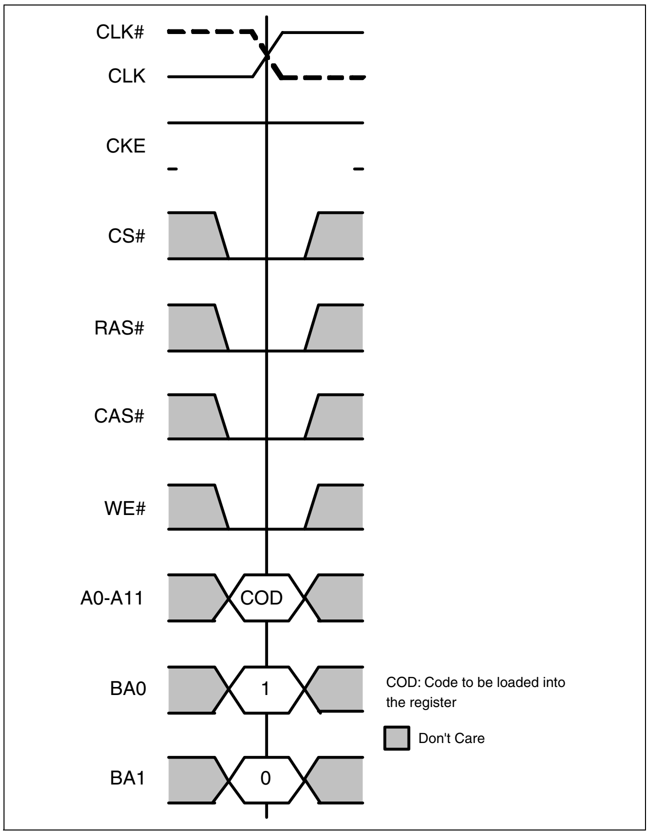

Figure 10 Extended Mode Register Bitmap

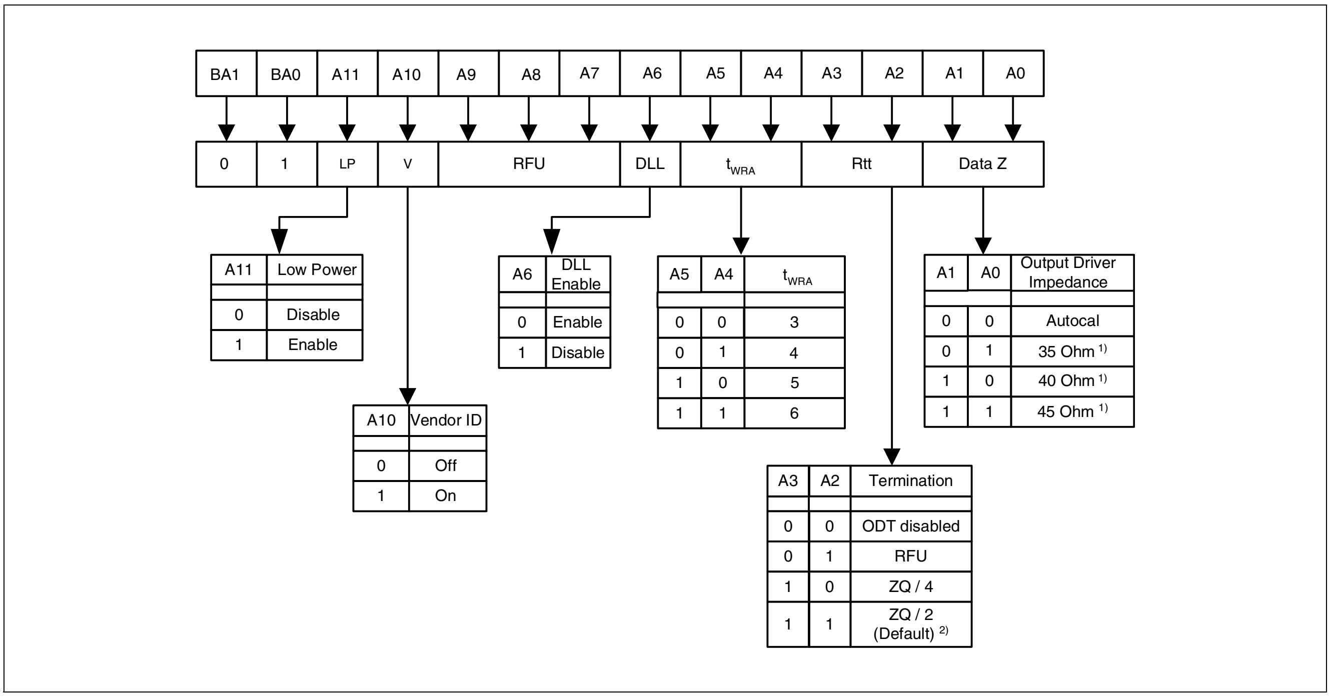

Figure 11 Extended Mode Register Bitmap

1. *Autocalibration is not supported for these settings.*
2. *Default termination values at Power Up.*

3. *The ODT disable function disables all terminators on th device.*
4. *If the user activates bits in an extended mode register in an optional field, either the optional field is activated (if option implemented on the device) or no action is taken by the device (if ioption not implemented).*
5. *WR (write recovery time for write with autoprecharge) in clock cycles is calculated by dividing tWR (in ns) and rounding up to the next integer (WR[cycles]=tWR[ns]/tCK[ns]). The mode register must be programmed to this value.*

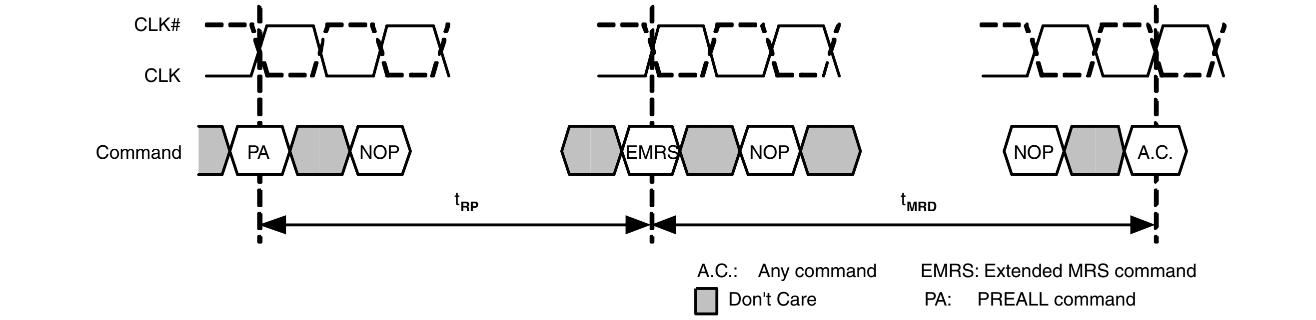

Figure 12 Extended Mode Register Set Timing

Table 16 EMRS Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Mode Register Set cycle time	t_{MRD}	5	—	4	—	4	—	t_{CK}	

3.4.1 DLL enable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL. (When the device exits self-refresh mode, the DLL is enabled automatically). Anytime the DLL is enabled, 200 cycles must occur before a READ command can be issued.

3.4.2 WR

The WR parameter is programmed using the register bits A4 and A5. This integer parameter defines as a number of clock cycles the Write Recovery time in a Write with Autoprecharge operation.

The following inequality has to be complied with : WR * $t_{CK} \geq t_{WR}$, where t_{CK} is the clock cycle time as defined in **Table 8** and t_{WR} the Write Recovery time as defined in **Table 23**.

*Note: Refer to **Figure 3.7.4** for more details.*

3.4.3 Termination Rtt

The data termination, Rtt , is used to set the value of the internal terminaton resistors. The GDDR III DRAM supports ZQ / 4 and ZQ / 2 termination values. The termination may also be disabled for testing and other purposes.

3.4.4 Output Driver Impedance

The Output Driver Impedance extended mode register is used to set the value of the data output driver impedance. When the autocalibration is used, the output driver impedance is set nominally to ZQ / 6.

3.4.5 Low Power

When the Low Power extended mode register is set, the device enters a low power mode of operation. This mode is not enabled for the HYB18T256324F–[16/20/22]. Setting this bit to HIGH will have no effect on the behavior of the GDDR3 DRAM.

3.4.6 Vendor Code and Revision Identification

The Manufacturer Vendor Code is selected by issuing an Extended Mode Register Set command with bit A10 set to 1 and bits A0-A9 and A11 set to the desired value. When the Vendor Code function is enabled the GDDR3 DRAM will provide the Infineon vendor code on DQ[3:0] and the revision identification on DQ[7:4]. The code will be driven onto the DQ bus after t_{RIDon} following the EMRS command that sets A10 to 1. The Vendor Code and Revision ID will be driven on DQ[7:0] until a new EMRS command is issued with A10 set back to 0. After t_{RDoff} following the second EMRS command, the data bus is driven back to HIGH. This second EMRS command must be issued before initiating any subsequent operation. Violating this requirement will result in unspecified operation.

Table 17 Revision ID and Vendor Code

Revision Identification	Infineon Vendor Code
DQ[7:4]	DQ[3:0]
0001	0010

Note: Please refer to Revision Release Note for Revision ID value

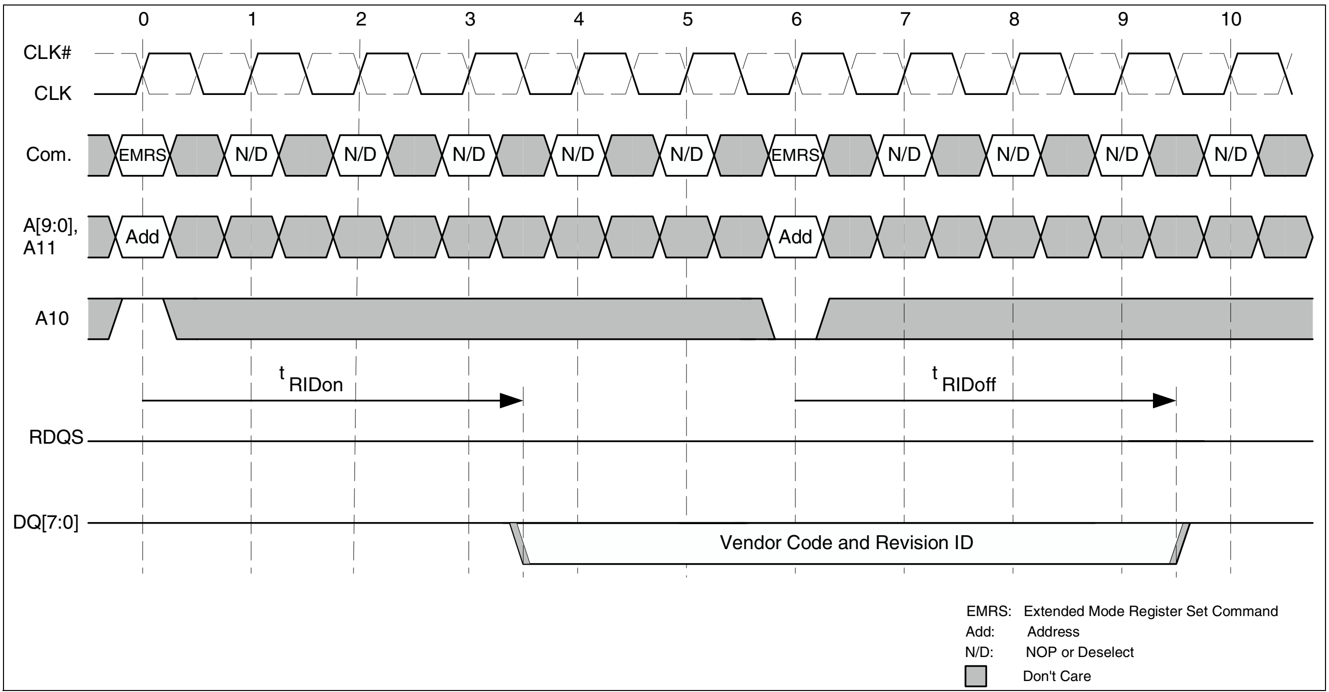

Figure 13 Timing of Vendor Code and Revision ID generation on DQ[7:0]

Table 18 Vendor Code and Revision ID Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
EMRS to DQ on time	t_{RIDon}	—	20	—	20	—	20	ns	
EMRS to DQ off time	t_{RIDoff}	—	20	—	20	—	20	ns	

3.5 Mode Register Set Command (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs read latency, test mode, DLL Reset and the value of the write latency. There is no default value for the mode register; therefore it must be written after power up to operate the GDDR3 Graphics RAM. During a Mode Register Set command the address inputs are sampled and stored in the mode register.

t_{MRD} must be met before any command can be issued to the Graphics SDRAM. The Mode Register contents can only be set or changed when the Graphics SDRAM is in idle state.

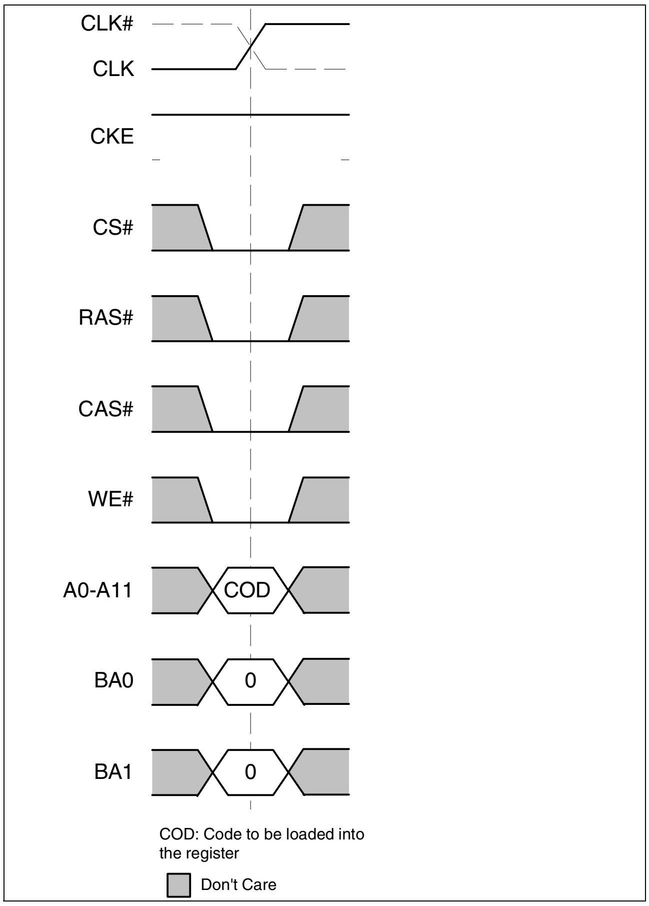

Figure 14 Mode Register Set Command

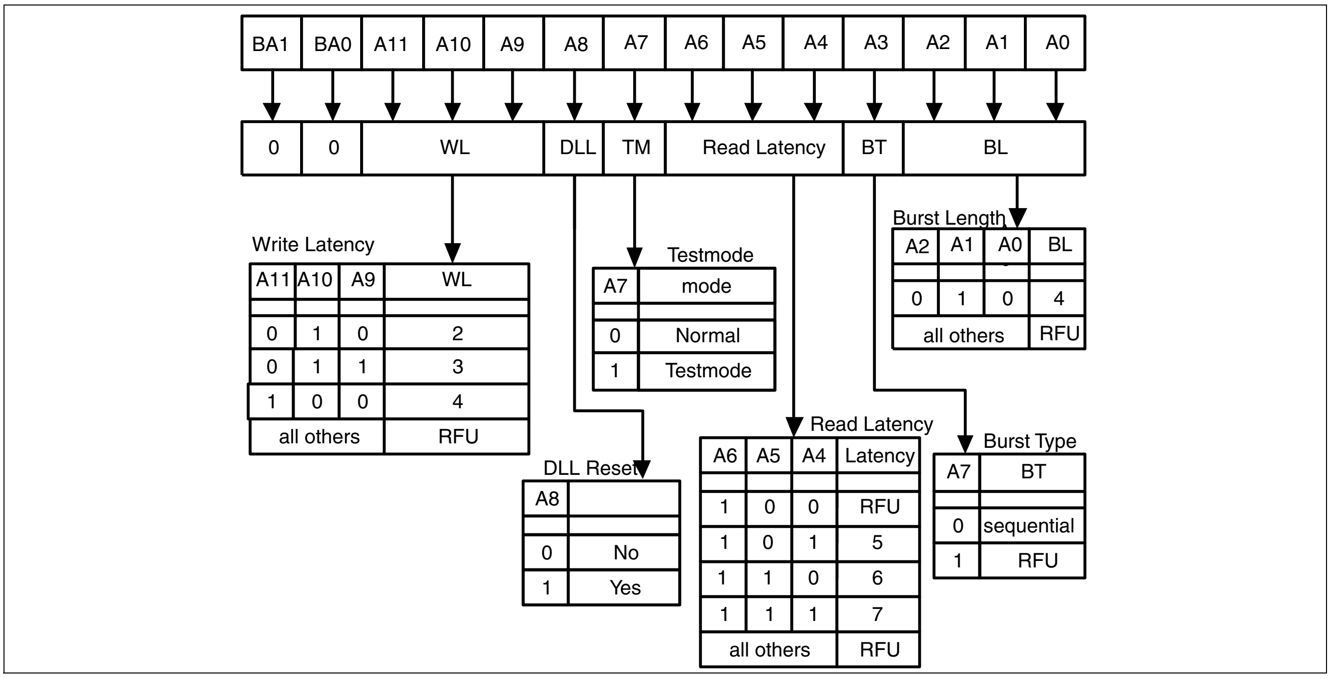

Figure 15 Mode Register Bitmap

Note: The DLL Reset command is self-clearing

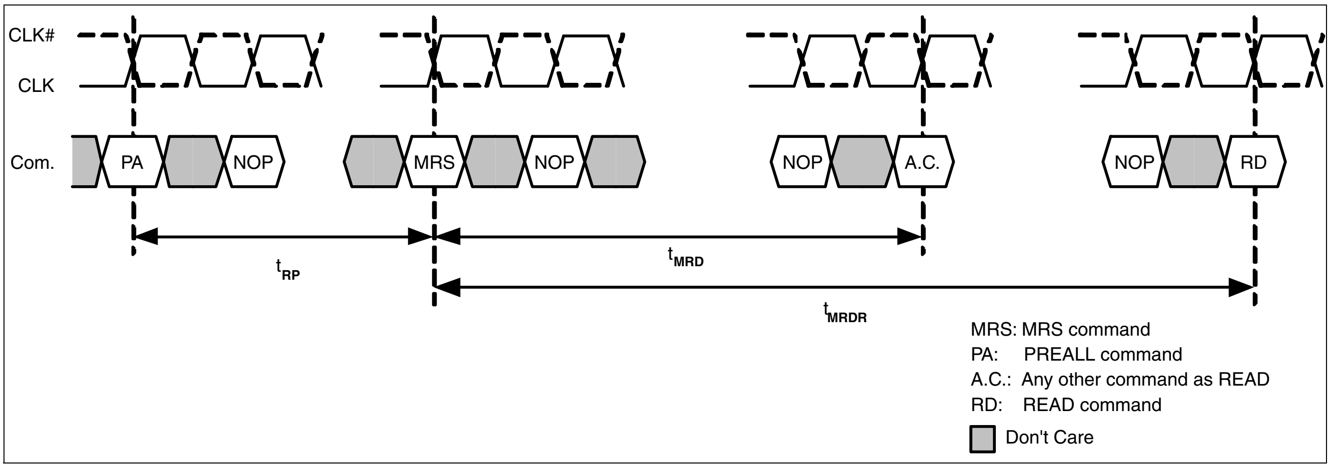

Figure 16 Mode Register Set Timing

Table 19 MRS Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Mode Register Set cycle time	t_{MRD}	5	—	4	—	4	—	t_{CK}	1, 2
Mode Register Set to READ timing	t_{MRDR}	15	—	12	—	12	—	t_{CK}	1

1. *This value of t_{MRD} applies only to the case where the "DLL reset" bit is not activated.*
2. *t_{MRD} is defined from MRS to any other command as READ.*

3.5.1 Burst length

Read and Write accesses to the GDDR3 Graphics RAM are burst oriented with burst length 4. This value must be programmed using the Mode Register Set command (A0 .. A2). The burst length determines the number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block if a boundary is reached. The block is uniquely selected by A2-Ai where Ai is the most significant bit for a given configuration. The starting location within this block is determined by the two least significant bits A0 and A1 which are set internally to the fixed value of zero each.

Reserved states should not be used, as unknow operation or incompatibility with future versions may result.

3.5.2 Burst type

Accesses within a given bank must be programmed to be sequential. This is done using the Mode Register Set command (A3) . This device does not support the burst interleave mode.

Table 20 Burst Type

Burst Length	Starting Column address	Order of accesses within the burst
		Type = Sequential
4	A1 A0	
	x x	0-1-2-3

The value applied at the balls A0 and A1 for the column address is "Don't care".

3.5.3 CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data as shown on **Figure 31**. The latency can be set to 5 to 7 clocks as shown in **Figure 15**.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally concident with clock edge n+m. Refer to Appendix, **Figure 42**, for values of operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

3.5.4 Write Latency

The WRITE latency, WL, is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data as shown in **Figure 21**. WL can be set from 2 to 4 clocks depending on the operating frequency. Setting the WRITE latency to 2 or 3 clocks will cause the device to enable the data input receivers on all ACT commands.

3.5.5 Test mode

The normal operating mode is selected by issuing a Mode Register Set command with bit A7 set to zero and bits A0-A6 and A8-A11 set to the desired value.

3.5.6 DLL Reset

The normal operating mode is selected by issuing a Mode Register Set command with bit A8 set to zero and bits A0-A7 and A9-A11 set to the desired values. A DLL Reset is initiated by issuing a Mode Register Set command with bit A8 set to one and bits A0-A7 and A9-A11 set to the desired values. The GDDR3 SGRAM returns automatically in the normal mode of operations once the DLL reset is completed.

3.6 Bank / Row Activation (ACT)

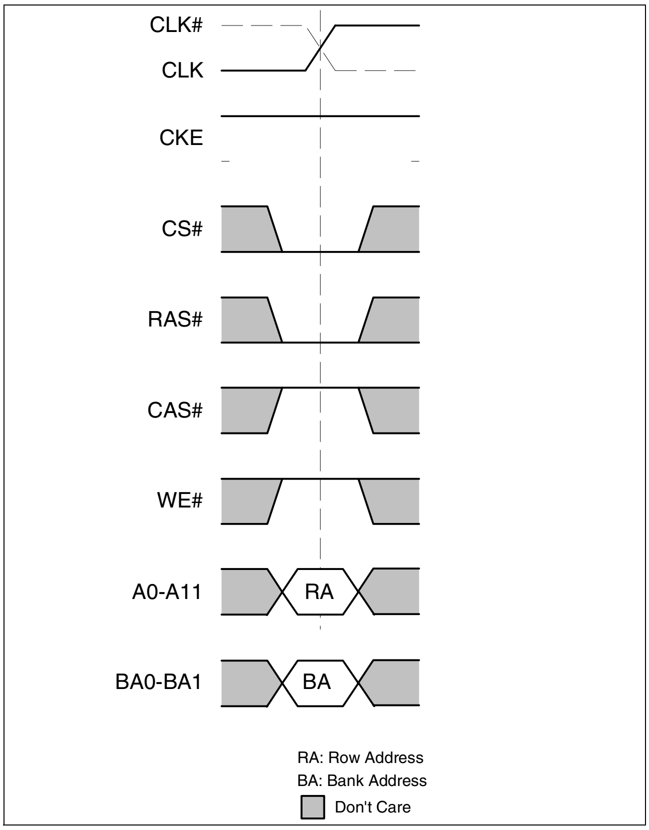

Figure 17 Activating a specific row

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACT command, which selects both the bank and the row to be activated.

After opening a row by issuing an ACT command, a READ or WRITE command may be issued after t_{RCD} to that row.

A subsequent ACT command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACT commands to the same bank is defined by t_{RC}.

A subsequent ACT command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACT commands to different banks is defined by t_{RRD}.

There is a minimum time t_{RAS} between opening and closing a row.

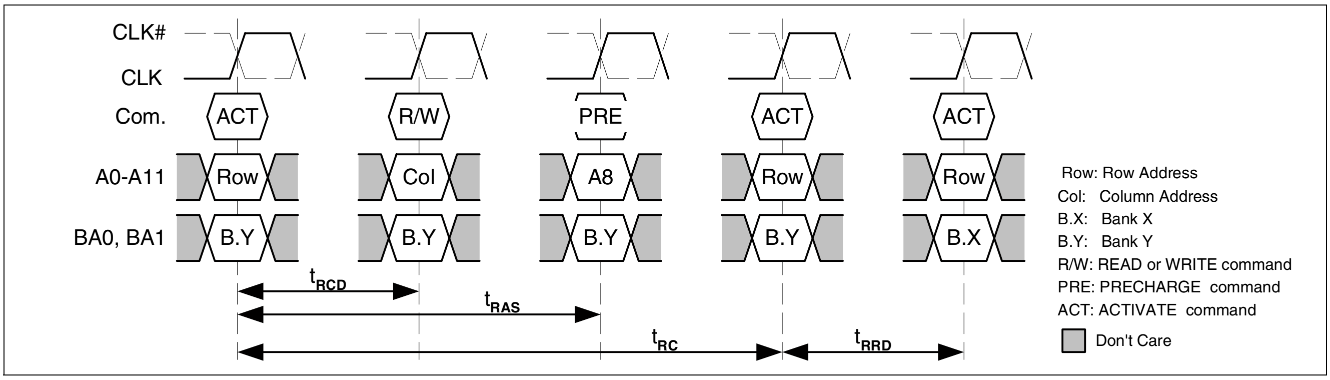

Figure 18 Bank Activation timing

Table 21 ACT Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Row Cycle Time	t_{RC}	37.2	—	37.2	—	39.6	—	ns	
Row Active Time	t_{RAS}	24.0	8 x t_{REFI}	24.0	8 x t_{REFI}	26.2	8 x t_{REFI}	ns	
ACT(a) to ACT(b) Command period	t_{RRD}	8.0	—	8.0	—	8.8	—	ns	
Row to Column Delay Time for Reads	t_{RCDRD}	16.0	—	16.0	—	17.5	—	ns	
Row to Column Delay Time for Writes	t_{RCDWR}	$t_{RCDWR(min)} = t_{RCDRD(min)}$ - (WL + 1) x $t_{CK(min)}$						ns	

3.7 Writes (WR)

3.7.1 Write Basic Information

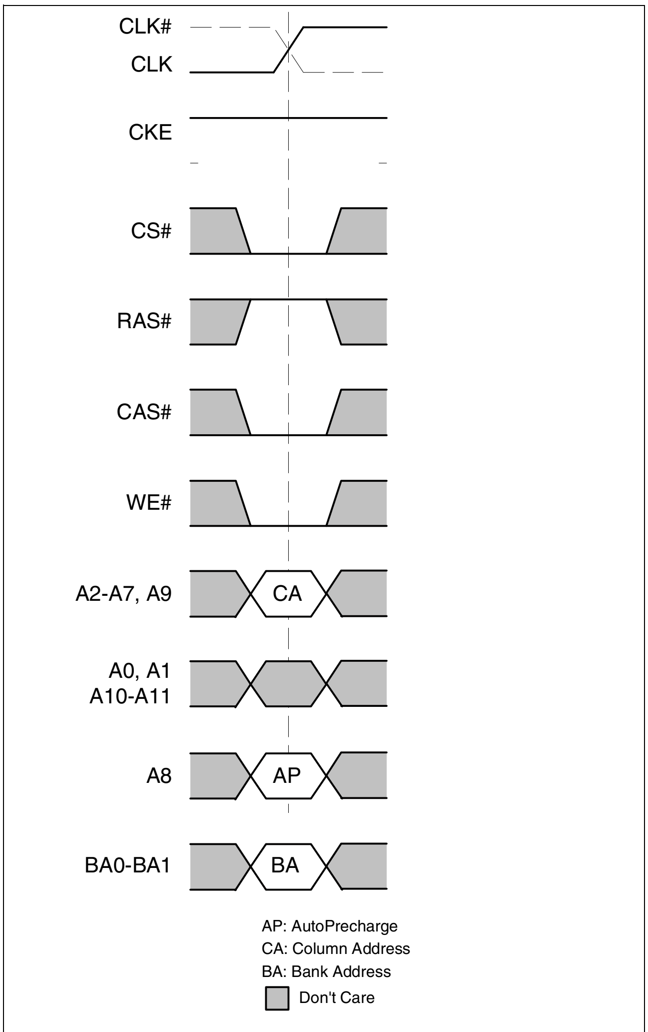

Figure 19 Write Command

Write bursts are initiated with a WR command, as shown in **Figure 19**. The column and bank addresses are provided with the WR command, and Auto Precharge is either enabled or disabled for that access. The length of the burst initiated with a WR command is always four. There is no interruption of WR bursts. The two least significant address bits A0 and A1 are 'Don't Care'.

For WR commands with Autoprecharge the row being accessed is precharged $t_{WR/A}$ after the completion of the burst. If t_{RAS}(min) is violated the begin of the internal Autoprecharge will be performed one cycle after t_{RAS}(min) is met. $t_{WR/A}$ can be programmed in the Mode Register. Choosing high values for $t_{WR/A}$ will prevent the chip to delay the internal Autoprecharge in order to meet t_{RAS}(min).

During WR bursts data will be registered with the edges of WDQS. The write latency can be programmed during Extended Mode Register Set. The first valid data is registered with the first valid rising edge of WDQS following the WR command. The externally provided WDQS must switch from HIGH to LOW at the beginning of the preamble. There is also a postamble requirement before the WDQS returns to HIGH. The WDQS signal can only transition when data is applied at the chip input and during pre- and postambles.

t_{DQSS} is the time between WR command and first valid rising edge of WDQS. Nominal case is when WDQS edges are aligned with edges of external CLK. Minimum and maximum values of t_{DQSS} define early and late WDQS operation. Any input data will be ignored before the first valid rising WDQS transition. t_{DQSL} and t_{DQSH} define the width of low and high phase of WDQS. The sum of t_{DQSL} and t_{DQSH} has to be t_{CK}.

Back to back WR commands are possible and produce a continuous flow of input data. There must be one NOP cycle between two back to back WR commands.

Any WR burst may be followed by a subsequent RD command. Figure 3.7.5 shows the timing requirements for a WR followed by a RD. A WR may also be followed by a PRE command to the same bank. t_{WR} has to be met as shown in Figure 3.7.8.

Setup and hold time for incoming DQs and DMs relative to the WDQS edges are specified as t_{DS} and t_{DH}. DQ and DM input pulse width for each input is defined as t_{DIPW}. The input data is masked if the corresponding DM signal is high.

All timing parameters are defined with graphics DRAM terminations on.

Table 22 Mapping of WDQS and DM signals

WDQS	Data mask signal	Controlled DQs
WDQS0	DM0	DQ0 - DQ7
WDQS1	DM1	DQ8 - DQ15
WDQS2	DM2	DQ16 - DQ23
WDQS3	DM3	DQ24 - DQ31

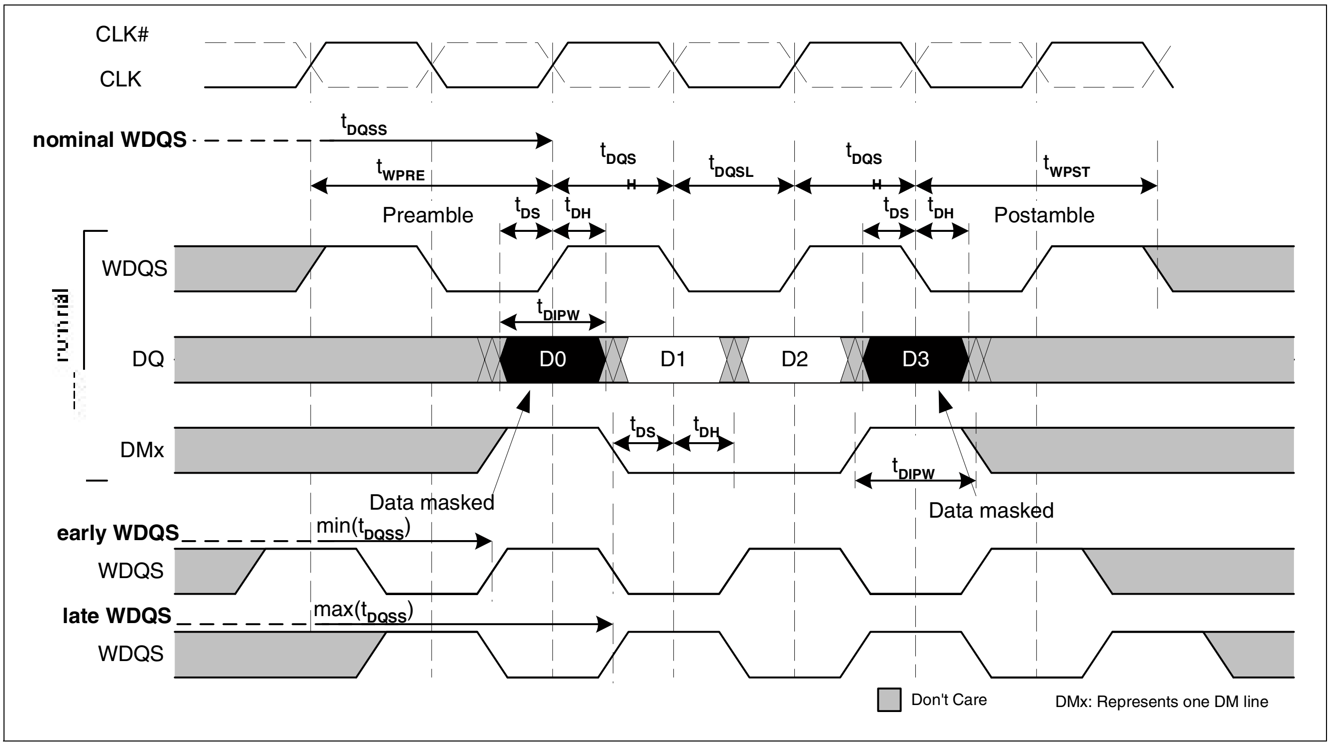

Figure 20 Basic Write Burst / DM Timing

Note: : WDQS can only transition when data is applied at the chip input and during pre- and postambles

Table 23 WR Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
CAS(a) to CAS(b) Command period	t_{CCD}	2	—	2	—	2	—	t_{CK}	1)
Write Cycle Timing Parameters for Data and Data Strobe									
Write command to first WDQS latching transition	t_{DQSS}	WL - 0.25	WL +0.25	WL - 0.25	WL +0.25	WL - 0.25	WL +0.25	t_{CK}	
Data-in and Data Mask to WDQS Setup Time	t_{DS}	0.35	—	0.375	—	0.375	—	ns	2)
Data-in and Data Mask to WDQS Hold Time	t_{DH}	0.35	—	0.375	—	0.375	—	ns	2)
Data-in and DM input pulse width (each input)	t_{DIPW}	0.45	—	0.45	—	0.45	—	t_{CK}	
WDQS input low pulse width	t_{DQSL}	0.45	—	0.45	—	0.45	—	t_{CK}	3)
WDQS input high pulse width	t_{DQSH}	0.45	—	0.45	—	0.45	—	t_{CK}	3)
WDQS Write Preamble Time	t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
WDQS Write Postamble Time	t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write to Read Command Delay	t_{WTR}	6.0	—	6.0	—	6.6	—	ns	2)4)
Write Recovery Time	t_{WR}	11.0	—	11.0	—	11.0	—	ns	2)4)

1) t_{CCD} *is either for gapless consecutive writes or gapless consecutive reads*

2) *Timing parameters defined with Graphics DRAM terminations on.*

3) t_{DQSL}. *and* t_{DQSH} *apply for the Write preamble and postamble as well.*

4) $_{tWTR}$ *and* t_{WR} *start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQSx signal*

3.7.2 Write - Basic Sequence

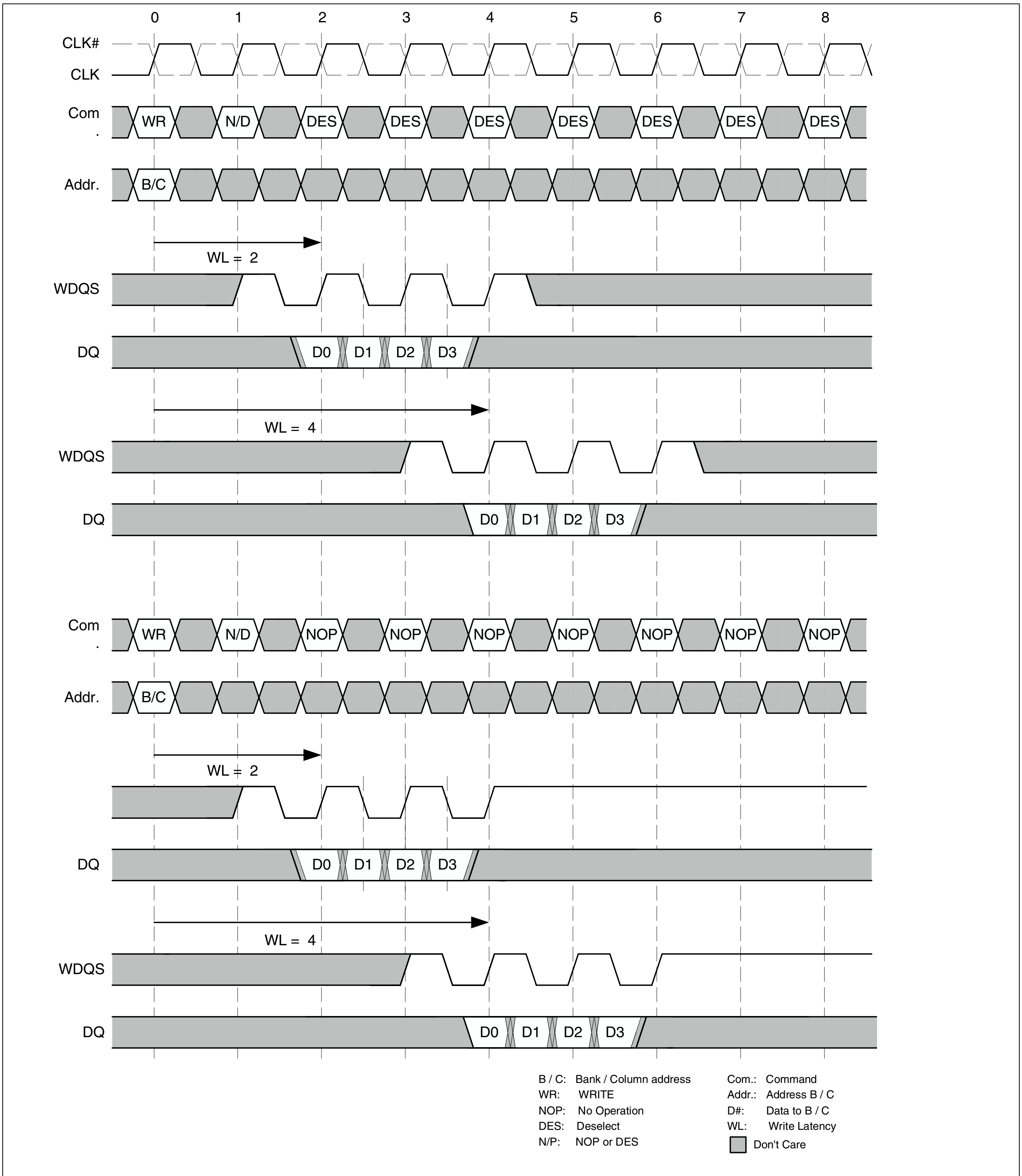

Figure 21 Write Burst Basic Sequence

1. *Shown with nominal value of* t_{DQSS}.
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*
3. *When NOPs are applied on the command bus, the WDQS and the DQ busses remain stable High.*
4. *When DESs are applied on the command bus, the status of the WDQS and DQ busses is unknown.*

3.7.3 Write - Consecutive Bursts

3.7.3.1 Gapless Bursts

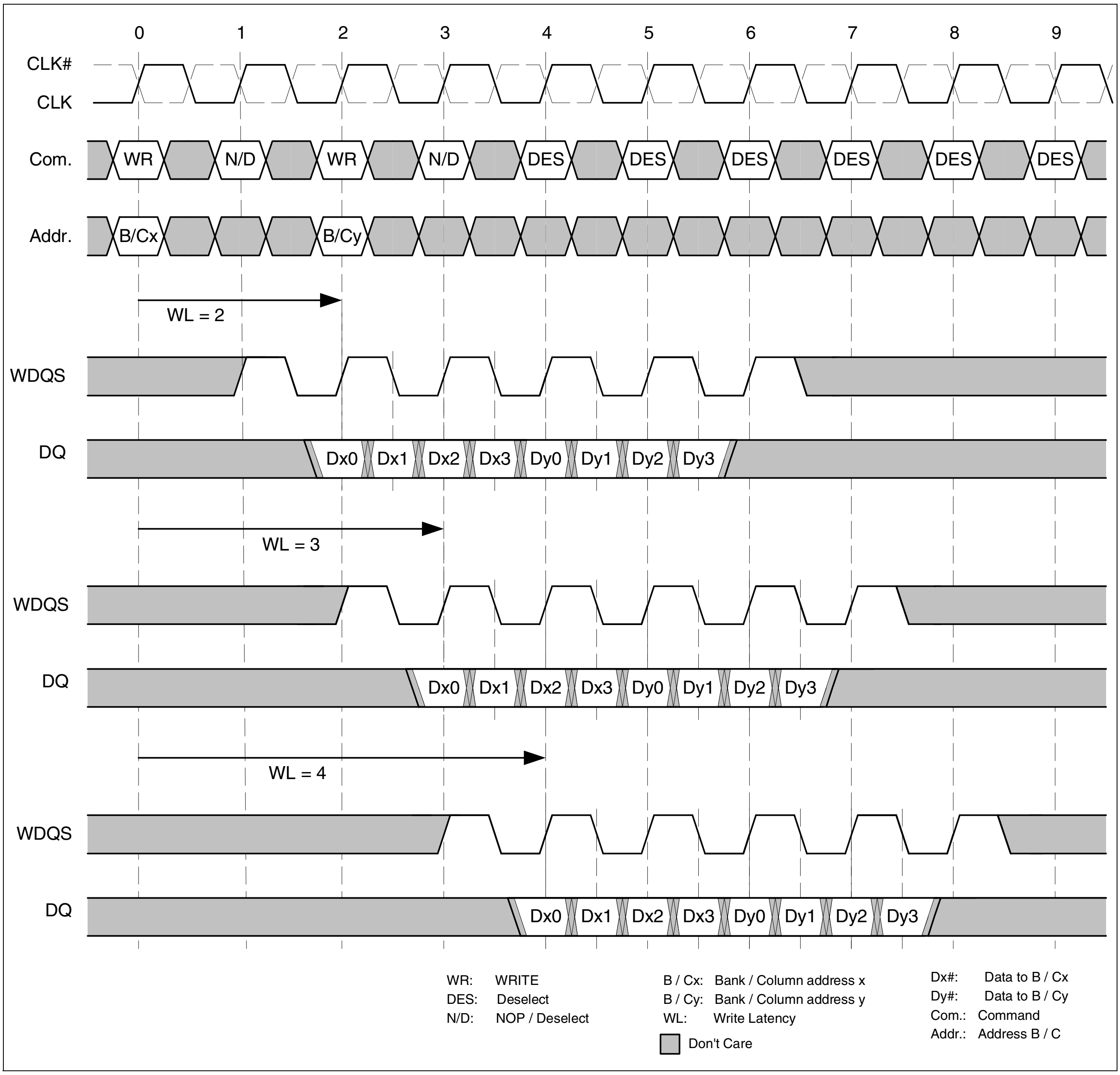

Figure 22 Gapless Write Bursts

1. *Shown with nominal value of* t_{DQSS}
2. *The second WR command may be either for the same bank or another bank*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*

3.7.3.2 Bursts with Gaps

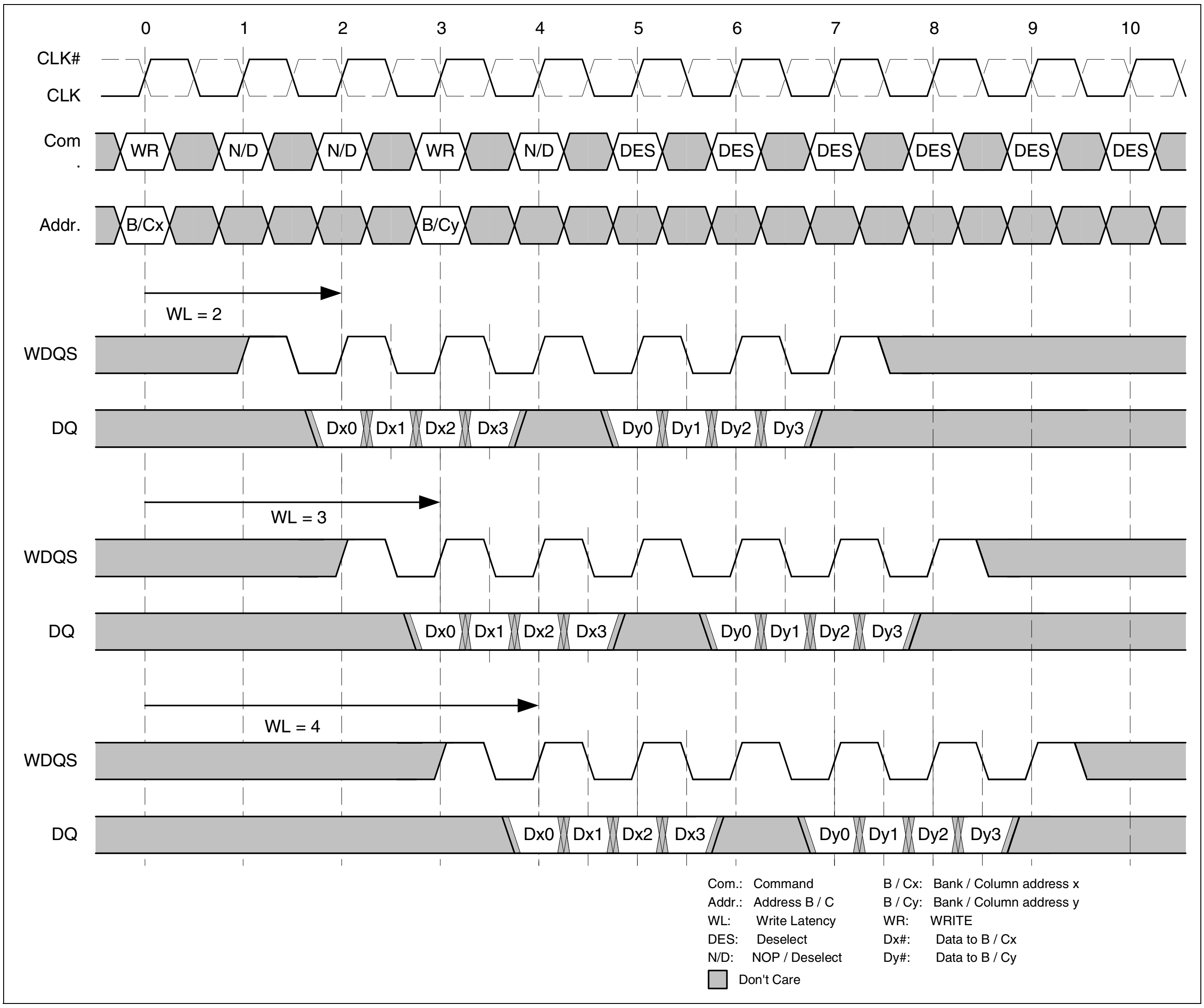

Figure 23 Consecutive Write Bursts with Gaps

1. *Shown with nominal value of t_{DQSS}.*
2. *The second WR command may be either for the same bank or another bank.*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

3.7.4 Write with Autoprecharge

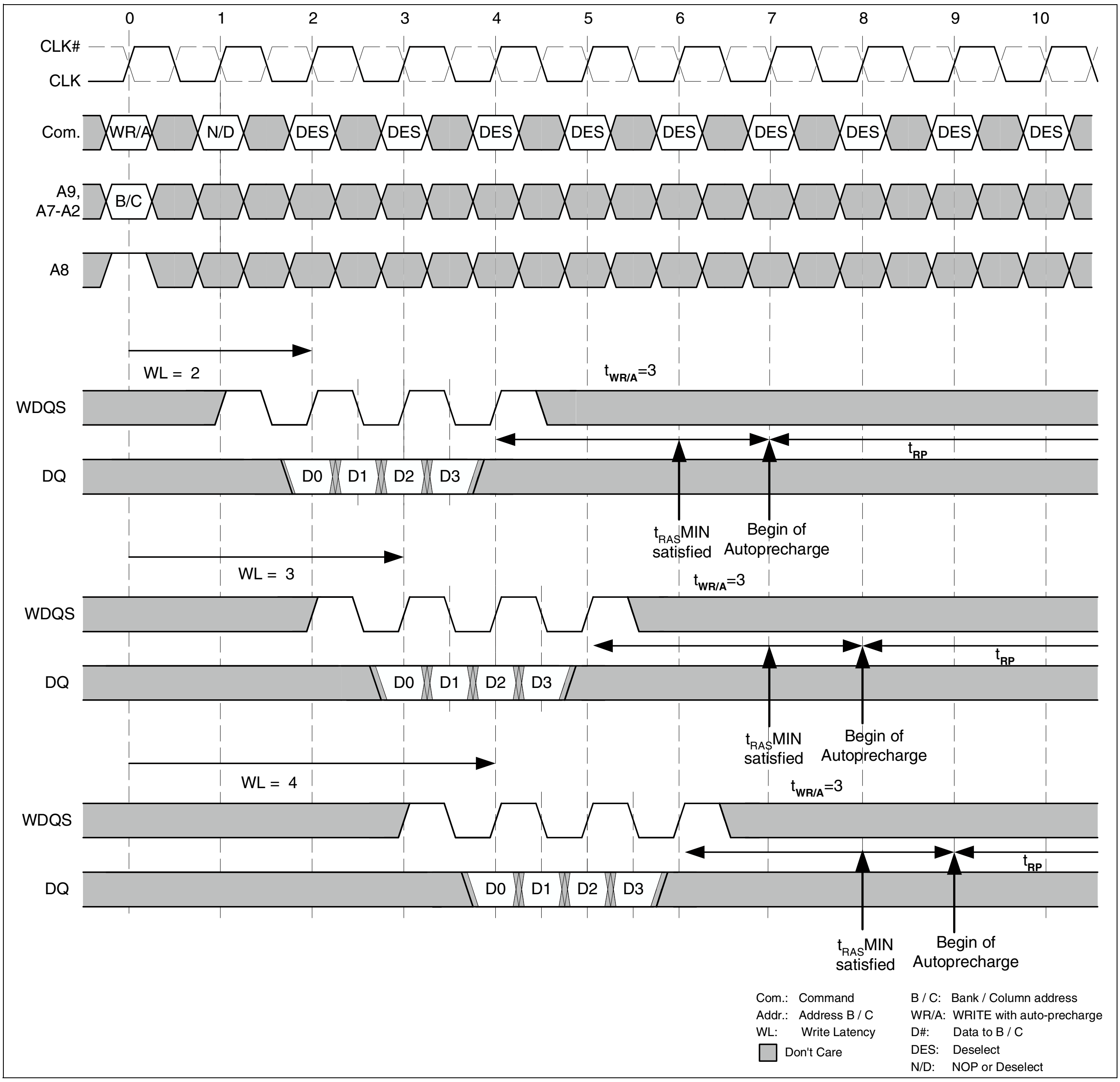

Figure 24 Write with Autoprecharge

1. *Shown with nominal value of t_{DQSS}*
2. *$t_{WR/A}$ starts at the first rising edge of CLK after the last valid edge of WDQS.*
3. *t_{RP} starts after $t_{WR/A}$ has been expired.*
4. *when issuing a WR/A command please consider that the t_{RAS} requirement also must be met at the beginning of t_{RP}*
5. *$t_{WR/A} * t_{CYC} \geq t_{WR}$*
6. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*

3.7.5 Write followed by Read

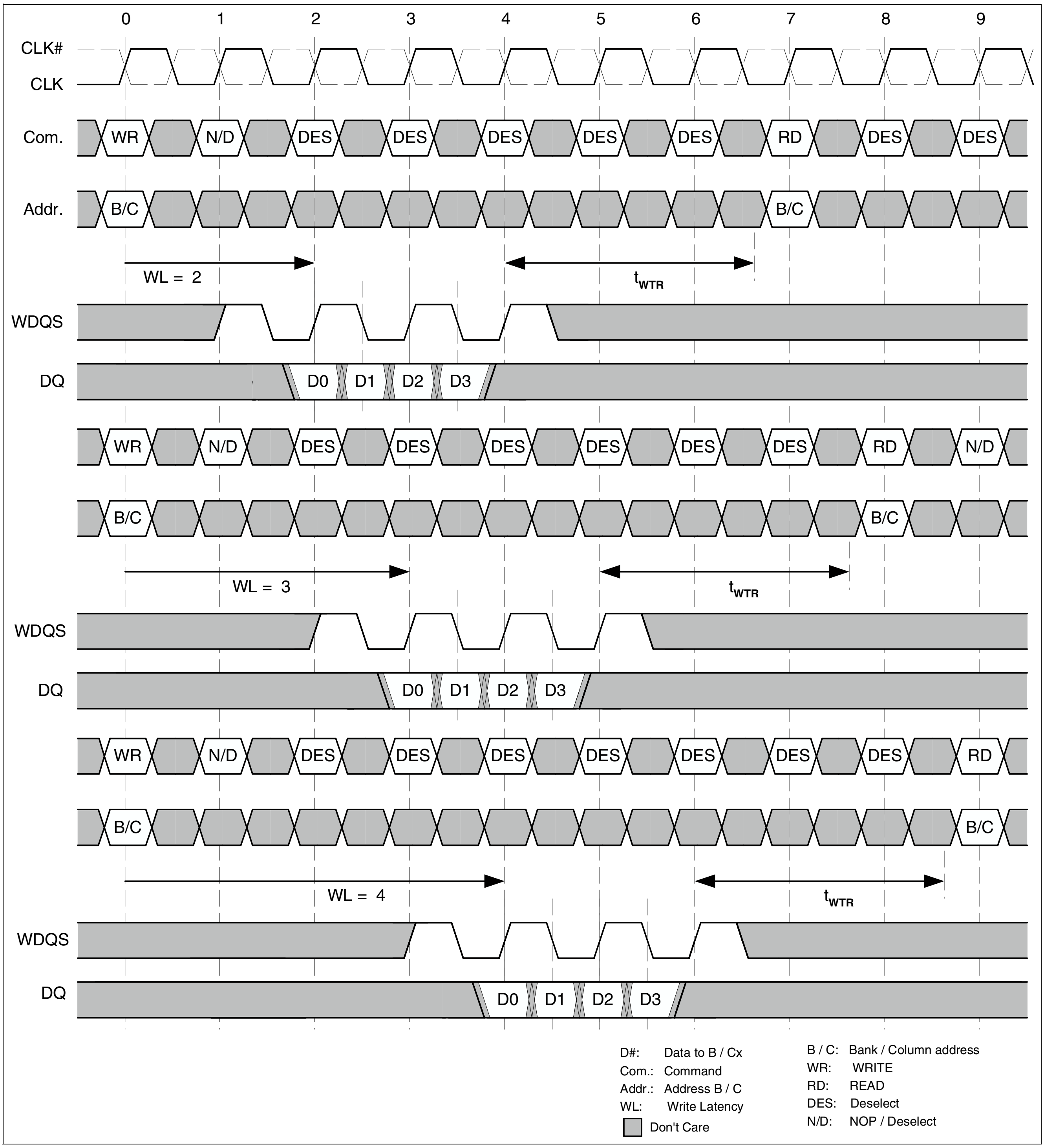

Figure 25 Write followed by Read

1. *Shown with nominal value of t_{DQSS}.*
2. *The RD command may be either for the same bank or another bank.*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

3.7.6 Write followed by DTERDIS

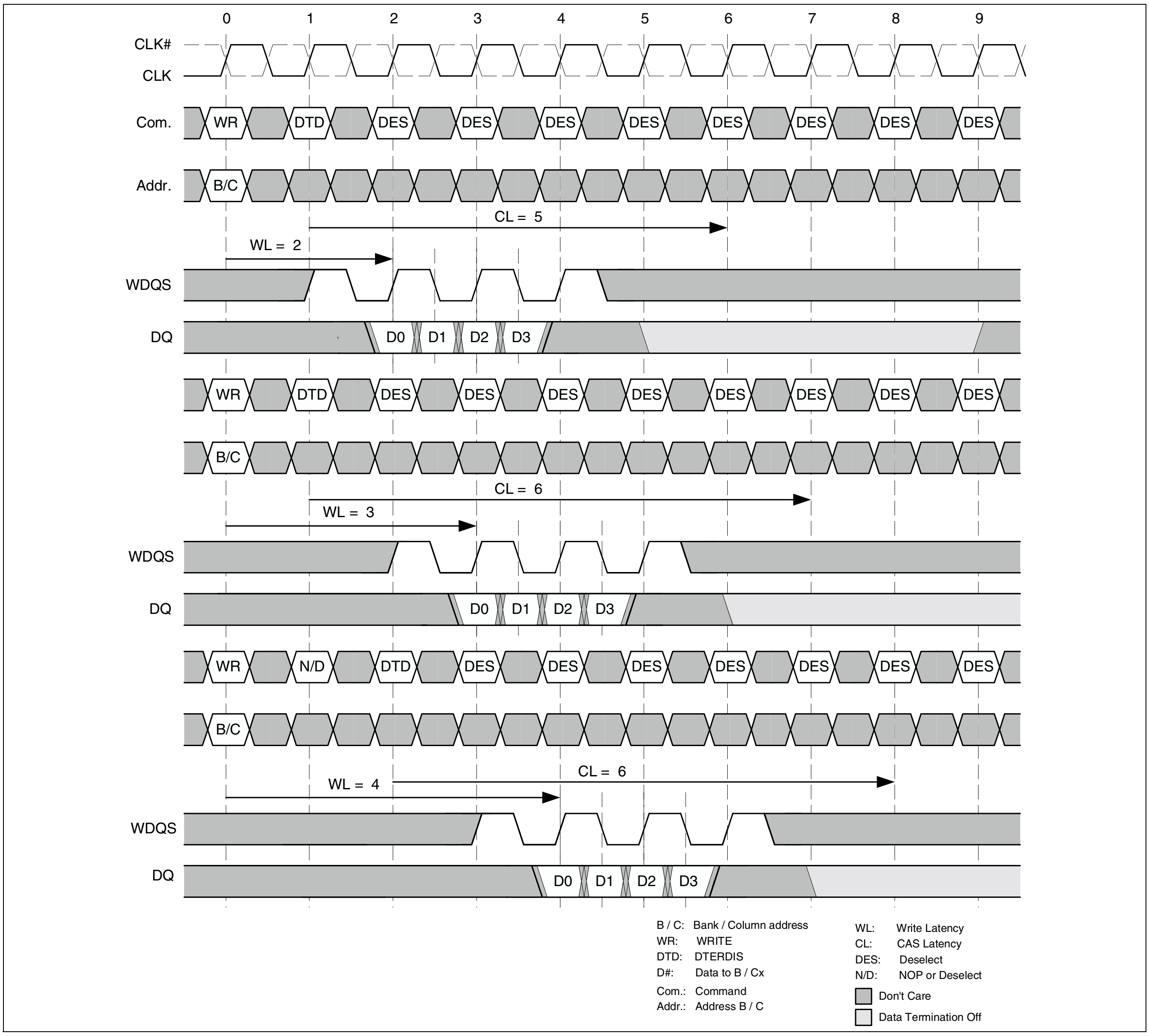

Figure 26 Write Command followed by DTERDIS

1. *Write shown with nominal value of t_{DQSS}.*
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*
3. *A margin of one clock has been introduced in order to make sure that the data termination are still on when the last Write data reaches the memory.*
4. *The minimum distance between Write and DTERDIS is (WL -CL + 4) clocks and always bigger than or equal to 1. For (CL=6 / WL=2) and (CL=7 / WL=3) as well as for (CL=7 / WL=2) the minimum distance between Write and DTERDIS is set to 1 clock. Please refer to table below:*

Table 24 WL / CL

WL \ CL	5	6	7
2	1	1	1
3	2	1	1
4	3	2	1

3.7.7 Write with Autoprecharge followed by Read / Read with Autoprecharge

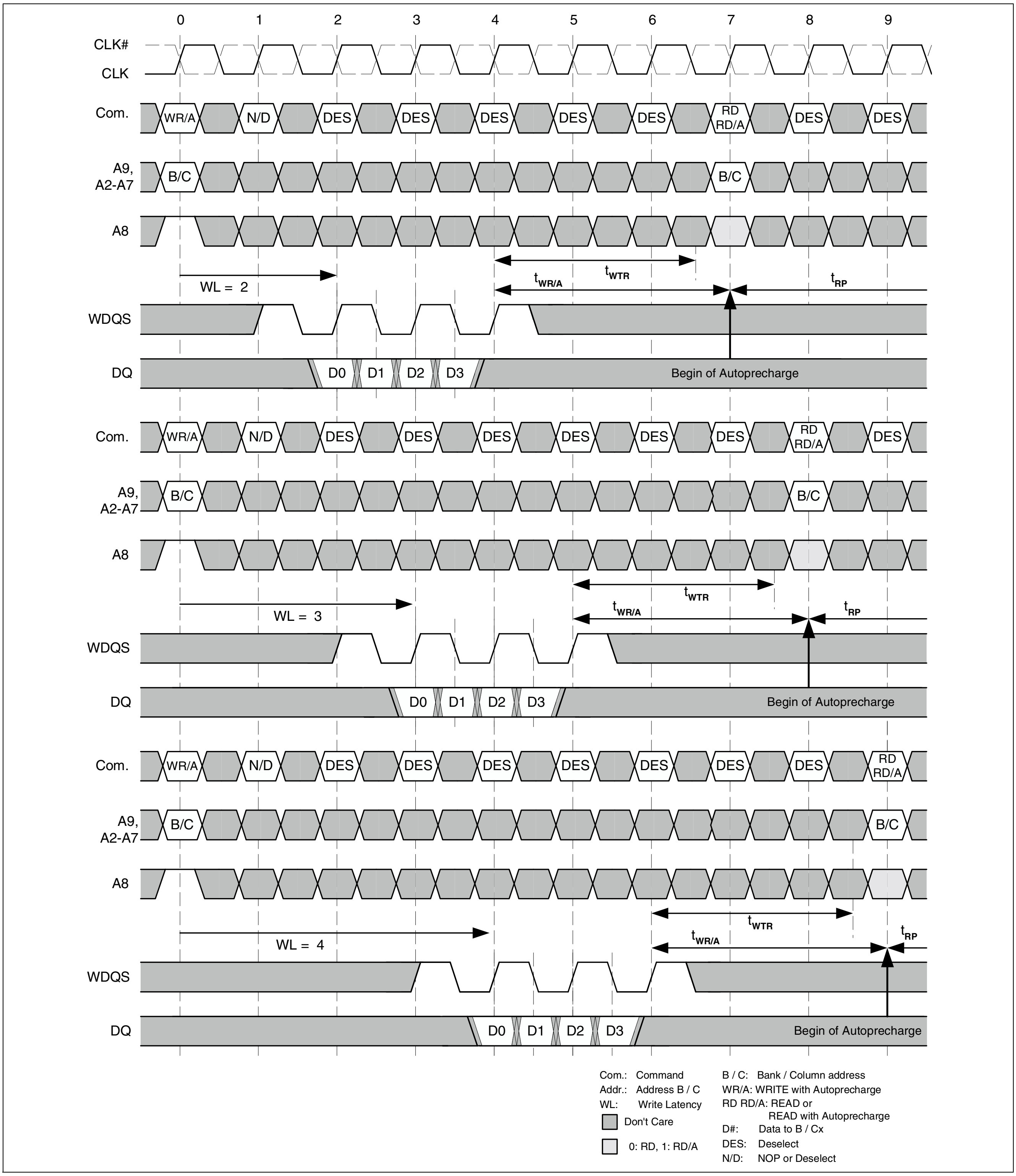

Figure 27 Write with Autoprecharge followed by Read or Read with Autoprecharge on another bank

1. *Shown with nominal value of t_{DQSS}.*
2. *The RD command is only allowed for another activated bank*
3. *tWR/A is set to 3 in this example*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*

3.7.8 Write followed by Precharge on same Bank

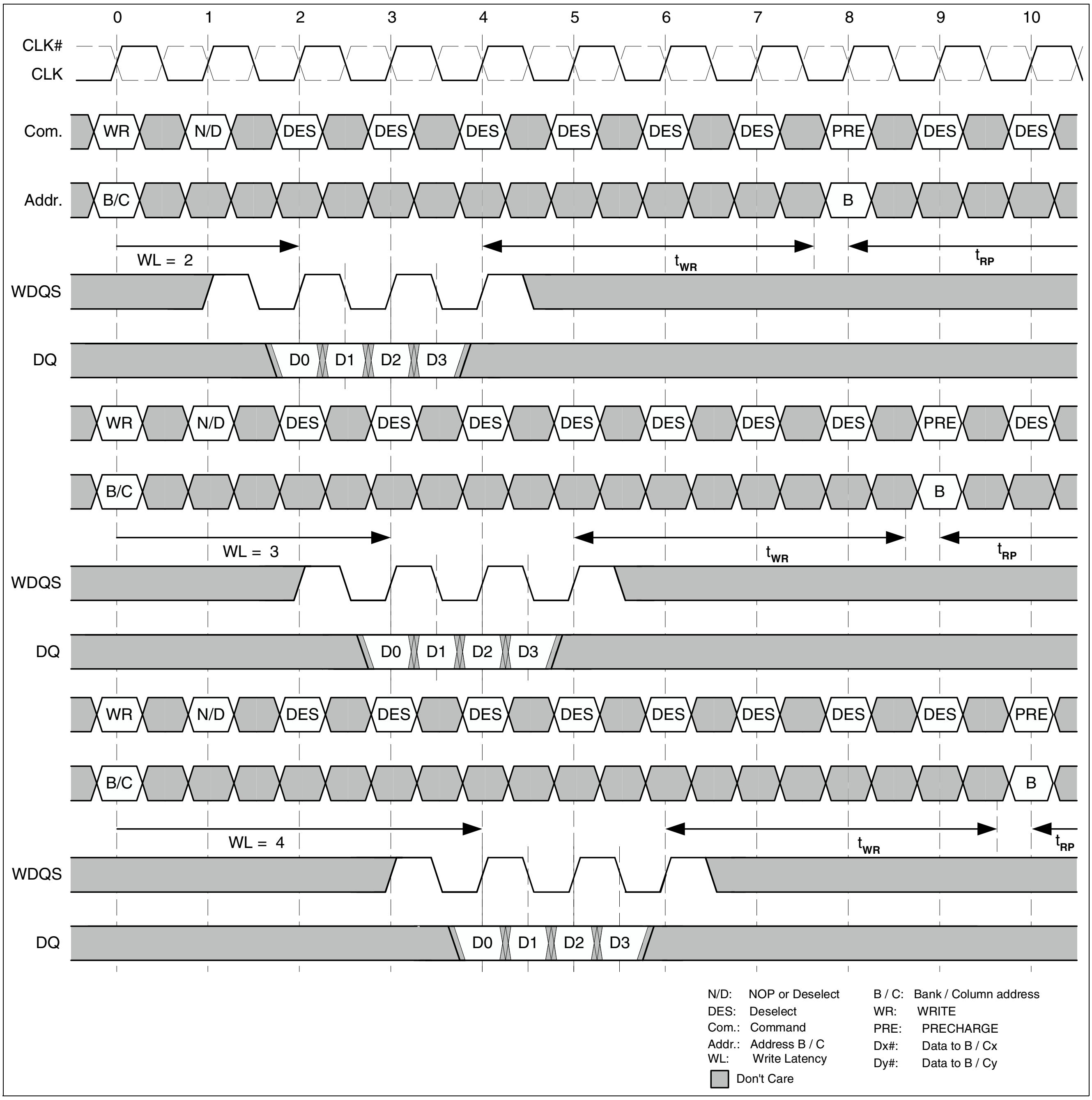

Figure 28 Write followed by Precharge on same Bank

1. *Shown with nominal value of* $t_{DQSS.}$
2. *WR and PRE commands are to same bank*
3. t_{RAS} *requirement must also be met before issuing PRE command*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*

3.8 Reads (RD)

3.8.1 Read - Basic Information

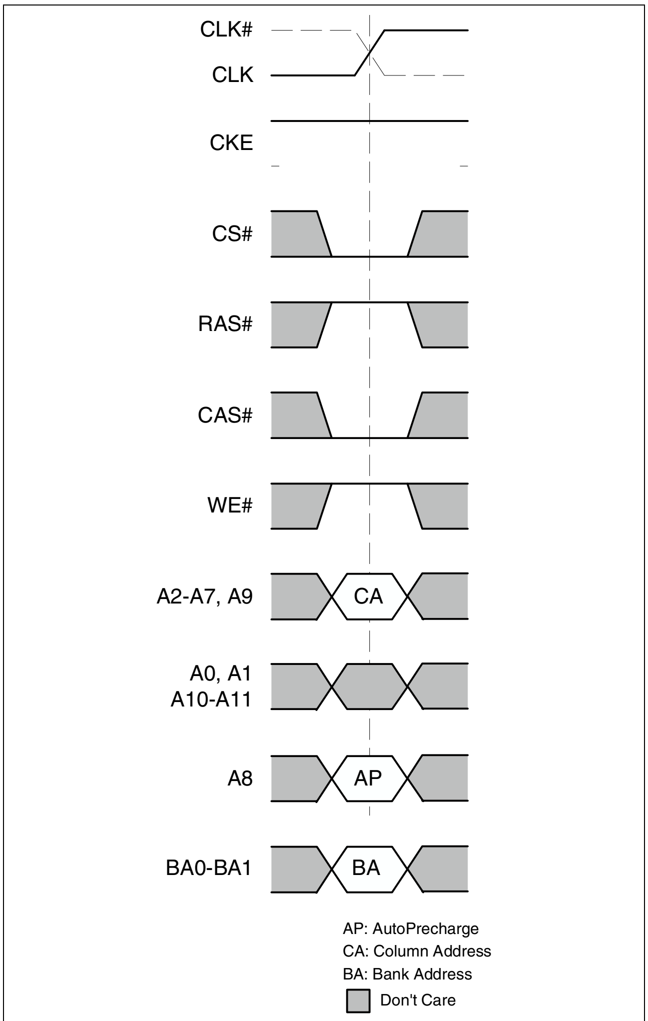

Figure 29 Read Command

Read bursts are initiated with a RD command, as shown in **Figure 29**. The column and bank addresses are provided with the RD command and Autoprecharge is either enabled or disabled for that access. The length of the burst initiated with a RD command is always four. There is no interruption of RD bursts. The two least significant start address bits are 'Don't Care'.

If Autoprecharge is enabled, the row being accessed will start precharge at the completion of the burst. The begin of the internal Autoprecharge will always be one cycle after t_{RAS}(min) is met.

During RD bursts the memory device drives the read data edge aligned with the RDQS signal which is also driven by the memory. After a programmable CAS latency of 5, 6 or 7 the data is driven to the controller. RDQS leaves HIGH state one cycle before its first rising edge (RD preamble t_{RPRE}). After the last falling edge of RDQS a postamble of t_{RPST} is performed.

t_{AC} is the time between the positive edge of CLK and the appearance of the corresponding driven read data. The skew between RDQS and the crossing point of CLK/$\overline{CLK}$ is specified as t_{DQSCK}. t_{AC} and t_{DQSCK} are defined relatively to the positive edge of CLK. t_{DQSQ} is the skew between a RDQS edge and the last valid data edge belonging to the RDQS edge. t_{DQSQ} is derived at each RDQS edge and begins with RDQS transition and ends with the last valid transition of DQs. t_{QHS} is the data hold skew factor and t_{QH} is the time from the first valid rising edge of RDQS to the first conforming DQ going non-valid and it depends on t_{HP} and t_{QHS}. t_{HP} is the minimum of t_{CL} and t_{CH}. t_{QHS} is effectively the time from the first data transition (before RDQS) to the RDQS transition. The data valid window is derived for each RDQS transition and is defined as t_{QH} minus t_{DQSQ}.

After completion of a burst, assuming no other commands have been initiated, data will go High-Z and RDQS will go HIGH. Back to back RD commands are possible producing a continuous flow of output data. There has to be one NOP cycle between back to back RD commands.

Any RD burst may be followed by a subsequent WR command. The minimum required number of NOP commands between the RD command and the WR command (t_{RTW}) depends on the programmed Read latency and the programmed Write latency

t_{RTW}(min)= (CL+4-WL)

Chapter 3.8.5 shows the timing requirements for RD followed by a WR with some combinations of CL and WL.

A RD may also be followed by a PRE command. Since no interruption of bursts is allowed the minimum time between a RD command and a PRE is two clock cycles as shown in **Chapter 3.8.6**.

All timing parameters are defined with controller terminations on.

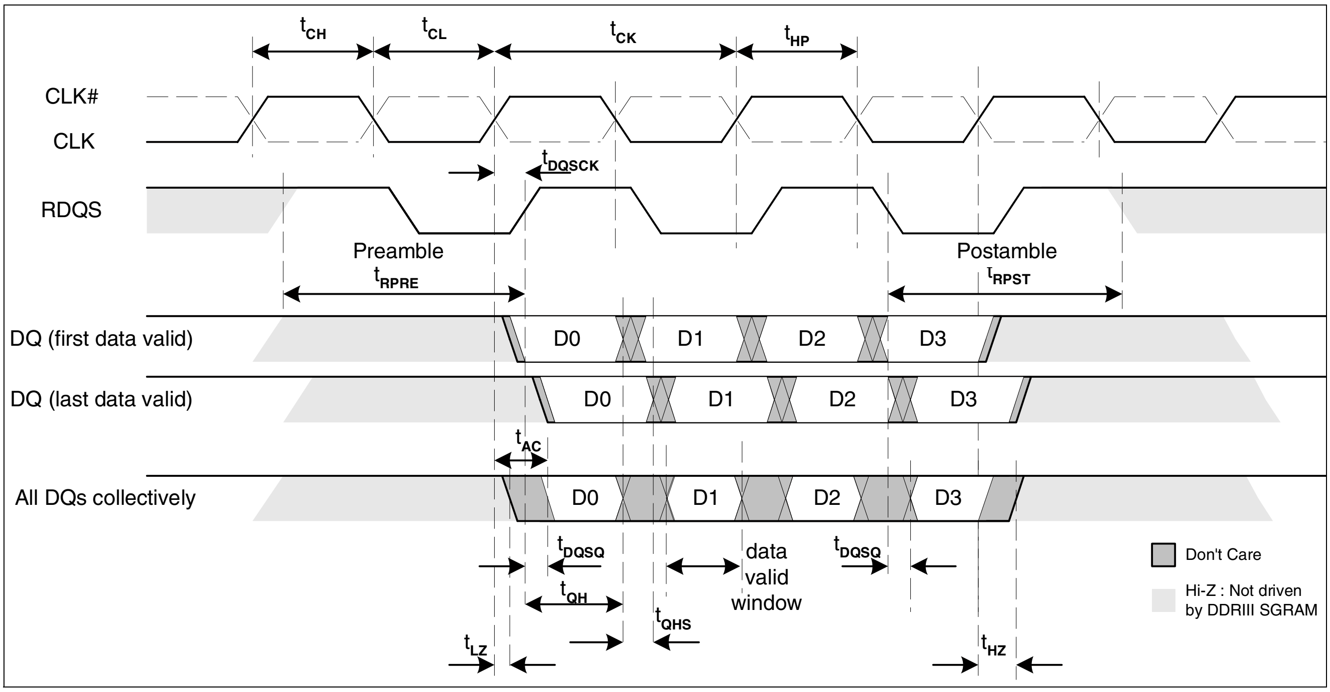

Figure 30 Basic Read Burst Timing

1. *The GDDR3 SGRAM switches off the DQ terminations one cycle before data appears on the busand drives the data bus HIGH.*
2. *The GDDR3 SGRAM drives the data bus HIGH one cycle after the last data driven on the bus before switching the termination on again.*

Table 25 READ Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Note
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
$\overline{CAS}$ (a) to $\overline{CAS}$ (b) Command period	t_{CCD}	2	—	2	—	2	—	t_{CK}	1
Read to Write command delay	t_{RTW}	t_{RTW}(min)= (CL+4-WL)						t_{CK}	2
Read Cycle Timing Parameters for Data and Data Strobe									
Data Access Time from Clock	t_{AC}	–0.4	0.4	–0.4	0.4	–0.45	0.45	ns	4
Read Preamble	t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Read Postamble	t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK	t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	n_s	4
Data-out low impedance time from CLK	t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	n_s	4
RDQS edge to Clock edge skew	t_{DQSCK}	–0.4	0.4	–0.4	0.4	–0.45	0.45	ns	4
RDQS edge to output data edge skew	t_{DQSQ}	—	0.225	—	0.225	—	0.25	ns	4
Data hold skew factor	t_{QHS}	0	0.225	0	0.225	0	0.25	ns	4
Data output hold time from RDQS	t_{QH}	t_{HP}–t_{QHS}		t_{HP}–t_{QHS}		t_{HP}–t_{QHS}		ns	4
Minimum clock half period	t_{HP}	0.45	—	0.45	—	0.45	—	t_{CK}	3

1. *t_{CCD} is either for gapless consecutive reads or gapless consecutive writes.*
2. *Please round up t_{RTW} to the next integer of t_{CK}.*
3. *t_{HP} is the minimum of t_{CL} and t_{CH}*
4. *Timing parameters defined with controller terminations on.*

3.8.2 Read - Basic Sequence

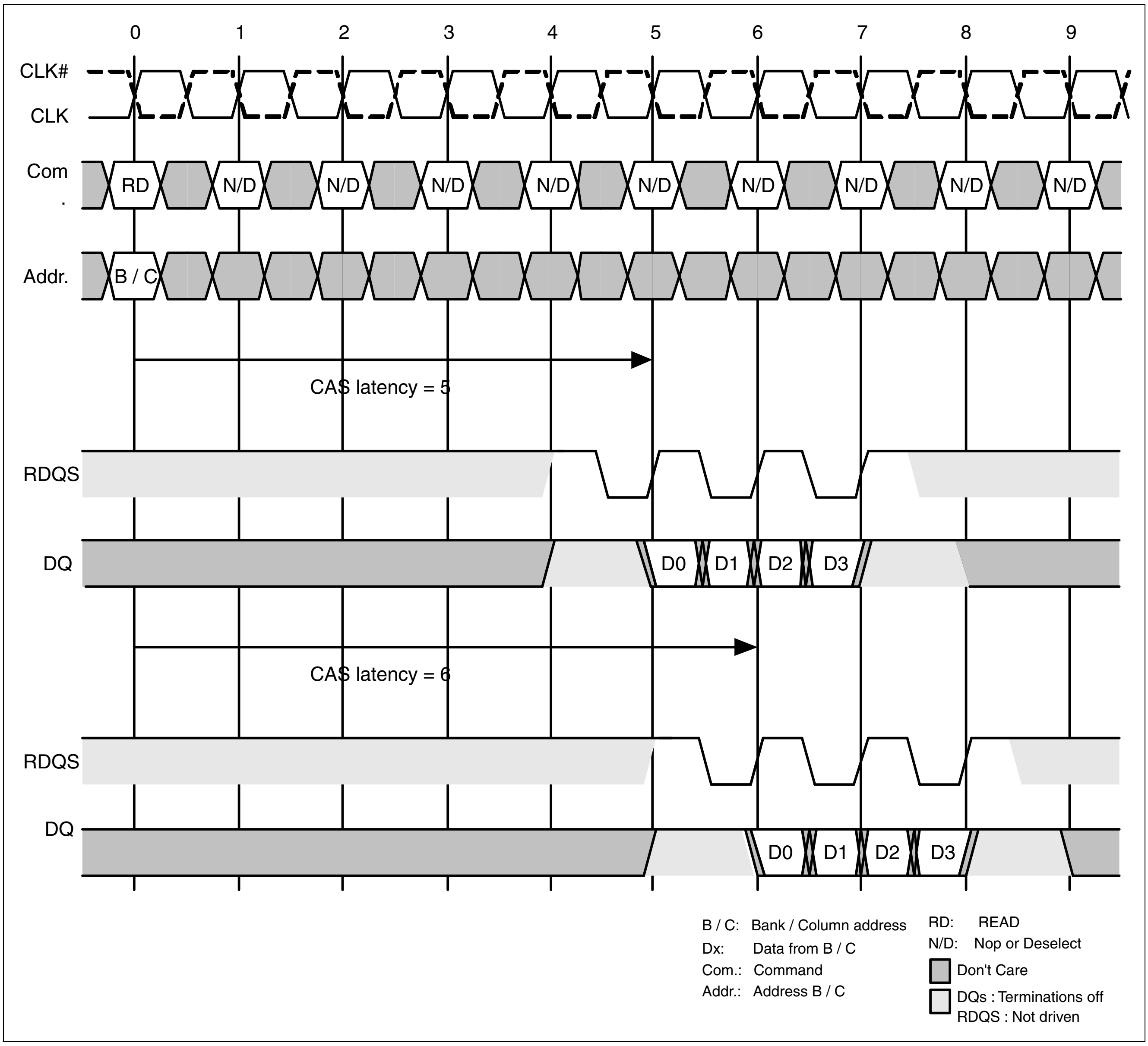

Figure 31 Read Burst

1. *Shown with nominal t_{AC} and t_{DQSQ}*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*

3.8.3 Consecutive Read Bursts

3.8.3.1 Gapless Bursts

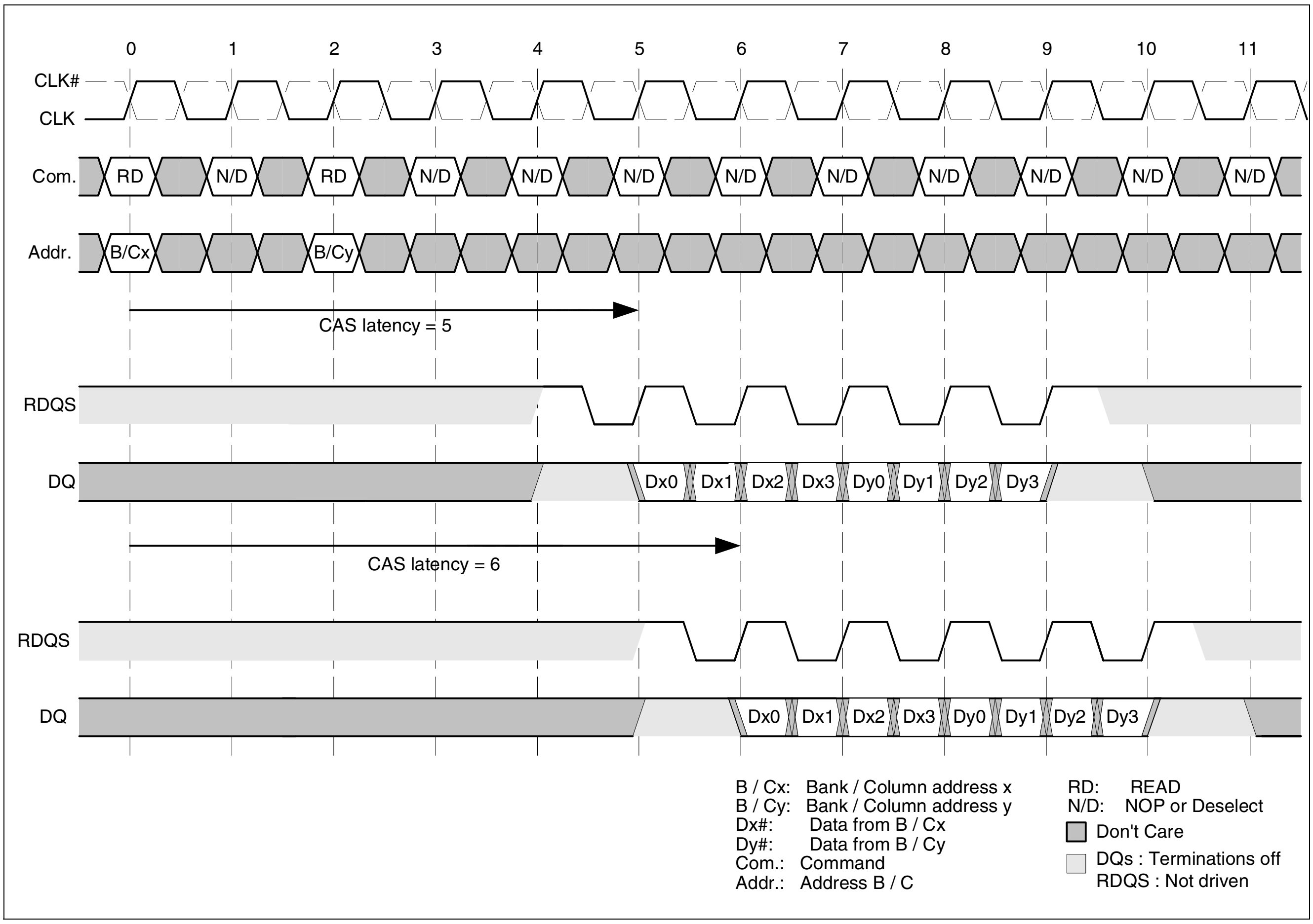

Figure 32 Gapless Consecutive Read Bursts

1. *The second RD command may be either for the same bank or another bank*
2. *Shown with nominal t_{AC} and t_{DQSQ}*
3. *Example applies only when READ commands are issued to same device*
4. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS*
5. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*

3.8.3.2 Bursts with Gaps

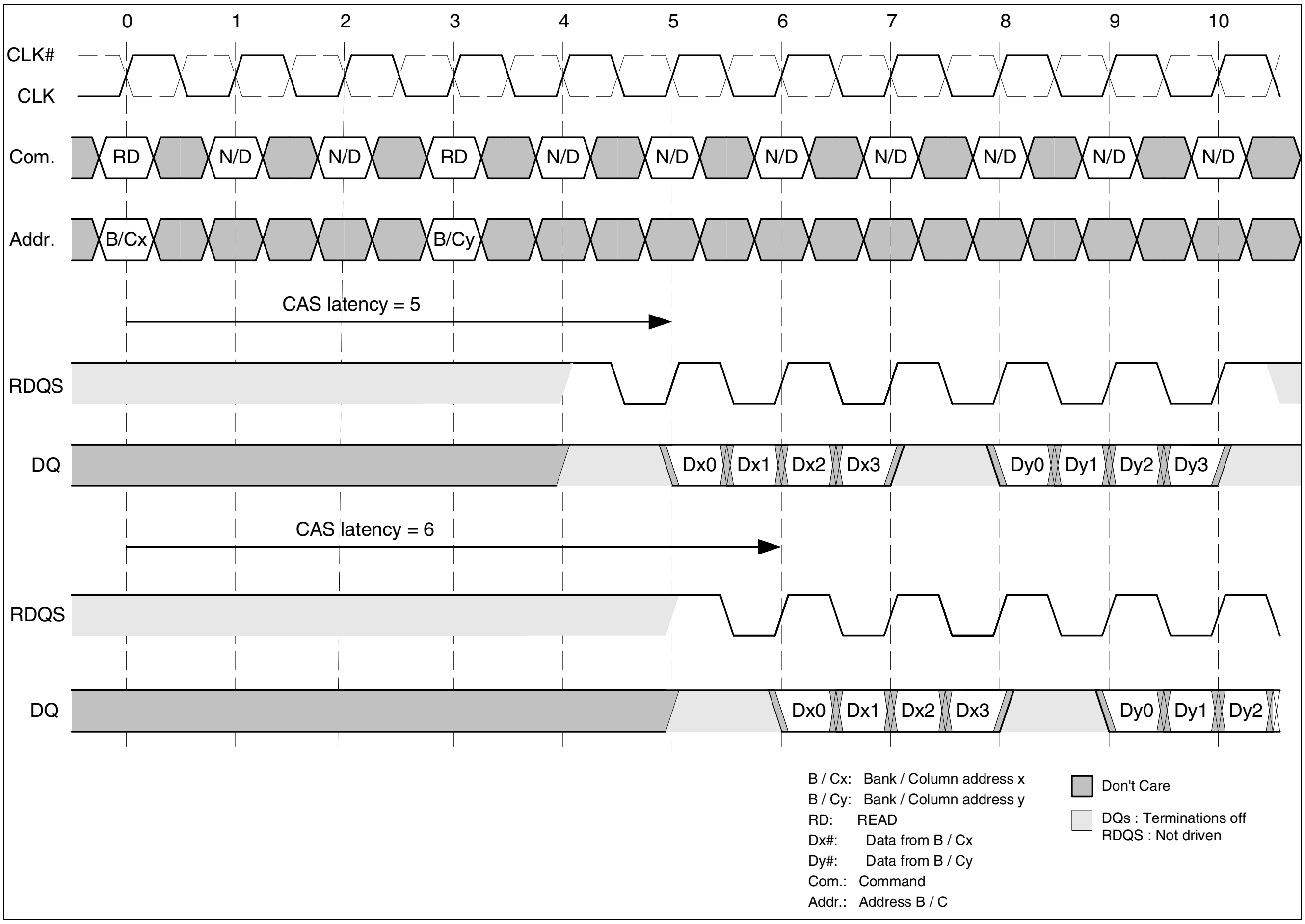

Figure 33 Consecutive Read Bursts with Gaps

1. *The second RD command may be either for the same bank or another bank*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*

3.8.3.3 Read followed by DTERDIS

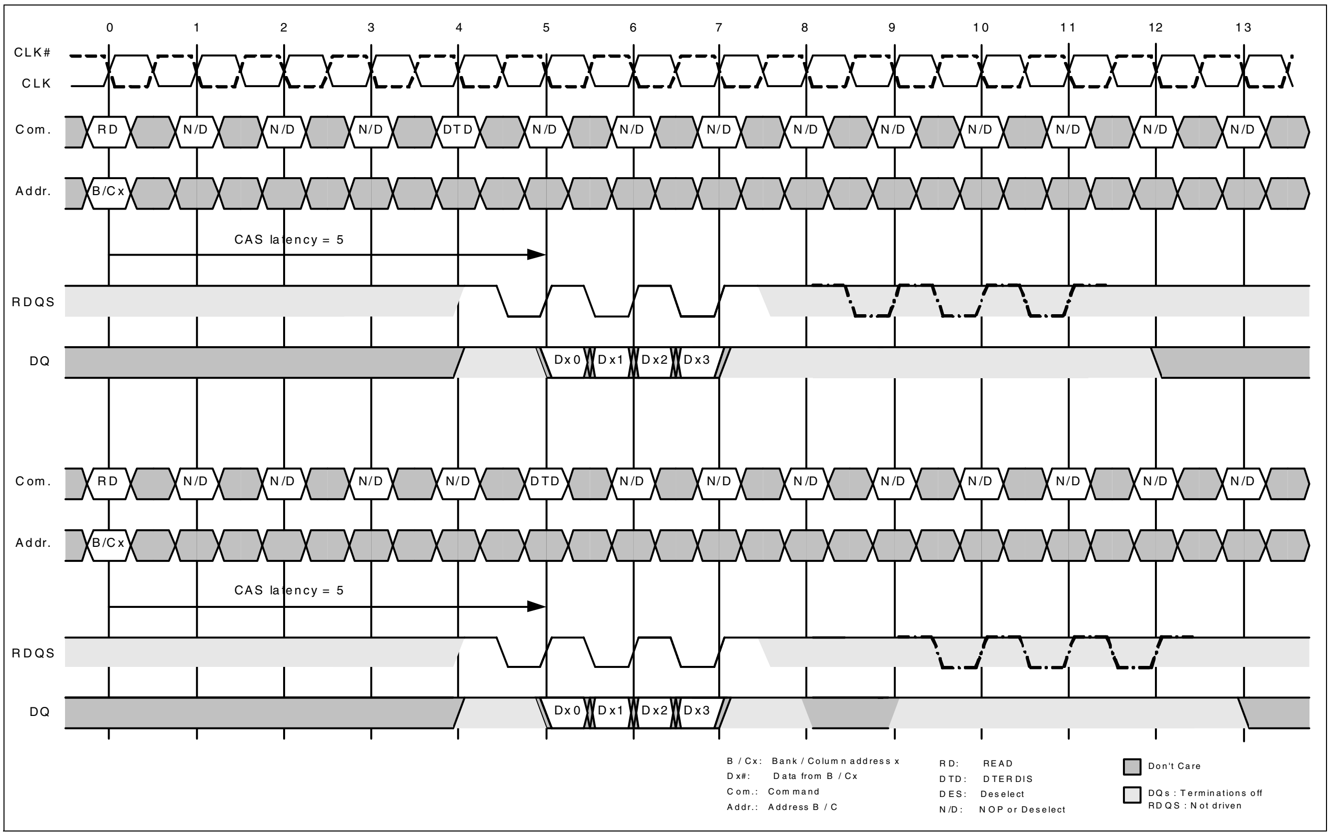

Figure 34 Read Command followed by DTERDIS

1. *At least 3 NOPs are required between a READ command and a DTERDIS command in order to avoid contention on the RDQS bus in a 2 rank system.*
2. *CAS Latency 5 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of (BL/2 + 2) clocks.*
4. *The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 rank system. In this case, RDQS would be driven by the second Graphics DRAM.*

3.8.4 Read with Autoprecharge

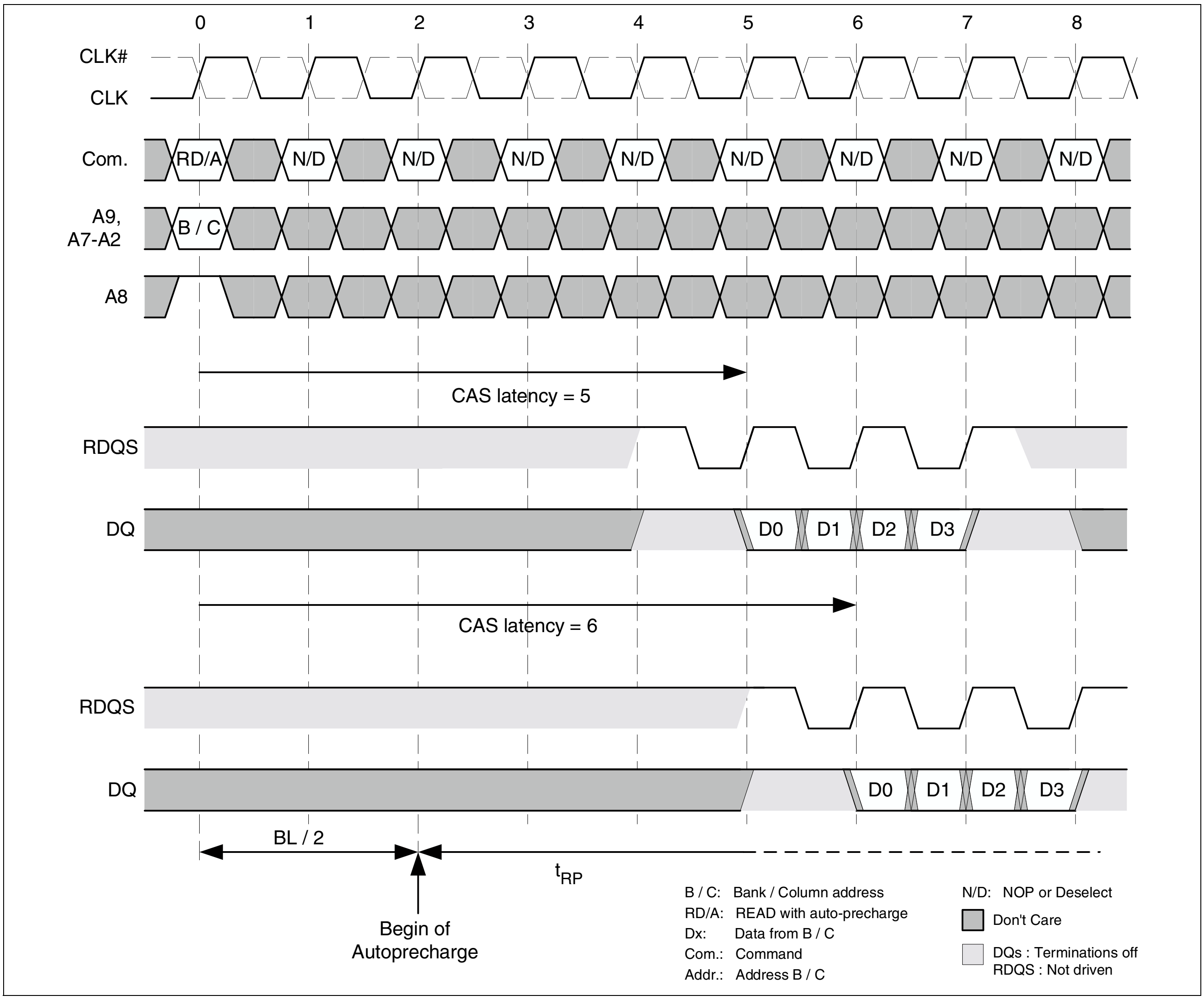

Figure 35 Read with Autoprecharge

1. *When issuing a RD/A command , the t_{RAS} requirement must be met at the beginning of Autoprecharge*
2. *Shown with nominal t_{AC} and t_{DQSQ}*
3. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS*
4. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*
5. *t_{RAS} Lockout support*

3.8.5 Read followed by Write

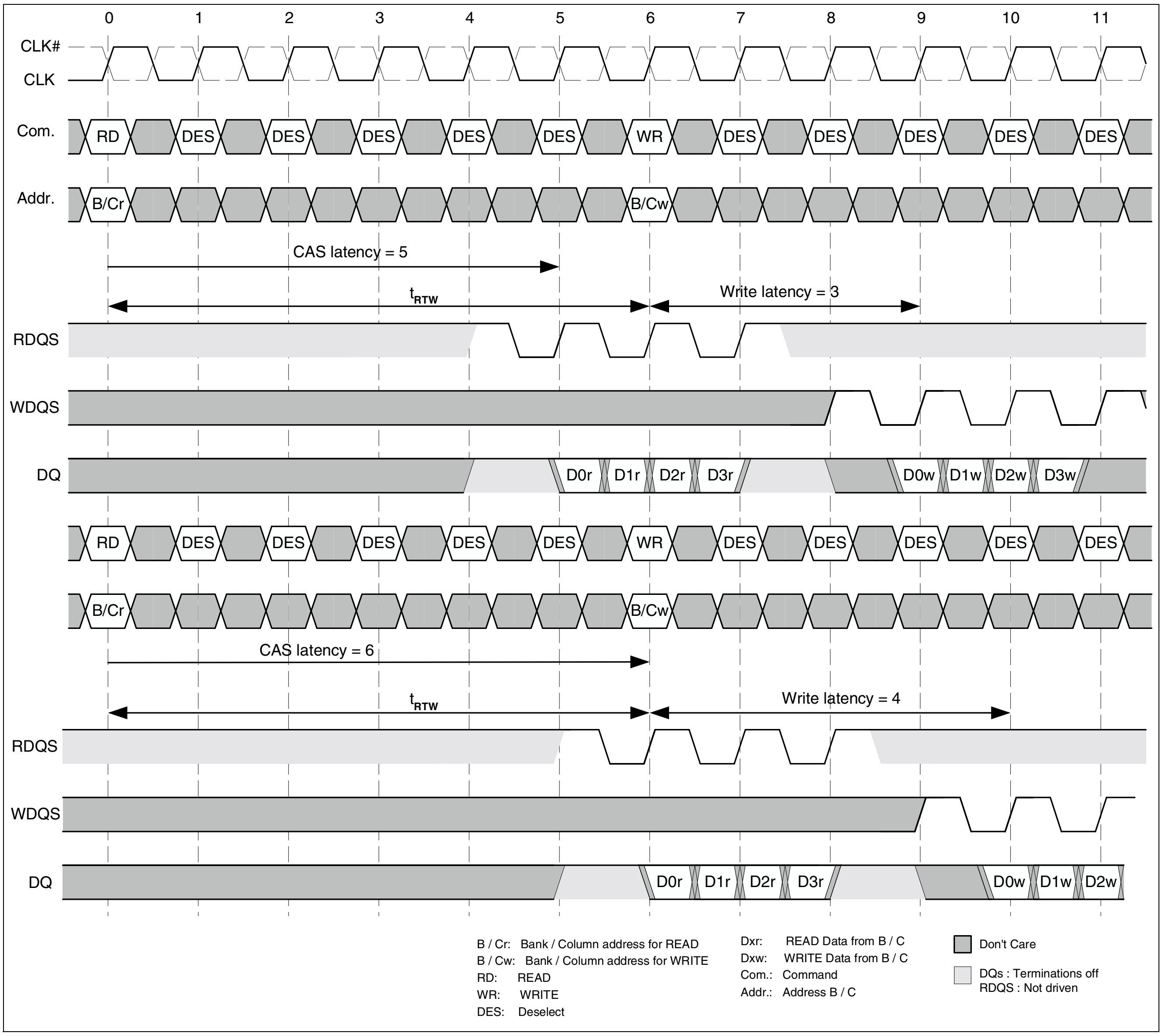

Figure 36 Read followed by Write

1. *Shown with nominal t_{AC}, t_{DQSQ} and t_{DQSS}*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*
5. *The Write command may be either on the same bank or on another bank*

3.8.6 Read followed by Precharge on the same Bank

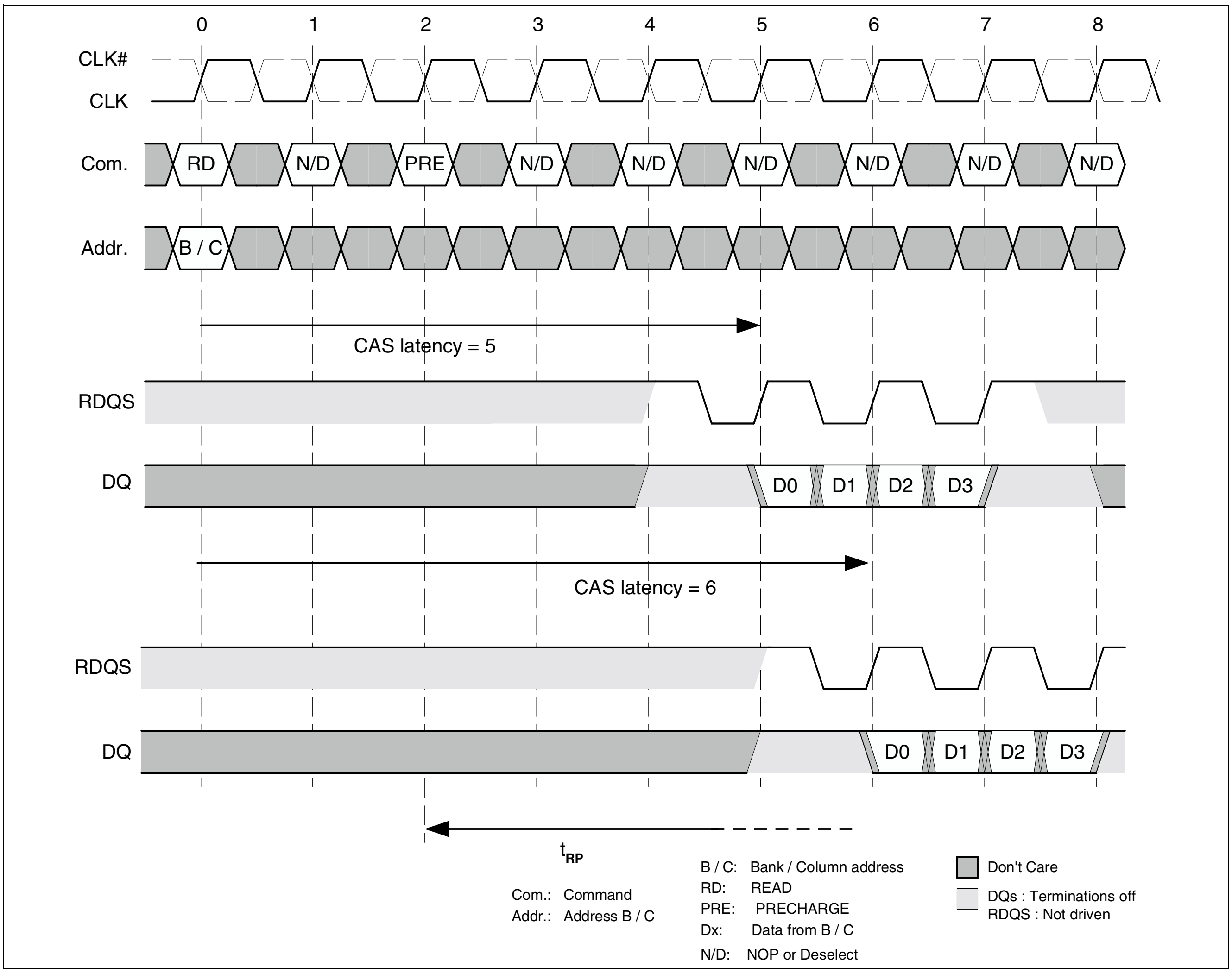

Figure 37 Read followed by Precharge on the same Bank

1. *t_{RAS} requirement must also be met before issuing PRE command*
2. *RD and PRE commands are applied to the same bank.*
3. *Shown with nominal t_{AC} and t_{DQSQ}*
4. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS*

3.9 Data Termination Disable (DTERDIS)

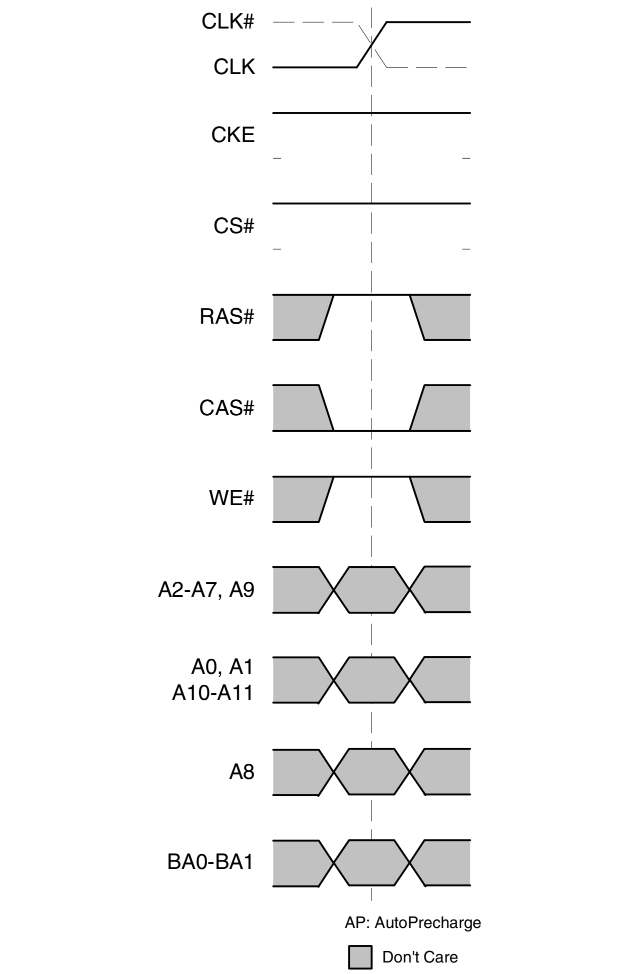

Figure 38 Data Termination Disable Command

The Data Termination Disable command is detected by the device by snooping the bus for Read commands when $\overline{CS}$ is high. The terminators are disabled starting at CL - 1 clocks after the DTERDIS command is detected and the duration is 4 clocks. The command and address terminators are always enabled.

DTERDIS may only be applied to the GDDR3 Graphics memory if it is not in the Power Down or in the Self Refresh state.

The timing relationship between DTERDIS and other commands is defined by the constraint to avoid contention on the RDQS bus (i.e Read to DTERDIS transistion) or the necessity to have a defined termination on the data bus during Write (i.e. Write to DTERDIS transition). ACT and PRE/PREALL may be applied at any time before or after a DTERDIS command.

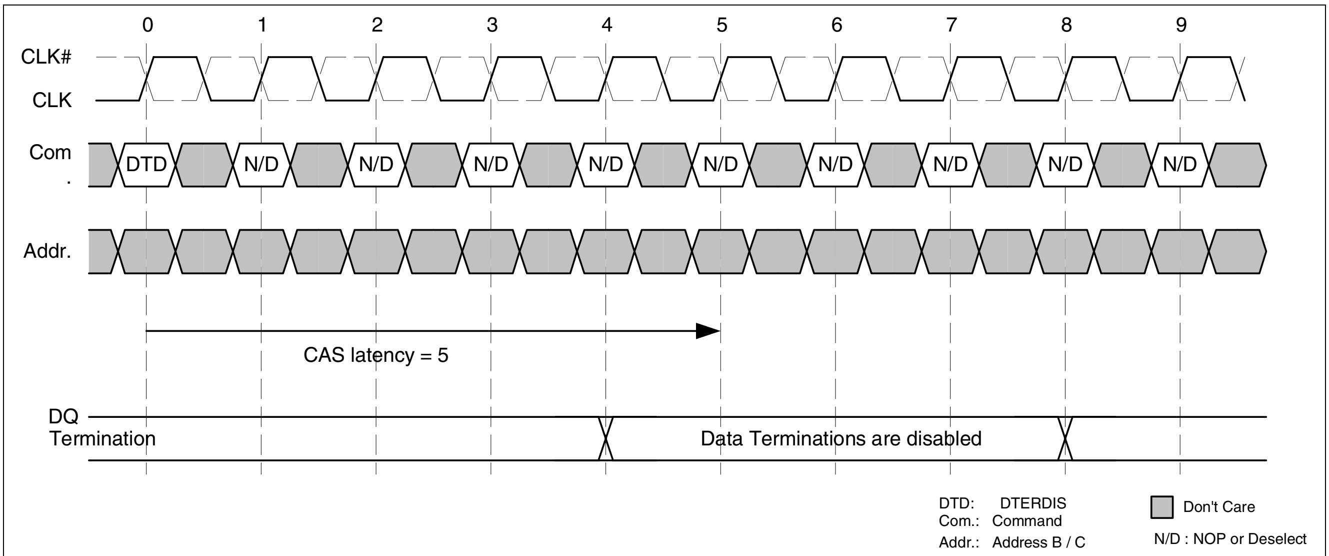

Figure 39 DTERDIS Timing

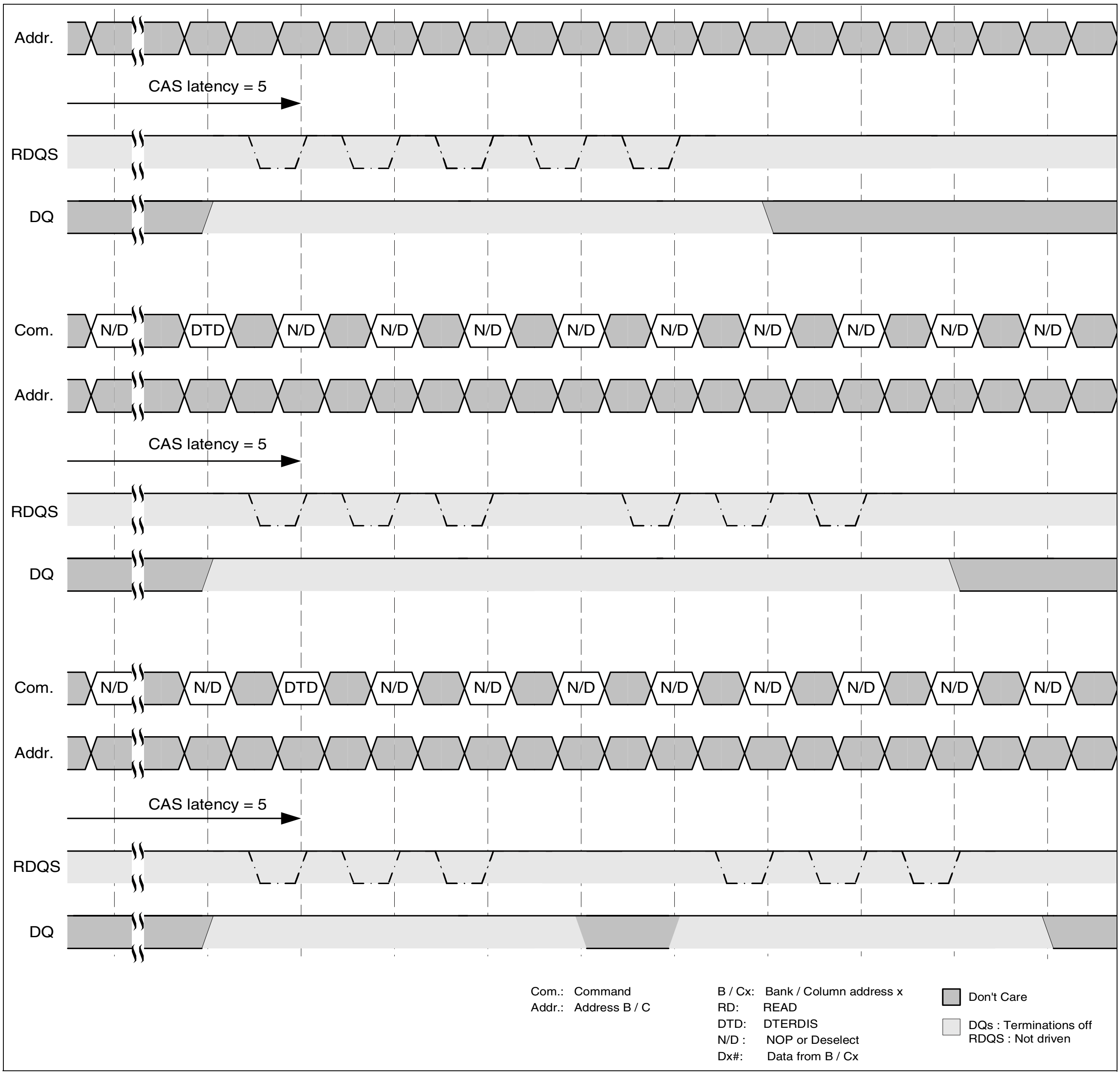

Figure 40 DTERDIS followed by DTERDIS

1. *At least 1NOP is required between 2 DTERDIS commands. This correspond to a Read to Read transistion on the other memory in a 2 rank system.*
2. *CAS Latency 5 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of (BL/2 + 2) clocks*
4. *The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 rank system. In this case, RDQS would be driven by the second Graphics DRAM.*

3.9.1 DTERDIS followed by READ

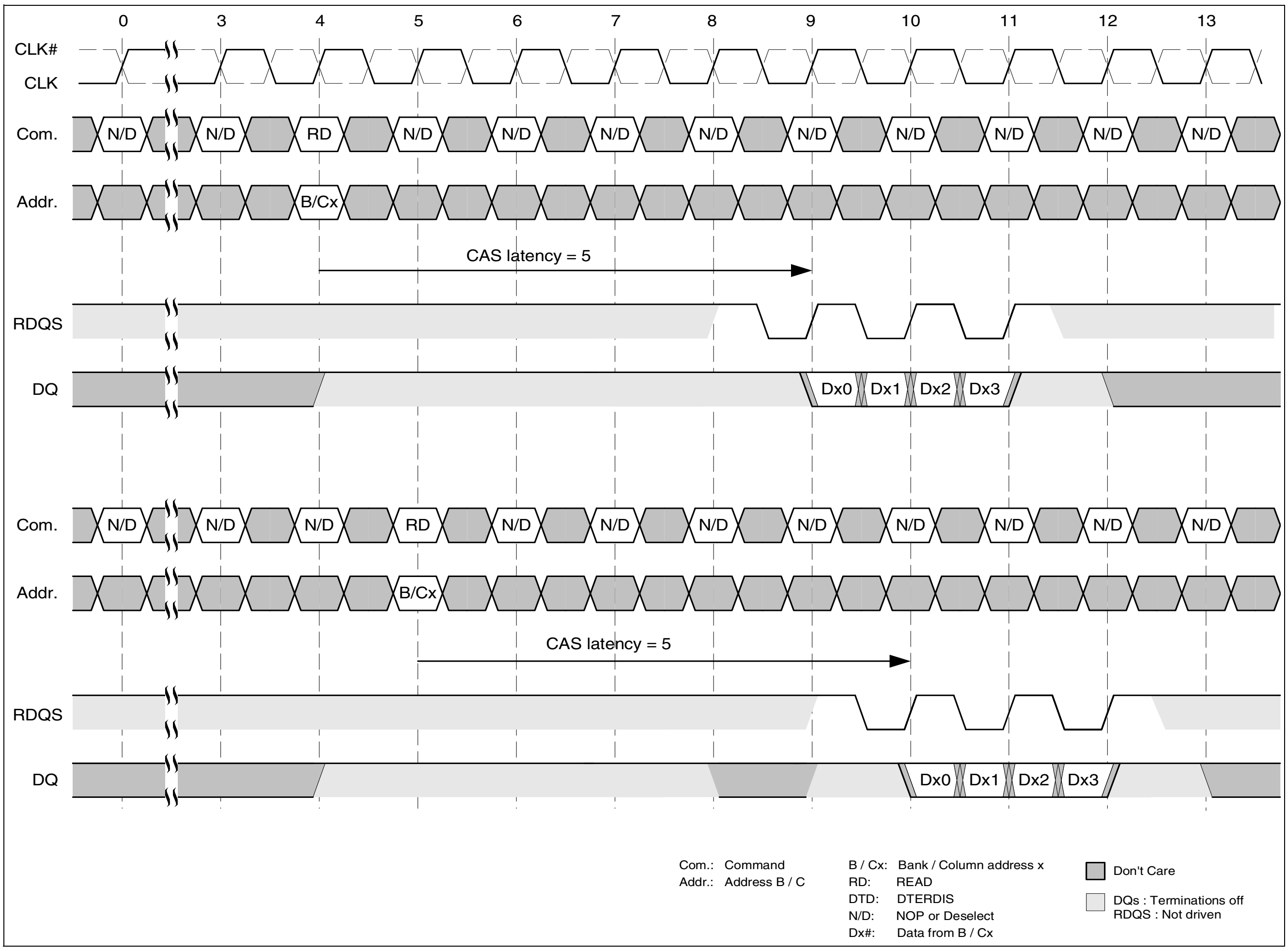

Figure 41 DTERDIS Command followed by READ

1. *At least 3 NOPs are required between a DTERDIS command and a READ command in order to avoid contention on the RDQS bus in a 2 rank system.*
2. *CAS Latency 5 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.*

3.9.2 DTERDIS followed by Write

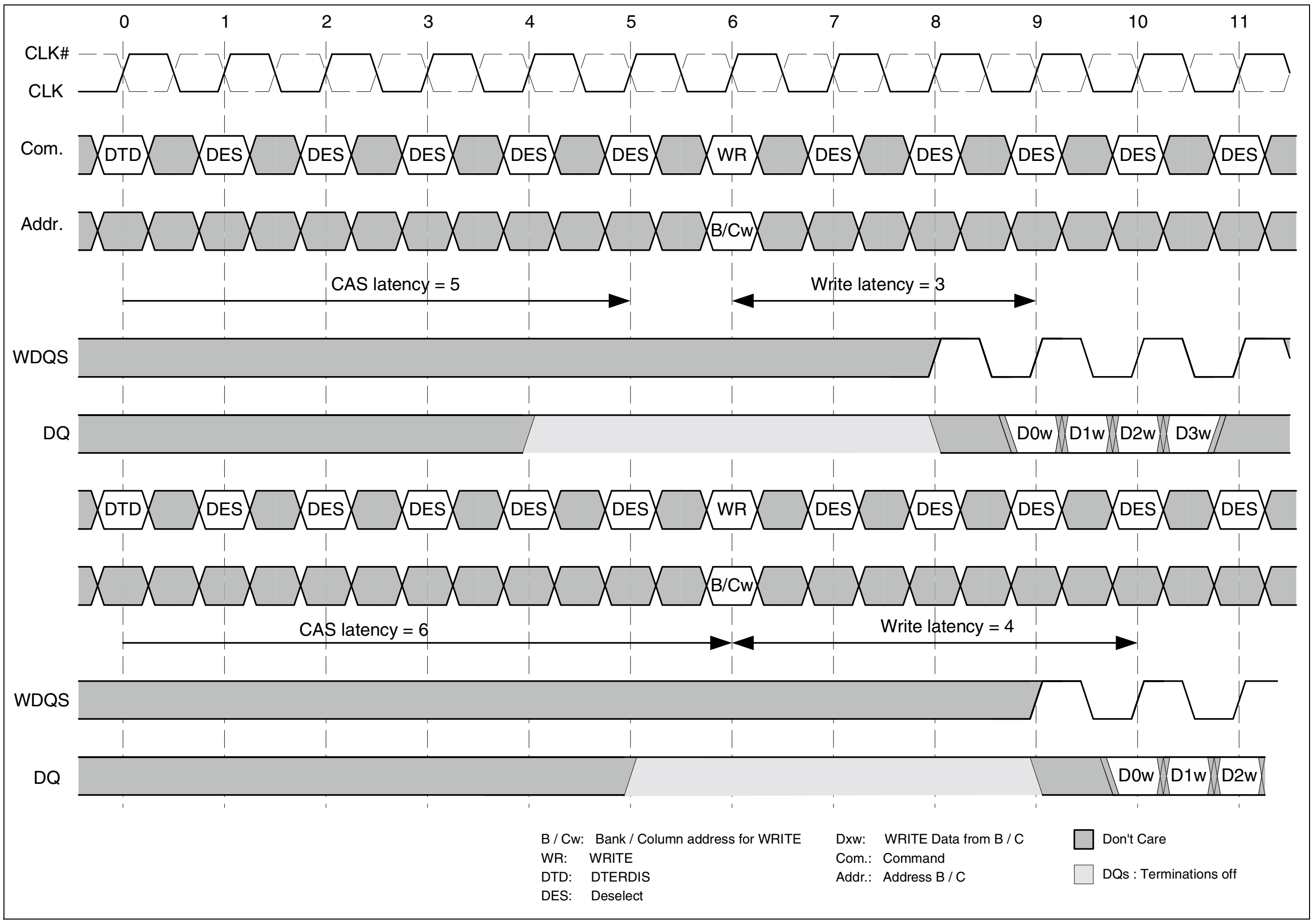

Figure 42 DTERDIS Command followed by Write

1. *Write shown with nominal value of t_{DQSS}*
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*
3. *The minimum distance between DTERDIS and Write is (CL -WL + 4) clocks.*

3.10 Precharge (PRE/PREALL)

The Precharge command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will enter the idle state and be available again for a new row access after the time t_{RP}. A8/AP sampled with the PRE command determines whether one or all banks are to be precharged. For PRE commands BA0 and BA1 select the bank. For PREALL inputs BA0 and BA1 are “Don’t Care”. The PRE/PREALL command may not be given unless the t_{RAS} requirement is met for the selected bank (PRE), or for all banks (PREALL).

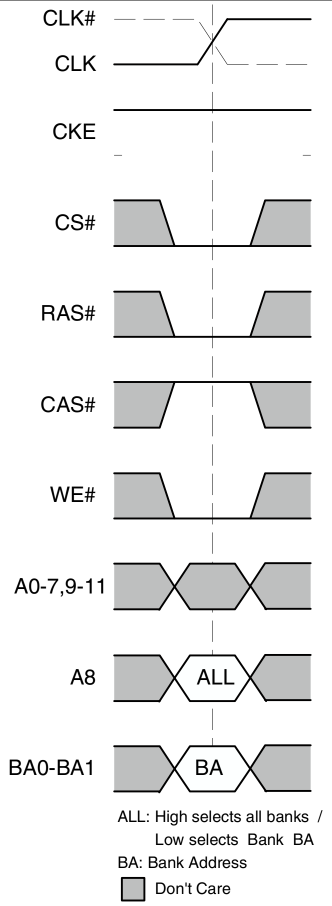

Figure 43 Precharge Command

Table 26 BA1, BA0 precharge bank selection

A8 / AP	BA1	BA0	precharged bank(s)
0	0	0	Bank 0 only
0	0	1	Bank 1 only
0	1	0	Bank 2 only
0	1	1	Bank 3 only
1	X	X	All banks

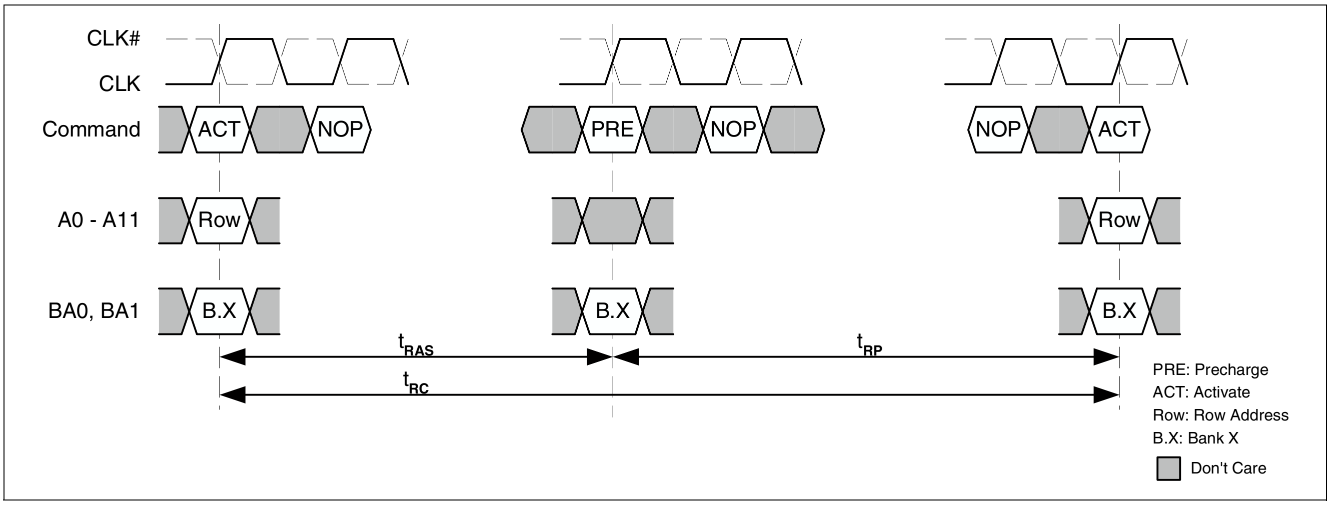

Figure 44 Precharge Timing

Table 27 Precharge Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Row Precharge Time	t_{RP}	13.2	–	13.2	–	13.2	–	ns	

3.11 Auto Refresh Command (AREF)

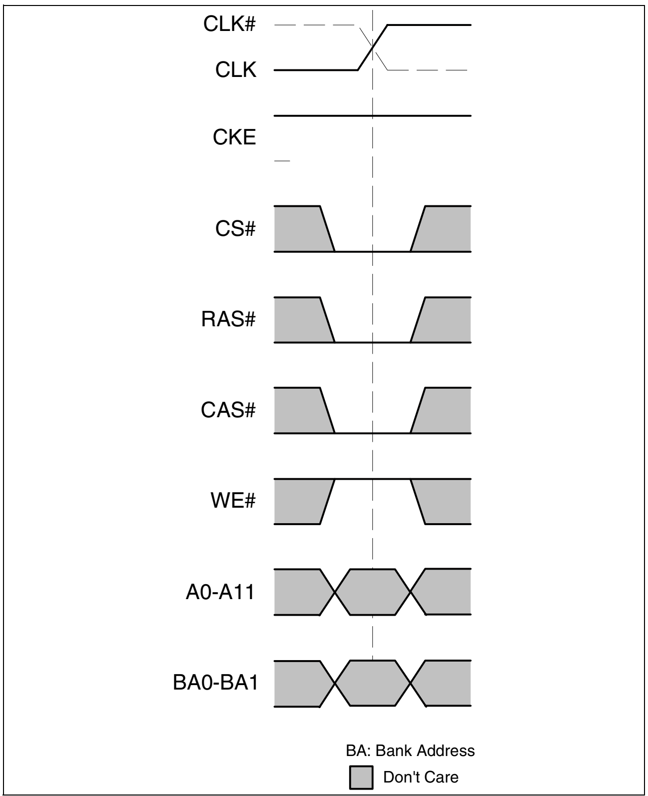

Figure 45 Auto Refresh Command

AREF is used to do a refresh cycle on one row in each bank. The addresses are generated by an internal refresh controller; external address pins are "DON'T CARE". All banks must be idle before the AREF command can be applied. The delay between the AREF command and the next ACT or subsequent AREF must be at least t_{RFC}(min). The refresh period starts when the AREF command is entered and ends t_{RFC} later at which time all banks will be in the idle state.

Within a period of t_{REF}=32ms the whole memory has to be refreshed. The average periodic interval time from AREF to AREF is then t_{REFI}(max)=7.8µs.

To improve efficiency bursts of AREF commands can be used. Such bursts may consist of maximum 8 AREF commands. t_{RFC}(min) is the minimum required time between two AREF commands inside one AREF burst. According to the number of AREF commands in one burst the average required time from one AREF burst to the next can be increased. Example: If the AREF bursts consists of 4 AREF commands, the average time from one AREF burst to the next is 4 * 7.8µs = 31.2µs.

The AREF command generates an update of the OCD output impedance and of the addresses, commands and DQ terminations. The timing parameter tKO (see section 2.3.2) must be complied with.

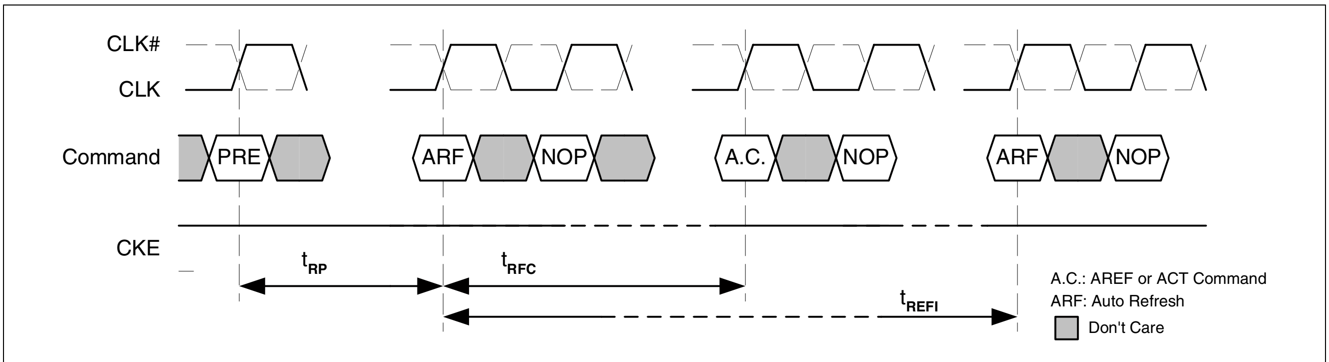

Figure 46 Auto Refresh Cycle

Table 28 Autorefresh Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Refresh Period (4096 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval	t_{REFI}	7.8		7.8		7.8		µs	
Delay from AREF to next ACT/ AREF	t_{RFC}	54	—	54	—	54	—	ns	

3.12 Self-Refresh

3.12.1 Self-Refresh Entry (SREFEN)

The Self-Refresh mode can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When in the Self-Refresh mode, the GDDR3 Graphics RAM retains data without external clocking. The Self-Refresh command is initiated like an Auto-Refresh command except CKE is disabled (LOW). Self Refresh Entry is only possible if all banks are precharged and t_{RP} is met.

The GDDR3 Graphics RAM has a build-in timer to accomodate Self-Refresh operation. The Self-Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the command is registered, CKE must be held LOW to keep the device in Self-Refresh mode. When the GDDR3 Graphics RAM has entered the Self-Refresh mode, all external control signals, except CKE are disabled. The address, command and data terminators remain on. The DLL and the clock are internally disabled to save power. The user may halt the external clock while the device is in Self-Refresh mode the next clock after Self-Refresh entry, however the clock must be restarted before the device can exit Self-Refresh operation.

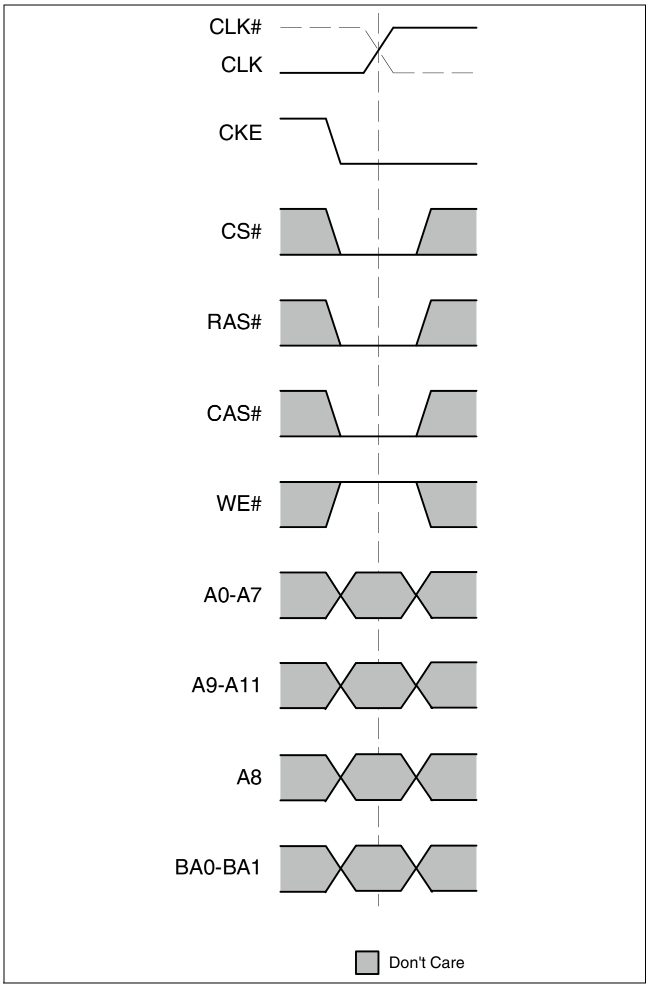

Figure 47 Self Refresh Entry Command

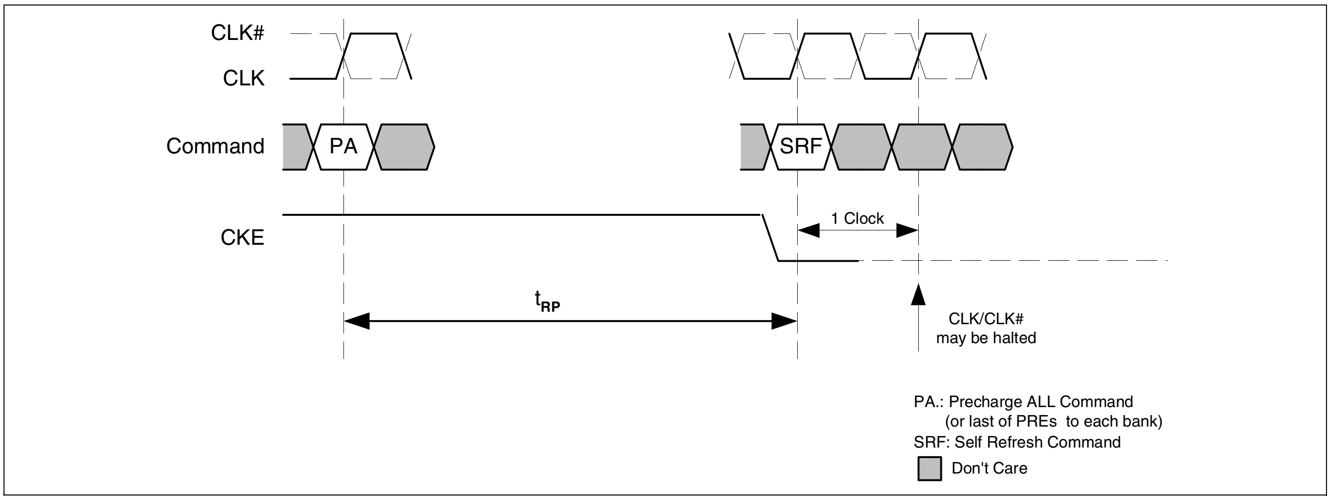

Figure 48 Self Refresh Entry

3.12.2 Self-Refresh Exit (SREFEX)

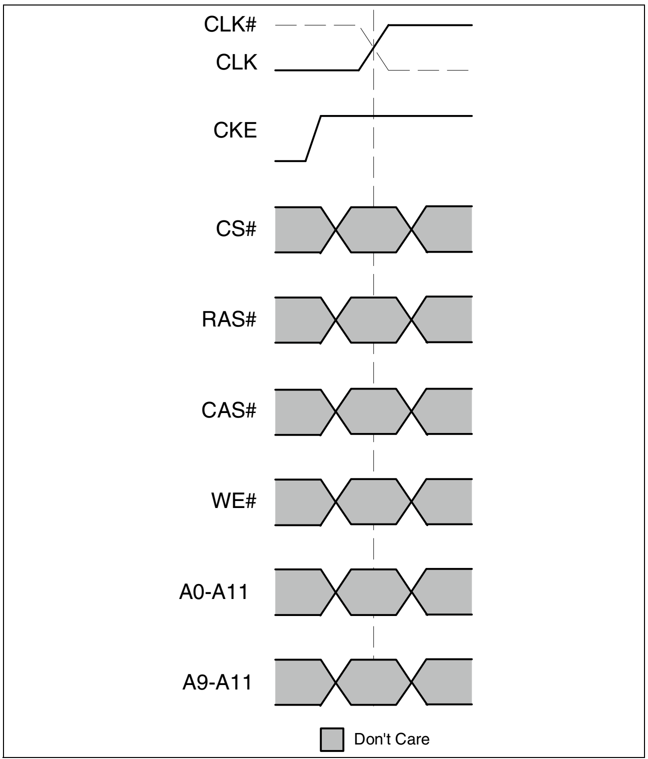

Figure 49 Self Refresh Exit Command

To exit the Self Refresh Mode, a stable external clock is needed before setting CKE high asynchronously. Once the Self-Refresh Exit command is registered, a delay equal or longer than tXSC (minimum 200 Clock Cycles) must be satisfied before any command can be applied. During this time, the DLL is automatically enabled, reset and calibrated.

CKE must remain HIGH for the entire Self-Refresh exit period and commands must be gated off with $\overline{CS}$ held HIGH. Alternately, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval.

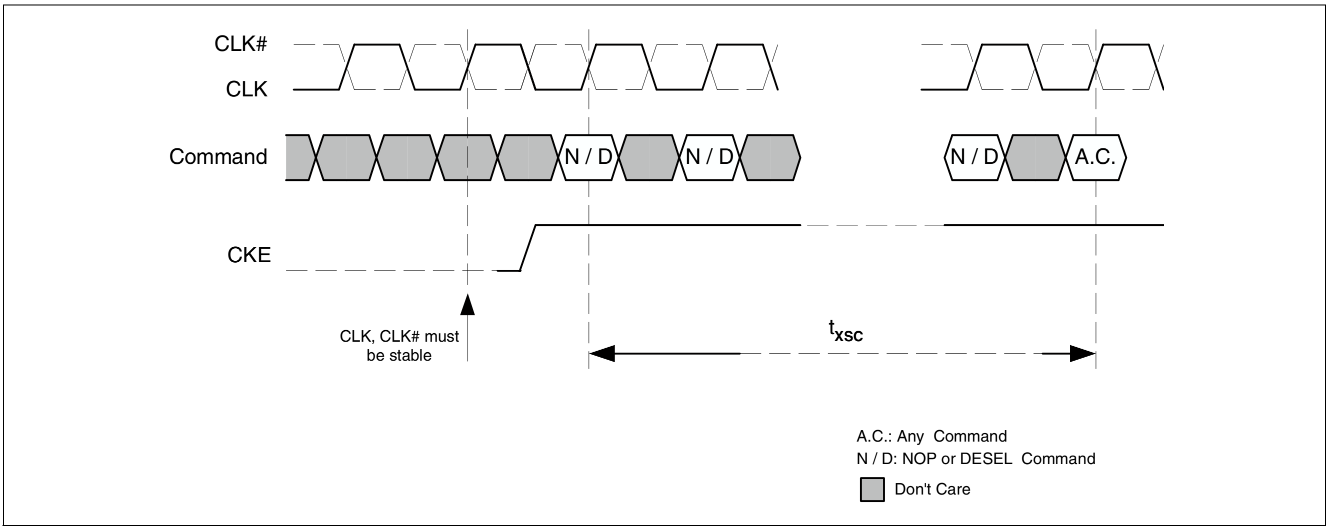

Figure 50 Self Refresh Exit

Table 29 Self Refresh Exit Timing Parameter for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Units	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Self Refresh Exit time	t_{XSC}	200	–	200	–	200	–	t_{CK}	

3.13 Power-Down

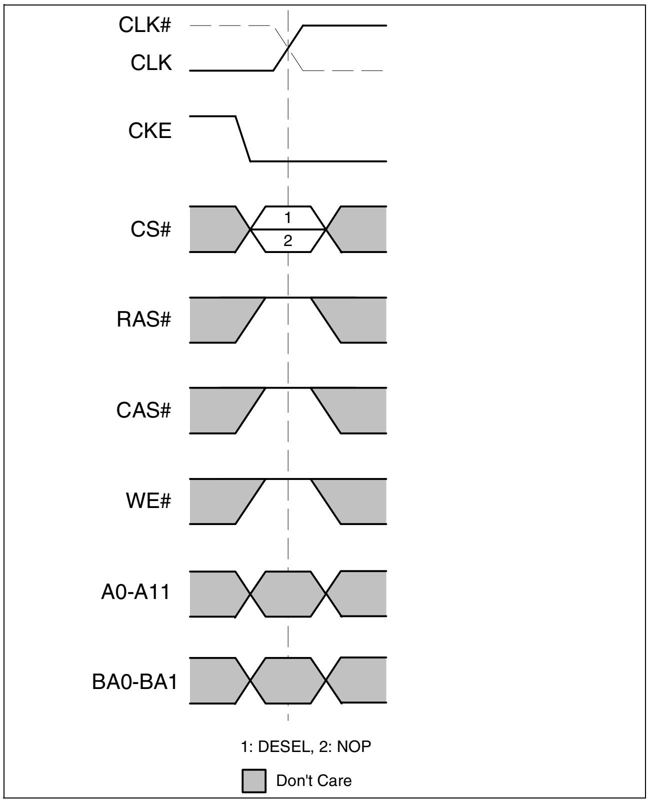

Figure 51 Power Down Command

Unlike SDR SDRAMs, the GDDR3 Graphics RAM requires CKE to be active at all times an access is in progress : From the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined after the rising edge of the Read Postamble. For Writes, a burst completion is defined one clock after the rising edge of the Write Postamble.

For Read with Autoprecharge and Write with Autoprecharge, the internal Autoprecharge must be completed before entering Power-Down.

Power-Down is entered when CKE is registered LOW (no access can be in progress). If Power-Down occurs when all banks are idle, this mode is referred to as Precharge Power-Down; if Power-Down occurs when there is a row active in any bank, this mode is referred to as Active Power-Down. Entering power-down deactivates the input and output buffers, excluding CLK, $\overline{\text{CLK}}$ and CKE. For maximum power saving, the user has the option of disabling the DLL prior to entering power-down. In that case the DLL must be enabled and reset after exiting power-down, and 200 cycles must occur before a READ command can be issued.

In Power-Down mode, CKE low and a stable clock signal must be maintained at the inputs of the GDDR3 Graphics RAM, all the other input signals are “Don’t Care”. Power down duration is limited by the refresh requirements of the device.

The Power-Down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESEL command). A valid executable command may be applied tXPN later.

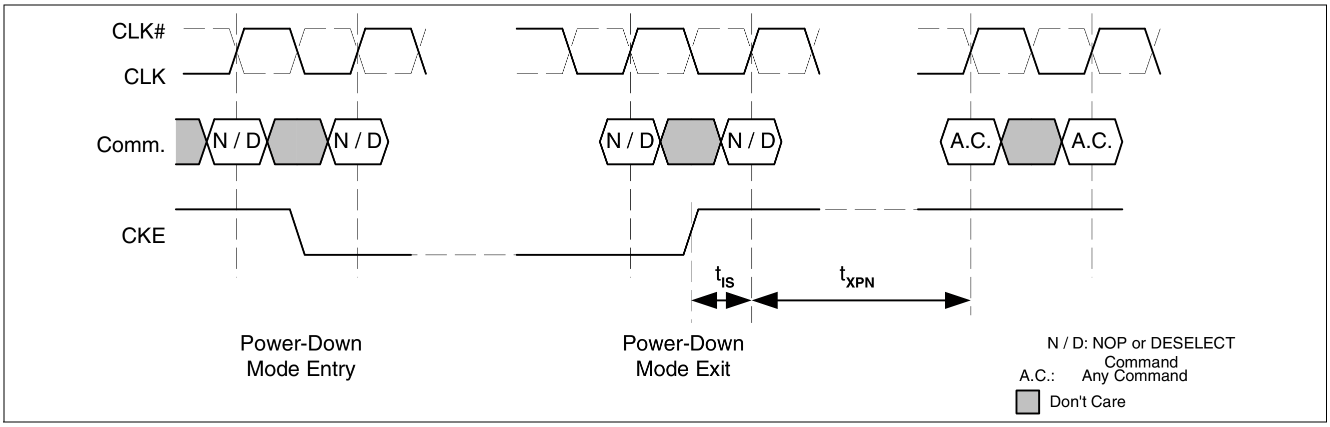

Figure 52 Power-Down Mode

Table 30 Power Down Exit Timing Parameter for –1.6, –2.0 and –2.2 speed sorts

Parameter	Symbol	Limit Values						Unit	Notes
		–1.6		–2.0		–2.2			
		min	max	min	max	min	max		
Precharge power-down exit timing	t_{XPN}	5	—	4	—	4	—	t_{CK}	

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 31 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		min.	max.	
Power Supply Voltage	V_{DD}	-0.5	2.5	V
Power Supply Voltage for Output Buffer	V_{DDQ}	-0.5	2.5	V
Input Voltage	V_{IN}	-0.5	V_{DDQ}+0.5	V
Output Voltage	V_{OUT}	-0.5	V_{DDQ}+0.5	V
Storage Temperature	T_{STG}	-55	+150	°C
Short Circuit Output Current	I_{OUT}	—	50	mA

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32 Operation Conditions

Parameter	Symbol	Range		Unit
		min.	max.	
Operation Temperature (Junction)	T_J	0	+90	°C
Operation Temperature (Case)	T_C	0	+85	°C
Power Dissipation	P_D	—	3.2	W

4.2 Recommended Power & DC Operation Conditions.

All values are recommended operating conditions unless otherwise noted. T_c = 0 to 85 °C.
(0°C ≤ T_C ≤ +85°C, V_{DD} = +2.0 V ± 0.10 V, V_{DDQ} = +2.0 V ± 0.10 V, see **Table 1**)

Table 33 Power & DC Operation Conditions

Parameter	Symbol	Speed sort	Limit Values			Unit	Notes
			min.	typ.	max.		
Power Supply Voltage	V_{DD}	–1.6	1.9	2.0	2.1	V	1)
		–2.0	1.9	2.0	2.1	V	1)
		–2.2	1.9	2.0	2.1	V	1)
Power Supply Voltage for I/O Buffer	V_{DDQ}	–1.6	1.9	2.0	2.1	V	1)
		–2.0	1.9	2.0	2.1	V	1)
		–2.2	1.9	2.0	2.1	V	1)
Reference Voltage	V_{REF}	–1.6	0.72*V_{DDQ}	0.73*V_{DDQ}	0.74*V_{DDQ}	V	2)
		–2.0	0.72*V_{DDQ}	0.73*V_{DDQ}	0.74*V_{DDQ}		2)3)
		–2.2	0.72*V_{DDQ}	0.73*V_{DDQ}	0.74*V_{DDQ}		2)3)
Output Low Voltage	$V_{OL(DC)}$				0.4*V_{DDQ}	V	
Input leakage current	I_{IL}		–5		+5	µA	4)
CLK Input leakage current	I_{ILC}		–5		+5	µA	
Output leakage current	I_{OL}		–5		+5	µA	4)

1) *V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.*
2) *V_{REF} is allowed ± 19mV for DC error and an additionnal ± 28mV for AC noise.*
3) *V_{REF} is expected to equal 73% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF} (DC). Thus, from 73% of V_{DDQ}.*
4) I_{IL} and I_{OL} are measured with ODT disabled.

4.3 DC & AC Logic Input Levels.

(0°C ≤ T_C ≤ +85°C, V_{DD} = +2.0 V ± 0.10 V, V_{DDQ} = +2.0 V ± 0.10 V, see **Table 1**)

Table 34 DC & AC Logic Input Levels

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input logic high voltage, DC	$V_{IH(DC)}$	0.7 *V_{DDQ} + 0.15	—	V	1
Input logic low voltage, DC	$V_{IL(DC)}$	—	0.7 *V_{DDQ} -0.15	V	1
Input logic high voltage, AC	$V_{IH (AC)}$	0.7 *V_{DDQ} +0.4	—	V	2,3
Input logic low voltage, AC	$V_{IL(AC)}$	—	0.7 *V_{DDQ} - 0.4	V	2,3
Input logic high, DC, RESET pin	$V_{IHR(DC)}$	0.8 *V_{DDQ}	V_{DDQ} + 0.3	V	
Input logoc low, DC, RESET pin	$V_{ILR(DC)}$	-0.3	0.2 *V_{DDQ}	V	

1. *The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level.*
2. *Input slew rate = 2 V/ns. If the input slew rate is less than 2 V/ns, input timing may be compromised. All slew rates are measured between $V_{IL(DC)}$ and $V_{IH(DC)}$.*
3. *V_{IH} overshoot : $V_{IH(MAX)}$ = V_{DDQ}+0.5 V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL(MIN)}$ = 0 V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.*

4.4 Differential Clock DC and AC Levels

(0°C ≤ T_C ≤ +85°C, V_{DD} = +2.0 V ± 0.10 V, V_{DDQ} = +2.0 V ± 0.10 V, see **Table 1**)

Table 35 Differential Clock DC and AC Input conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock Input Mid-Point Voltage, CLK and $\overline{\text{CLK}}$	$V_{MP(DC)}$	V_{REF} - 0.1	V_{REF} + 0.1	V	1
Clock Input Voltage Level, CLK and $\overline{\text{CLK}}$	$V_{IN(DC)}$	0.42	V_{DDQ} + 0.3	V	1
Clock DC Input Differential Voltage, CLK and $\overline{\text{CLK}}$	$V_{ID(DC)}$	0.3	V_{DDQ}	V	1
Clock AC Input Differential Voltage, CLK and $\overline{\text{CLK}}$	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.5	V	1, 2
AC Differential Crossing Point Input Voltage	$V_{IX(AC)}$	V_{REF} - 0.15	V_{REF} + 0.15	V	1, 3

1. *All voltages referenced to V_{SS}*
2. *V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{\text{CLK}}$.*
3. *The value of V_{IX} is expected to equal 0.7 x V_{DDQ} of the transmitting device and must track variations in the DC level of the same.*

4.5 Output Test Conditions

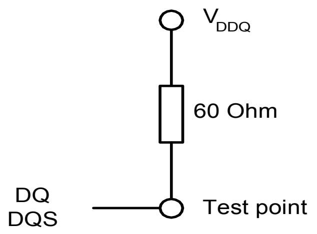

Figure 53 Output Test Circuit

Note: V_{DDQ}=2.0 ±0.1 V, Tc=0 °C to 85 °C, see ***Table 1***

4.6 Pin Capacitances

Table 36 Capacitances

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: CLK, $\overline{\text{CLK}}$	CCK	2.0	4.0	pF	
Input capacitance delta: CLK, $\overline{\text{CLK}}$	CDCK		0.1	pF	1
Input capacitance: A0-A11, BA0-1,CKE, $\overline{\text{CS}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{WE}}$, CKE, RES	CI	2.0	4.0	pF	
Input capacitance delta: A0-A11, BA0-1,CKE, $\overline{\text{CS}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{WE}}$, CKE, RES	DCI		0.6	pF	1
Input capacitance: DQ0-DQ31, RDQS0-RDQS3, WDQS0-WDQS3, DM0-DM3	CIO	2.5	4.5	pF	
Input capacitance delta: DQ0-DQ31, RDQS0-RDQS3, WDQS0-WDQS3, DM0-DM3	DCIO		0.6	pF	2

1. *The input capcitance per pin group will not differ by more than this maximum amount for any given device.*
2. *The IO capacitance per RDQS and DQ byte / group will not differ by more than this maximum amount for any given device.*

4.7 Driver current characteristics

4.7.1 Driver IV characteristics at 40 Ohms

Figure 54 represents the driver Pull-Down and Pull-Up IV characteristics under process, voltage and temperature best and worst case conditions. The actual Driver Pull-Down and Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240Ω, setting the nominal driver output impedance to 40Ω.

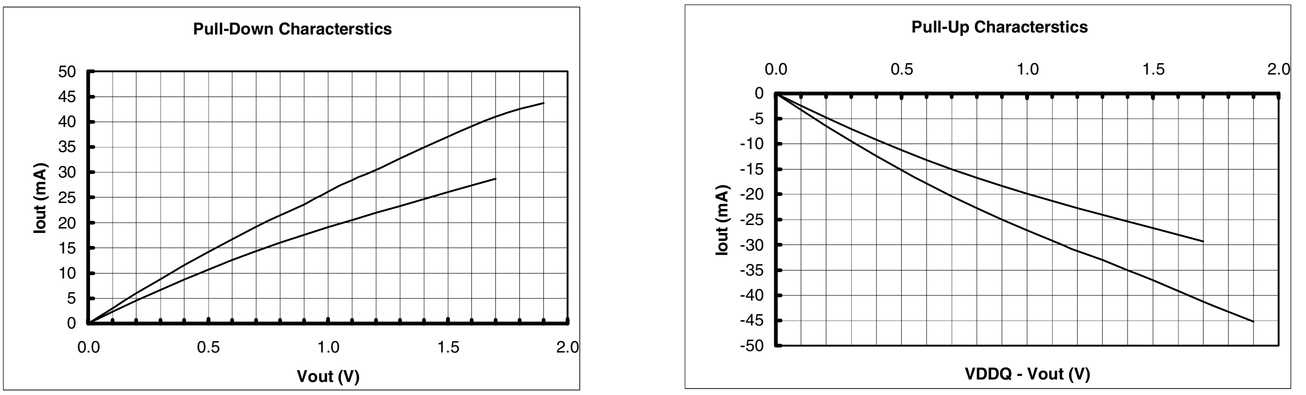

Figure 54 40 Ohm Driver Pull-Down and Pull-Up characteristics

Table 37 lists the numerical values of the minimum and maximum allowed values of the output driver Pull-Down and Pull-Up IV characteristics.

Table 37 Programmed Driver IV Characteristics at 40 Ohm

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.1	2.32	3.04	-2.44	-3.27
0.2	4.56	5.98	-4.79	-6.42
0.3	6.69	8.82	-7.03	-9.45
0.4	8.74	11.56	-9.18	-12.37
0.5	10.70	14.19	-11.23	-15.17
0.6	12.56	16.72	-13.17	-17.83
0.7	14.34	19.14	-15.01	-20.37
0.8	16.01	21.44	-16.74	-22.78
0.9	17.61	23.61	-18.37	-25.04
1.0	19.11	26.10	-19.90	-27.17
1.1	20.53	28.45	.21.34	-29.17
1.2	21.92	30.45	-22.72	-31.25
1.3	23.29	32.73	-24.07	-33.00
1.4	24.65	34.95	-25.40	-35.00
1.5	26.00	37.10	-26.73	-37.00
1.6	27.35	39.15	-28.06	-39.14
1.7	28.70	41.01	-29.37	-41.25
1.8	-	42.53	-	-43.29
1.9	-	43.71	-	-45.23

4.8 Termination IV Characteristic at 60 Ohms

Figure 55 represents the DQ termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual DQ termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240Ω, setting the nominal DQ termination impedance to 60Ω. (Extended Mode Register programmed to ZQ/4).

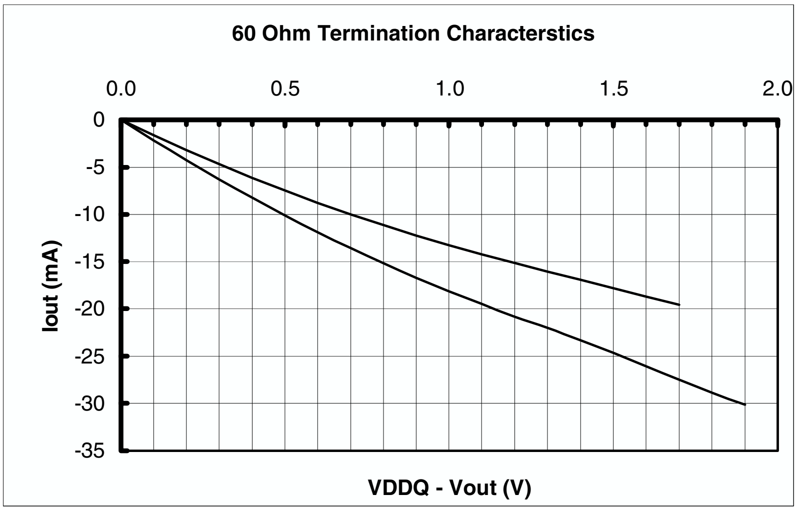

Figure 55 60 Ohm Active Termination Characteristic

Table 38 lists the numerical values of the minimum and maximum allowed values of the output driver termination IV characteristic.

Table 38 Programmed Terminator Characterisitc at 60 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
				1.0	-13.27	-18.11
0.1	-1.63	-2.18		1.1	-14.23	-19.45
0.2	-3.19	-4.28		1.2	-15.14	-20.83
0.3	-4.69	-6.30		1.3	-16.04	-22.00
0.4	-6.12	-8.25		1.4	-16.94	-23.33
0.5	-7.49	-10.11		1.5	-17.82	-24.67
0.6	-8.78	-11.89		1.6	-18.70	-26.09
0.7	-10.01	-13.58		1.7	-19.58	-27.50
0.8	-11.16	-15.19		1.8	-	-28.86
0.9	-12.25	-16.69		1.9	-	-30.15

4.9 Termination IV Characteristic at 120 Ohms

Figure 56 represents the DQ or ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240Ω, setting the nominal termination impedance to 120Ω. (Extended Mode Register programmed to ZQ/2 for DQ terminations or CKE = 0 at the RES transition during Power-Up for ADD/CMD terminations).

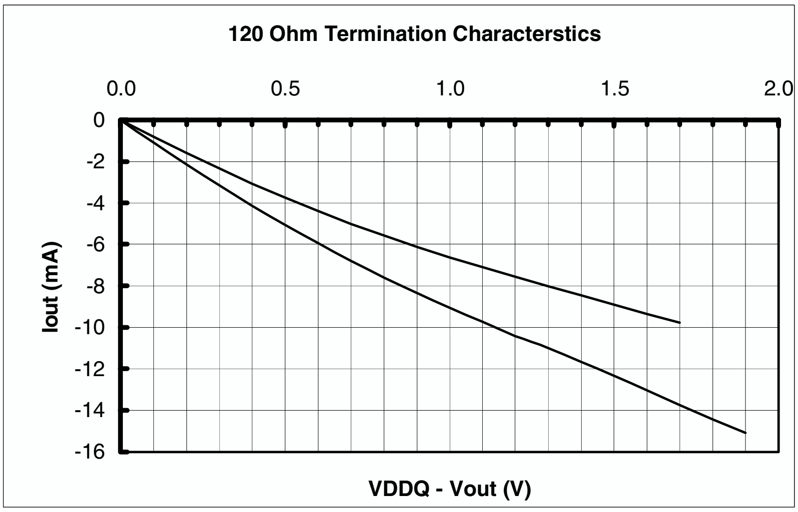

Figure 56 120 Ohm Active Termination Characteristic

Table 39 lists the numerical values of the minimum and maximum allowed values of the termination IV characteristic.

Table 39 Programmed Terminator Characterisitics at 120 Ohm

Voltage(V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
				1.0	-6.63	-9.06
0.1	-0.81	-1.09		1.1	-7.11	-9.72
0.2	-1.60	-2.14		1.2	-7.57	-10.42
0.3	-2.34	-3.15		1.3	-8.02	-11.00
0.4	-3.06	-4.12		1.4	-8.47	-11.67
0.5	-3.74	-5.06		1.5	-8.91	-12.33
0.6	-4.39	-5.94		1.6	-9.35	-13.05
0.7	-5.00	-6.79		1.7	-9.79	-13.75
0.8	-5.58	-7.59		1.8	-	-14.43
0.9	-6.12	-8.35		1.9	-	-15.08

4.10 Termination IV Characteristic at 240 Ohms

Figure 57 represents the ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual ADD/CMD termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240Ω, setting the nominal termination impedance to 240Ω. (CKE = 1at the RES transition during Power-Up for ADD/CMD terminations).

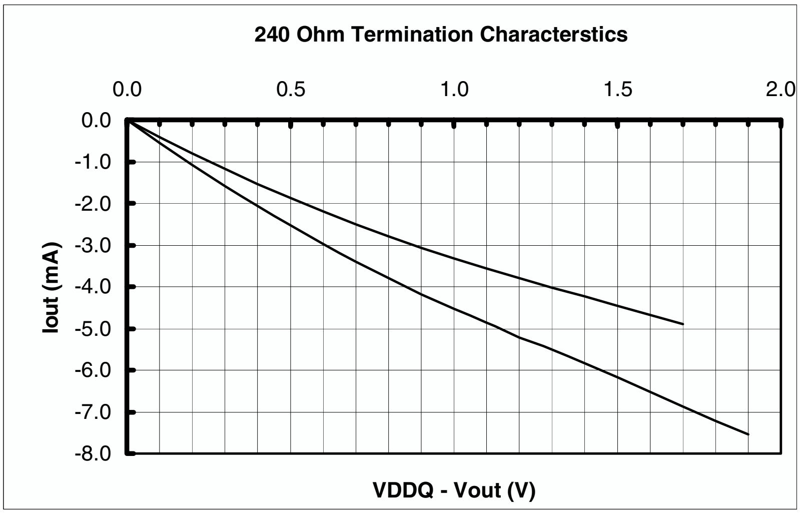

Figure 57 240 Ohm Active Termination Characteristic

Table 40 lists the numerical values of the minimum and maximum allowed values of the ADD/CMD termination IV characteristic.

Table 40 Programmed Terminator Characterisitc at 240 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
				1.0	-3.32	-4.53
0.1	-0.41	-0.55		1.1	-3.56	-4.86
0.2	-0.80	-1.07		1.2	-3.79	-5.21
0.3	-1.17	-1.58		1.3	-4.01	-5.50
0.4	-1.53	-2.06		1.4	-4.23	-5.83
0.5	-1.87	-2.53		1.5	-4.46	-6.17
0.6	-2.20	-2.97		1.6	-4.68	-6.52
0.7	-2.50	-3.40		1.7	-4.90	-6.88
0.8	-2.79	-3.80		1.8	-	-7.21
0.9	-3.06	-4.17		1.9	-	-7.54

4.11 Operating Currents

4.11.1 Operating Current Ratings

(0°C ≤ T_C ≤ +85°C, V_{DD} = +2.0 V ± 0.10 V, V_{DDQ} = +2.0 V ± 0.10 V, see **Table 1**)

Table 41 Operating Current Ratings

Parameter	Symbol	–1.6	–2.0	–2.2	Unit	Notes
		typ.	typ.	typ.		
Operating Current	I_{DD0}	274	238	222	mA	1)2)3)
Operating Current	I_{DD1}	297	258	241	mA	1)2)3)
Precharge Power-Down Standby Current	I_{DD2P}	99	86	81	mA	1)2)3)
Precharge Floating Standby Current	I_{DD2F}	156	136	127	mA	1)2)3)
Precharge Quiet Standby Current	I_{DD2Q}	113	98	92	mA	1)2)3)
Active Power-Down Standy Current	I_{DD3P}	99	86	81	mA	1)2)3)
Active Standby Current	I_{DD3N}	182	158	148	mA	1)2)3)
Operating Current Burst Read	I_{DD4R}	474	412	385	mA	1)2)3)
Operating Current Burst Write	I_{DD4W}	320	278	265	mA	1)2)3)
Auto-Refresh Current (t_{RC}=min(t_{RFC}))	I_{DD5B}	430	374	348	mA	1)2)3)
Auto-Refresh Current at t_{REFI}	I_{DD5D}	101	88	83	mA	1)2)3)
Self Refresh Current	I_{DD6}	11	11	11	mA	1)2)3)4)
Operating Current	I_{DD7}	630	548	509	mA	1)2)3)

1) *I_{DD} specifications are tested after the device is properly initialized.*
2) *Input slew rate = 2 V/ns.*
3) *Mesured with Output open and On Die termination off.*
4) *Enables on-chip refresh and address counter.*

4.12 Operating Current Measurement Conditions

(0°C ≤ T_C ≤ +85°C, V_{DD} = +2.0V ± 0.10 V, V_{DDQ} = +2.0 V ± 0.10 V, see **Table 1**)

Table 42 Operating Current Measurement Conditions

Symbol	Parameter/Condition
I_{DD0}	Operating Current - One bank, Activate - Precharge t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}) Databus inputs are SWITCHING; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands.
I_{DD1}	Operating Current - One bank, Activate - Read - Precharge One bank is accessed with t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}), CL = CL(min), Address and control inputs are SWITCHING; $\overline{CS}$ = HIGH between valid commands. I_{out}=0mA
I_{DD2P}	Precharge Power-Down Standby Current All banks idle, power-down mode, CKE is LOW, t_{CK}=min(t_{CK}), Data bus inputs are STABLE.
I_{DD2F}	Precharge Floating Standby Current All banks idle; $\overline{CS}$ is LOW, CKE is HIGH, t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus input are STABLE.

Table 42 Operating Current Measurement Conditions

Symbol	Parameter/Condition
I_{DD2Q}	Precharge Quiet Standby Current $\overline{CS}$ is HIGH, all banks idle, CKE is HIGH, t_{CK}=min(t_{CK}), Address and other control inputs STABLE, Data bus inputs are STABLE.
I_{DD3P}	Active Power-Down Standby Current All banks active, CKE is LOW, Address and control inputs are STABLE; Data bus inputs are STABLE; standard active power-down mode.
I_{DD3N}	Active Standby Current All banks active, $\overline{CS}$ is HIGH, CKE is HIGH, t_{RC}=max(t_{RAS}), t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING; I_{out} = 0 mA.
I_{DD4R}	Operating Current - Burst Read All banks active; Continuous read bursts, CL = CL(min); tCK=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD4W}	Operating Current - Burst Write All banks active; Continuous write bursts; t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5B}	Burst Auto Refresh Current Refresh command at t_{RC}=min(t_{RFC}); t_{CK}=min(t_{CK}); CKE is HIGH, $\overline{CS}$ is HIGH between all valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5D}	Distributed Auto Refresh Current tCK=tCKmin; Refresh command every tREFI; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD6}	Self Refresh Current CKE ≤ max(V_{IL}), external clock off, CK and $\overline{CK}$ LOW; Address and control inputs are STABLE; Data Bus inputs are STABLE.
I_{DD7}	Operating Bank Interleave Read Current 1. All banks interleaving with CL = CL(min); tRCD = tRCDRD(min); tRRD = tRRD(min); Iout=0mA; Address and control inputs are STABLE during DESELECT; Data bus inputs are SWITCHING. 2: Timing pattern: -1.6 (600 MHz, CL=7) : t_{CK} = 2.5ns, t_{RCDRD} = 7. t_{CK}; t_{RRD} = 4. t_{CK}; t_{RC} = 18. t_{CK} Read: A0 RA3 D D A1 D D RA0 A2 D D RA1 A3 D D RA2 D D TBD TBD TBD -2.0 (500 MHz, CL7) : t_{CK} = 2.0ns, t_{RCDRD} = 7. t_{CK}; t_{RRD} = 4. t_{CK}; t_{RC} = 18. t_{CK} Read: A0 RA3 D D A1 D D RA0 A2 D D RA1 A3 D D RA2 D D -2.2 (455 MHz, CL6) : t_{CK} = 2.2ns, t_{RCDRD} = 7. t_{CK}; t_{RRD} = 4. t_{CK}; t_{RC} = 18. t_{CK} Read: A0 RA3 D D A1 D D RA0 A2 D D RA1 A3 D D RA2 D D

1. *Data Bus consists of DQ, DM, WDQS*
2. *Definitions for IDD : LOW is defined as VIN = 0.4 x V_{DDQ}; HIGH is defined as V_{IN} = V_{DDQ};*
   STABLE is defined as inputs are stable at a HIGH level.
   SWITCHING is defined as inputs are changing between HIGH and LOW every clock cycle for address and control signals, and inputs changing 50% of each data transfer for DQ signals.
3. *Legend : A=Activate, RA=Read with Autoprecharge, D=DESELECT*

4.13 Summary of timing parameters for –1.6, –2.0 and –2.2 ns speed sorts in DLL on mode

Table 43 Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Read latency	Sym-bol	Limit Values						Unit	Notes
			–1.6		–2.0		–2.2			
			min	max	min	max	min	max		
Clock and Clock Enable										
Clock Cycle Time	7	t_{CK7}	1.6	3.3	2.0	4.0	2.2	4.0	ns	
	6	t_{CK6}	2.0	3.3	2.0	4.0	2.2	4.0	ns	
	5	t_{CK5}	—	—	—	—	2.7	4.0	ns	
System frequency	7	f_{CK7}	300	600	250	500	250	455	MHz	
	6	f_{CK6}	300	500	250	500	250	455	MHz	
	5	f_{CK5}	—	—	—	—	250	370	MHz	
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Minimum clock half period		t_{HP}	0.45	—	0.45	—	0.45	—	t_{CK}	1)
Command and Address Setup and Hold Timing										
Address/Command input setup time		t_{IS}	0.6	—	0.75	—	0.75	—	ns	
Address/Command input hold time		t_{IH}	0.6	—	0.75	—	0.75	—	ns	
Address/Command input pulse width		t_{IPW}	0.85	—	0.85	—	0.85	—	t_{CK}	
Mode Register Set Timing										
Mode Register Set cycle time		t_{MRD}	5	—	4	—	4	—	t_{CK}	
Mode Register Set to READ timing		t_{MRDR}	15	—	12	—	12	—	t_{CK}	
Row Timing										
Row Cycle Time		t_{RC}	37.2	—	37.2	—	39.6	—	ns	
Row Active Time		t_{RAS}	24.0	8 x t_{REFI}	24.0	8 x t_{REFI}	26.2	8 x t_{REFI}	ns	
ACT(a) to ACT(b) Command period		t_{RRD}	8.0	—	8.0	—	8.8	—	ns	
Row Precharge Time		t_{RP}	13.2	—	13.2	–	13.2	–	ns	
Row to Column Delay Time for Reads		t_{RCDRD}	16.0	—	16.0	–	17.5	–	ns	
Row to Column Delay Time for Writes		t_{RCDWR}	$t_{RCDWR(min)} = t_{RCDRD(min)}$ - (WL + 1) x $t_{CK(min)}$						ns	
Column Timing										
CAS(a) to CAS(b) Command period		t_{CCD}	2	—	2	—	2	—	t_{CK}	2)
Write to Read Command Delay		t_{WTR}	6.0	—	6.0	—	6.6	—	ns	3)
Read to Write command delay		t_{RTW}	t_{RTW}(min)= (CL+4-WL)						t_{CK}	4)
Write Cycle Timing Parameters for Data and Data Strobe										
Write command to first WDQS latching transition		t_{DQSS}	WL - 0.25	WL +0.25	WL - 0.25	WL +0.25	WL - 0.25	WL +0.25	t_{CK}	
Data-in and Data Mask to WDQS Setup Time		t_{DS}	0.35	—	0.375	—	0.375	—	ns	

Table 43 Timing Parameters for –1.6, –2.0 and –2.2 speed sorts

Parameter	Read latency	Symbol	Limit Values						Unit	Notes
			–1.6		–2.0		–2.2			
			min	max	min	max	min	max		
Data-in and Data Mask to WDQS Hold Time		t_{DH}	0.35	—	0.375	—	0.375	—	ns	
Data-in and DM input pulse width (each input)		t_{DIPW}	0.45	—	0.45	—	0.45	—	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.45	—	0.45	—	0.45	—	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.45	—	0.45	—	0.45	—	t_{CK}	
DQS Write Preamble Time		t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS Write Postamble Time		t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write Recovery Time		t_{WR}	11.0	—	11.0	—	11.0	—	ns	3
Read Cycle Timing Parameters for Data and Data Strobe										
Data Access Time from Clock		t_{AC}	–0.4	0.4	–0.4	0.4	–0.45	0.45	ns	
Read Preamble		t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Read Postamble		t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK		t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
Data-out low impedance time from CLK		t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
DQS edge to Clock edge skew		t_{DQSCK}	–0.4	0.4	–0.4	0.4	–0.45	0.45	ns	
DQS edge to output data edge skew		t_{DQSQ}	—	0.225	—	0.225	—	0.25	ns	
Data hold skew factor		t_{QHS}	0	0.225	0	0.225	0	0.25	ns	
Data output hold time from DQS		t_{QH}	$t_{HP}–t_{QHS}$		$t_{HP}–t_{QHS}$		$t_{HP}–t_{QHS}$		ns	
Refresh/Power Down Timing										
Refresh Period (4096 cycles)		t_{REF}	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval		t_{REFI}	7.8		7.8		7.8		µs	
Delay from AREF to next ACT/ AREF		t_{RFC}	54	—	54	—	54	—	ns	
Self Refresh Exit time		t_{XSC}	200	—	200	—	200	—	t_{CK}	
Precharge Power Down Exit time		t_{XPN}	5	—	4	—	4	—	t_{CK}	
Active Power Down Exit time		t_{XARD}	8	—	6	—	6	—	t_{CK}	
Other Timing Parameters										
RES to CKE setup timing		t_{ATS}	10	—	10	—	10	—	ns	
RES to CKE hold timing		t_{ATH}	10	—	10	—	10	—	ns	
Termination update Keep Out timing		t_{KO}	10	—	10	—	10	—	ns	
Rev. ID EMRS to DQ on timing		t_{RIDon}	—	20	—	20	—	20	ns	
Rev. ID EMRS to DQ off timing		t_{RIDoff}	—	20	—	20	—	20	ns	

1) *t_{HP} is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK, $\overline{CLK}$ inputs*

2) *t_{CCD} is either for gapless consecutive reads or gapless consecutive writes.*

3) *t_{WTR} and t_{WR} start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQS signal.*

4) *Please round up t_{RTW} to the next integer of t_{CK}.*

4.14 AC Characteristics and Settings

The following tables are meant as a guideline to correctly set the most important timing parameters depending on speed sort and clock frequency.

Table 44 HYB18T256324F–16

Frequency / t_{CK}	CAS Latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{RCDRD}	t_{RCDWR}	Unit
600 MHz / 1.6ns	7	23	33	15	8	7	5	10	7	t_{CK}
500 MHz / 2.0ns	7	19	27	12	7	6	4	8	6	t_{CK}
455 MHz / 2.2ns	7	17	25	11	6	5	4	8	6	t_{CK}
400 MHz / 2.5ns	6	15	22	10	6	5	4	7	5	t_{CK}
370 MHz / 2.7ns	6	14	20	9	5	5	3	6	5	t_{CK}
300 MHz / 3.0ns	6	12	17	8	4	4	3	5	4	t_{CK}

Table 45 HYB18T256324F–20

Frequency / t_{CK}	CAS Latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{RCDRD}	t_{RCDWR}	Unit
500 MHz / 2.0ns	7	19	27	12	7	6	4	8	5	t_{CK}
455 MHz / 2.2ns	7,6	17	25	11	6	5	4	8	5	t_{CK}
400 MHz / 2.5ns	7,6	15	22	10	6	5	4	7	4	t_{CK}
370 MHz / 2.7ns	6	14	20	9	5	5	3	6	4	t_{CK}
300 MHz / 3.0ns	6	12	17	8	4	4	3	5	3	t_{CK}

Table 46 HYB18T256324F–22

Frequency / t_{CK}	CAS Latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{RCDRD}	t_{RCDWR}	Unit
455 MHz / 2.2ns	7	18	25	12	6	5	4	8	5	t_{CK}
400 MHz / 2.5ns	7,6	16	22	11	6	5	4	7	5	t_{CK}
370 MHz / 2.7ns	7,6	15	20	10	5	5	4	7	4	t_{CK}
300 MHz / 3.0ns	5	12	17	8	4	4	3	6	4	t_{CK}
266 MHz / 3.8ns	5	11	15	7	4	3	3	5	3	t_{CK}
250MHZ / 4.0ns	5	10	14	7	4	3	3	5	3	t_{CK}

5 Package Outlines

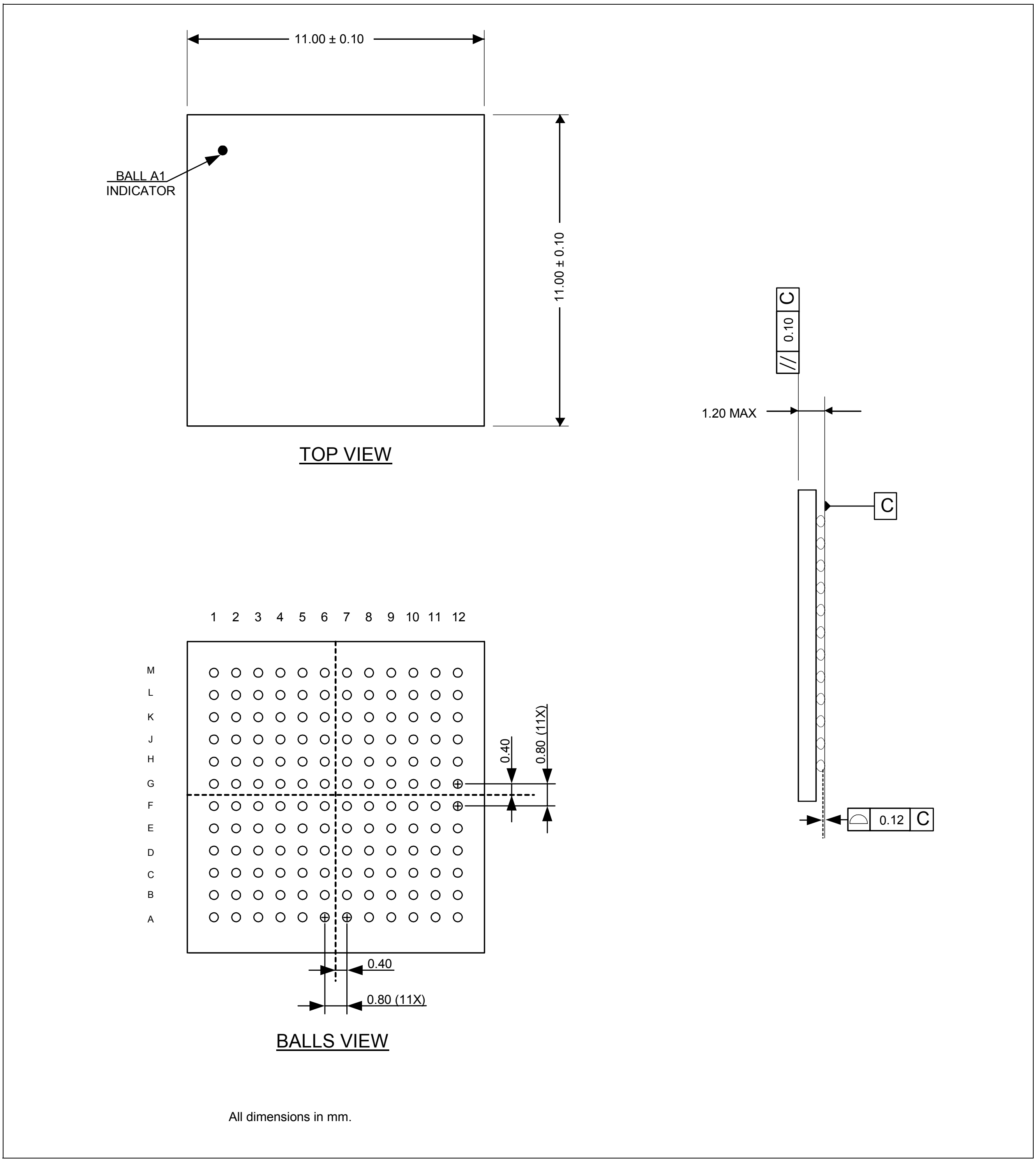

Figure 58 Package Outline FBGA

1. *The package is conforming with JEDEC MO216*
2. *The inner matrix of 4x4 balls is reserved for thermal contacts*

5.1 Package Thermal Characteristics

Table 47 P-FBGA 144 Package Thermal Resitances

	Theta_jA						**Theta_jB**	**Theta_jC**
JEDEC Board	1s0p			2s0p				
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	-	-
K/W	48.8	40.2	35.1	27.0	23.5	22.0	6.0	3.9

1. *Theta_jA : Junction to Ambient thermal resistance. The values have been obtained by simulation using the conditions stated in the JEDEC JESD-51 standard.*
2. *Theta_jB : Junction to Board thermal resistance. The value has been obtained by simulation.*
3. *Theta_jC : Junction to Case thermal resistance. The value has been obtainned by simulation.*

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