

#### Ordering Information

MFR62320A-JO	MPO/MTP Connector
MFR62320A-JX	MPX Connector

#### Applications

- High-speed interconnects within and between Switches, Routers and Transport equipment
- Proprietary backplanes
- Low cost OC-192 VSR (Very Short Reach) connections
- InfiniBand™ connections
- Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

#### Features

- Data rate 155Mbps to 2.5Gbps per channel
- 4 parallel channels, total 10Gbps capacity
- Differential CML (Current-Mode Logic) interface
- Link length up to 300m (with 500MHz·km fiber)
- Channel BER  $10^{-12}$  when used with MFT62320A-J
- Designed for multimode fiber ribbon
- MPO/MTP or MPX connector options
- Surface-mount package
- Pick-and-placeable; reflow solderable
- Matches the MFT62320A-J Transmitter

#### Description

The MFT62320A-J and MFR62320A-J make a very high speed transmitter and receiver pair for parallel fiber applications. This pair, coupled through a multimode parallel fiber ribbon cable, constitutes a complete parallel fiber link. These links provide high-speed interconnects for use within and between large capacity switches, routers and data transport equipment. The transmitter and receiver have a differential CML interface and support MPO/MTP and MPX fiber connectors.

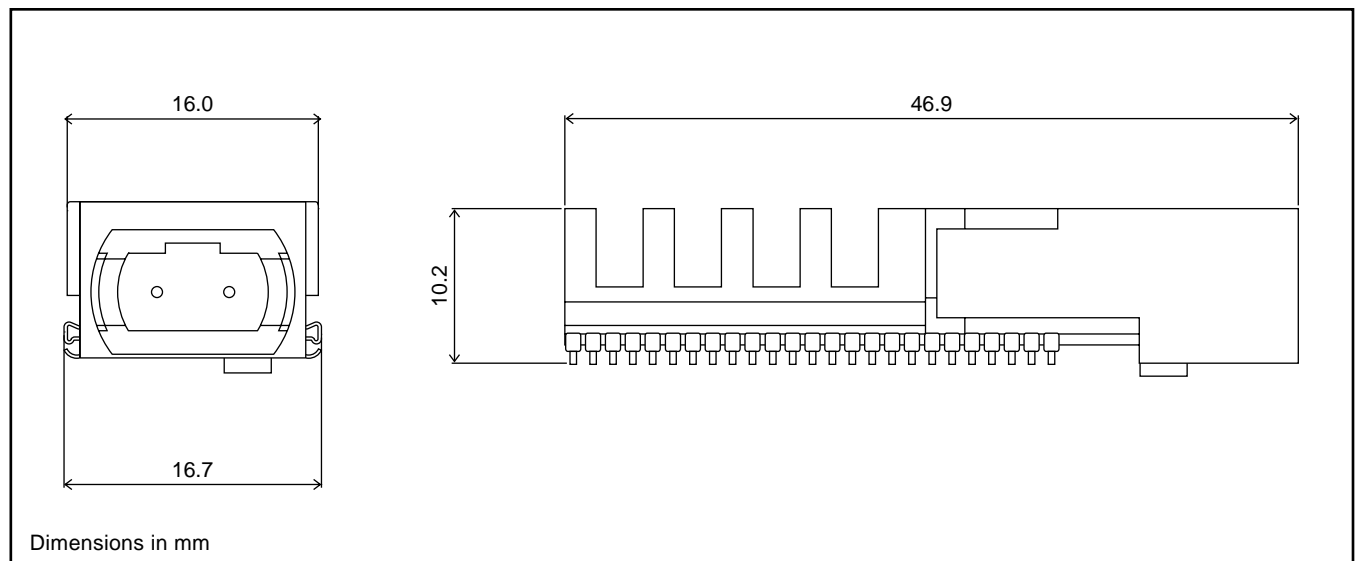


Figure 1 - MFR62320A-JO: MPO/MTP Connector Option

## Absolute Maximum Ratings (note 1)

	Parameter	Symbol	Min	Max	Unit
1	Supply voltage	$V_{CC}$	-0.5	4.0	V
2	Voltage on any pin	$V_{PIN}$	-0.5	$V_{CC}+0.3$	V
3	Operating and storage moisture	$M_{OS}$	20	85	%
4	Storage temperature	$T_{STG}$	-40	+100	°C
5	ESD resistance all I/O (note 2)	$V_E$	-400	400	V

## Recommended Operating Conditions (note 3)

	Parameter	Symbol	Min	Max	Unit
1	Case temperature (note 4, fig. 6)	$T_{CASE}$	0	80	°C
2	Supply voltage (note 5)	$V_{CC}$	3.3-5%	3.3+5%	V
3	Data rate per channel	$f_D$	0.155	2.5	Gbps
4	Optical wavelength	$\lambda$	830	860	nm
5	CML differential load impedance (Fig. 4)	$Z_O$	80	120	$\Omega$
6	Power supply noise (1MHz to 2GHz)	$V_{NPS}$		100	$mV_{p-p}$

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Note 2: Human body model.

Note 3: Data patterns are to have maximum run lengths and DC balance shifts no worse than those of a Pseudo Random Bit Sequence of length  $2^{23}-1$  (PRBS-23).

Note 4: An air flow parallel to the PCB, and parallel with the module's heatsink flanges, is recommended. See figure 6 for information about ambient temperature vs. air flow.

Note 5: The heat sink of the module is at  $V_{CC}$  potential. To prevent accidental short circuit to any other component in the system, each module is supplied with an adhesive thermally conductive strip attached to the top of the heat sink.

**Characteristics** (note 1)

	Parameter	Symbol	Min	Typ	Max	Unit	
1	Power consumption (0.155 to 2.5 Gbps)	$P_D$			0.8	W	
2	Power supply current	$I_{CC}$			253	mA	
3	Saturation (average power)	$P_{SAT}$	-3			dBm	
4	Sensitivity (note 2)	$P_{S12}$			-15	dBm	
5	Stressed receiver sensitivity (note 3)	$P_{SS}$			-10.1	dBm	
6	Stressed receiver eye opening (note 4)	$P_{SE}$	108			ps	
7	Jitter	Total (note 5)	$T_J$		153	ps <sub>p-p</sub>	
8	Contribution	Deterministic (note 6)	$D_J$		46	ps <sub>p-p</sub>	
9	CML differential output rise/fall time (20-80%, Fig. 5)		$t_{RC}, t_{FC}$		160	ps	
10	CML differential output voltage (Fig. 3,4,5)		$V_{OCML}$	250	350	450	mV
11	CML differential output reflection coefficient		$S_{22}$		-5	dB	
12	Channel skew (note 7)		$t_{SK}$		175	ps	
13	Return Loss (note 9)		RL	12		dB	
14	NMOS output voltage	Low ( $I_{sink} = 3mA$ )	$V_{LNMOS}$		0.4	V	
15		High	$V_{HNMOS}$	2.4		V	
16	Receiver Signal Detect (RX_SD) (note 8)	Assert level	$P_{AS}$		-15.5	dBm	
17		De-assert level	$P_{DS}$	-31		dBm	
18		Hysteresis	$P_{AS}-P_{DS}$	0.5		dBm	
19		Assert time (fig. 7)	$T_{AS}$		10	μs	
20		De-assert time (fig. 7)	$T_{DS}$		10	μs	

Note 1: Operating conditions are as per Recommended Operating Conditions. Test pattern PRBS-23 at 2.5Gbps with 50/125μm fiber, unless otherwise specified.

Note 2: Sensitivity for a channel (as defined in IEEE 802.3z Gigabit Ethernet) is specified at a BER of  $10^{-12}$  using a fast rise/fall time source with low RIN and Extinction Ratio not less than 6 dB. All channels not under test are receiving signals with an average input power of 6 dB, or higher, above worst case sensitivity.

Note 3: The stressed receiver sensitivity is measured using 2.4 dB Inter-Symbol Interference, ISI, (min), 33 ps Duty Cycle Dependent Deterministic Jitter, DCD DJ (min) and 6 dB ER (ER Penalty = 2.2 dB). All channels not under test are receiving signals with an average input power of 6 dB, or higher, above worst case sensitivity.

Note 4: The stressed receiver eye opening represents the eye at TP4 as defined in IEEE 802.3z Gigabit Ethernet Specification 38.5. The stressed receiver eye opening is measured using 2.4 dB ISI (min), 33 ps DCD DJ (min), 6 dB ER (ER Penalty = 2.2 dB) and an average input optical power of -9.6 dBm (0.5 dB above Minimum Stressed Receiver Sensitivity as defined in IEEE 802.3z Gigabit Ethernet Specification Section 38.5). All channels not under test are receiving signals with an average input power of 6 dB, or higher, above worst case sensitivity.

Note 5: Total Jitter,  $T_J$ , equals  $TP3$  to  $TP4$  as defined in IEEE 802.3z Gigabit Ethernet Specification 38.5. Total jitter is specified at a BER of  $10^{-12}$  ( $T_J = DJ + RJ_{rms} \times 2Q$ , where  $Q=7$  for BER  $10^{-12}$  and  $RJ$ =Random Jitter).

Note 6: Deterministic jitter includes duty cycle distortion.

Note 7: Electrical channel skew is measured with the input signals having equal amplitude and no input optical channel skew.

Note 8: All channels not under test are receiving signals with an average input power of 6 dB, or higher, above the channel under test.

Note 9: Return loss is the ratio between received optical power and optical power reflected back into the fiber.

## Cleaning the Optical Interface

A protective connector plug is supplied with each module. This plug should remain in place prior to use, and be re-attached whenever a fiber cable is not inserted. This will keep the optical interface free from dust or other contaminants, which may potentially degrade the optical signal. Before re-attaching the connector plug to the module, visually inspect the plug and remove any contamination. If the optical interface becomes contaminated, it can be cleaned with high-pressure nitrogen. Liquids or physical contact with the optical interface are not advised due to potential damage.

## Assembly on Printed Circuit Board

The module can be soldered by hand or by a reflow process.

- For hand soldering, a soldering iron with its tip connected to ground should be used. Solder extractors, including replacement parts, should be of the non-static generating type.
- For reflow soldering, the recommendations advised by Zarlink in the technical note "MFTN6005A Manufacturing Guidelines" should be followed. This document provides guidelines about choice of solder, reflow temperature and time profile etc.

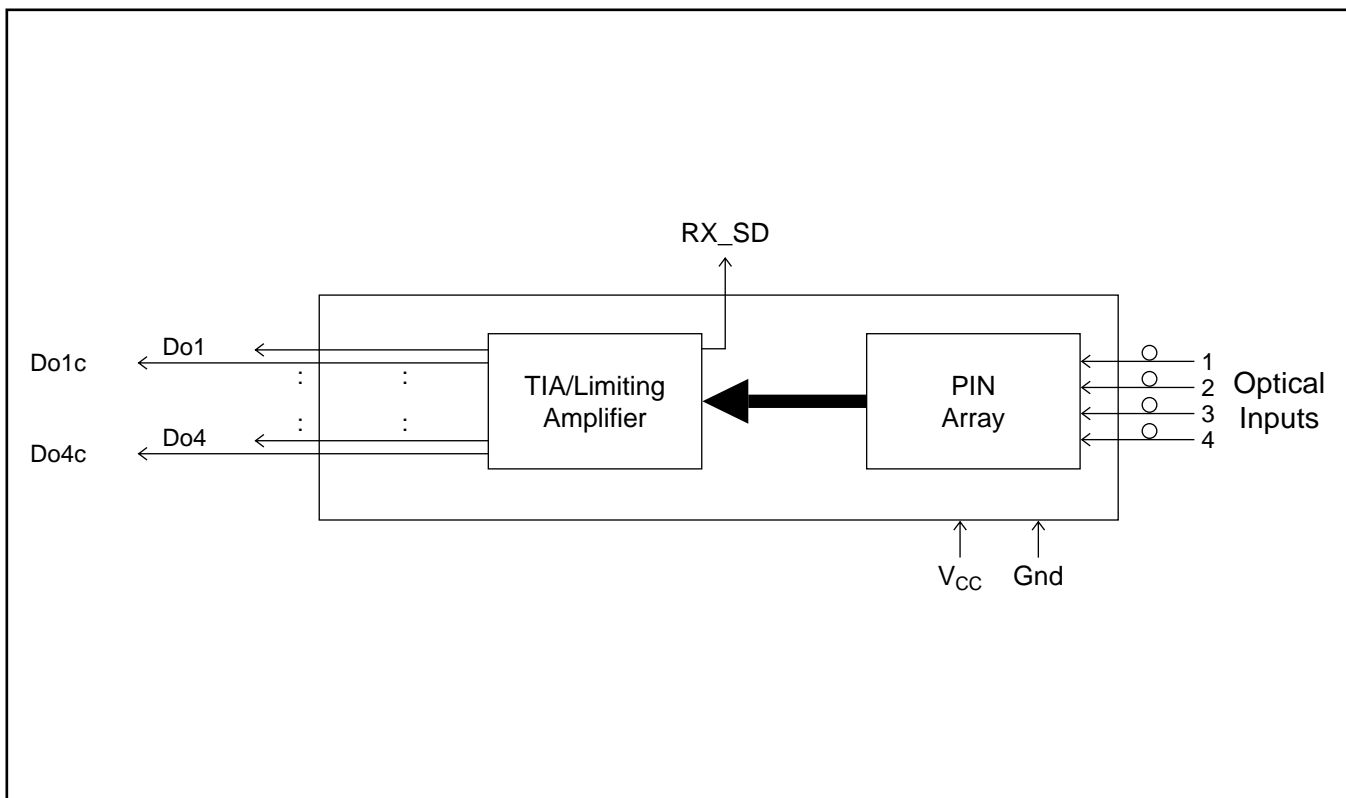
Use of solder with no-clean flux, i.e. solder that does not require washing after assembly, is recommended. Washing the module with any kind of liquid is not advised due to potential damage.

## Electrostatic Discharge (ESD)

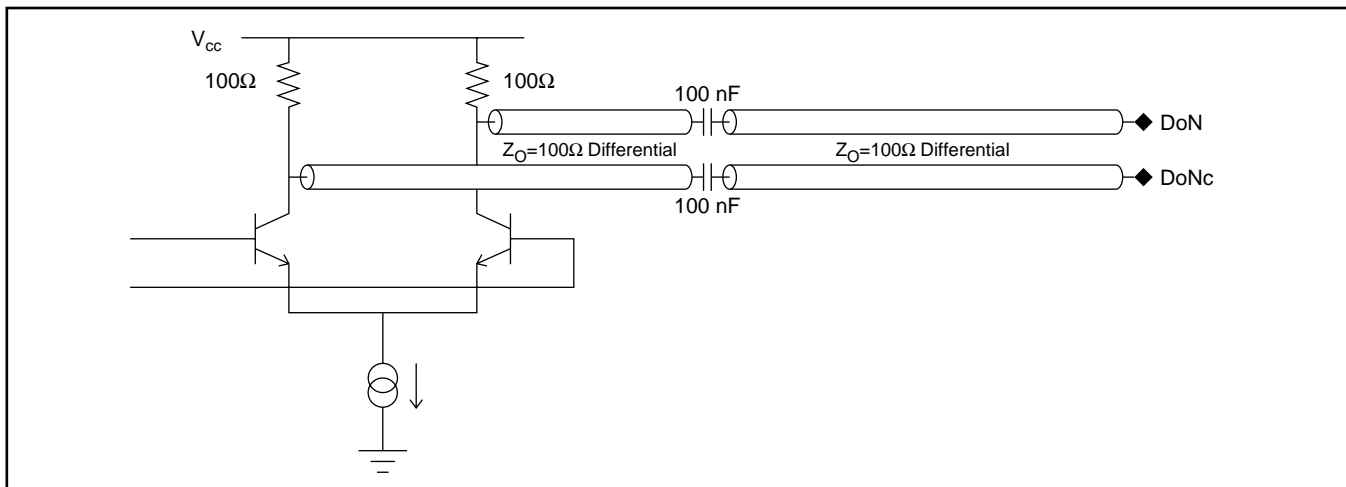
The module is classified as Class 1 according to MIL-STD-883, test method 3015. When handling the modules, precautions for ESD sensitive devices should be taken. These precautions include use of ESD protected work areas with wrist straps, controlled work benches, floors etc. The recommendations advised by Zarlink in the technical note "MFTN6005A Manufacturing Guidelines" should be followed.

## Electromagnetic Interference (EMI)

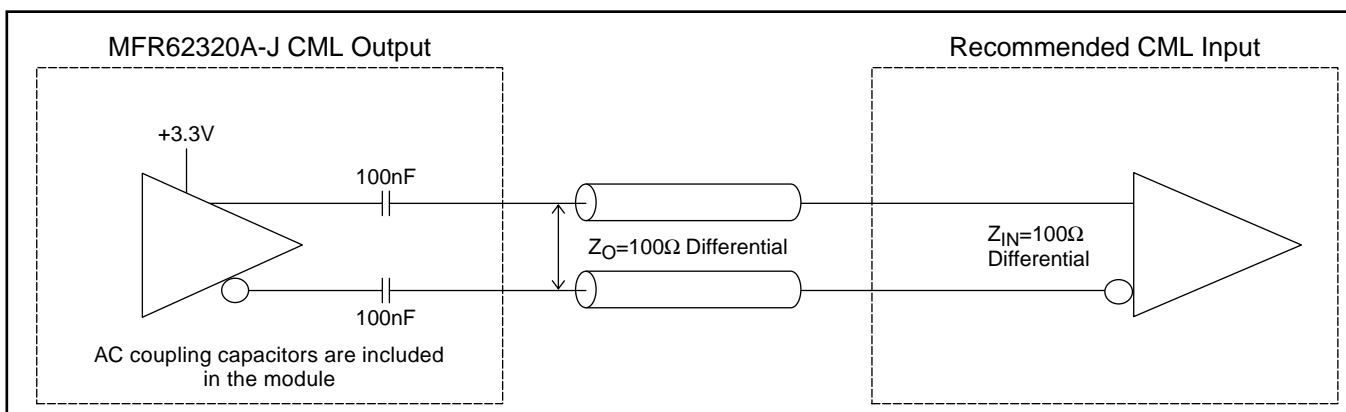
- Emission: The electromagnetic emission is tested in front of the module (module fitted with EMI shield "-JOS option"), with the module mounted in a front-panel cutout as shown in fig. 10. The specification is to FCC Class B with 6dB margin.
- Immunity: The electromagnetic immunity is tested without a front panel or enclosure. The module specification is maintained with an applied field of 10V/m for frequencies between 80MHz and 1GHz.



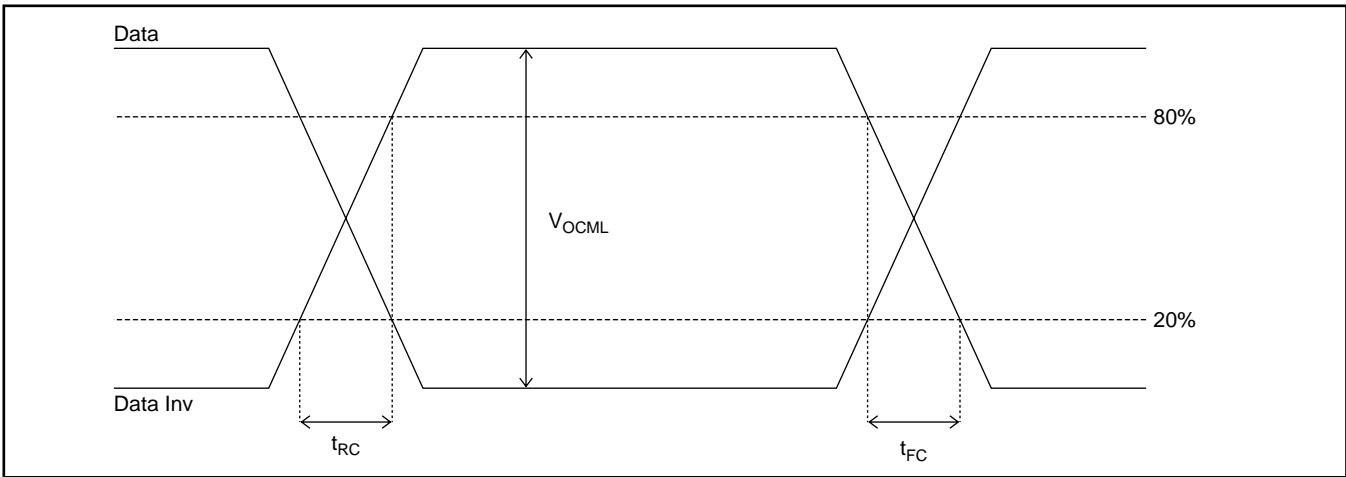
**Figure 2 - Block Diagram**



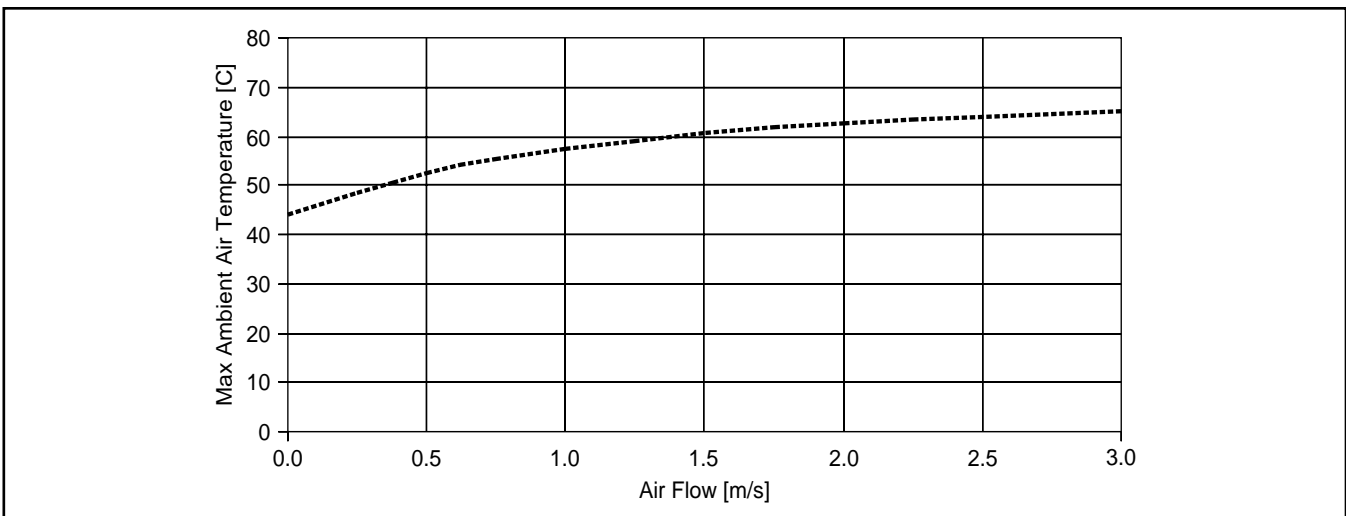
**Figure 3 - Data Output Equivalent Circuit**



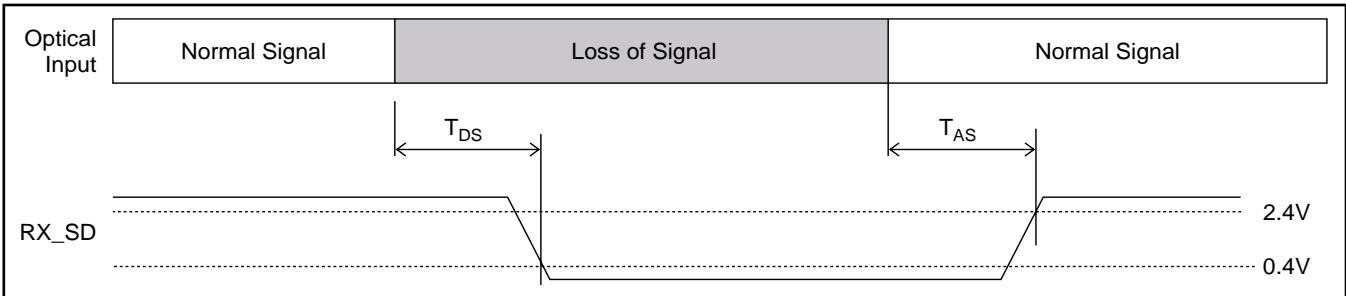
**Figure 4 - Differential CML Interface**



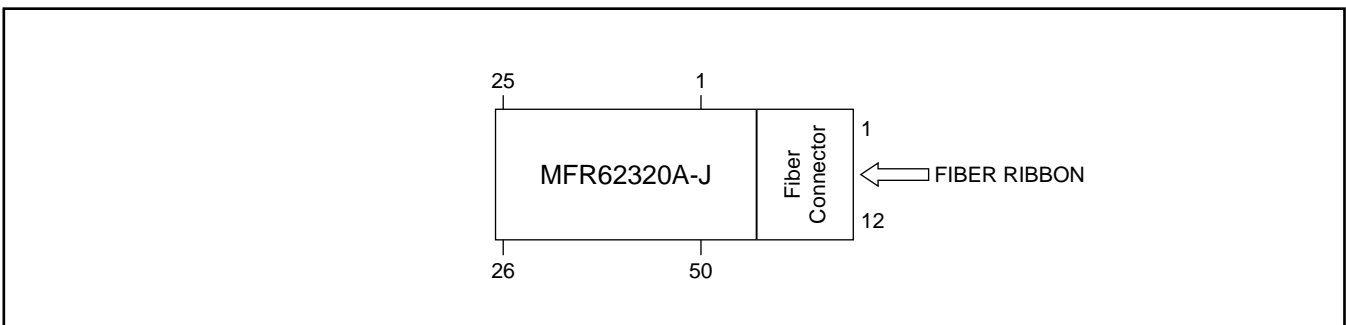
**Figure 5 - CML Differential Signals**



**Figure 6 - Max Air Temperature vs. Air Flow for Case Temperature Max 80°C**



**Figure 7 - Receiver Signal Detect Timing Diagram**



**Figure 8 - Pin Assignment (Top View)**

**Pin Description**

No	Name	Logic	Description
1	Gnd		Ground
2	V <sub>CC</sub>		Positive power supply
3	V <sub>CC</sub>		Positive power supply
4			Not Connected
5	RX_SD	NMOS	Receiver Signal Detect channels 1 and 4 (channels 2 and 3 are not monitored). High = Signal detected. Low = No signal detected. Open drain with internal pull-up resistor 40kΩ (note 1).
6			Not Connected
7	Gnd		Ground
8			Not Connected
9			Not Connected
10	Gnd		Ground
11			Not Connected
12			Not Connected
13	Gnd		Ground
14			Not Connected
15			Not Connected
16	Gnd		Ground
17			Not Connected
18			Not Connected
19	Gnd		Ground
20	Do1	CML	Data output No 1.
21	Do1c	CML	Data output No 1, inv.
22	Gnd		Ground
23	Do2	CML	Data output No 2.
24	Do2c	CML	Data output No 2, inv.
25	Gnd		Ground

No	Name	Logic	Description
50	Gnd		Ground
49	V <sub>CC</sub>		Positive power supply
48	V <sub>CC</sub>		Positive power supply
47			Not Connected
46			Not Connected
45			Not Connected
44	Gnd		Ground
43			Not Connected
42			Not Connected
41	Gnd		Ground
40			Not Connected
39			Not Connected
38	Gnd		Ground
37			Not Connected
36			Not Connected
35	Gnd		Ground
34			Not Connected
33			Not Connected
32	Gnd		Ground
31	Do4c	CML	Data output No 4, inv.
30	Do4	CML	Data output No 4.
29	Gnd		Ground
28	Do3c	CML	Data output No 3, inv.
27	Do3	CML	Data output No 3.
26	Gnd		Ground

Note 1: All RX\_SD pins may be tied together (wired OR) to create one Receiver Signal Detect (RX\_SD) output.

Mechanical Drawings

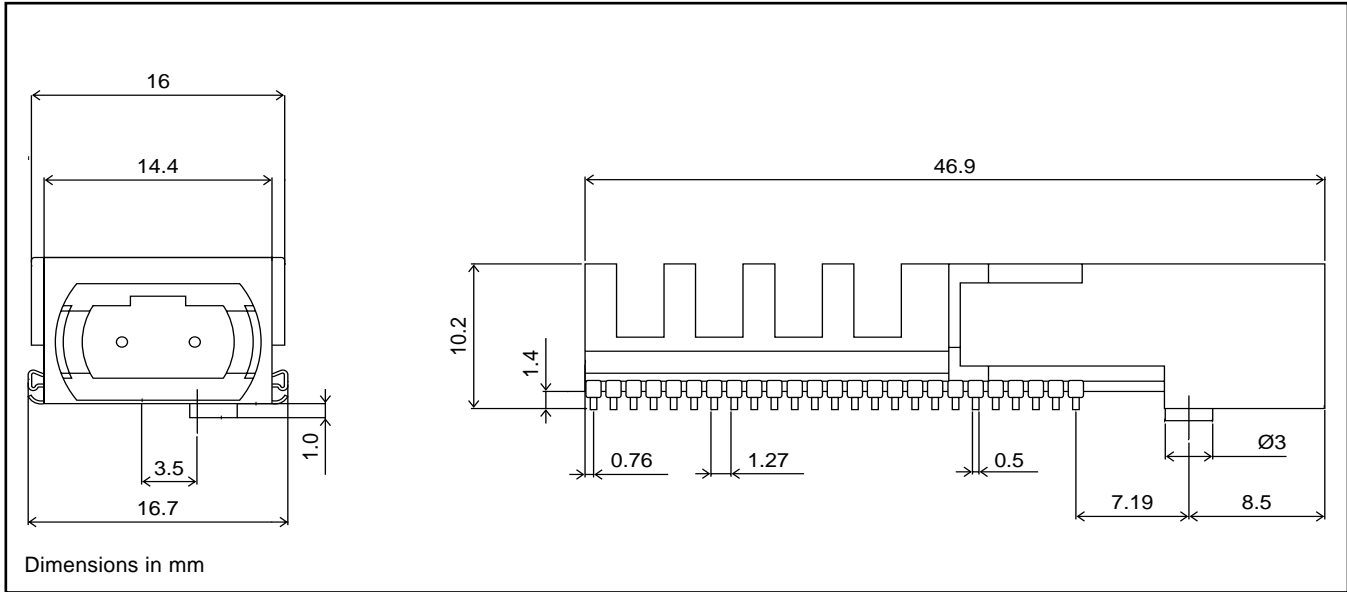


Figure 9 - MFR62320A-JO: MPO/MTP Connector Option

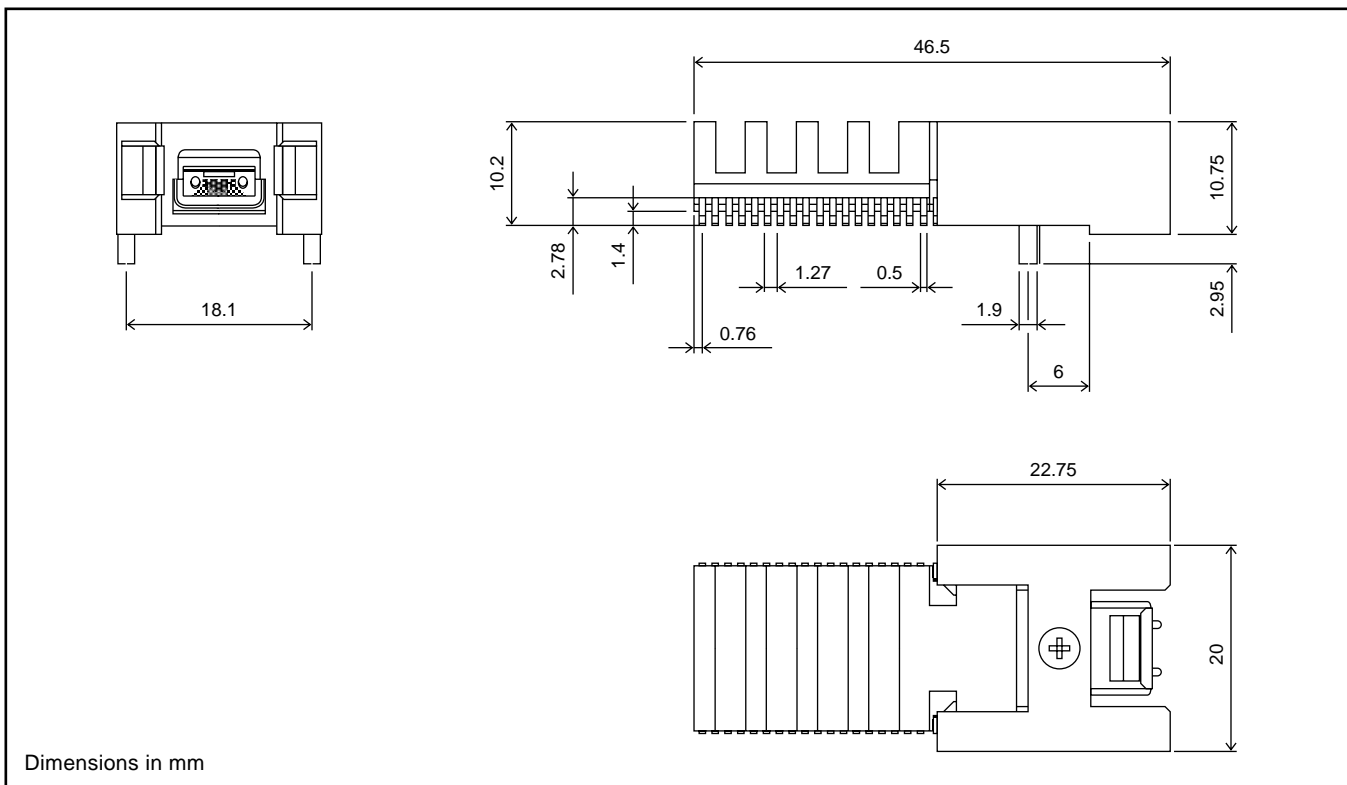
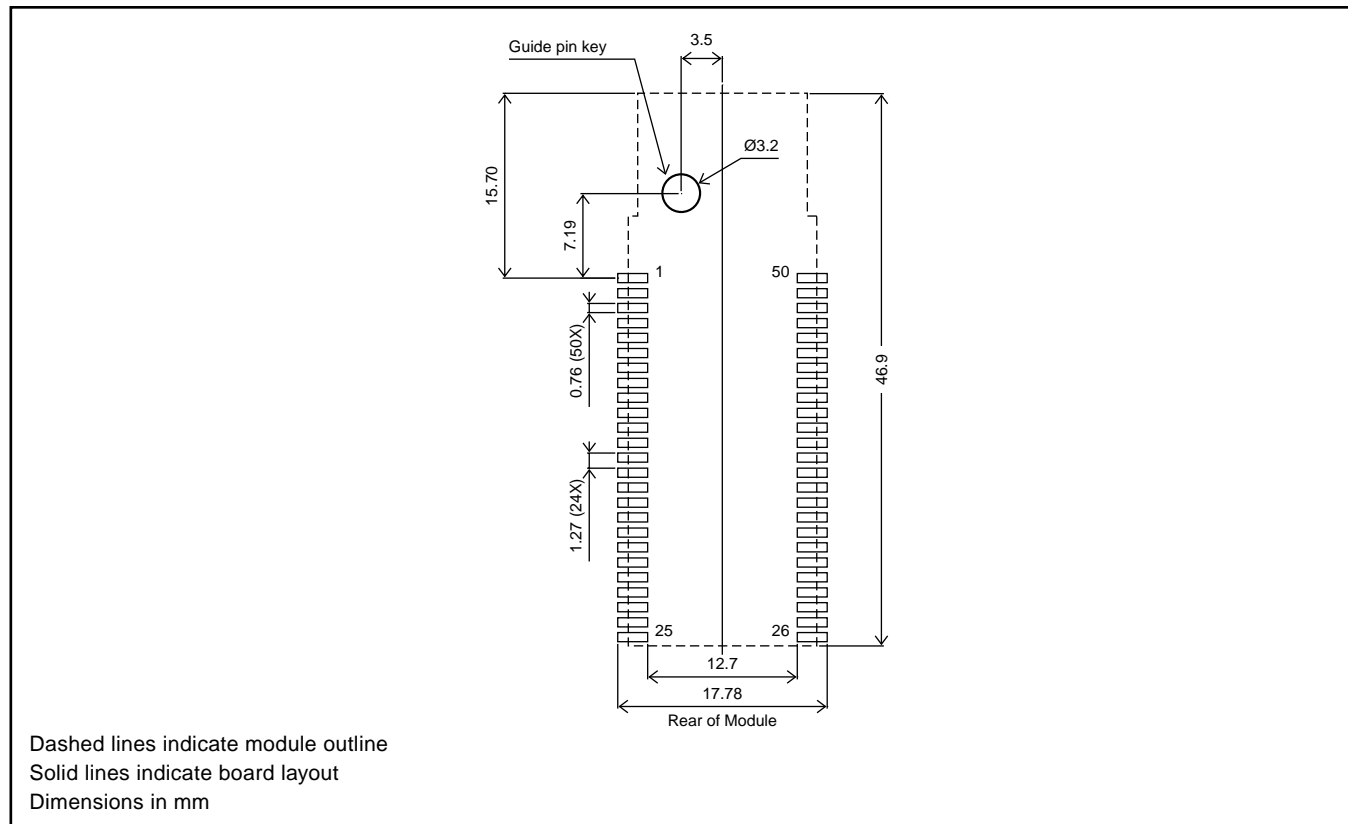
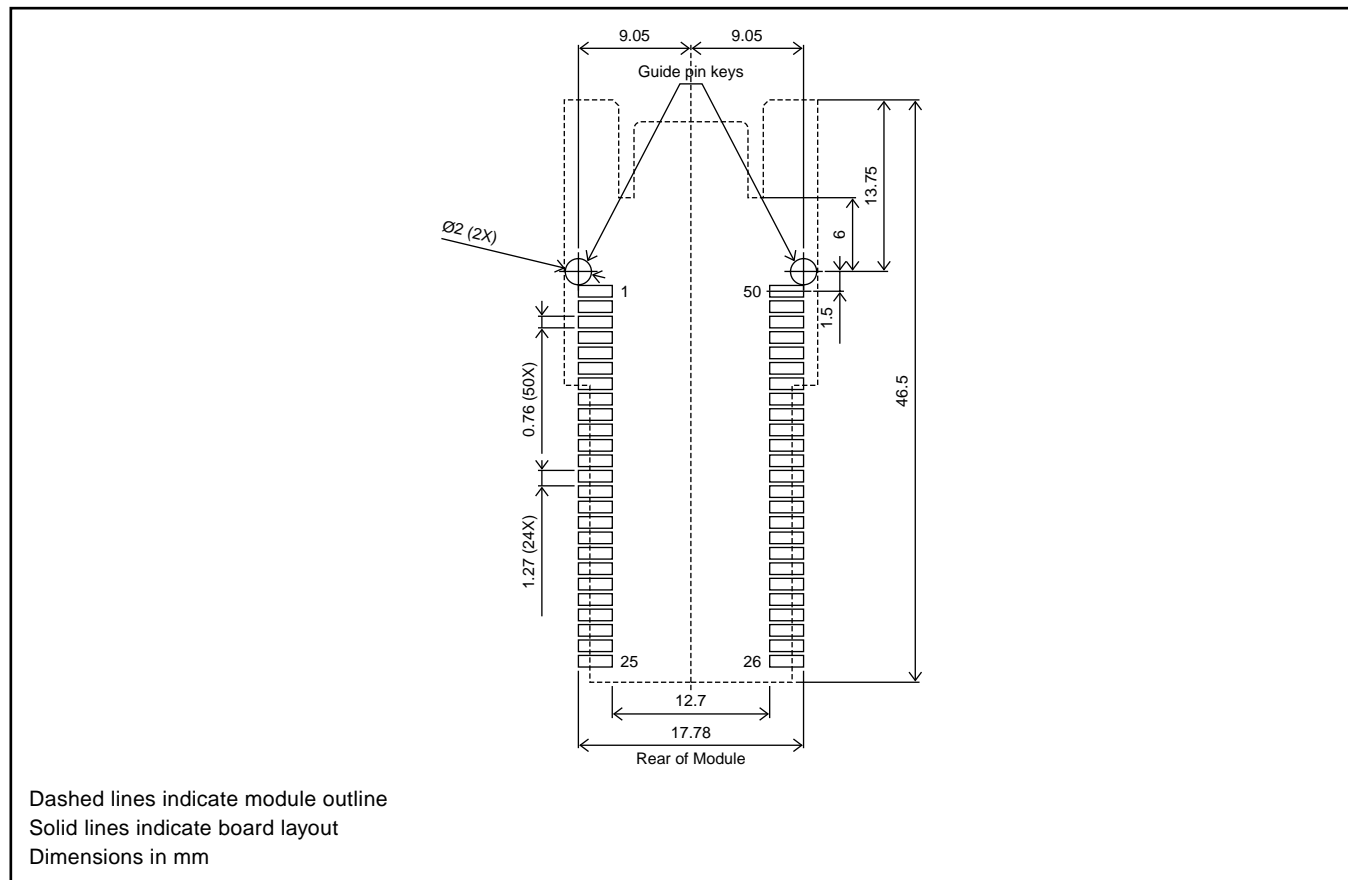


Figure 10 - MFR62320A-JX: MPX Connector Option

**PCB Footprints**

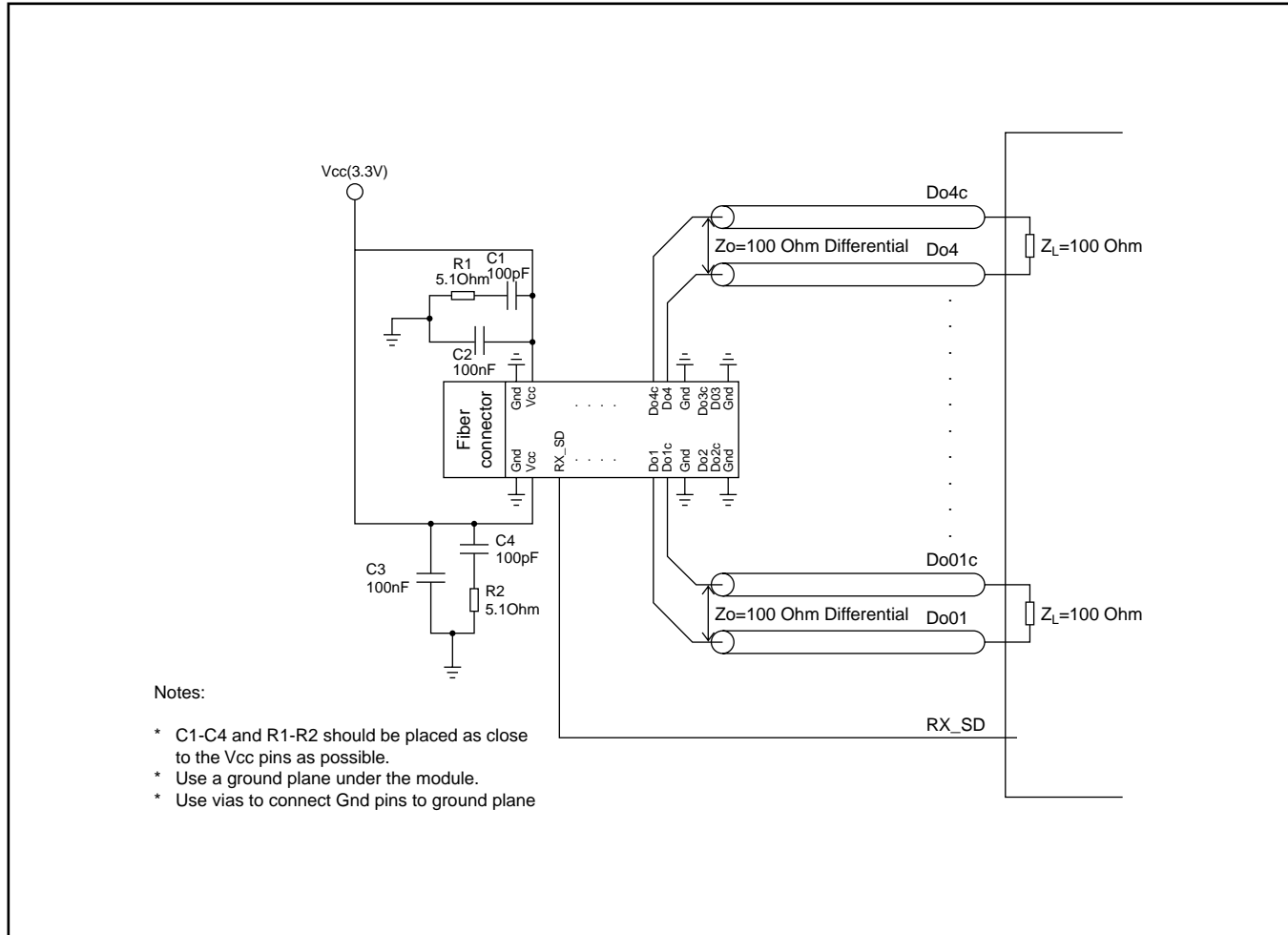


**Figure 11 - MFR62320A-JO: MPO/MTP Connector Option (Top View)**



**Figure 12 - MFR62320A-JX: MPX Connector Option (Top View)**

**Electrical Connections**



**Notes:**

- \* C1-C4 and R1-R2 should be placed as close to the Vcc pins as possible.
- \* Use a ground plane under the module.
- \* Use vias to connect Gnd pins to ground plane

**Figure 13 - Recommended Electrical Connections**



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