PRI 5610 – High Precision 26 Bit Analog/Digital Converter

The PRI 5610 is an integrating analog/digital converter of the highest precision class. Its resolution of 32 bits, its excellent significant precision of up to 26 bits, the easiness to adapt it to different hardware and to control it with a microprocessor make it the first choice whenever high linearity, resolution and conversion rate are required.

The microprocessor software controls the conversion time, the filter properties and the handling of error messages. The remaining nonlinearity of less than 0.1 ppm (type PRI 5610E) and the typical temperature coefficient of only 0.2 ppm/°C are some of the outstanding features of this highest precision device.

Among other applications, the PRI 5610 is most suitable for use in precision measuring and weighing, for data acquisition and in testing and calibrating systems.

Package: 28 lead ceramic package.

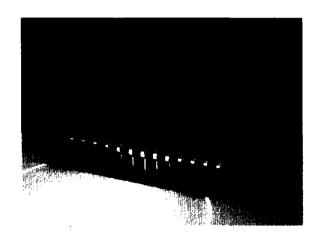
Three types with different nonlinearity class are available:

PRI 5610 E: max. 0,08 ppm
 PRI 5610 F: max. 0,2 ppm
 PRI 5610 G: max. 0,5 ppm

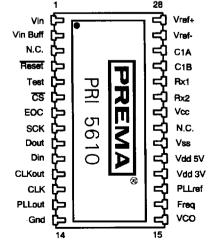
The **PRI 5610** already contains many functions that are needed in the system, thus saving many components on the board:

- freely programmable digital filter
- standardized serial interface
- FIFO for easy use in multitasking systems
- freely programmable underflow and overflow recognition
- provides a buffered input signal
- reference frequency of 50 Hz or 60 Hz and a digital phase and frequency discriminator for clocking with a phase-locked loop (PLL)

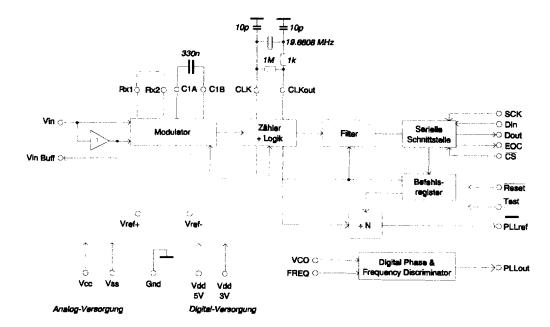
Two separated digital supply voltage inputs allow a low-loss 3V operation of the internal logic while input and output terminals remain compatible with the 5V TTL standard, but also allow operation with a single 5V supply voltage.



The range of the analog supply voltage depends on the maximum power loss allowed and the required input voltage.

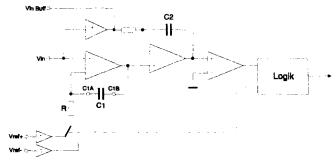


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The Multiple Ramp Method with 2nd Order Noise Shaping

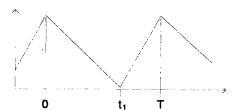
The conversion method used with the PRI 5610 is an improved version of the multiple ramp method developed and patented by PREMA. It provides an improved and faster convergence, improved filtering and lower temperature drift.



Modulator circuit

An amplifier which operates as integrator with the capacitor C_1 continuously integrates a current which is proportional to the input voltage V_{in} being measured. This procedure has inherent high linearity, because it does not require periodic switch of the input voltage. Errors dependent on the input level, as they are usually generated by voltage dependent semiconductor switching capacitances, do not occur in this case.

The capacitor C is periodically discharged by switching the reference voltage from V_{ref-} to V_{ref+} . During the discharge time the oscillator pulses are counted and continuously added up. The comparator detects when the integrator output signal passes zero during down integration.



Output voltage of integrator V_{int}

The zero pass defines the last counted clock pulse and effects the reference voltage to be switched back to reference voltage V_{ref}. The total change of charge on the capacitor during one measuring cycle is zero. Therefore

$$\frac{1}{\mathbf{R} \cdot \mathbf{C}} \int_{0}^{t_{1}} (\mathbf{V}_{in} - \mathbf{V}_{ref+}) \cdot \mathbf{dt} = \frac{1}{\mathbf{R} \cdot \mathbf{C}} \int_{t_{1}}^{T} (\mathbf{V}_{in} - \mathbf{V}_{ref-}) \cdot \mathbf{dt}$$

i.e. the total discharge time t_1 is proportional to the average input voltage.

The second integrator shapes the quantisation noise, to provide effective noise suppression with a following digital filter. This quantisation method simultaneously allows high precision and short conversion time.

Filter coefficients are controlled by the microprocessor, which reads and displays or processes the filtered value.

By this way of voltage/time conversion, the result is neither affected by the loss factor of the capacitor nor by drifts of the capacitance C. This method is also independent of the clock frequency, since times T and t₁ are measured with the same frequency.



The input V_{in} directly leads to the high impedance integrator input and the buffer amplifier, preventing a load of the signal source.

The properties of the conversion method and the electrical parameters of the **PRI 5610** keep the demands upon the external components low.

Filtering

The PRI 5610 contains a digital filter that supports the processing of measured data in the best way. Die digital filter suppresses the quantisation noise produced by the analog/digital conversion and limits the bandwidth of the input signal. The bandwidth

and the output data rate of the digital filter can be programmed easily.

Further filtering by use of the microprocessor leads to a further increase in precision.

Conversion Time and Resolution

The measuring time and the precision achievable depend on the programming of the filter coefficient. The device-internal filter performs a first filter step,

a second filter step is done by the evaluation software in the microprocessor environment.

All values in table 1 are typical values by exclusive use of the device-internal digital filter.

Filter coefficient of in- ternal filter (N1)	Measuring time [ms]	Sample rate [1/s]	Significant bits (3·σ) typ.	Significant digits (3·σ) typ.	Amplification* (int. filter = N13)
1	6,67	150	15.6	4.7	1
3	20	50	19.3	5.8	27
6	40	25	21.5	6.5	216
15	100	10	22.5	6.8	3,375
30	200	5	22.8	6.9	27,000

Table 1: Measuring time and precision as a function of filter coefficient N1 of the device-internal filter, without external comb filter $(1 \le N1 \le 32)$

* The amplification of the filter is defined as the ration of filter output signal with filter coefficients N1 and N2 to the filter output signal at N1=N2=1. The number of significant bits can be further increased by averaging in the external processor

(table 2).

Starting with a filter coefficient of N1=15 for the internal filter, the PRI 5610 meets the following specification:

Filter coefficient of exter- nal filter (N2)	Significant bits (3·σ) typ.	Significant digits (3·σ) typ.	Amplification* (int. + ext. filter = N13·N2)
1	22.5	6.8	3,375
10	23.3	7.0	33,750
100	24.5	7.4	337,500
1000	26.6	8.0	3,337,500

Table 2: Enhancement of precision with an external 1st order comb filter as a function of the filter coefficient N2 (at N1=15)

Values in the upper precision range are approximate values, using an optimum board design, calm ambient air and $V_{dd3}V = 3V$. All measurements in the higher precision range rely on effective shielding and appropriate board design – see also the applica-

tion notes in this brochure.

The standard deviation has been calculated from 256 measurements as a moving average at a sample rate of 10 samples per second.

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Electrical Properties

Test conditions, unless otherwise specified:

 $V_{cc} = +15 \text{ V}; V_{ss} = -15 \text{ V};$

 $V_{ref+} = 7.0 \text{ V}; \quad V_{ref-} = -7.0 \text{ V}; \quad Gnd = 0 \text{ V};$

 $V_{dd} 5V = 5.0 \text{ V}; V_{dd} 3V = 3.0 \text{ V};$

 $f_q = 19.6608 \text{ MHz}; T_a = 23^{\circ}\text{C}$

Connection Test to ground.

All voltages given are related to the ground connection Gnd, unless otherwise indicated. Calm ambient air.

Parameter	Sym- bol	Test conditions		min. typ.		max.			Unit			
PRI 5610 Version ²⁾	50,	Conditions	E	F	G	E	F	G	E	F	G	
Basic resolution		unfiltered					17					Bit
Data word length							32				-	Bit
Partial integration time	fuMeas						150					Hz
Data output rate	fs			4.69						150		S ⁻¹
Accuracy: Error all sources (24h, ±1°C) Error all sources (1 yr, ±1°C) Linearity error eff. quantisation noise		before filtering				0.2 0.4 0.05 0.8	0.5 1.0 0.1 0.8	1.0 2.0 0.2 2.0	0.4 0.7 0.08 1.0	1.0 2.0 0.2 1.0	2.0 4.0 0.5 4.0	ppm FS ¹⁾ ppm FS ± ppm FS ± LSB
Drift Offset Signal FS¹) Temperature range Warm-up time	Та	V _{dd3v} =3V		10			0.5 0.1 5			2 0.4 50		± μV/°C μV/°C °C min
Analog inputs Input voltage (bipolar) Reference voltage V _{ref+} Input resistance V _{ref+} Input resistance V _{ref+} Input resistance V _{ref-} Input resistance V _{in}	Vin Vref+ Vref- Rref+ Rref- Rin	V _S =(V _{ref+} -V _{ref-})		-+0.05 / _{ref-} +2\ -8.0 1 1	•		7.0 -7.0 5 5 5			8.0 / _{ref+} –2		V V GΩ GΩ GΩ
Analog outputs Current out of VinBuff	l _o				_					0.5		mA
Supply Supply current (Vdd5v) Supply current (Vdd3v) Supply current (Vdd3v) Supply current (Vcc) Supply current (Vss) Supply current (Vss) Supply voltage rejection Vcc, Vss Supply voltage rejection Vdd	Idd5V Idd3V Idd3V Icc Iss Vdd5V Vdd3V Vcc Vss Vp, Vn	V _{dd3V} =3V V _{dd3V} =5V		4.5 2.7			5 9 20 2.5 2.5 5.0 3.0 12.0 –12.0 1			5.5 5.5		mA mA mA V V V ppm FS/V

¹⁾ FS = full scale

²⁾ Where only one value is given, this applies for versions E, F and G.



Operating the Serial Interface

The serial interface of the ADC allows a fast communication with a superordinated controller on a serial bus system. The on-chip FIFO allows a loss-free data transfer from the ADC to the controller also for high sample rates.

The serial interface is compatible with the following standards:

- Motorola SPI (Modus CPOL=0, CPHA=0; fully compatible)
- National Semiconductor Microwire (fully compatible)
- Texas Instruments TMS320 (with inverter for SCK signal)

 Hitachi SCI (hardware compatible; requires software manipulation, due to LSB in first place)
 The interface consists of five signal lines:

• EOC:

End Of Conversion

• $\overline{\mathbf{CS}}$:

Chip Select

• SCK:

Serial Clock

• DOUT:

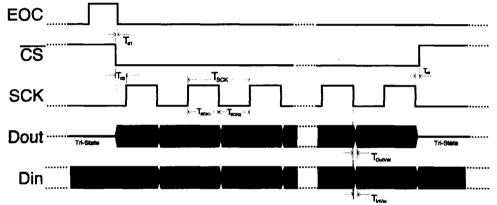
Data Output

• DIN:

Data Input

Although the manufacturer specific protocols are basically the same, the names of the signal connections differ in some cases. The following table shows the signal names for the respective standards:

	MSI	SPI	Microwire	SCI
Serial clock in SCK	SCLK	SCK	SK	SCK
Serial data in DIN	DIN	MISO	SI	RxD
Serial data out DOUT	DOUT	MOSI	SO	TxD



A detailed description of the transfer protocol can be found in the full data sheet, which can be obtained through the address on the back cover.

Filtering

The optimum suppression of the quantisation noise is achieved by a low pass filter with a slope of better than -40 dB/decade, since the quantisation noise shows a high pass characteristics of +40 dB/decade. The digital filter of the PRI 5610 uses the series connection of three first order comb filters with a total slope of -60 dB/decade. The quantisation noise is now suppressed by approximately -50 dB/decade, so extending the measuring by a given factor time leads to the maximum improvement of the accuracy. The characteristics of the digital filter can be also used to suppress annoying hum from the mains supply. At a sampling frequency of 150 Hz the frequency response shown above for a filter coefficient of N=15 for the internal digital filter goes through zero at 50 Hz ($\Omega_{50\text{Hz}} = 2.09$) and at 60 Hz $(\Omega_{60\text{Hz}} = 2.51; \ \Omega = 2\pi \cdot f \cdot T_S = 2\pi \cdot f \cdot f_S \text{ with } T_S =$ sub-sampling time, fS = sampling

150 Hz).

Due to the good suppression of hum, a filter coefficient of 15 proves to be convenient for most applications.

The output data rate of the digital filter refers to the sub-sampling rate fS, divided by the number of filter coefficients. After 3·N partial measurements of the converter the filter has settled and is in steady state. For N additions, the value is multiplied by the factor N^3 . The result is therefore amplified by this cubic factor, so the output signal of the filter now varies by more than ± 1 LSB. Therefore is necessary to scale the output signal in an appropriate way to provide a stable value.

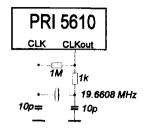
A more extensive description of filtering and notes to improve the significant accuracy with an external filter are given in the longform data sheet.

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Application Notes

Use of a quartz for clock generation

The **PRI 5610** should be clocked with a quartz with a frequency of 19,6608 MHz. The following circuit has proved to be reliable:

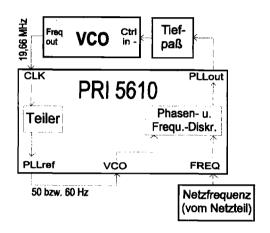


Use of phase and frequency discriminator

Alternatively, a regulator circuit can be used to generate the clock, instead of a quartz.

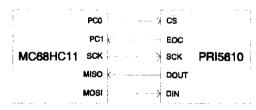
The **PRI 5610** contains a divider that, depending on the content of the register PLL60HZ generates a frequency of 50 Hz or 60 Hz, respectively, at the output PLLref out of a frequency of f_q =19,6608 MHz at CLK. By using a voltage controlled oscillator (VCO) for clock generation instead of a quartz with fixed frequency, an optimum synchrony with the mains frequency and thereby filtering of hum on the signal is achieved.

Netzfrequenz (vom Netzteil) = mains frequency (from mains supply) Teiler = divider $Tiefpa\beta = low pass$



Connection to the Microprocessor

The diagram below shows an example to connect the PRI 5610 to the Motorola controller MC68HC11. This controller allows to configure the ports PC0...PC7 as input or output ports.



Connection of the PRI 5610 to the microcontroller MC68HC11

For more application notes, please ask for our longform data sheet.

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Specifications may be changed without prior notice. The longform data sheet can be obtained through:

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