SP93804

SUB-NANOSECOND QUAD COMPARATOR/GLITCH DETECTOR

The SP93804 contains four independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93804 can also be used as two matched dual devices, due to comparators 1 and 2 being clocked separately from comparators 3 and 4.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

ORDERING INFORMATION

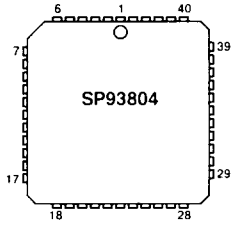
SP93804 B HG (Industrial Quad Cerpac (J-Form) package)

FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay <1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 4 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance
- Dual and Octal Versions SP93802/SP93808

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers



HG44

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/P Vcc2	12	NC	23	VMM	34	NC
2	O/P Vcc2	13	G2	24	RES	35	-I/P3
3	G4	14	NC	25	CLK1	36	+I/P3
4	NC	15	Q2	26	CLK1	37	NC
5	Q4	16	Q2	27	VEE1	38	-I/P4
6	Q4	17	NC	28	VMM	39	+I/P4
7	NC	18	G1	29	-I/P1	40	NC
8	G3	19	Q1	30	+I/P1	41	VEE2
9	NC	20	Q1	31	NC	42	CLK2
10	Q3	21	O/P Vcc1	32	-I/P2	43	CLK2
11	Q3	22	I/P Vcc1	33	+I/P2	44	VMM

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc - VMM	+6V
Supply voltage VMM - VEE	-6V
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Output current	≤30mA
Maximum input voltage	
Common mode positive	≤Vcc
Common mode negative	≥VEE
Differential input voltage	≤±3.8V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, I/P and O/P V_{CC} = +5V ± 0.25V,
V_{EE} = -5V ± 0.25V, V_{MM} = 0V (see Fig.4), Load = 50Ω to V_{CC} -2V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		38.5	50	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Negative supply current	I_{EE}		16.0	21	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Positive supply voltage	V_{CC}	I/P MAX +1.55	5.0	I/P MIN +7.3	V	
Negative supply voltage	V_{EE}	-5.5	-5.0	-4.9	V	
Input offset voltage	V_{OS}	-3.5		+3.5	mV	
Input bias current	I_B		5.25	9	μA	
Input offset current	I_{OS}		0.95	1.2	μA	
Input capacitance	C_I		1.5 (Note 1)		pF	
Input impedance	R_I		250		kΩ	Measured at DC
Differential input range	V_{DIF}			±3.8	V	
Common mode input range	CMIR	-2.1		+2.6	V	
Output voltage high	V_{OH}	V_{CC}-1.050		V_{CC}-0.81	V	+25°C, V_{IN} > 60mV
		V_{CC}-1.140		V_{CC}-0.91	V	-40°C, V_{IN} > 60mV
		V_{CC}-0.965		V_{CC}-0.704	V	+85°C, V_{IN} > 60mV
Output voltage low	V_{OL}	V_{CC}-1.712		V_{CC}-1.544	V	+25°C, V_{IN} < -60mV
		V_{CC}-1.792		V_{CC}-1.650	V	-40°C, V_{IN} < -60mV
		V_{CC}-1.638		V_{CC}-1.465	V	+85°C, V_{IN} < -60mV
Gain (transparent mode)			20		dB	Differential
Common mode rejection	CMRR	50	50		dB	+25°C, with respect to I/P
Supply voltage rejection	PSRR		70		dB	+25°C, with respect to I/P offset
Clock input:						
Common mode range	CMRC	V_{MM}+2V		V_{CC}-1.35V	V	
Differential swing	DS	400		1600	mV	

NOTES 1 Guaranteed but not tested

Dynamic Characteristics (Note 1)

See dynamic test circuit Fig.9.

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Latch setup time	t_S		150		ps	20mV overdrive
Hold time	t_H		600		ps	20mV overdrive
Input to Q delay	t_{IQ}		800		ps	20mV overdrive
Latch to Q delay	t_{LQ}		1500		ps	20mV overdrive
Glitch capture regeneration	t_{RD}		900		ps	20mV overdrive at Qn
Propagation delay matching	t_{PDM}	-100		+100	ps	Within each device
Min. compare pulse width	t_{PW}		950		ps	20mV overdrive
Min. reset pulse width	t_{RM}		800		ps	
Max. flip flop reset time	t_{RR}		800		ps	
Min. hold time of Qn after reset	t_{GH}		800		ps	
Delay between Qn and Gn	t_{QG}		900		ps	
Propagation delay RES to Gn	t_{RG}		800		ps	

NOTES 1 Guaranteed but not tested

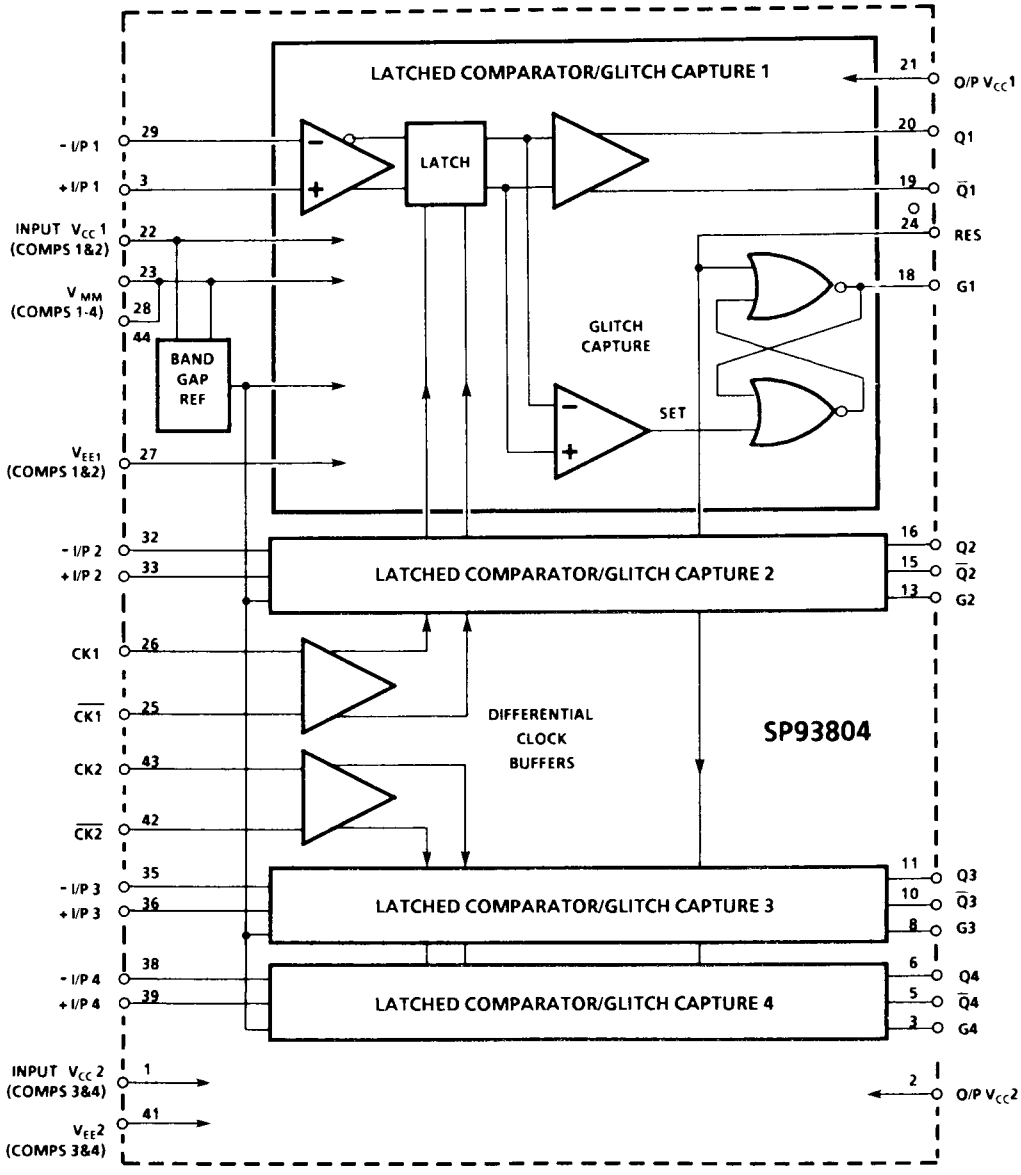


Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)

PIN FUNCTIONS

Name	Pin	Description
I/P $V_{CC}1$	22	Positive supply connection for comparators 1 and 2, and the bandgap reference.
O/P $V_{CC}1$	21	Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 1 and 2 (emitter follower outputs, see Fig.5).
I/P $V_{CC}2$	1	Positive supply connection for comparators 3 and 4.
O/P $V_{CC}2$	2	Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 3 and 4 (emitter follower outputs, see Fig.5).
-I/Pn +I/Pn	29/32, 35/38, 30/33, 36/39	Inverting and non-inverting inputs to comparators 1 to 4, respectively.
Qn/$\overline{Qn}$	6/5, 11/10, 16/15, 20/19	Q and Q outputs of comparators 1 to 4, respectively.
Gn	18,13,8,3	Outputs of glitch capture circuits 1 to 4, respectively.
RES	24	Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'.
CLK1, $\overline{CLK1}$	25, 26	Clock input pins for comparators 1 and 2. Active low signal which latches the outputs of comparators 1 and 2.
CLK2, $\overline{CLK2}$	42, 43	Clock input pins for comparators 3 and 4. Active low signal which latches the outputs of comparators 3 and 4.
$V_{EE}1$	27	Negative supply voltage for comparators 1 and 2.
$V_{EE}2$	41	Negative supply voltage for comparators 3 and 4.
V_{MM}	23,44,28	Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref.

OPERATING NOTES

Transparent Mode

The SP93804 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93804 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

Supply Connections

The SP93804 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from V_{CC}, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage (V_{MM}), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P V_{CC} pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93804 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

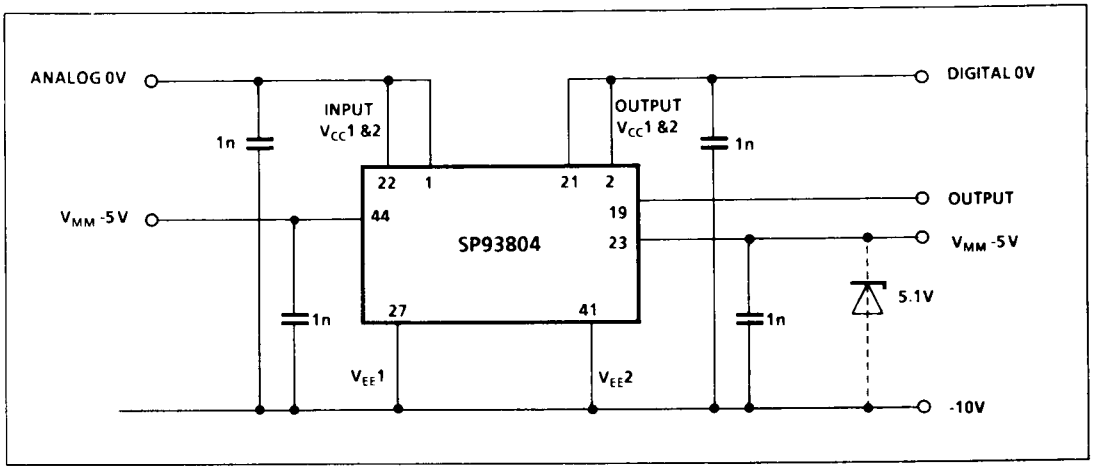


Fig.3 Connection to 0V, -5V and -10V

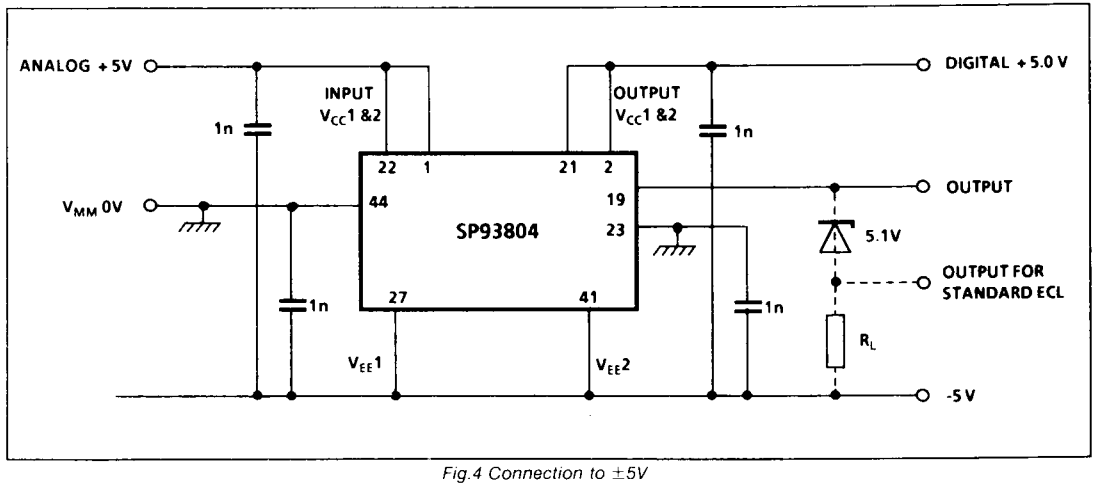


Fig.4 Connection to ±5V

External Components

The Qn, $\overline{Q}$n and Gn outputs are open emitters and therefore required external pulldown resistors (R_L). These resistors may be in the range of 50-250Ω connected to V_{CC}-2V (V_T) or 250-2000Ω connected to V_{MM}.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and V_{EE} is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

Clock Inputs

The SP93804 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two dual comparators as comparators 1 and 2 can be clocked separately from comparators 3 and 4.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device V_{CC} connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

A range of clock input configurations are possible according to the various supply operating.

$\overline{CLK1}$ (pin 25) comparators 1 and 2 latch when low.
$\overline{CLK1}$ (pin 26) inverse clock for comparators 1 and 2.
$\overline{CLK2}$ (pin 43) comparators 3 and 4 latch when low.
$\overline{CLK2}$ (pin 42) inverse clock for comparators 3 and 4.

The clock inputs should have fast rise times and low jitter. The SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator

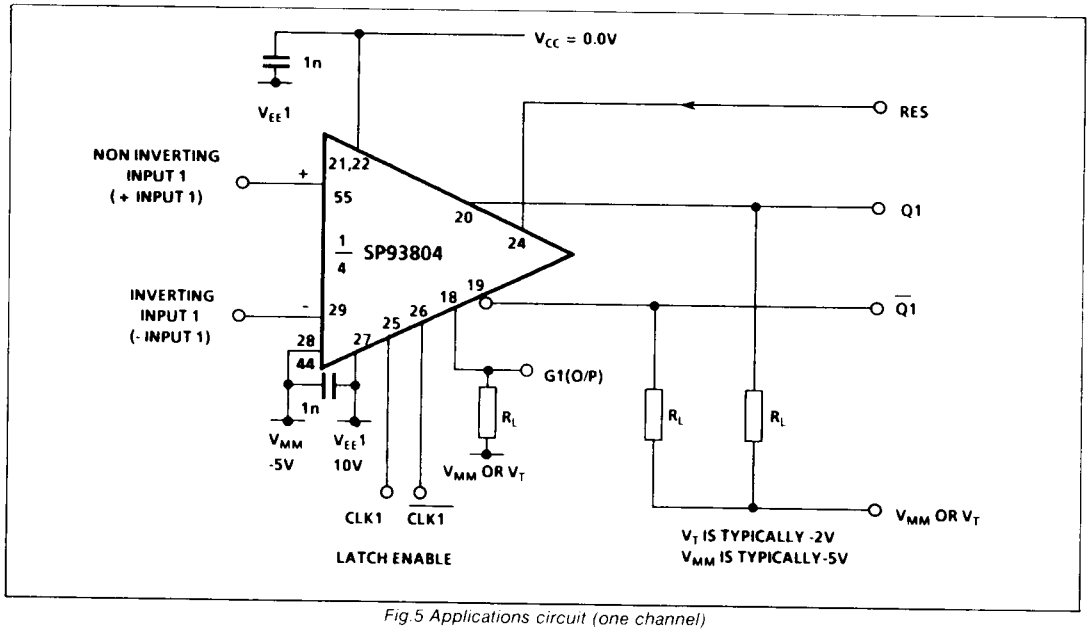


Fig.5 Applications circuit (one channel)

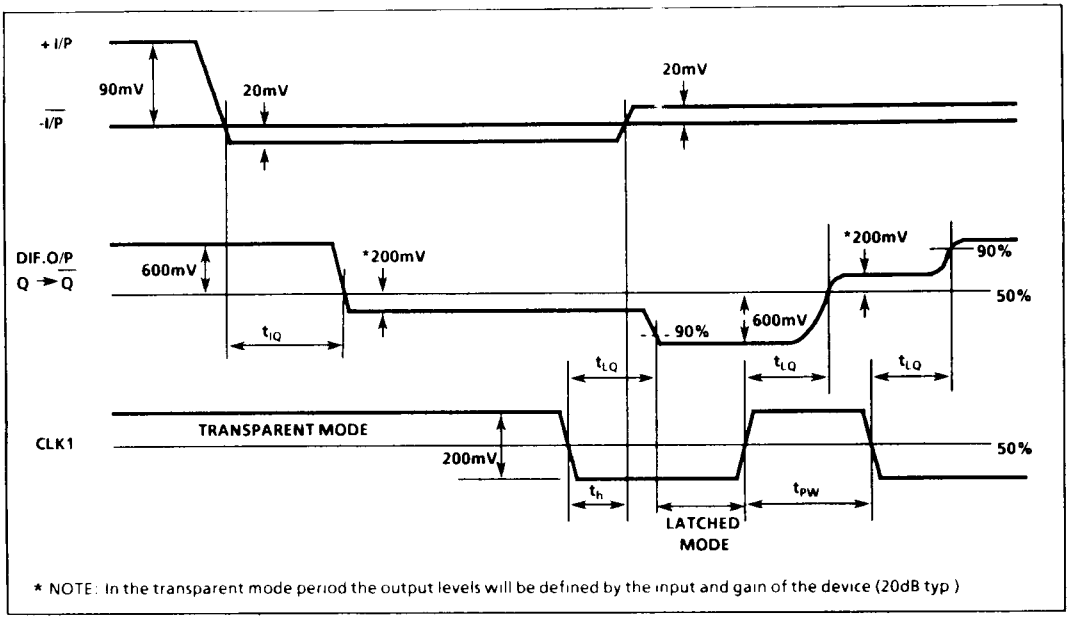


Fig.6 Comparator timing diagram

I/P	CLK	Qn + 1
X	0	Qn
1	1	1
0	1	0

X = Don't Care

Table 1 Truth table for comparator

RES	SET(1) (n + 1)	Gn + 1
1	X	0
0	↗	↗
0	↘	1
0	1	1
0	0	Gn(2)
↘	1	↗
↘	0	0

X = Don't Care

Table 2 Truth table for glitch capture circuit

Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' (V_{CC}-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

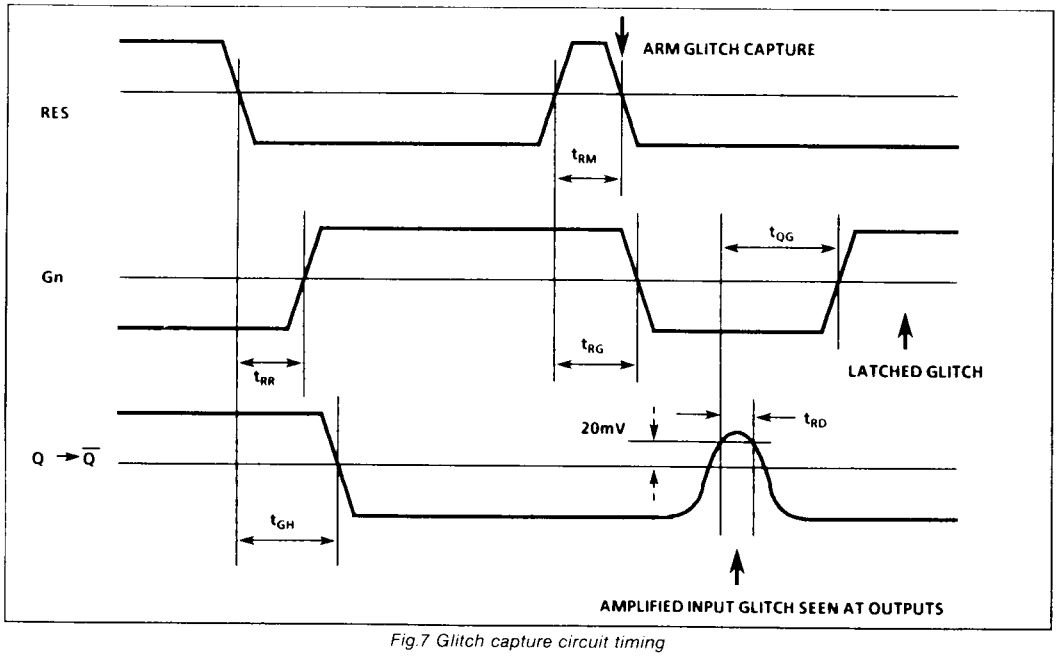
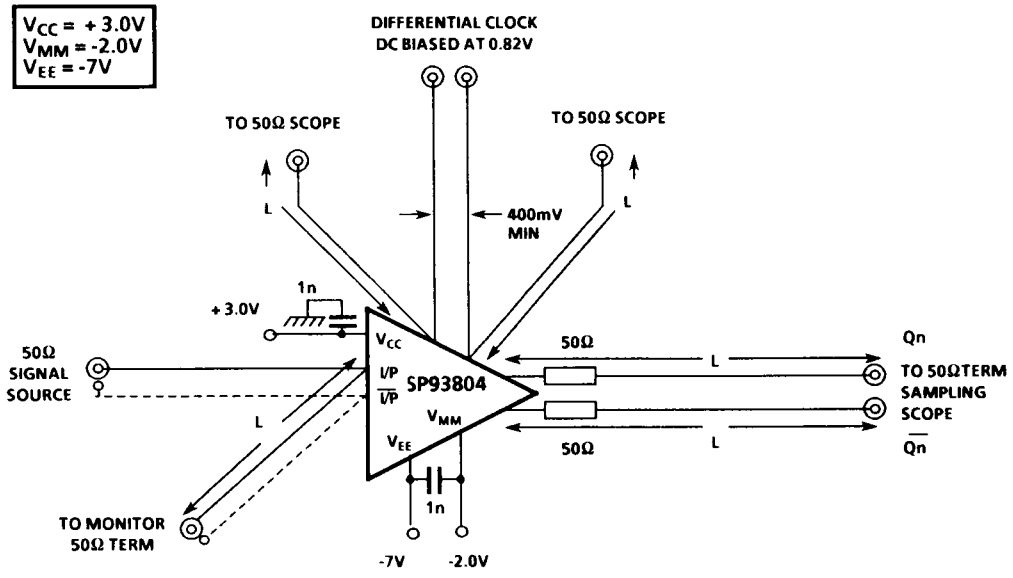


Fig.7 Glitch capture circuit timing



NOTES:-
The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) An SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

Fig.8 - Comparator Test Circuit (one channel)