

**FEATURES:**

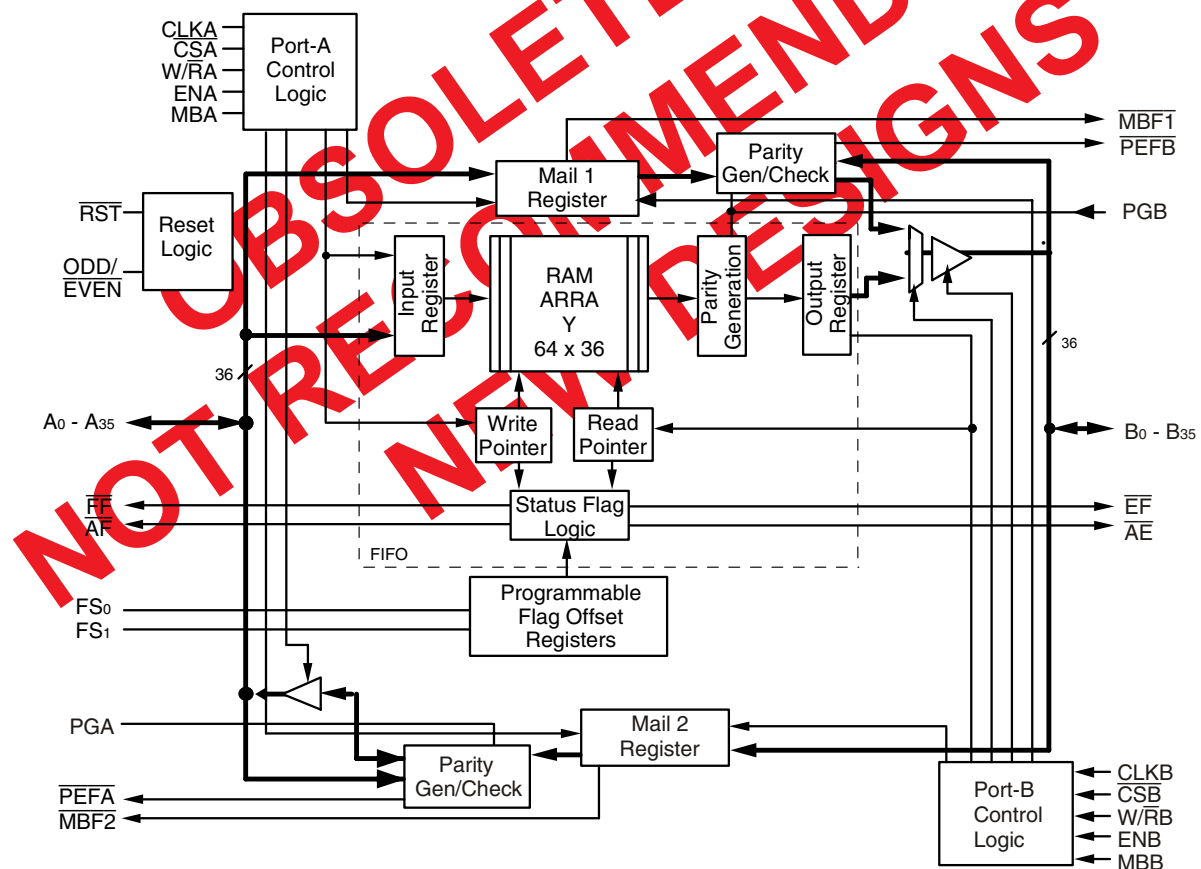
- Free-running CLKA and CLKB may be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- 64 x 36 storage capacity
- Synchronous data buffering from Port A to Port B
- Mailbox bypass register in each direction
- Programmable Almost-Full (AF) and Almost-Empty (AE) flags
- Microprocessor Interface Control Logic
- Full Flag (FF) and Almost-Full (AF) flags synchronized by CLKA
- Empty Flag (EF) and Almost-Empty (AE) flags synchronized by CLKB
- Passive parity checking on each Port
- Parity Generation can be selected for each Port
- Supports clock frequencies up to 67MHz
- Fast access times of 10ns
- Available in 132-pin Plastic Quad Flatpack (PQF) or space-saving 120-pin Thin Quad Flatpack (PF)
- Industrial temperature range (-40°C to +85°C) is available
- Green parts available, see ordering information

**DESCRIPTION:**

The IDT723611 is a monolithic, high-speed, low-power, CMOS Synchronous (clocked) FIFO memory which supports clock frequencies up to 67MHz and has read access times as fast as 10ns. The 64 x 36 dual-port FIFO buffers data from Port A to Port B. The FIFO has flags to indicate empty and full conditions, and two programmable flags, Almost-Full (AF) and Almost-Empty (AE), to indicate when a selected number of words is stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices may be used in parallel to create wider data paths.

The IDT723611 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

**FUNCTIONAL BLOCK DIAGRAM**



IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc. SyncBIFIFO is a trademark of Integrated Device Technology, Inc.

3024 drw 01

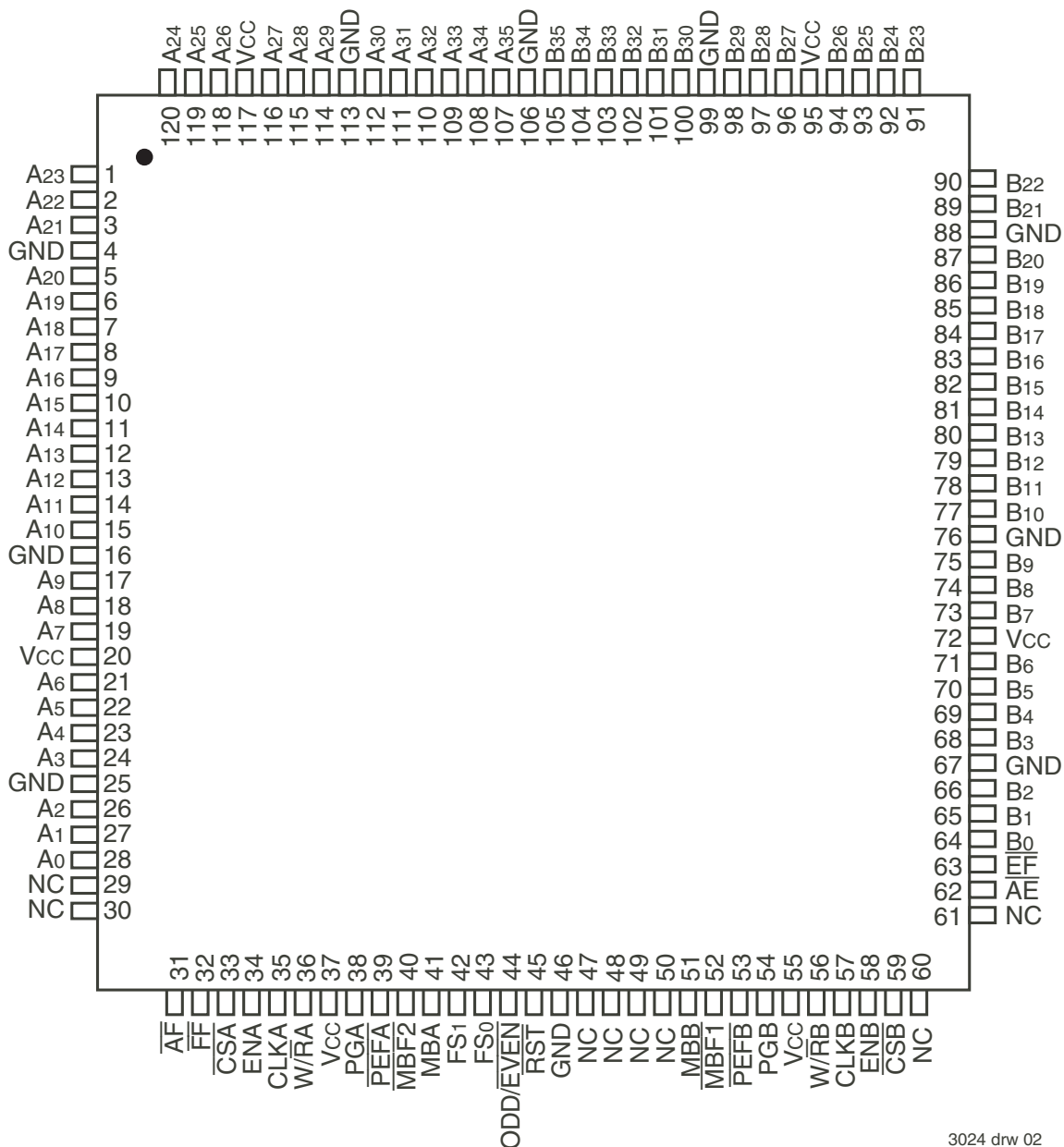
### DESCRIPTION (CONTINUED)

The Full Flag ( $\overline{FF}$ ) and Almost-Full ( $\overline{AF}$ ) flag of the FIFO are two-stage synchronized to the port clock that writes data into its array (CLKA). The Empty

Flag ( $\overline{EF}$ ) and Almost-Empty ( $\overline{AE}$ ) flag of the FIFO are two-stage synchronized to the port clock that reads data from its array.

The IDT723611 is characterized for operation from 0°C to 70°C.

### PIN CONFIGURATIONS



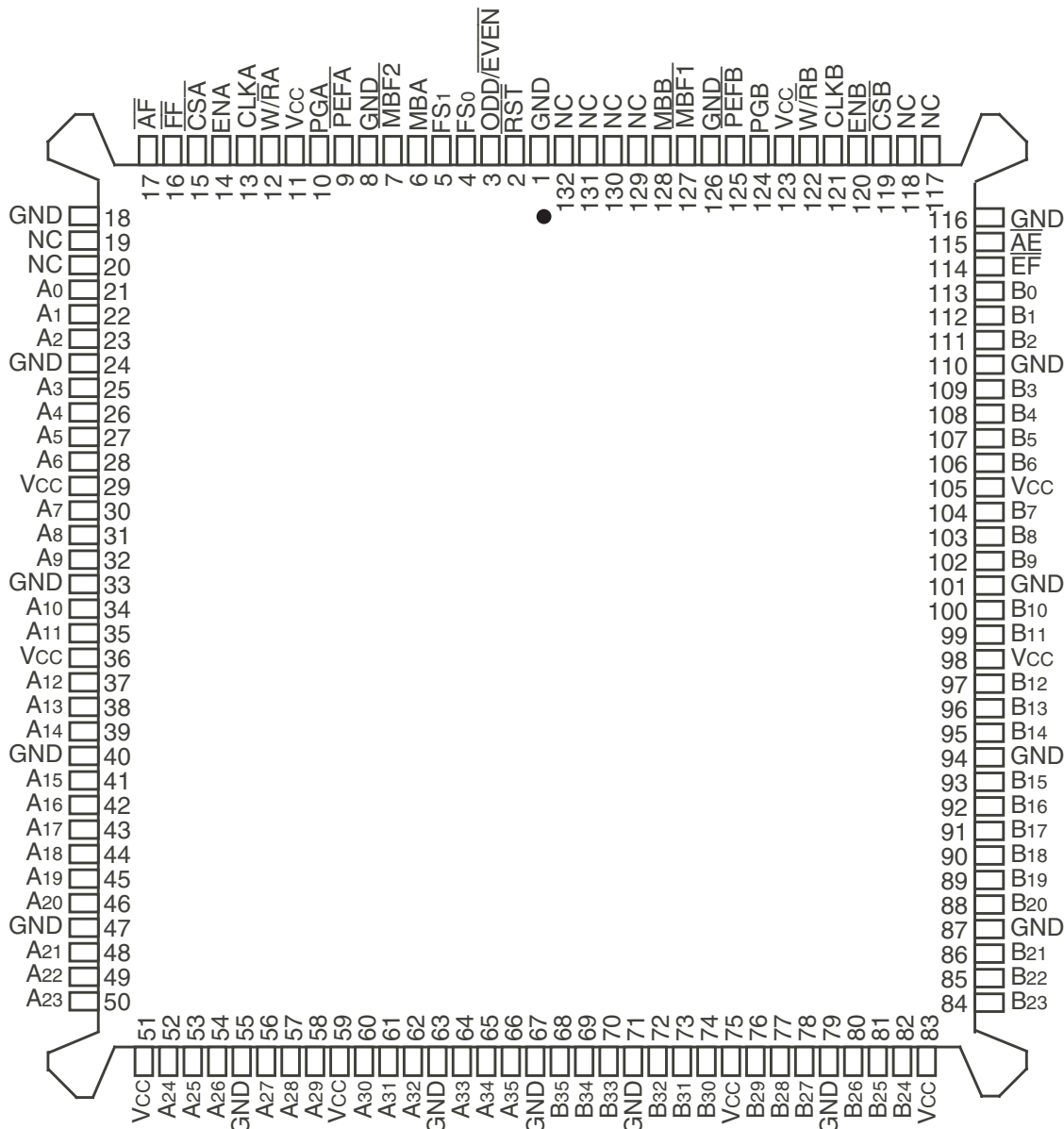
3024 drw 02

**NOTE:**

1. Pin 1 identifier in corner.
2. NC = No internal connection

TQFP (PN120-1, order code: PF)  
TOP VIEW

### PIN CONFIGURATIONS (CONTINUED)



3024 dnr 03

**NOTES:**

1. Electrical pin 1 in center of beveled edge.
2. NC = No internal connection.

PQFP (PQ132-1, order code: PQF)  
TOP VIEW

## PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Offset register, X.
B0-B35	Port-B Data	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and can be asynchronous or coincident to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EF}$ is LOW, the FIFO is empty, and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is HIGH. $\overline{EF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO memory.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is synchronized to the LOW-to-HIGH/ transition of CLKA. When $\overline{FF}$ is LOW, the FIFO is full, and writes to its memory are disabled. $\overline{FF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the Almost-Full and Almost-Empty Offset register (X).
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects the FIFO output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
$\overline{ODD/}$ $\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when $\overline{ODD/EVEN}$ is HIGH, and even parity is checked when $\overline{ODD/EVEN}$ is LOW. $\overline{ODD/EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port-A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the $\overline{ODD/EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having $\overline{CSA}$ LOW, ENA HIGH, $\overline{W/RA}$ LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the state of A0-A35 inputs.
$\overline{PEFB}$	Port-B Parity Error Flag	O	When any byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as (Port B) B0-B8, B9-B17, B18-B26, B27-B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the $\overline{ODD/EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having $\overline{CSB}$ LOW, ENB HIGH, $\overline{W/RB}$ LOW, MBB HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs

## PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
PGA	Port-A Parity Generation	I	Parity is generated for mail2 register reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port-B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AF}$ , $\overline{MBF1}$ , and $\overline{MBF2}$ flags HIGH and the $\overline{EF}$ , $\overline{AE}$ , and $\overline{FF}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select Almost-Full and Almost-Empty flag offset.
$\overline{W/RA}$	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when $\overline{W/RA}$ is HIGH.
$\overline{W/RB}$	Port-B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when $\overline{W/RB}$ is HIGH.

## ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
V <sub>CC</sub>	Supply Voltage Range	-0.5 to 7	V
V <sub>I</sub> <sup>(2)</sup>	Input Voltage Range	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>O</sub> <sup>(2)</sup>	Output Voltage Range	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Clamp Current, (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	±20	mA
I <sub>OK</sub>	Output Clamp Current, (V <sub>O</sub> = < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50	mA
I <sub>OUT</sub>	Continuous Output Current, (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±50	mA
I <sub>CC</sub>	Continuous Current Through V <sub>CC</sub> or GND	±500	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to 150	°C

### NOTES:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

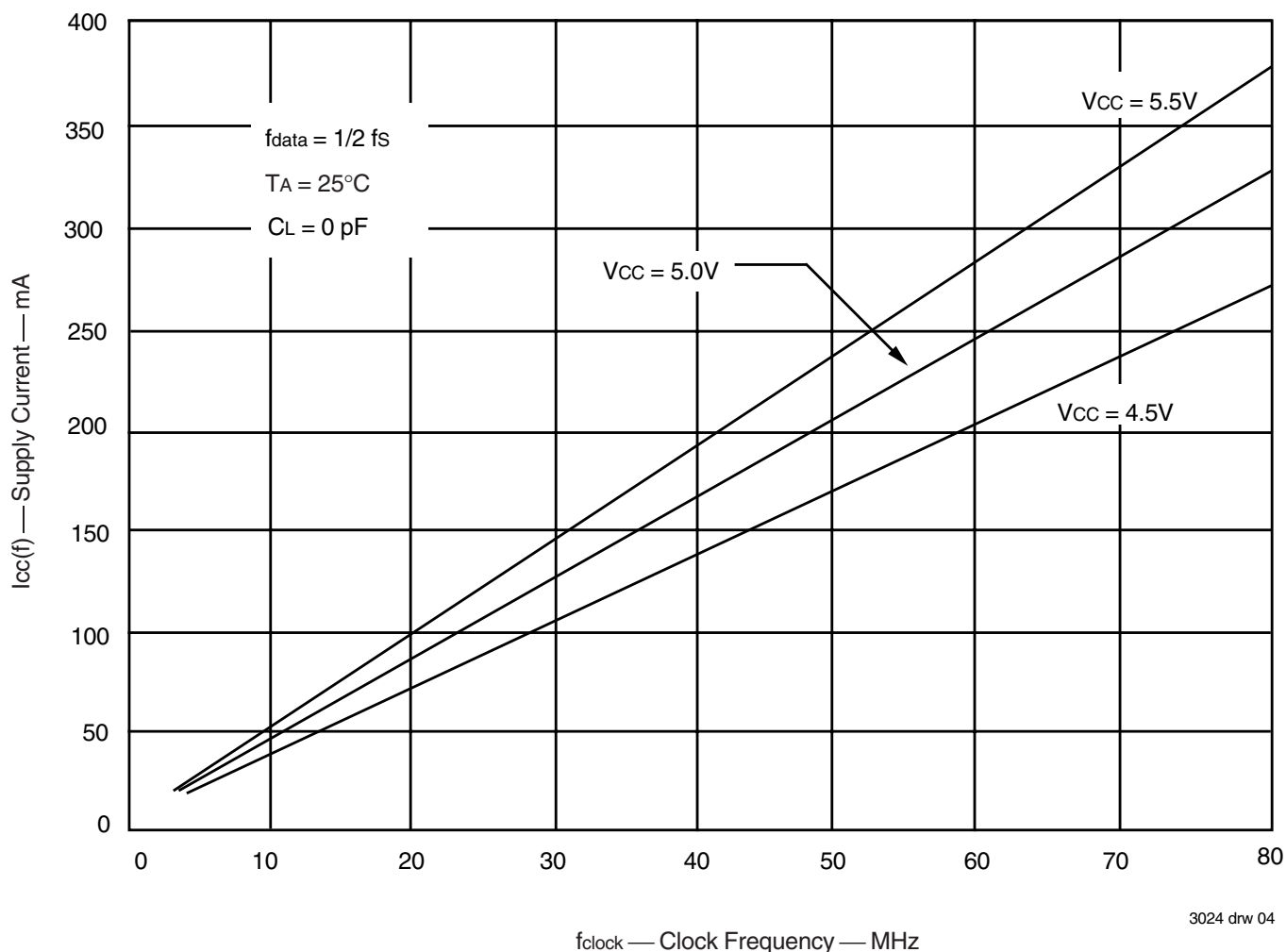
Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IH</sub>	High-Level Input Voltage	2	—	V
V <sub>IL</sub>	Low-Level Input Voltage	—	0.8	V
I <sub>OH</sub>	High-Level Output Current	—	-4	mA
I <sub>OL</sub>	Low-Level Output Current	—	8	mA
T <sub>A</sub>	Operating Free-Air Temperature	0	70	°C

## ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Parameter	Test Conditions		IDT723611 Commercial & Industrial <sup>(1)</sup> t <sub>A</sub> = 15, 20 ns			Unit
			Min.	Typ. <sup>(2)</sup>	Max.	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5V,	I <sub>OH</sub> = -4 mA	2.4	—	—	V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5V,	I <sub>OL</sub> = 8 mA	—	—	0.5	V
I <sub>LI</sub>	V <sub>CC</sub> = 5.5V,	V <sub>I</sub> = V <sub>CC</sub> or 0	—	—	±50	μA
I <sub>LO</sub>	V <sub>CC</sub> = 5.5V,	V <sub>O</sub> = V <sub>CC</sub> or 0	—	—	±50	μA
I <sub>CC</sub> <sup>(3)</sup>	V <sub>CC</sub> = 5.5V,	I <sub>O</sub> = 0 mA, V <sub>I</sub> = V <sub>CC</sub> or GND				
			Outputs HIGH	—	60	mA
			Outputs LOW	—	130	
			Outputs Disabled	—	60	
C <sub>IN</sub>	V <sub>I</sub> = 0,	f = 1 MHz	—	4	—	pF
C <sub>OUT</sub>	V <sub>O</sub> = 0,	f = 1 MHz	—	8	—	pF

### NOTES:

- Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- For additional I<sub>CC</sub> information, see the following page.



3024 drw 04

Figure 1. Typical Characteristics: Supply Current vs Clock Frequency

## CALCULATING POWER DISSIPATION

The I<sub>cc</sub>(f) data for the graph was taken while simultaneously reading and writing the FIFO on the IDT723611 with CLKA and CLKB operating at frequency f<sub>s</sub>. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

With I<sub>cc</sub>(f) taken from Figure 1, the maximum power dissipation (PT) of the IDT723611 may be calculated by:

$$PT = V_{CC} \times I_{CC}(f) + \sum (CL \times V_{OH} - V_{OL})^2 \times f_o$$

where:

- CL = output capacitance load
- f<sub>o</sub> = switching frequency of an output
- V<sub>OH</sub> = output high-level voltage
- V<sub>OL</sub> = output low-level voltage

When no read or writes are occurring on this device, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f<sub>s</sub> is calculated by:

$$PT = V_{CC} \times f_s \times 0.290 \text{ mA/MHz}$$

## TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURES

(Commercial: Vcc = 5.0V ±10%, TA = 0°C to +70°C; Industrial; Vcc = 5.0V ± 10%, TA = 40°C to +85°C)

Symbol	Parameter	Commercial		Com'l & Ind'l <sup>(1)</sup>		Unit
		IDT723611L15		IDT723611L20		
		Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	–	66.7	–	50	MHz
tCLK	Clock Cycle Time, CLKA or CLKB	15	–	20	–	MHz
tCLKH	Pulse Duration, CLKA or CLKB HIGH	6	–	8	–	ns
tCLKL	Pulse Duration, CLKA or CLKB LOW	6	–	8	–	ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	ns
tENS1	$\overline{CSA}$ , W/ $\overline{RA}$ , before CLKA↑; $\overline{CSB}$ , W/ $\overline{RB}$ before CLKB↑	6	–	6	–	ns
tENS2	ENA before CLKA↑; ENB before CLKB↑	4	–	5	–	ns
tENS3	MBA before CLKA↑; $\overline{ENB}$ before CLKB↑	4	–	5	–	ns
tPGS	Setup Time, ODD/ $\overline{EVEN}$ and PGB before CLKB↑ <sup>(1)</sup>	4	–	5	–	ns
tRSTS	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑ <sup>(2)</sup>	5	–	6	–	ns
tFSS	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	6	–	ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	1	–	ns
tENH1	$\overline{CSA}$ , W/ $\overline{RA}$ after CLKA↑; $\overline{CSB}$ , W/ $\overline{RB}$ after CLKB↑	1	–	1	–	ns
tENH2	ENA after CLKA↑; ENB after CLKB↑	1	–	1	–	ns
tENH3	MBA after CLKA↑; MBB after CLKB↑	1	–	1	–	ns
tPGH	Hold Time, ODD/ $\overline{EVEN}$ and PGB after CLKB↑ <sup>(2)</sup>	0	–	0	–	ns
tRSTH	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑ <sup>(3)</sup>	6	–	6	–	ns
tFSH	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	ns
tSKEW1 <sup>(4)</sup>	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EF}$ , $\overline{FF}$	8	–	8	–	ns
tSKEW2 <sup>(4)</sup>	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$ , $\overline{AF}$	14	–	16	–	ns

### NOTES:

1. Industrial Temperature Range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Only applies for a rising edge of CLKB that does a FIFO read.
3. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
4. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

## SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, CL = 30 PF

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C; Industrial; VCC = 5.0V ± 10%, TA = 40°C to +85°C)

Symbol	Parameter	Commercial		Com'l & Ind'l <sup>(1)</sup>		Unit
		IDT723611L15		IDT723611L20		
		Min.	Max.	Min.	Max.	
fs	Clock Frequency, CLKA or CLKB	–	66.7	–	50	MHz
ta	Access Time, CLKB↑ to B0-B35	2	10	2	12	ns
twFF	Propagation Delay Time, CLKA↑ to FF	2	10	2	12	ns
tREF	Propagation Delay Time, CLKB↑ to EF	2	10	2	12	ns
tPAE	Propagation Delay Time, CLKB↑ to AE	2	10	2	12	ns
tPAF	Propagation Delay Time, CLKA↑ to AF	2	10	2	12	ns
tPMF	Propagation Delay Time, CLKA↑ to MBF1 LOW or MBF2 HIGH and CLKB↑ to MBF2 LOW or MBF1 HIGH	1	9	1	12	ns
tPMR	Propagation Delay Time, CLKA↑ to B0-B35 <sup>(2)</sup> and CLKB↑ to A0-A35 <sup>(3)</sup>	3	12	3	14	ns
tMDV	Propagation Delay Time, MBB to B0-B35 Valid	1	11	1	11.5	ns
tDPDE	Propagation Delay Time, A0-A35 Valid to PEFA Valid; B0-B35 Valid to PEFB Valid	3	12	3	13	ns
tPOPE	Propagation Delay Time, ODD/EVEN to PEFA and PEFB	3	11	3	12	ns
tPOPB <sup>(4)</sup>	Propagation Delay Time, ODD/EVEN to Parity Bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	ns
tPEPE	Propagation Delay Time, CSA, ENA, W/RA, MBA, or PGA to PEFA; CSB, ENB, W/RB, MBB, or PGB to PEFB	1	12	1	13	ns
tPEPB <sup>(4)</sup>	Propagation Delay Time, CSA, ENA, W/RA, MBA, or PGA to Parity Bits (A8, A17, A26, A35); CSB, ENB, W/RB, MBB, or PGB to Parity Bits (B8, B17, B26, B35)	3	14	3	15	ns
trSF	Propagation Delay Time, RST to AE LOW and (AF, MBF1, MBF2) HIGH	1	15	1	20	ns
tEN	Enable Time, CSA and W/RA LOW to A0-A35 Active and CSB LOW and W/RB HIGH to B0-B35 Active	2	10	2	12	ns
tDIS	Disable Time, CSA or W/RA HIGH to A0-A35 at high impedance and CSB HIGH or W/RB LOW to B0-B35 at high impedance	1	9	1	10	ns

### NOTES:

- Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
- Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
- Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
- Only applies when reading data from a mail register.

## SIGNAL DESCRIPTION

### RESET ( $\overline{RST}$ )

The IDT723611 is reset by taking the Reset ( $\overline{RST}$ ) input LOW for at least four port-A clock (CLKA) and four port-B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the Full Flag ( $\overline{FF}$ ) LOW, the Empty Flag ( $\overline{EF}$ ) LOW, the Almost-Empty flag ( $\overline{AE}$ ) LOW, and the Almost-Full flag ( $\overline{AF}$ ) HIGH. A reset also forces the Mailbox Flags ( $\overline{MBF1}$ ,  $\overline{MBF2}$ ) HIGH. After a reset,  $\overline{FF}$  is set HIGH after two LOW-to-HIGH transitions of CLKA. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the  $\overline{RST}$  input loads the Almost-Full and Almost-Empty Offset register (X) with the value selected by the Flag Select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

**TABLE 1 — FLAG PROGRAMMING**

Almost-Full and Almost-Empty Flag Offset Register (X)	FS1	FS0	$\overline{RST}$
16	H	H	↑
12	H	L	↑
8	L	H	↑
4	L	L	↑

### FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by the port-A Chip Select ( $\overline{CSA}$ ) and the port-A Write/Read select ( $\overline{W/\overline{RA}}$ ). The A0-A35 outputs are in the high-impedance state when either  $\overline{CSA}$  or  $\overline{W/\overline{RA}}$  is HIGH. The A0-A35 outputs are active when both  $\overline{CSA}$  and  $\overline{W/\overline{RA}}$  are LOW. Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when  $\overline{CSA}$  is LOW,  $\overline{W/\overline{RA}}$  is HIGH, ENA is HIGH, MBA is LOW, and  $\overline{FF}$  is HIGH (see Table 2).

The port-B control signals are identical to those of port A. The state of the port-B data (B0-B35) outputs is controlled by the port-B Chip Select ( $\overline{CSB}$ ) and the port-B Write/Read select ( $\overline{W/\overline{RB}}$ ). The B0-B35 outputs are in the high-impedance state when either  $\overline{CSB}$  or  $\overline{W/\overline{RB}}$  is HIGH. The B0-B35 outputs are active when both  $\overline{CSB}$  and  $\overline{W/\overline{RB}}$  are LOW. Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when  $\overline{CSB}$  is LOW,  $\overline{W/\overline{RB}}$  is LOW, ENB is HIGH, MBB is LOW, and  $\overline{EF}$  is HIGH (see Table 3).

The setup and hold-time constraints to the port clocks for the port Chip Selects ( $\overline{CSA}$ ,  $\overline{CSB}$ ) and Write/Read selects ( $\overline{W/\overline{RA}}$ ,  $\overline{W/\overline{RB}}$ ) are only for enabling write and read operations and are not related to HIGH-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select can change states during the setup and hold-time window of the cycle.

### SYNCHRONIZED FIFO FLAGS

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another.  $\overline{FF}$  and  $\overline{AF}$  are synchronized to CLKA.  $\overline{EF}$  and  $\overline{AE}$  are synchronized to CLKB. Table 4 shows the relationship to the flags to the FIFO.

**TABLE 2 — PORT-A ENABLE FUNCTION TABLE**

$\overline{CSA}$	$\overline{W/\overline{RA}}$	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, Mail2 Register	None
L	L	H	L	↑	Active, Mail2 Register	None
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (set $\overline{MBF2}$ HIGH)

**TABLE 3 — PORT-B ENABLE FUNCTION TABLE**

$\overline{CSB}$	$\overline{W/\overline{RB}}$	ENB	MBB	CLKB	B0-B35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	None
L	H	H	H	↑	In High-Impedance State	Mail2 Write
L	L	L	L	X	Active, FIFO Output Register	None
L	L	H	L	↑	Active, FIFO Output Register	FIFO Read
L	L	L	H	X	Active, Mail1 Register	None
L	L	H	H	↑	Active, Mail1 Register	Mail1 Read (set $\overline{MBF1}$ HIGH)

### EMPTY FLAG ( $\overline{EF}$ )

The FIFO Empty Flag is synchronized to the port clock that reads data from its array (CLKB). When the  $\overline{EF}$  is HIGH, new data can be read to the FIFO output register. When the  $\overline{EF}$  is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an  $\overline{EF}$  monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles. Therefore, an  $\overline{EF}$  is LOW if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The  $\overline{EF}$  of the FIFO is set HIGH by the second LOW-to-HIGH transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on CLKB begins the first synchronized cycle of a write if the clock transition occurs at time  $t_{SKEW1}$  or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 5).

### FULL FLAG ( $\overline{FF}$ )

The FIFO Full Flag is synchronized to the port clock that writes data to its array (CLKA). When the  $\overline{FF}$  is HIGH, an SRAM location is free to receive new data. No memory locations are free when the  $\overline{FF}$  is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls the  $\overline{FF}$  monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. Therefore, a  $\overline{FF}$  is LOW if less than two CLKA cycles have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the  $\overline{FF}$  HIGH and data can be written in the following clock cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time  $t_{SKEW1}$  or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 6).

### ALMOST-EMPTY FLAG ( $\overline{AE}$ )

The FIFO Almost-Empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the  $\overline{AE}$  flag monitors a

write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The  $\overline{AE}$  flag is LOW when the FIFO contains X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions on the port-B clock (CLKB) are required after a FIFO write for the  $\overline{AE}$  flag to reflect the new level of fill. Therefore, the  $\overline{AE}$  flag of a FIFO containing (X+1) or more words remains LOW if two CLKB cycles have not elapsed since the write that filled the memory to the (X+1) level. The  $\overline{AE}$  flag is set HIGH by the second CLKB LOW-to-HIGH transition after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition on CLKB begins the first synchronization cycle if it occurs at time  $t_{SKEW2}$  or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 7).

### ALMOST-FULL FLAG ( $\overline{AF}$ )

The FIFO Almost-Full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an  $\overline{AF}$  flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The  $\overline{AF}$  flag is LOW when the FIFO contains (64-X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions on the port-A clock (CLKA) are required after a FIFO read for the  $\overline{AF}$  flag to reflect the new level of fill. Therefore, the  $\overline{AF}$  flag of a FIFO containing [64-(X+1)] or less words remains LOW if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. The  $\overline{AF}$  flag is set HIGH by the second CLKA LOW-to-HIGH transition after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A LOW-to-HIGH transition on CLKA begins the first synchronization cycle if it occurs at time  $t_{SKEW2}$  or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 8).

### MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT723611 to pass command and control information between port A and port B. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when port-A write is selected by  $\overline{CSA}$ ,  $W/\overline{RA}$ , and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when port-B write is selected by  $\overline{CSB}$ ,  $W/\overline{RB}$ , and ENB with MBB HIGH. Writing data to a mail register sets its corresponding flag ( $\overline{MBF1}$  or  $\overline{MBF2}$ ) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port-B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B Mailbox select (MBB) input is LOW and from the mail1 register when MBB is HIGH. Mail2 data is always present on the port-A data (A0-A35) outputs when they are active. The Mail1 Register Flag ( $\overline{MBF1}$ ) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by  $\overline{CSB}$ ,  $W/\overline{RB}$ , and ENB with MBB HIGH. The Mail2 Register Flag ( $\overline{MBF2}$ ) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A read is selected by  $\overline{CSA}$ ,  $W/\overline{RA}$ , and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

**TABLE 4 — FIFO FLAG OPERATION**

Number of Words in the FIFO	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

**NOTE:**

1. X is the value in the Almost-Empty flag and Almost-Full flag register.

### PARITY CHECKING

The port-A (A0-A35) inputs and port-B (B0-B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port Parity Error Flag (PEFA, PEFB). Odd or even parity checking can be selected, and the Parity Error Flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the Odd/Even parity (ODD/EVEN) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port Parity Error Flag (PEFA, PEFB) output. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, and port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35. When Odd/Even parity is selected, a port Parity Error Flag (PEFA, PEFB) is LOW if any byte on the port has an odd/even number of LOW levels applied to its bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA=HIGH). When port-A read from the mail2 register with parity generation is selected with CSA LOW, ENA HIGH, W/RA LOW, MBA HIGH, and PGA HIGH, the port-A Parity Error Flag (PEFA) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB=HIGH). When a port-B read from the mail1 register with parity generation is selected with CSB LOW, ENB HIGH, W/RB LOW, MBB HIGH, and PGB HIGH, the port-B Parity Error Flag (PEFB) is held HIGH regardless of the levels applied to the B0-B35 inputs.

### PARITY GENERATION

A HIGH level on the port-A Parity Generate select (PGA) or port-B Parity Generate select (PGB) enables the IDT723611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the Parity Generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/EVEN select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-B Parity Generate select (PGB) and ODD/EVEN have setup and hold time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port Write/Read select (W/RA, W/RB) input is LOW, the port Mail select (MBA, MBB) input is HIGH, Chip Select (CSA, CSB) is LOW, Enable (ENA, ENB) is HIGH, and the port Parity Generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.

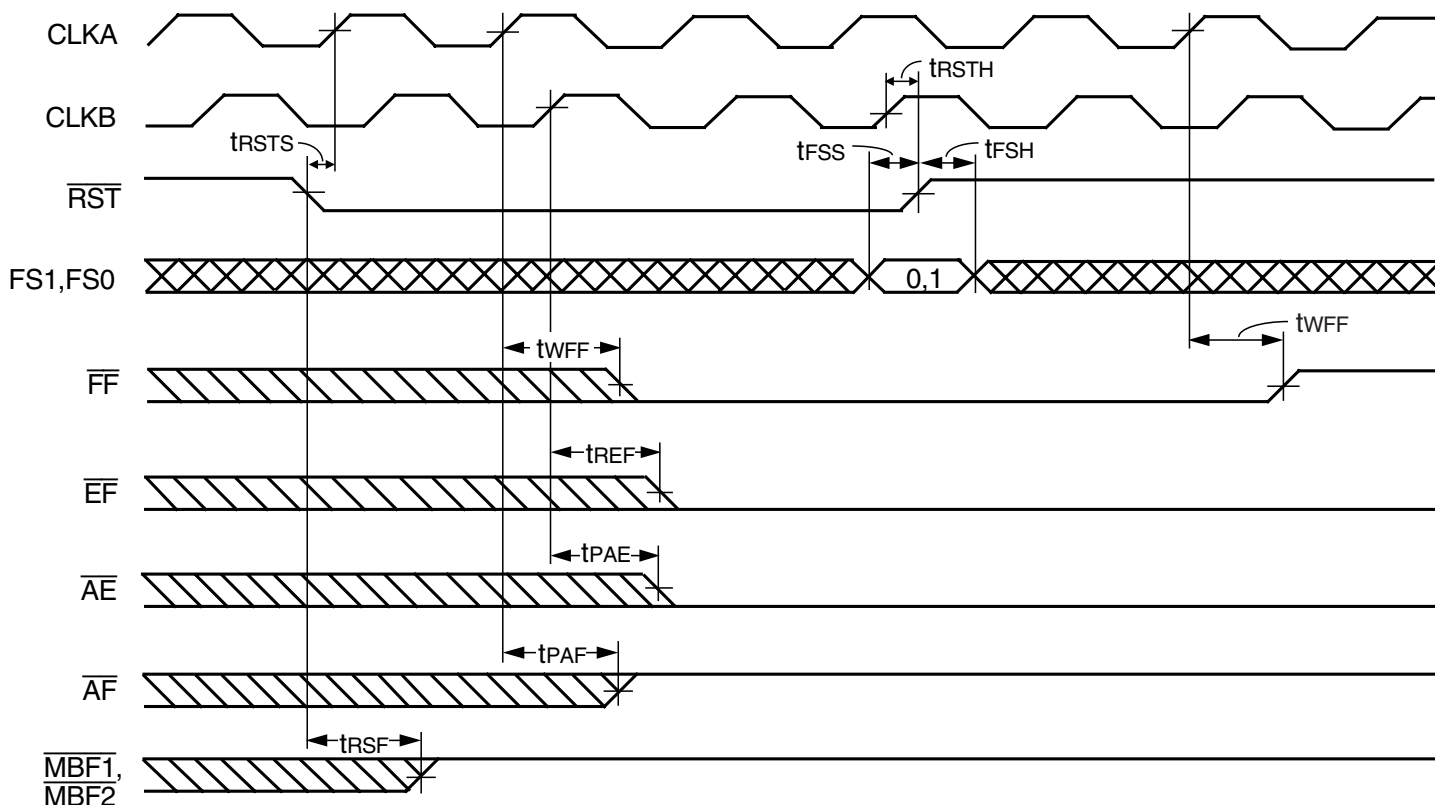
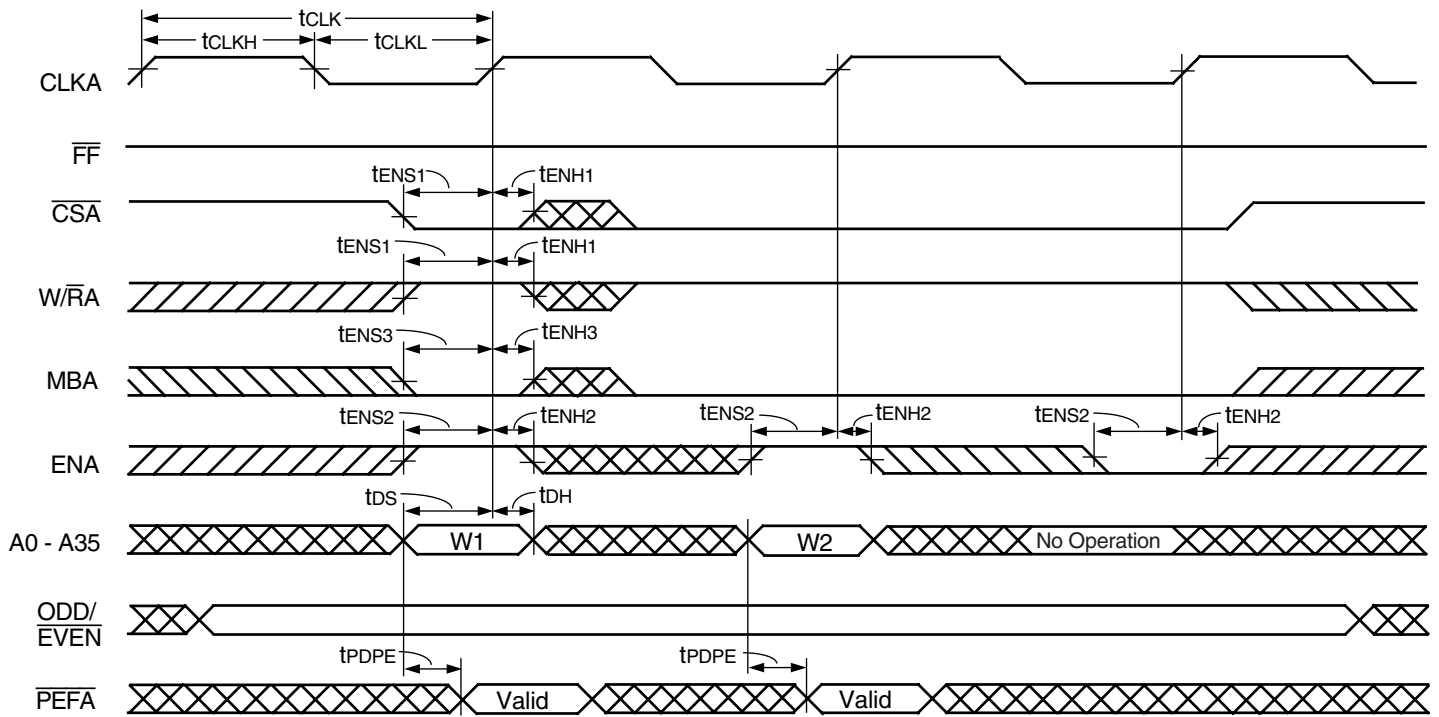


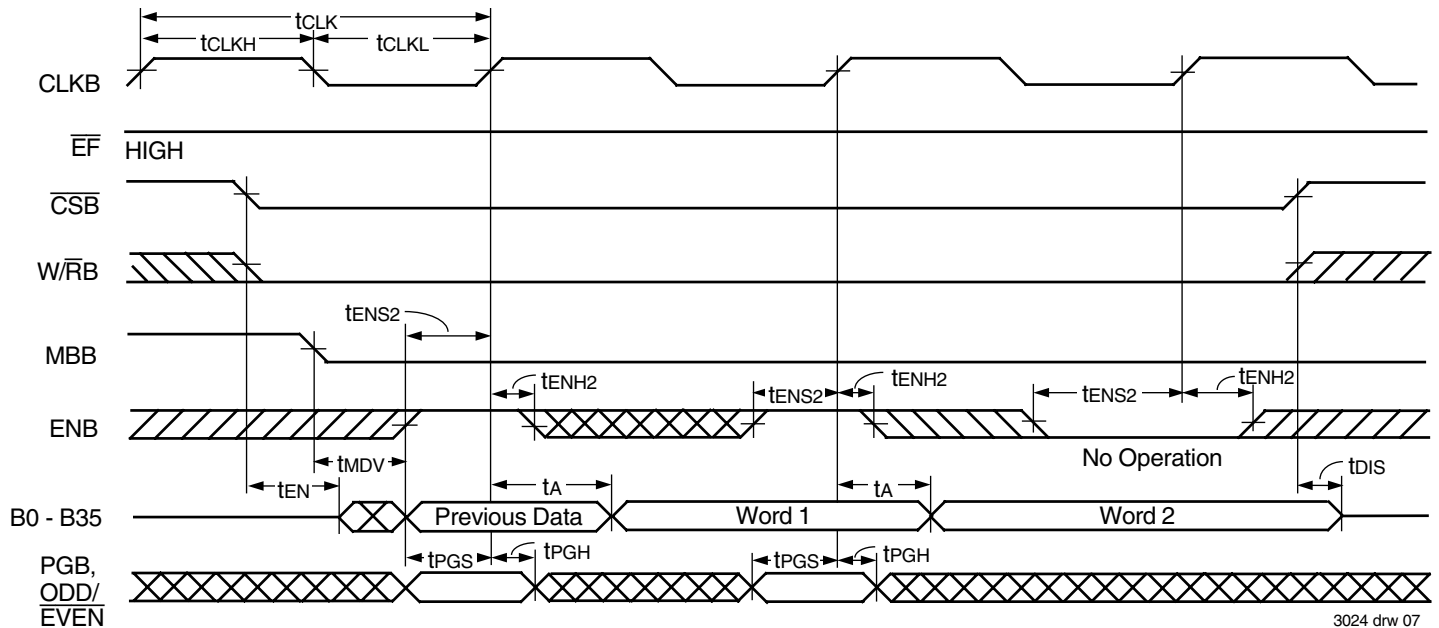
Figure 2. Device Reset Loading the X Register with the Value of Eight

3024drw 05



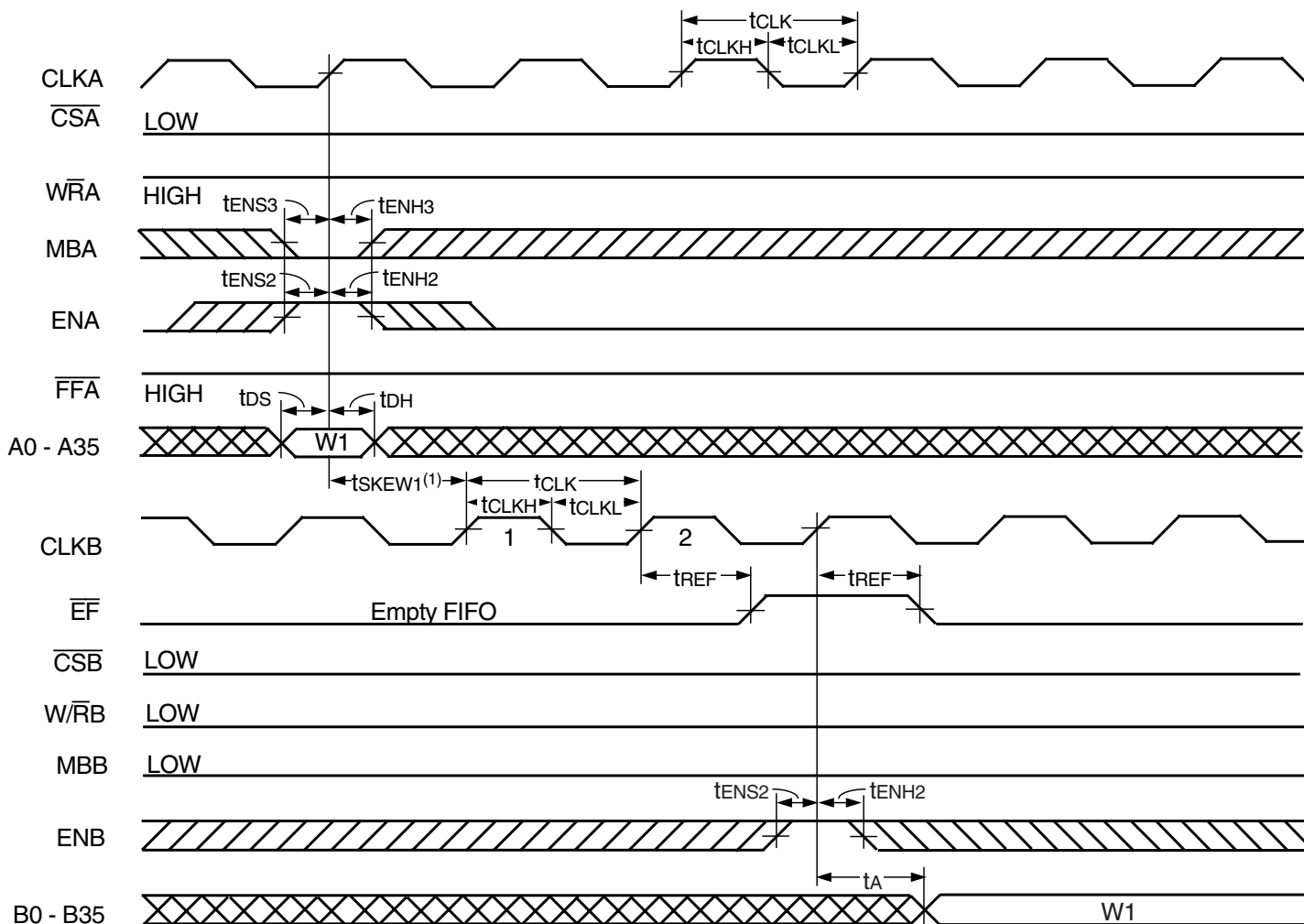
3024 drw 06

Figure 3. FIFO Write Cycle Timing



3024 drw 07

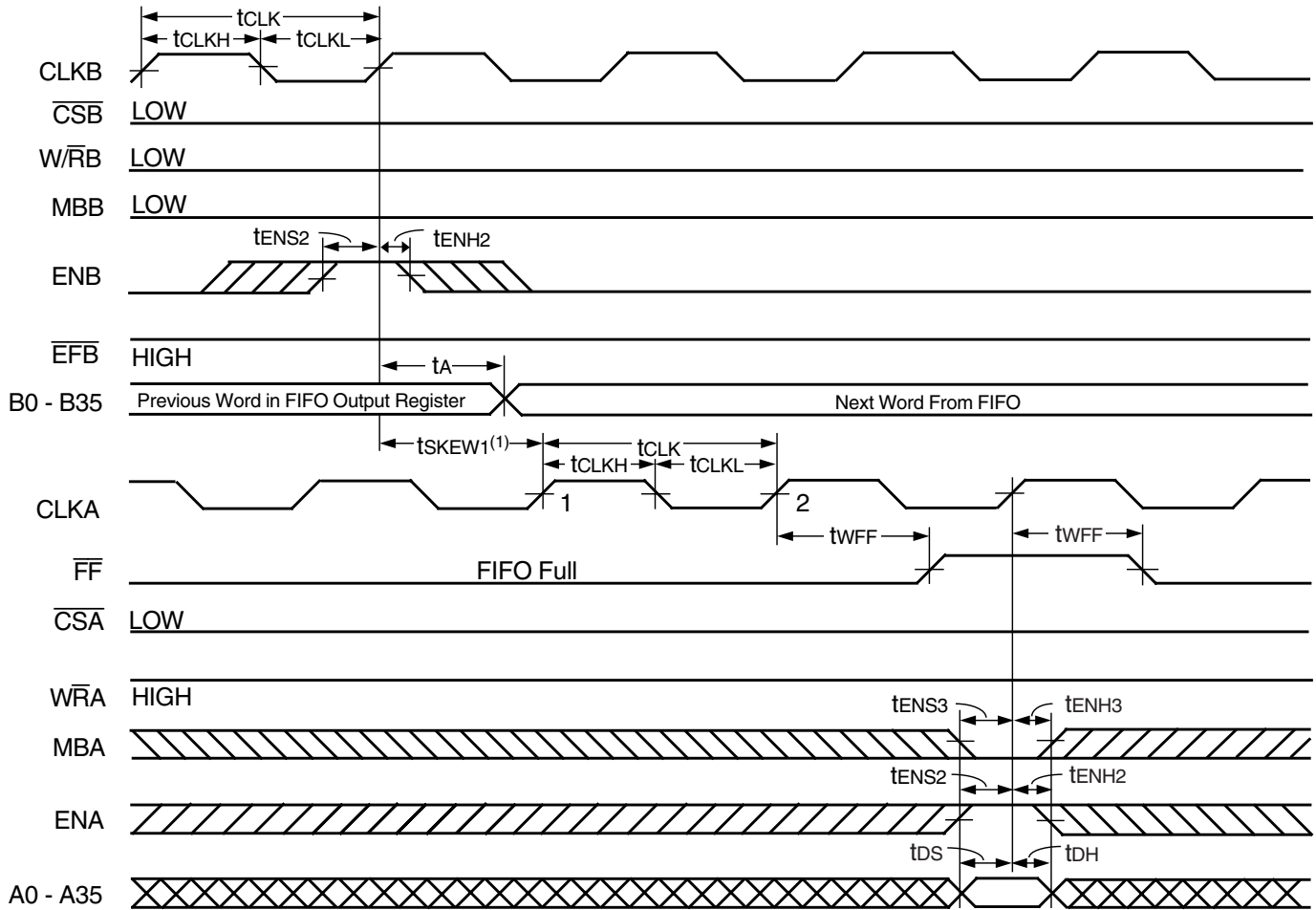
Figure 4. FIFO Read Cycle Timing



3024 drw 08

**NOTE:**  
1.  $t_{SKEW1}$  is the minimum time between a rising  $CLKA$  edge and a rising  $CLKB$  edge for  $\overline{EF}$  to transition HIGH in the next  $CLKB$  cycle. If the time between the rising  $CLKA$  edge and rising  $CLKB$  edge is less than  $t_{SKEW1}$ , then the transition of  $\overline{EF}$  HIGH may occur one  $CLKB$  cycle later than shown.

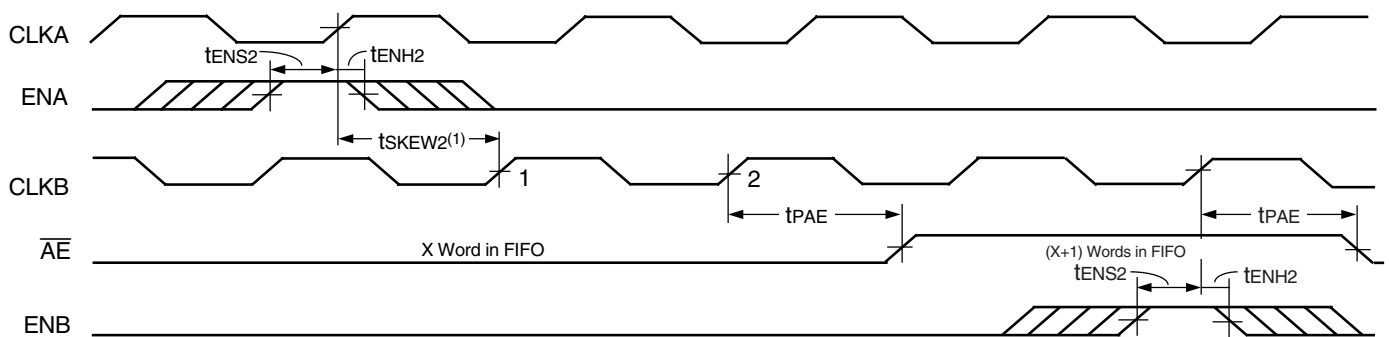
Figure 5.  $\overline{EF}$  Flag Timing and First Data Read when the FIFO is Empty



3024 drw 09

**NOTE:**  
1.  $t_{SKEW1}$  is the minimum time between a rising CLKB edge and a rising CLKA edge for  $\overline{FF}$  to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than  $t_{SKEW1}$ , then the transition of  $\overline{FF}$  HIGH may occur one CLKA cycle later than shown.

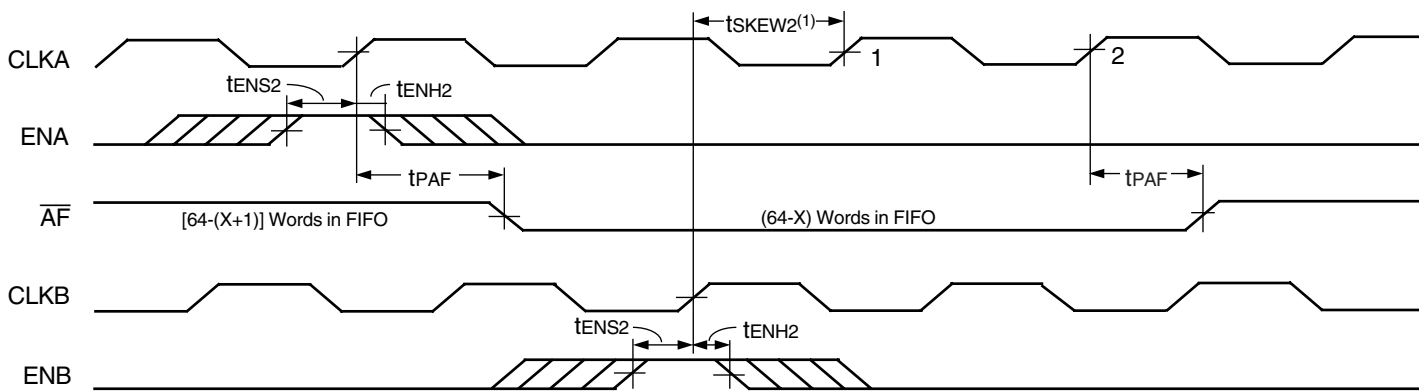
**Figure 6.  $\overline{FF}$  Flag Timing and First Available Write when the FIFO is Full**



3024 drw 10

**NOTES:**  
1.  $t_{SKEW2}$  is the minimum time between a rising CLKA edge and a rising CLKB edge for  $\overline{AE}$  to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than  $t_{SKEW2}$ , then  $\overline{AE}$  may transition HIGH one CLKB cycle later than shown.  
2. FIFO write ( $\overline{CSA} = L$ ,  $W/RA = H$ ,  $MBA = L$ ), FIFO read ( $\overline{CSB} = L$ ,  $W/RB = L$ ,  $MBB = L$ ).

**Figure 7. Timing for  $\overline{AE}$  when the FIFO is Almost-Empty**

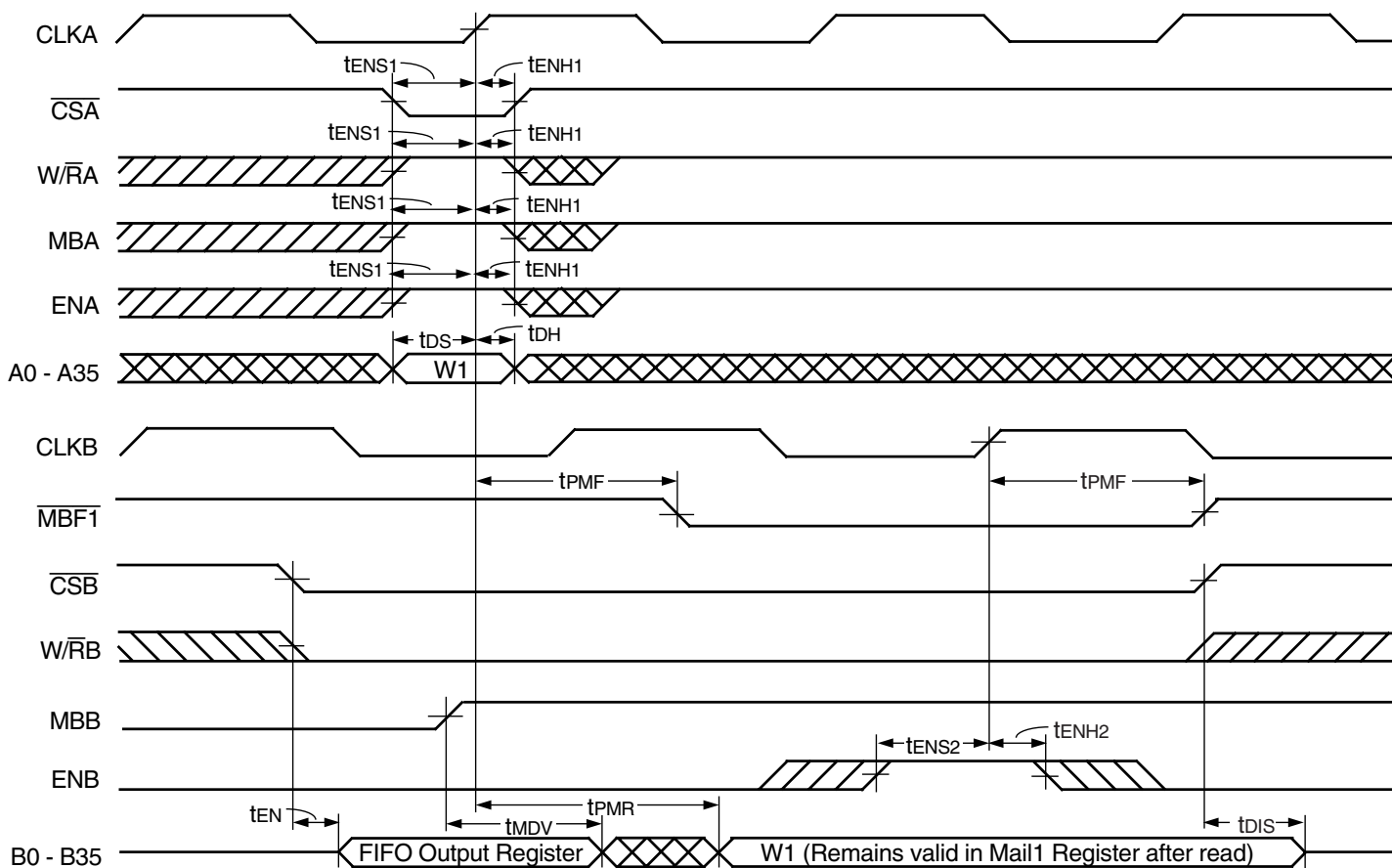


3024 drw 11

**NOTES:**

1.  $t_{SKEW2}$  is the minimum time between a rising CLKA edge and a rising CLKB edge for  $\overline{AF}$  to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than  $t_{SKEW2}$ , then  $\overline{AF}$  may transition HIGH one CLKB cycle later than shown.
2. FIFO write ( $\overline{CSA} = L, W/\overline{RA} = H, MBA = L$ ), FIFO read ( $\overline{CSB} = L, W/\overline{RB} = L, MBB = L$ ).

**Figure 8. Timing for  $\overline{AF}$  when the FIFO is Almost-Full**

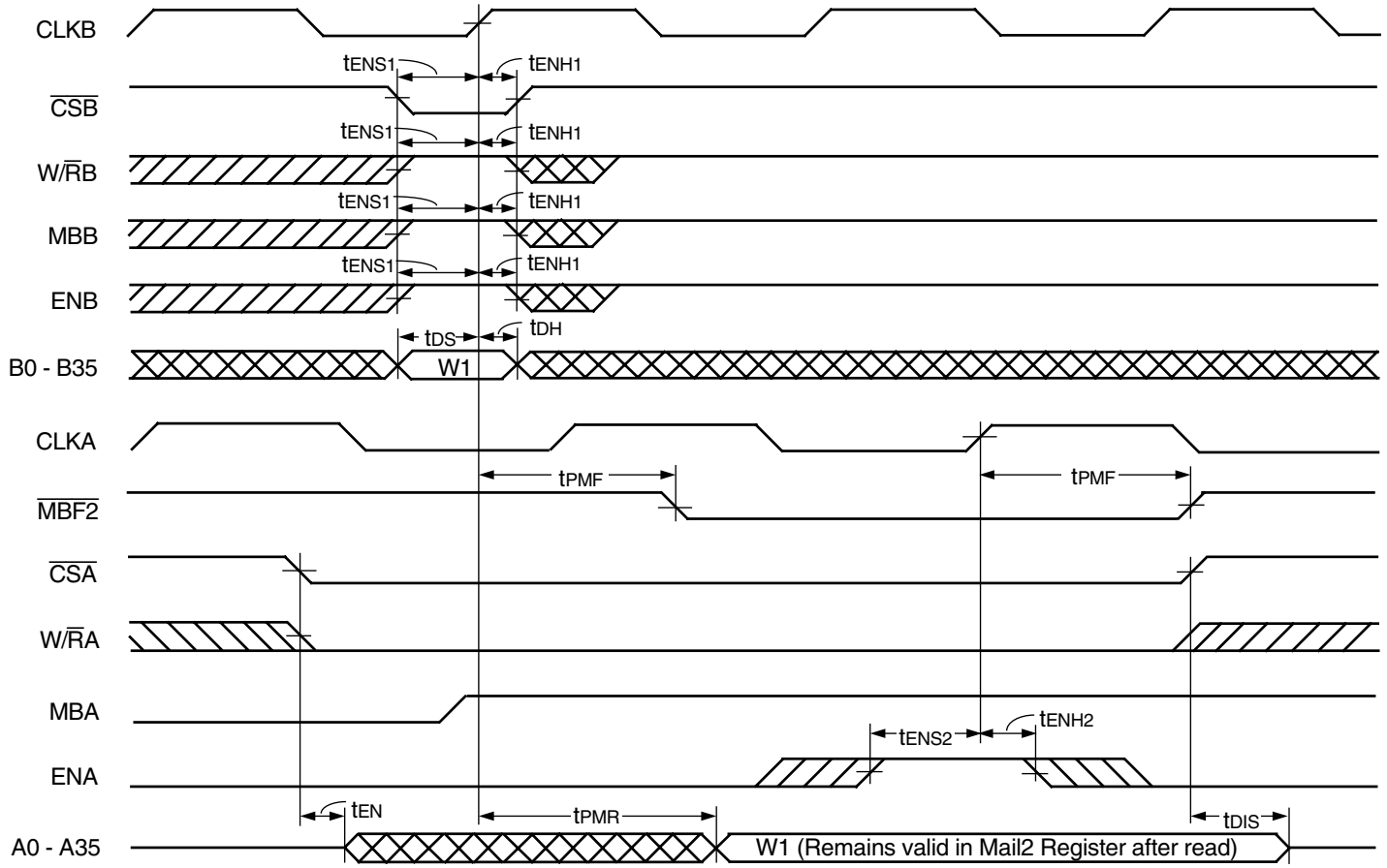


3024 drw 12

**NOTE:**

1. Port-B parity generation off ( $PGB = L$ )

**Figure 9. Timing for Mail1 Register and  $\overline{MBF1}$  Flag**

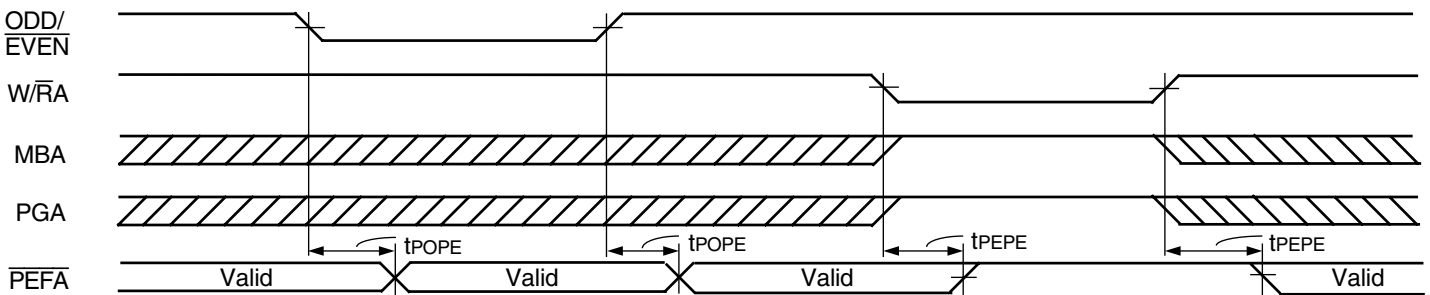


3024 drw 13

NOTE:

1. Port-A parity generation off (PGA = L)

Figure 10. Timing for Mail2 Register and  $\overline{MBF2}$  Flag

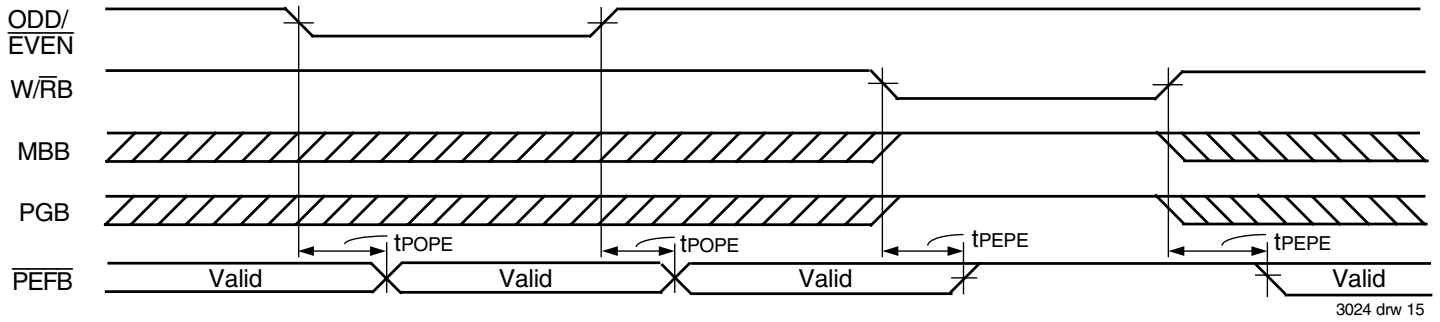


3024 drw 14

NOTE:

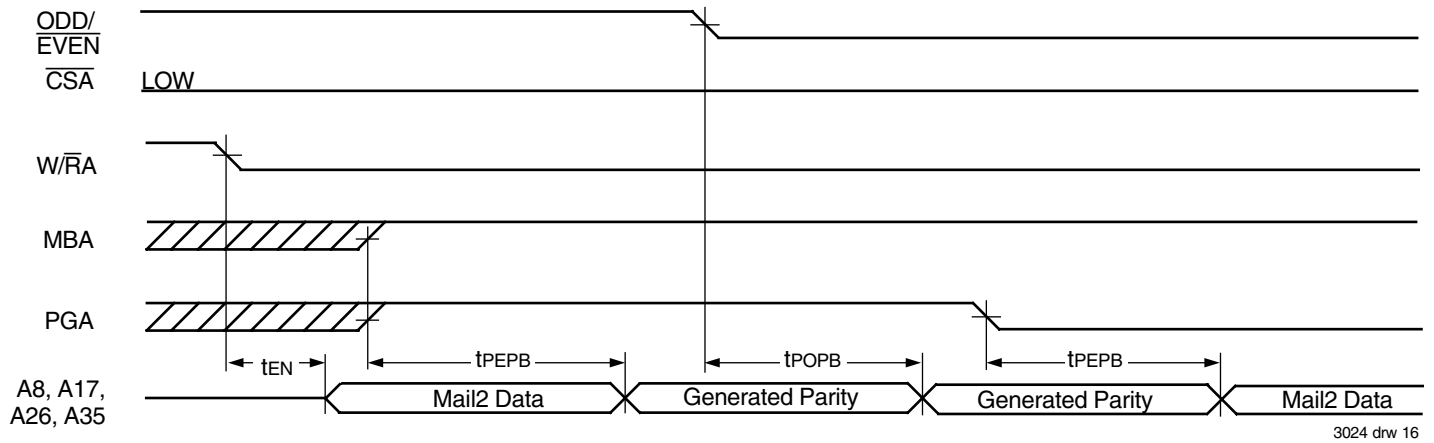
1.  $\overline{CSA}$  = L and ENA = H.

Figure 11. ODD/ $\overline{EVEN}$ ,  $\overline{W/RA}$ , MBA, and PGA to  $\overline{PEFA}$  Timing



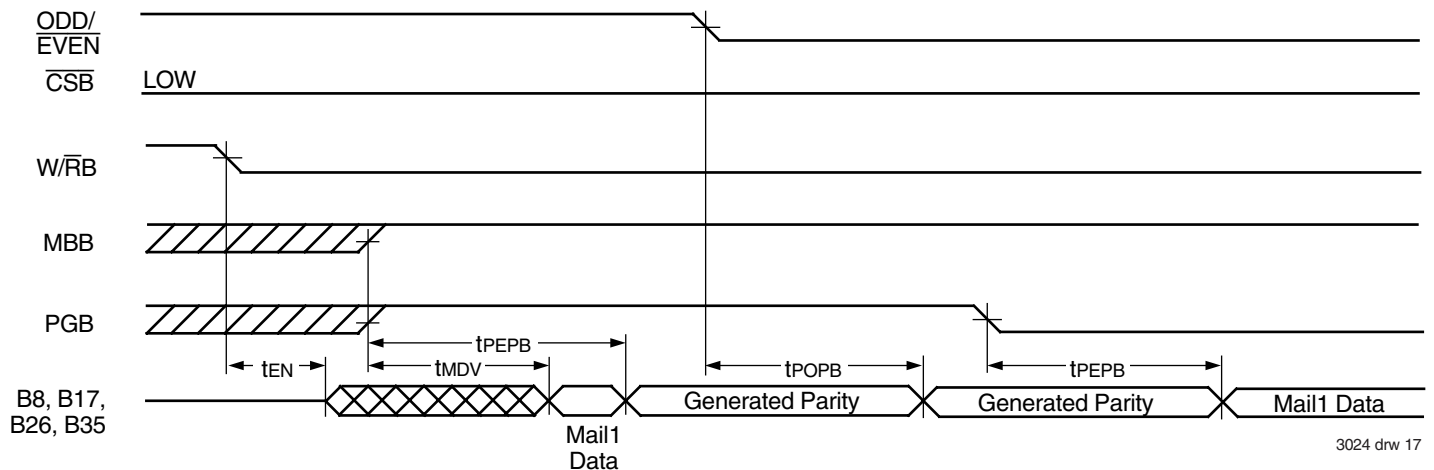
NOTE:  
1.  $\overline{CSB} = L$  and  $ENB = H$ .

Figure 12. ODD/ $\overline{EVEN}$ ,  $\overline{W/RB}$ ,  $\overline{MBB}$ , and  $\overline{PGB}$  to  $\overline{PEFB}$  Timing



NOTE:  
1.  $ENA = H$ .

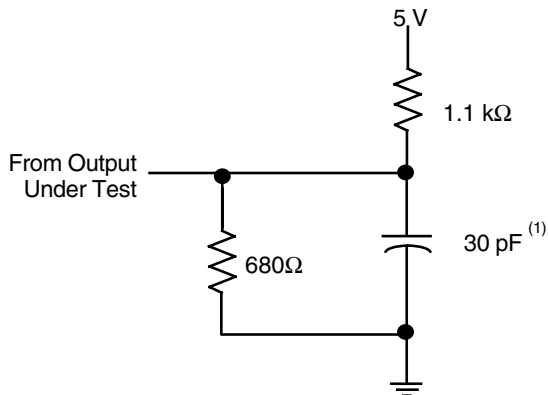
Figure 13. Parity Generation Timing when reading from the Mail2 Register



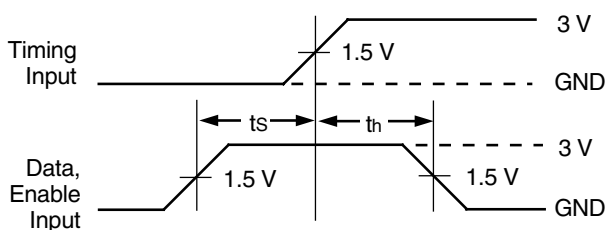
NOTE:  
1.  $ENB = H$ .

Figure 14. Parity Generation Timing when reading from the Mail1 Register

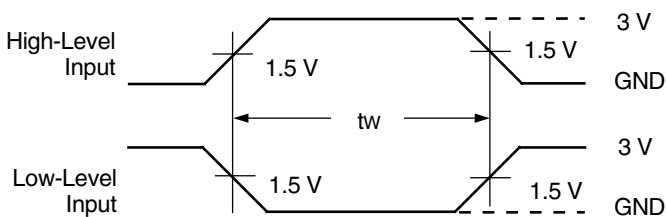
PARAMETER MEASUREMENT INFORMATION



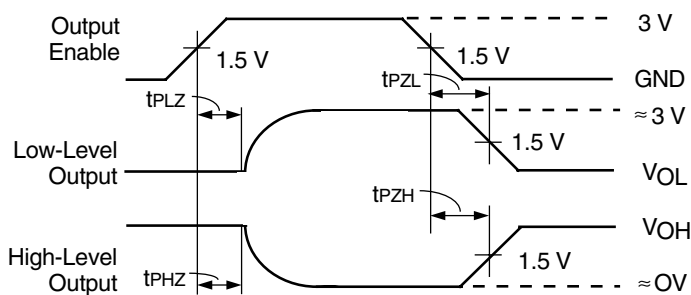
PROPAGATION DELAY  
LOAD CIRCUIT



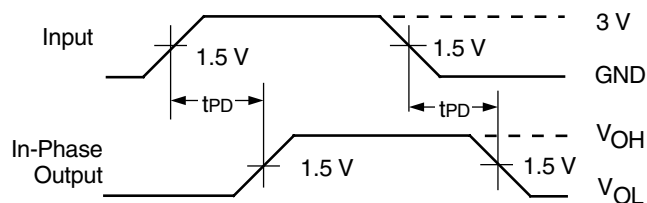
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES



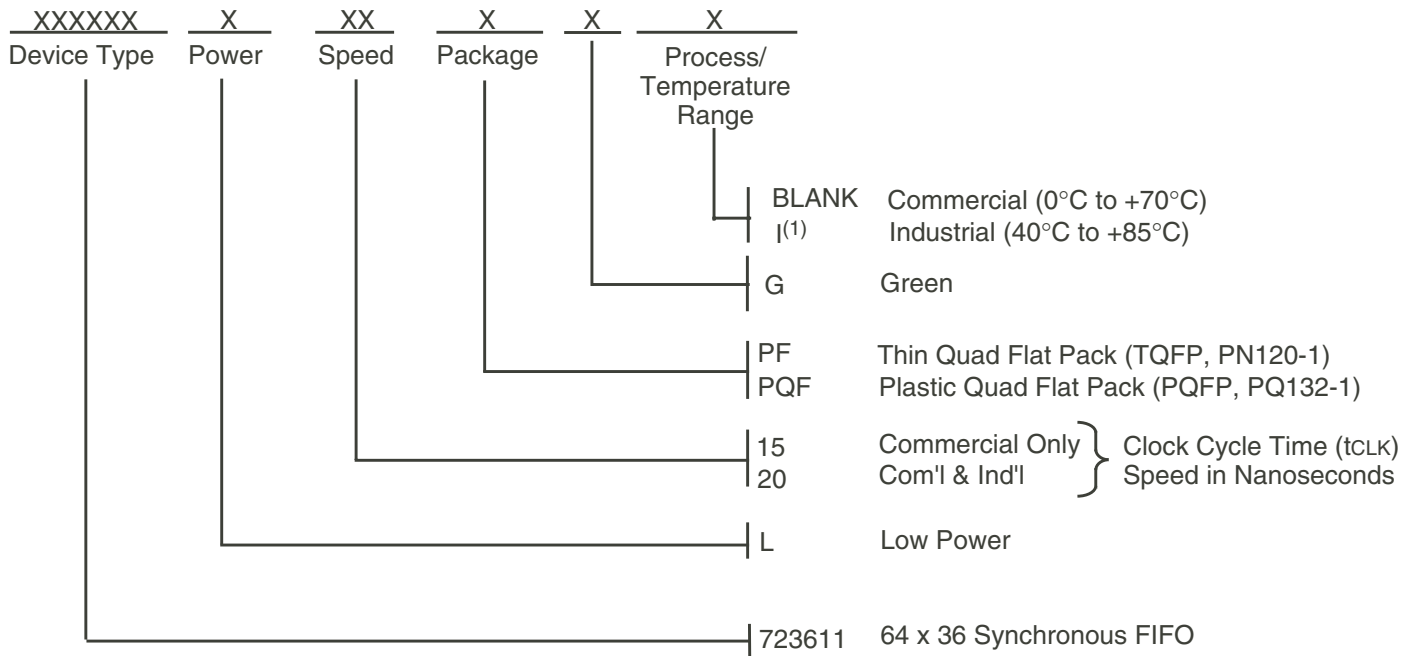
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

3024 drw 18

NOTE:  
1. Includes probe and jig capacitance.

Figure 16. Load Circuit and Voltage Waveforms

## ORDERING INFORMATION



3024 drw 19

### NOTES:

1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your sales office.

## DATASHEET DOCUMENT HISTORY

03/05/2002	pgs. 1, 6, 8, 9 and 20.
06/01/2005	pgs. 1,2,3 and 20.
02/13/2009	pg. 20.
07/31/2010	PDN# FS-10-04 issued. See IDT.com for PDN specifics.
10/21/2013	Datasheet changed to Obsolete Status.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.