

- ◆ Frequency Stability to Stratum 3 of GR-1244
- ◆ Low Cost ASIC Based Design
- ◆ Very Low Phase Jitter: < 1 pSec
- ◆ +3.3Vdc or +5.0Vdc Operation
- ◆ Precision Low Aging "AT" Cut Crystal
- ◆ Through-Hole or Surface Mount Configuration
- ◆ 6/6 RoHS Compliant



Electrical Characteristics

Parameter	Sym	Conditions	Min	Typical	Max	Unit
Power Requirements						
Power Supply	V _{cc}	± 5% 114L ± 5% 114S	3.135 4.75	3.30 5.0	3.465 5.25	Vdc Vdc
Turn-On Power	P _{max}	V _{cc} =Max. Std. Load		3.5	4.0	W
Steady State Power	P _{ss}	V _{cc} =Max. Std. Load @ +25°C		1.5		W
Warm-Up Time	T _{wu}	To within ± 0.3ppm @ +25°C			5	minutes
Frequency Stabilities						
Center Frequency	f _{nom}		8	10 12.8 16.384 19.44 20	38.88	MHz
Initial Tolerance	f _{cal}	T _a =+25°C (At time of Shipment)		±0.1		ppm
Freq. vs. Temp.	Δf/ΔTemp	0° to +70°C -40° to +85°C		±0.075 ±0.150	±0.125 ±0.250	ppm
Freq. vs. Voltage	Δf/ΔV _{cc}	V _{cc} ±5%		± 0.05		ppm
Freq. vs Time (Aging)	Δf/ΔTime	Per day 20 years		±0.005 ±2.5		ppm
24 Hour Holdover Stability	Δf/24Hr	Inclusive of Temp., Supply Variation and 24Hrs. Aging		±0.20	±0.37	ppm
Total Free-Running Accuracy	Δf/Life	All Cond. for 20 Yrs. (Ref. to f _{nom})			±4.6	ppm
Electronic Frequency Adjust (Optional)	Δf/V _c	f _{min} @ V _c =0V f _{max} @ V _c =V _{cc} f _{nom} @ V _c =0.5V _{cc}	±9.2			ppm
Waveform: CMOS Output						
Symmetry	Sym	@ 50% Level	40	50	60	%
Amplitude	V _o	Logic "1" Logic "0"	0.9V _{cc}		0.1V _{cc}	V V
Rise/Fall Times	t _r , t _f	20% to 80%		6	10	ns
Load	RL	Output to Ground		10kΩ // 15pF		
Phase Noise	P _n	Offset = 10Hz		-80		dBc/Hz
@ f _c =20MHz		100Hz		-115		dBc/Hz
		1kHz		-135		dBc/Hz
		10kHz		-140		dBc/Hz
		100kHz		-143		dBc/Hz
Phase Jitter		12kHz to 20MHz Bandwidth			1.0	ps RMS

