



512Kx32 SRAM MODULE *PRELIMINARY**

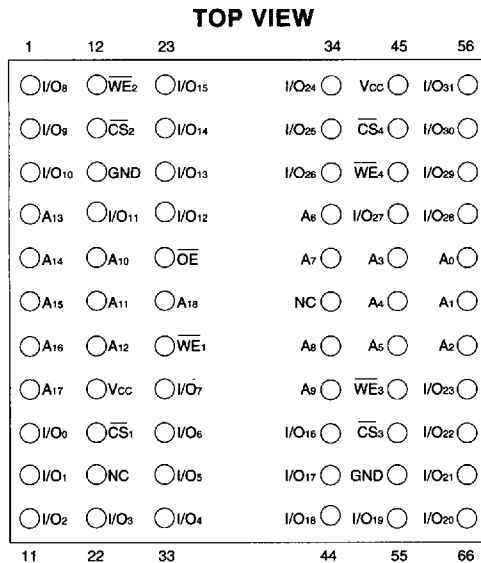
FEATURES

- Access Times of 17, 20, 25, 35, 45, 55nS
- Packaging
 - 66 pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402), SMD Number 5962-94611 (Pending)
 - 68 lead, 40mm Hermetic CQFP, 5.1mm (0.200") (Package 501) SMD Number 5962-95624 (Pending)
 - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") Package Under Development (Package 502)
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32-XHX - 13 grams typical
 - WS512K32-XG4X - 20 grams typical

* This data sheet describes a product under development and is subject to change, without notice.

4 SRAM MODULES

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH2X, SMD 5962-94611 (Pending)



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
WE ₁₋₄	Write Enables
CS ₁₋₄	Chip Selects
OE	Output Enable
V _{cc}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

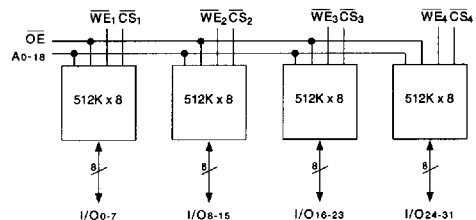
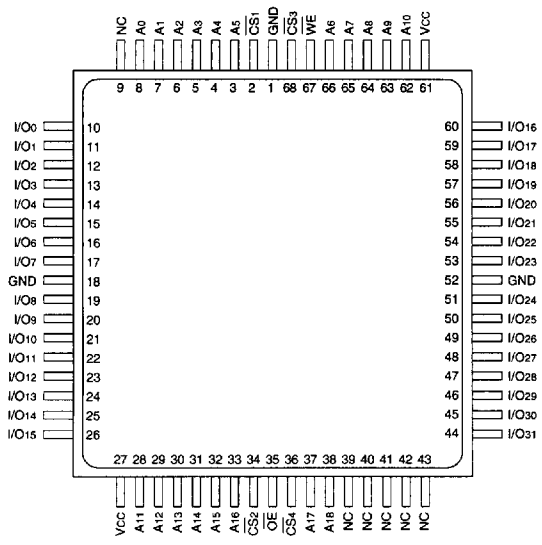




FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4X, SMD 5962-95624 (Pending)

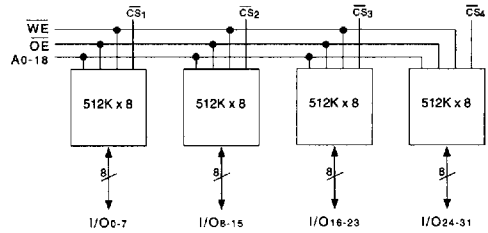
TOP VIEW



PIN DESCRIPTION

Table with 2 columns: Pin Name and Description. Includes I/O0-31, A0-18, WE, CS1-4, OE, Vcc, GND, and NC.

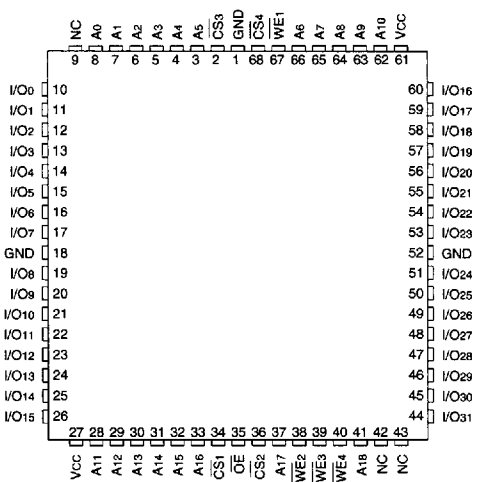
BLOCK DIAGRAM



4 SRAM MODULES

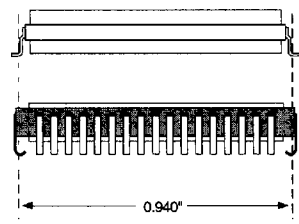
FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2X

TOP VIEW



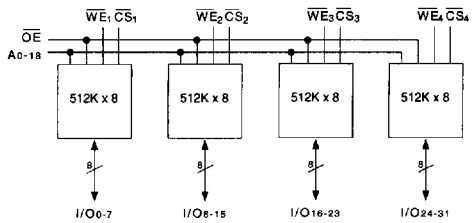
PIN DESCRIPTION

Table with 2 columns: Pin Name and Description. Includes I/O0-31, A0-18, WE1-4, CS1-4, OE, Vcc, GND.



The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Table with 5 columns: Parameter, Symbol, Min, Max, Unit. Rows include Operating Temperature, Storage Temperature, Signal Voltage Relative to GND, Junction Temperature, and Supply Voltage.

TRUTH TABLE

Table with 6 columns: CS, OE, WE, Mode, Data I/O, Power. Rows show combinations of control signals and their effects on data I/O and power state.

RECOMMENDED OPERATING CONDITIONS

Table with 5 columns: Parameter, Symbol, Min, Max, Unit. Rows include Supply Voltage, Input High Voltage, Input Low Voltage, and Operating Temp (Mil).

CAPACITANCE (TA = +25°C)

Table with 5 columns: Parameter, Symbol, Conditions, Max, Unit. Rows include OE capacitance, WE1-4 capacitance (HIP (PGA), CQFP G4, CQFP G2), CS1-4 capacitance, Data I/O capacitance, and Address input capacitance.

This parameter is guaranteed by design but not tested.

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DC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Table with 5 columns: Parameter, Symbol, Conditions, Min, Max, Units. Rows include Input Leakage Current, Output Leakage Current, Operating Supply Current x 32 Mode, Standby Current, Output Low Voltage, and Output High Voltage.

NOTE: DC test conditions: VIH = VCC - 0.3V, VIL = 0.3V

DATA RETENTION CHARACTERISTICS

(TA = -55°C to +125°C)

Table with 6 columns: Parameter, Symbol, Conditions, Min, Typ, Max, Units. Rows include Data Retention Supply Voltage and Data Retention Current.

* Also available in Low Power version, please call factory for information.



AC CHARACTERISTICS
(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Table with 13 columns: Parameter, Symbol, -17 (Min, Max), -20 (Min, Max), -25 (Min, Max), -35 (Min, Max), -45 (Min, Max), -55 (Min, Max), Units. Rows include Read Cycle Time, Address Access Time, Output Hold from Address Change, Chip Select Access Time, Output Enable to Output Valid, Chip Select to Output in Low Z, Output Enable to Output in Low Z, Chip Disable to Output in High Z, Output Disable to Output in High Z.

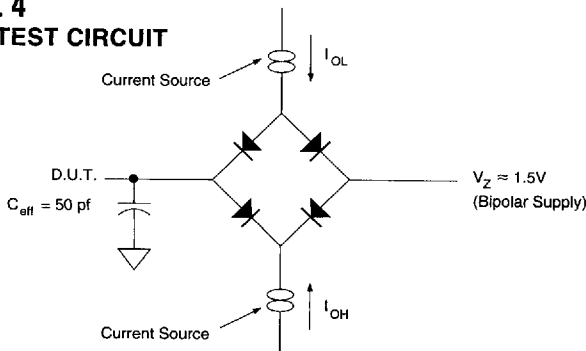
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Table with 13 columns: Parameter, Symbol, -17 (Min, Max), -20 (Min, Max), -25 (Min, Max), -35 (Min, Max), -45 (Min, Max), -55 (Min, Max), Units. Rows include Write Cycle Time, Chip Select to End of Write, Address Valid to End of Write, Data Valid to End of Write, Write Pulse Width, Address Setup Time, Address Hold Time, Output Active from End of Write, Write Enable to Output in High Z, Data Hold Time.

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

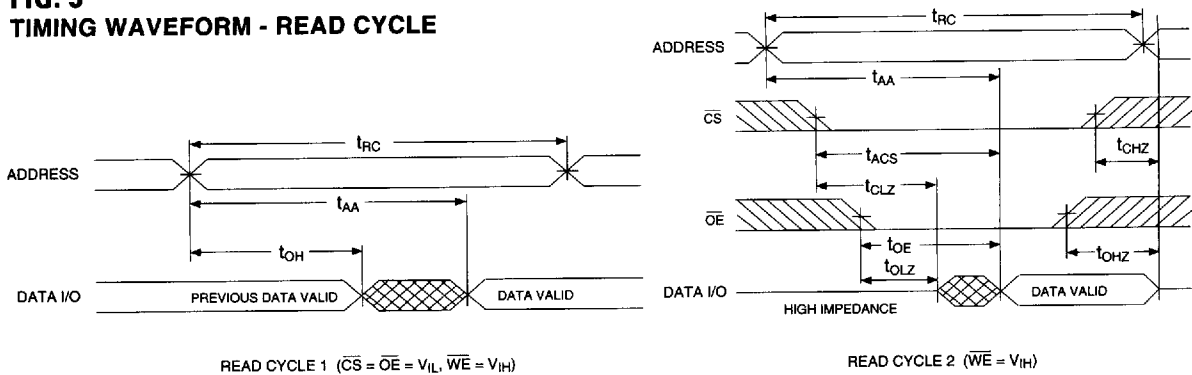
Table with 3 columns: Parameter, Typ, Unit. Rows include Input Pulse Levels, Input Rise and Fall, Input and Output Reference Level, Output Timing Reference Level.

NOTES:

Vz is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Zo = 75 Ohm.
Vz is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 5
TIMING WAVEFORM - READ CYCLE



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SRAM MODULES

FIG. 6
WRITE CYCLE - \overline{WE} CONTROLLED

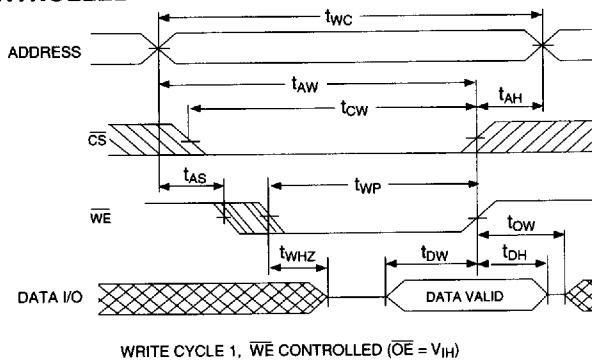
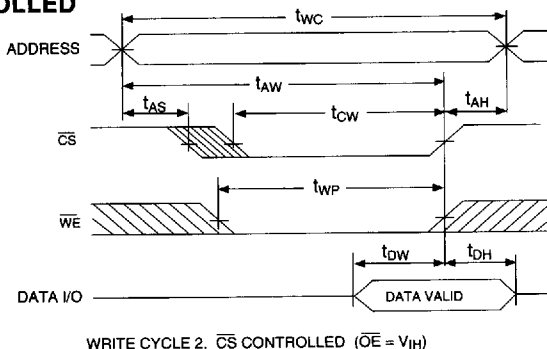


FIG. 7
WRITE CYCLE - \overline{CS} CONTROLLED





ORDERING INFORMATION

W S 512K 32 X - XXX X X

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to 85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H2 = Ceramic Hex-In-line Package, HIP (Package 402)
- G2 = 22mm Ceramic Quad Flat Pack, CQFP (Package 500)
- G4 = 40mm Ceramic Quad Flat Pack, CQFP (Package 501)
- G4T = 40mm Low Profile CQFP (Package 502)

ACCESS TIME IN nS

IMPROVEMENT MARK:

- N = No Connect at pin 21 and 39 in HIP for Upgrades

ORGANIZATION, 512Kx32

- User configurable as 1Mx16 or 2Mx8

SRAM

WHITE MICROELECTRONICS

4 SRAM MODULES

Device Type	Speed	Package	SMD Number
512K x 32 SRAM Module	55nS	66 pin HIP	5962-94611 05HXX*
512K x 32 SRAM Module	45nS	66 pin HIP	5962-94611 06HXX*
512K x 32 SRAM Module	35nS	66 pin HIP	5962-94611 07HXX*
512K x 32 SRAM Module	25nS	66 pin HIP	5962-94611 08HXX*
512K x 32 SRAM Module	20nS	66 pin HIP	5962-94611 09HXX*
512K x 32 SRAM Module	17nS	66 pin HIP	5962-94611 10HXX*
512K x 32 SRAM Module	55nS	68 pin CQFP	5962-95624 05HXX*
512K x 32 SRAM Module	45nS	68 pin CQFP	5962-95624 06HXX*
512K x 32 SRAM Module	35nS	68 pin CQFP	5962-95624 07HXX*
512K x 32 SRAM Module	25nS	68 pin CQFP	5962-95624 08HXX*
512K x 32 SRAM Module	20nS	68 pin CQFP	5962-95624 09HXX*
512K x 32 SRAM Module	17nS	68 pin CQFP	5962-95624 10HXX*

* Pending