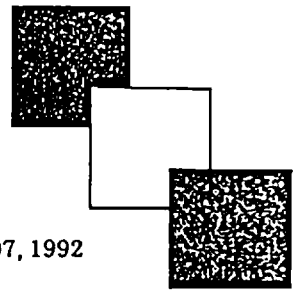
NEW PRODUCT

HB56G51232CC-××S Series

524,288-Word×32-Bit High Density Dynamic RAM Card



HITACHI

Rev.1
Dec. 07, 1992

Description

The HB56G51232CC-××S is a 512K×32 dynamic RAM Card, mounted 4 pieces of 4Mbit DRAM (HM51S4800ALTT) sealed in TSOP package.

An outline of the HB56G51232CC-××S is 88-pin two piece connector package.

Therefore, the HB56G51232CC-××S makes high density and it is possible to expand easily for memory system. The HB56G51232CC-××S provides common data inputs and outputs.

Decoupling capacitors are mounted each memory.

Feature

- 88-pin two piece connector package
  - Lead pitch 1.0mm
- Single 5V (± 5%) supply
- High speed
  - t_{RAC} ..... 70ns/80ns (max.)
  - t_{CAC} ..... 27ns (max.)
- Low power dissipation
  - Active mode ..... 2.36W/2.15W (max.)
  - Standby mode ..... 47.0mW (max.)
- Fast page mode capability
- 1,024refresh cycle / 128ms (Distributed Refresh)
- 3 variations of refresh
  - /RAS only refresh
  - /CAS before /RAS refresh
  - Self-refresh
- CMOS interface

Ordering information

Part No.	Access time	Package
HB56G51232CC-7ALS	70ns	88-pin 2 piece connector type
HB56G51232CC-8ALS	80ns	

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Pin Assignment

Pin Name	Pin No.
GND	1
DQ0	2
DQ1	3
DQ2	4
DQ3	5
DQ4	6
DQ5	7
DQ6	8
Vcc(5V)	9
DQ7	10
NC	11
NC	12
A0	13
A2	14
Vcc(5V)	15
A4	16
NC	17
A6	18
A8	19
NC	20
NC	21
/RAS0	22
/CAS0	23
/CAS1	24
NC	25
/RAS2	26
Vcc(5V)	27
PD2	28
PD4	29
PD6	30
NC	31
NC	32
NC	33
DQ9	34
NC	35
DQ10	36
Vcc(5V)	37
DQ11	38
DQ12	39
DQ13	40
DQ14	41
DQ15	42
DQ16	43
GND	44

Pin No.	Pin Name
45	GND
46	DQ18
47	DQ19
48	DQ20
49	DQ21
50	DQ22
51	DQ23
52	DQ24
53	DQ25
54	NC
55	NC
56	GND
57	A1
58	A3
59	A5
60	A7
61	A9
62	NC
63	GND
64	NC
65	NC
66	/CAS2
67	GND
68	/CAS3
69	NC
70	/WE
71	PD1
72	PD3
73	GND
74	PD5
75	PD7
76	PD8
77	NC
78	NC
79	NC
80	DQ27
81	DQ28
82	DQ29
83	DQ30
84	DQ31
85	DQ32
86	DQ33
87	DQ34
88	GND

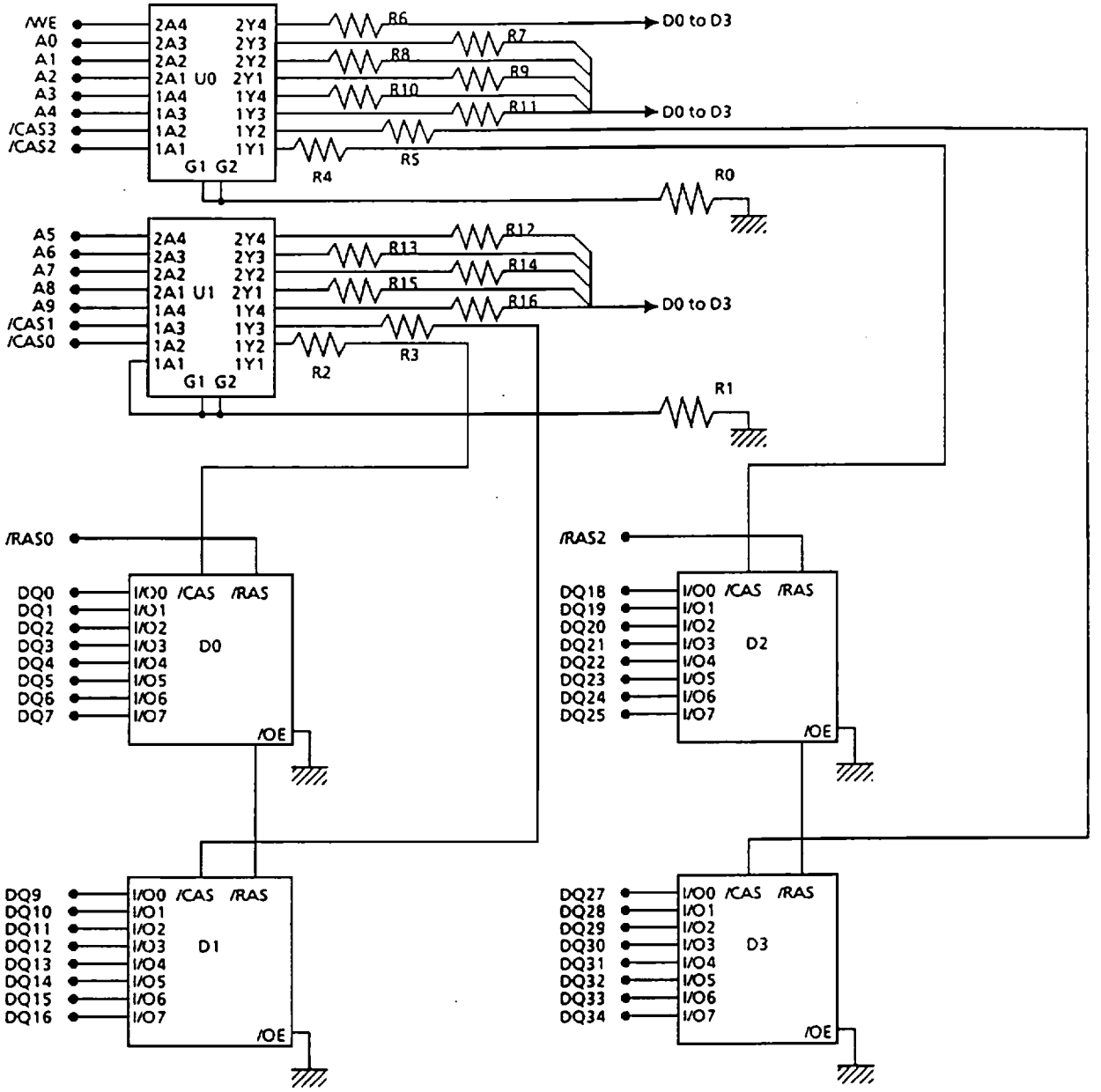
Pin Description

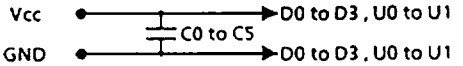
Pin Name	Description	
A0 to A9	Address input	
—	Row address	A0 to A9
—	Column address	A0 to A8
—	Refresh address	A0 to A9
/WE	Write enable	
/RAS0 , /RAS2	Row address strobe	
/CAS0 to /CAS3	Column address strobe	
DQ0 to DQ7 DQ9 to DQ16 DQ18 to DQ25 DQ27 to DQ34	Data input/output	
PD1 to PD8	Presence detect pins	
Vcc	Power supply	
GND	Ground	

Presence Detect Pinout

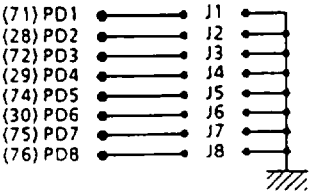
Pin Name	Pin No.	HB56G51232CC	
		-7ALS	-8ALS
PD1	71	NC	NC
PD2	28	Vss	Vss
PD3	72	Vss	Vss
PD4	29	Vss	Vss
PD5	74	NC	NC
PD6	30	Vss	NC
PD7	75	NC	Vss
PD8	76	Vss	Vss

Block Diagram



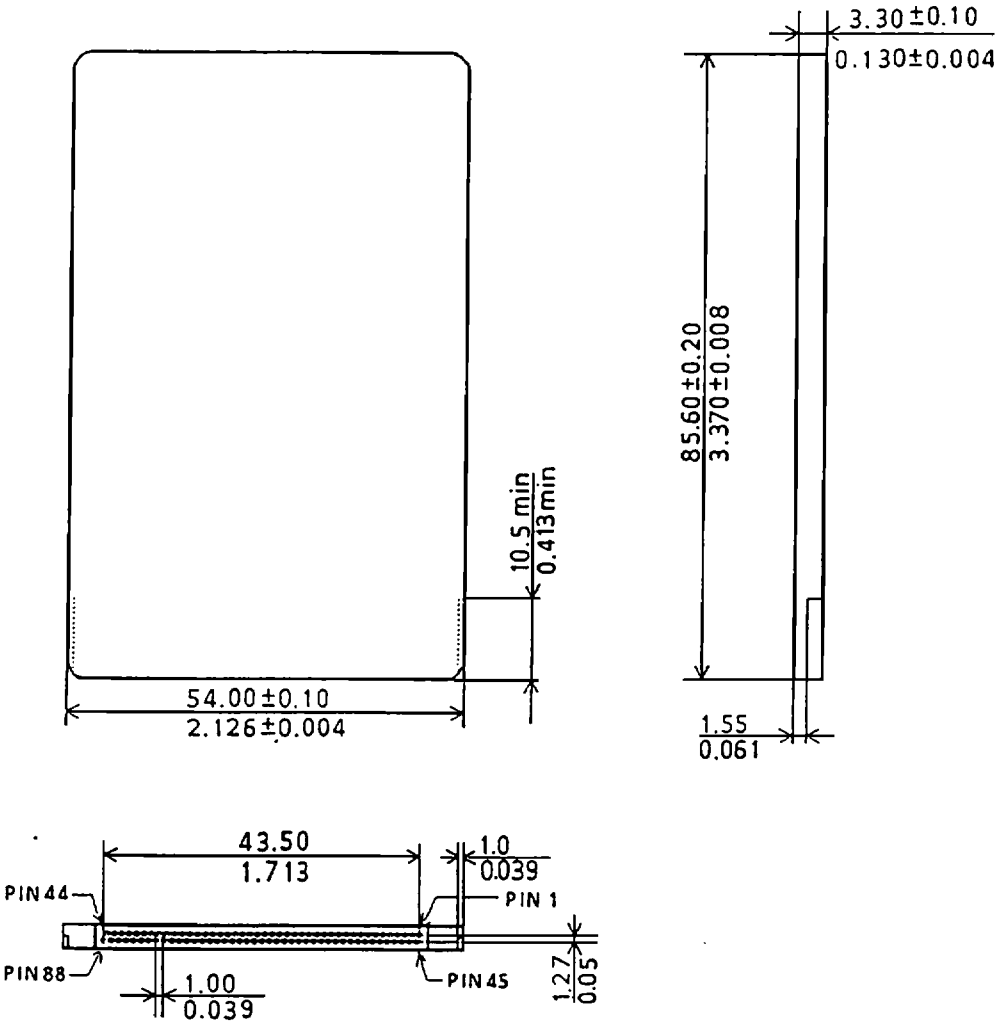


Note : D0 to D3 : HM51S4800ALTT
U0 to U1 : SN74AC11244PW
C0 to C9 : Chip Capacitor
R0 to R16 : Chip Resistor



■ Physical Outline

Unit : mm / inch



■ Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		I_{out}	50	mA
Power dissipation		P_T	4	W
Operating temperature		T_{opr}	0 to +55	°C
Storage temperature		T_{stg}	−40 to +85	°C

■ Electrical Characteristics

☆ Recommended DC Operating Conditions (T_a = 0 to +55°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	/RAS, DQ	V_{IH}	2.4	—	6.25	V	1
	Others pin		3.7	—	5.75		
Input low voltage	/RAS, DQ	V_{IL}	−1.0	—	0.8	V	1
	Others pin		−0.5	—	1.4		

Note : 1. All voltage referenced to V_{SS}

☆ DC Electrical Characteristics (Ta = 0 to +55°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) 4)

Parameter	Symbol	HB56G51232CC				Unit	Test Condition	Note
		-7ALS		-8ALS				
		Min.	Max.	Min.	Max.			
Operating current	I_{CC1}	–	450	–	410	mA	t_{RC} = min.	1,2
Standby current	I_{CC2}	–	9	–	9	mA	TTL interface /RAS = V_{IH} /CAS ≧ V_{CC} – 0.2V D_{OUT} = High-Z	
		–	1	–	1	mA	CMOS interface /RAS,/CAS ≧ V_{CC} – 0.2V D_{OUT} = High-Z	5
/RAS - only refresh current	I_{CC3}	–	450	–	410	mA	t_{RC} = min.	2
Standby current	I_{CC5}	–	20	–	20	mA	/RAS = V_{IH} /CAS ≧ V_{CC} – 0.2V D_{OUT} = enable	1
/CAS before /RAS refresh current	I_{CC6}	–	450	–	410	mA	t_{RC} = min.	
Page mode current	I_{CC7}	–	450	–	410	mA	t_{PC} = min.	1,3
Self - refresh mode current	I_{CC9}	–	1	–	1	mA	CMOS interface /RAS,/CAS ≦ 0.2V D_{OUT} = High-Z	
Battery backup current (Standby with CBR refresh)	I_{CC10}	–	2	–	2	mA	Standby:CMOS interface D_{OUT} = High-Z CBR refresh:t_{RC} = 125μs t_{RAS} ≦ 1μs /WE = V_{IH}, /CAS = V_{IL}	5
Input leakage current	I_{LI}	–10	10	–10	10	μA	0V ≦ V_{IN} ≦ 7V	
Output leakage current	I_{LO}	–10	10	–10	10	μA	0V ≦ V_{OUT} ≦ 7V D_{OUT} = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{OUT} = –5mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{OUT} = 4.2mA	

Note : 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed once or less while /RAS = V_{IL}.
3. Address can be changed once or less while /CAS = V_{IH}.
4. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.
5. $t_{RAS} = t_{RAS(min)}$ to 1μS
Input voltage : All pins : V_{IH} ≧ V_{CC} – 0.2V or V_{IL} ≦ 0.2V.

☆ Capacitance ($Ta = 25°C$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input capacitance (Address)	C_{I1}	–	20	pF	1
Input capacitance (/WE, /CAS)	C_{I2}	–	20	pF	1
Input capacitance (/RAS)	C_{I3}	–	35	pF	1
Output capacitance (DQ0 to DQ7, DQ9 to DQ16 DQ18 to DQ25, DQ27 to DQ34)	$C_{I/O}$	–	25	pF	1,2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. /CAS = V_{IH} to disable D_{OUT}.

☆ AC Characteristics ($Ta = 0$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$) 1), 14)

- Read, Write and Refresh Cycle (Common parameters)

Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
Ramdom read or write cycle time	t_{RC}	130	–	150	–	ns	
/RAS precharge time	t_{RP}	50	–	60	–	ns	
/RAS pulse width	t_{RAS}	70	10000	80	10000	ns	
/CAS pulse width	t_{CAS}	20	10000	20	10000	ns	
Row address set-up time	t_{ASR}	7	–	7	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	ns	
/RAS to /CAS delay time	t_{RCD}	20	43	20	53	ns	8
/RAS to column address delay time	t_{RAD}	15	28	15	33	ns	9
/RAS hold time	t_{RSH}	27	–	27	–	ns	
/CAS hold time	t_{CSH}	70	–	80	–	ns	
/CAS to /RAS precharge time	t_{CRP}	15	–	15	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	–	128	–	128	ms	15

- Read Cycle

Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
Access time from /RAS	t_{RAC}	–	70	–	80	ns	2,3
Access time from /CAS	t_{CAC}	–	27	–	27	ns	3,4,13
Access time from address	t_{AA}	–	42	–	47	ns	3,5,13
Read command set-up time	t_{RCS}	7	–	7	–	ns	
Read command hold time to /CAS	t_{RCH}	0	–	0	–	ns	
Read command hold time to /RAS	t_{RRH}	0	–	0	–	ns	
Column address to /RAS lead time	t_{RAL}	42	–	47	–	ns	
Output buffer turn-off time	t_{OFF}	0	22	0	22	ns	6

- Write Cycle

Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
Write command set-up time	t_{WCS}	0	–	0	–	ns	10
Write command hold time	t_{WCH}	15	–	15	–	ns	
Write command pulse width	t_{WP}	10	–	10	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	11
Data-in hold time	t_{DH}	22	–	22	–	ns	11

- Refresh Cycle

Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
/CAS set-up time (/CAS before /RAS refresh cycle)	t_{CSR}	17	–	17	–	ns	
/CAS hold time (/CAS before /RAS refresh cycle)	t_{CHR}	10	–	10	–	ns	
/RAS precharge to /CAS hold time	t_{RPC}	10	–	10	–	ns	
/CAS precharge time in normal mode	t_{CPN}	10	–	10	–	ns	

- Fast Page Mode Cycle

Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
Fast page mode cycle time	t_{PC}	45	–	50	–	ns	
Fast page mode /CAS precharge time	t_{CP}	10	–	10	–	ns	
Fast page mode /RAS pulse width	t_{RASC}	–	100000	–	100000	ns	12
Access time from /CAS precharge	t_{ACP}	–	47	–	52	ns	3,13
/RAS hold time from /CAS precharge	t_{RHCP}	47	–	52	–	ns	

- Self-refresh mode

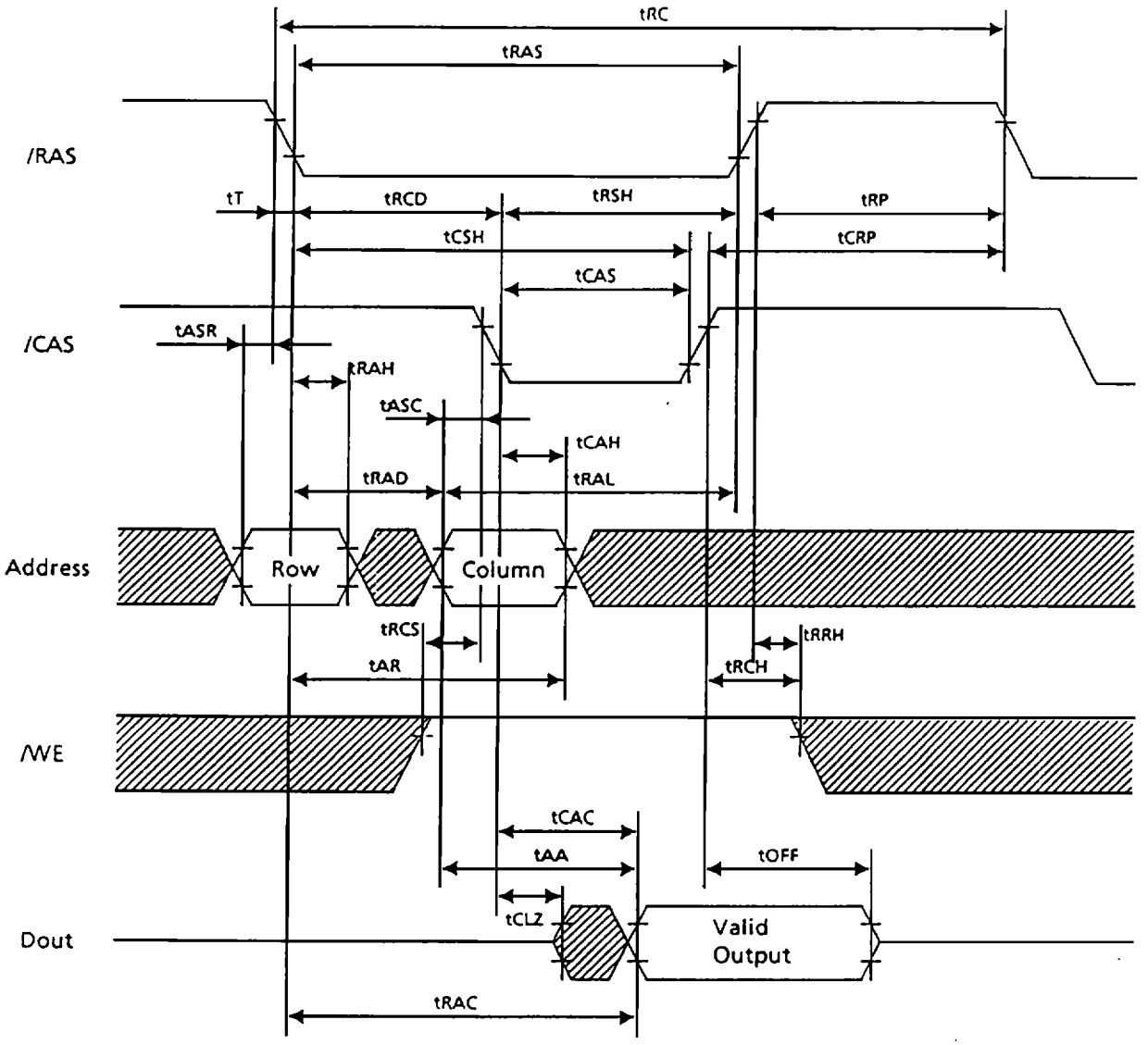
Parameter	Symbol	HB56G51232CC				Unit	Note
		-7ALS		-8ALS			
		Min.	Max.	Min.	Max.		
/RAS pulse width (self-refresh)	t_{RASS}	100	–	100	–	μs	
/RAS precharge time (self-refresh)	t_{RPS}	130	–	150	–	ns	
/CAS hold time (self-refresh)	t_{CHS}	-57	–	-57	–	ns	16

Notes

1. AC measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) and $t_{RAD} \leqq t_{RAD}$ (max.).If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.), $t_{RAD} \leqq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.), $t_{RAD} \geqq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geqq t_{WCS}$ (min.))
11. These parameters are referenced to /CAS leading edge in an early write cycle.
12. t_{RASC} defines /RAS pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (/RAS clock such as /RAS-only refresh).
15. t_{REF} defines is 1,024 refresh cycles.
16. Repetitive self-refresh mode without refreshing all memory is not allowed. Once you exit from self-refresh mode, all memory cells need to be refreshed before re-entering the self-refresh mode again.

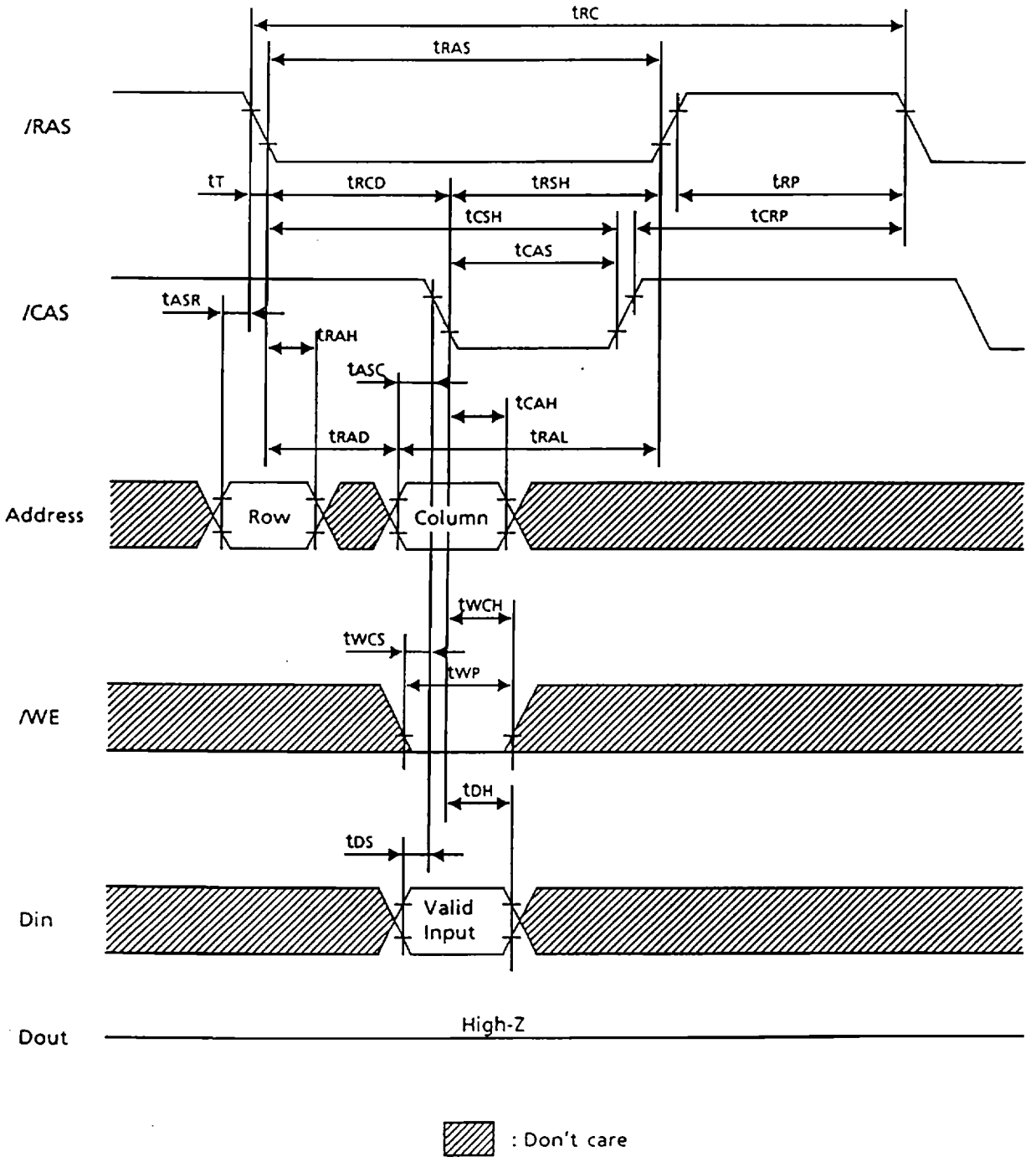
■ Timing waveform

Read cycle

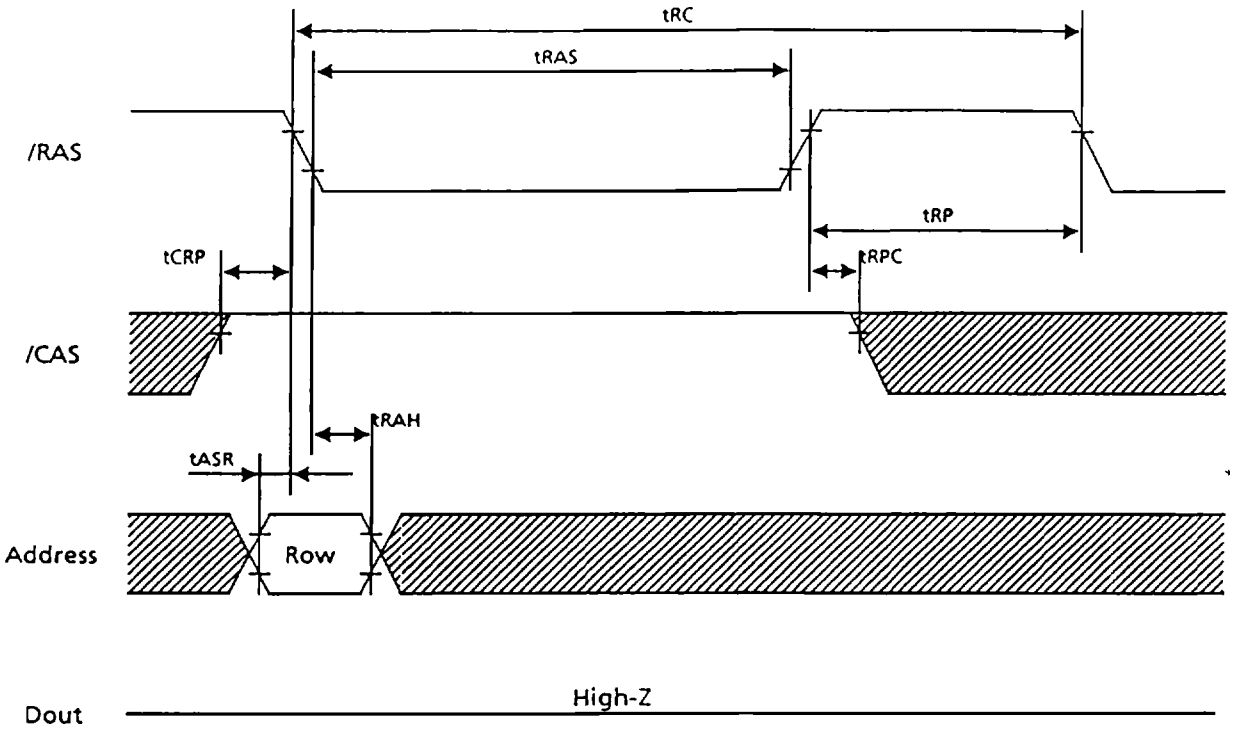


: Don't care

Early Write Cycle

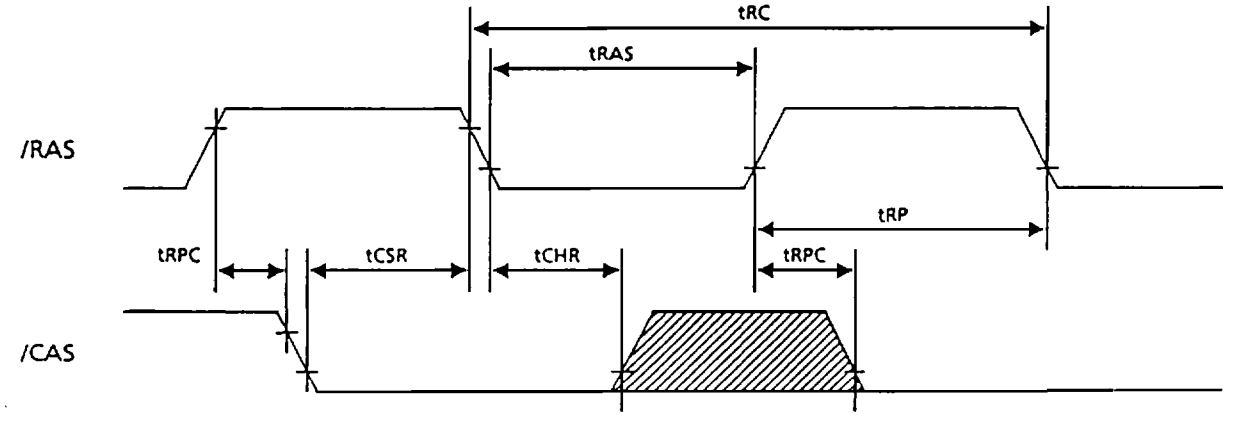


/RAS Only Refresh Cycle



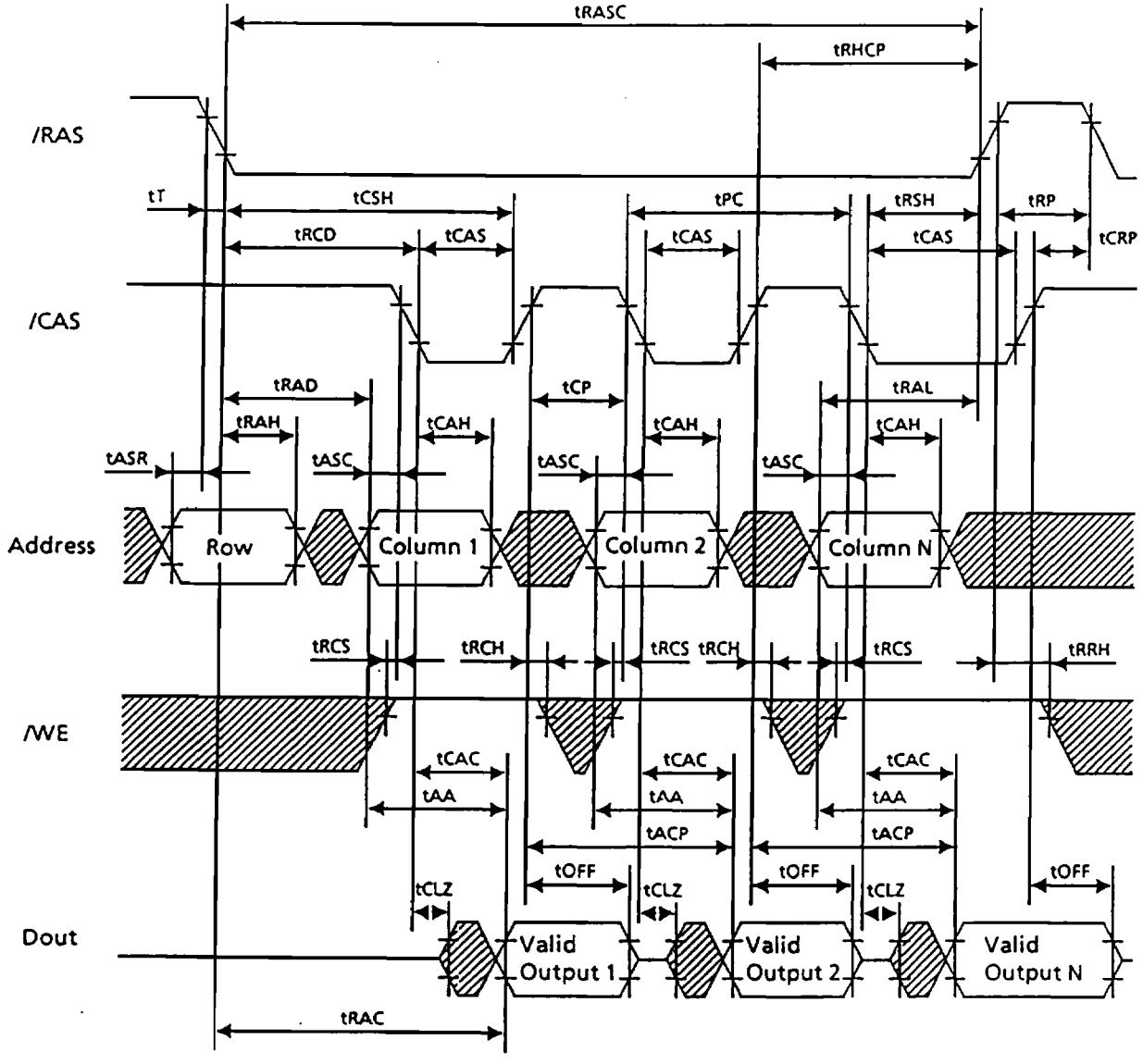
1 /WE : Don't care
2 ▨ : Don't care

/CAS before /RAS Refresh Cycle



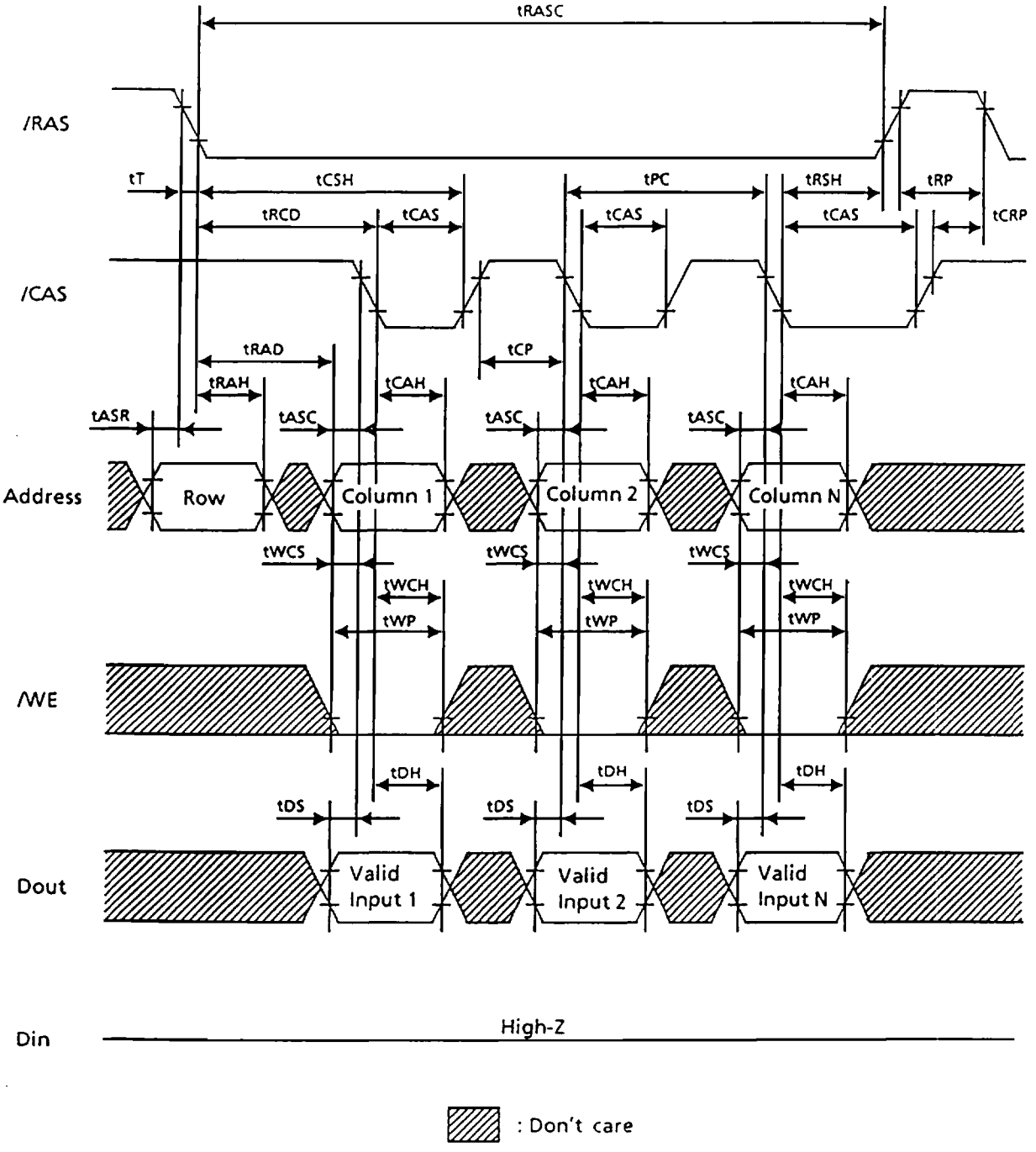
1 Address, Din : Don't care
2 Dout: High-Z
3 ▨ : Don't care
4 /WE = VIH

Fast Page Mode Read Cycle

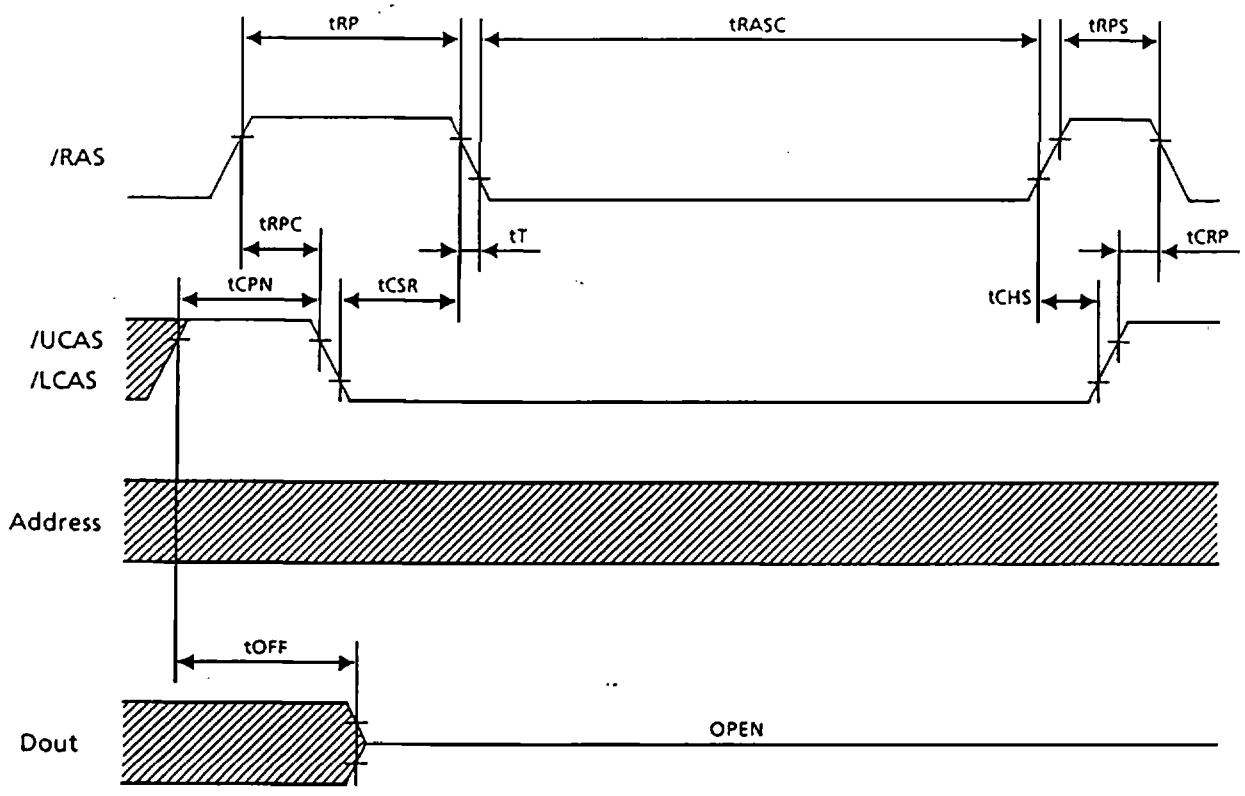


: Don't care

Fast Page Mode Early Write Cycle



Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, 10 μs ≦ t_{RASS} ≧ 100 μs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≧ 100 μs, then /RAS precharge time should use t_{RPS} instead of t_{RP}.
2. If you use /RAS only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

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Revision Record

Rev.	Date	Content of Modification	Drawn by	Approved by
0	Oct. 30. '92	Initial issue	T.Sugano	K.Yamazaki
1	Dec.07.'92	Change the part name from HB56GS51232CC to HB56G51232CC-××S	T. Sugano	K. Yamazaki