National Semiconductor

54F/74F401
CRC Generator/Checker

General Description

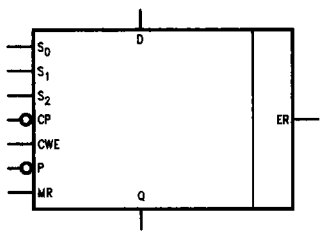
The 'F401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 'F401 is fully compatible with all TTL families.

Features

- Eight selectable polynomials
- Error indicator
- Separate preset and clear controls
- Automatic right justification
- Fully compatible with all TTL logic families
- 14-pin package
- 9401 equivalent
- Typical applications:
  - Floppy and other disk storage systems
  - Digital cassette and cartridge systems
  - Data communication systems

Ordering Code: See Section 5

Logic Symbol



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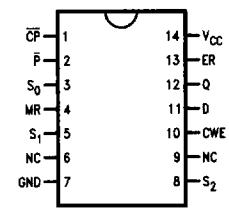
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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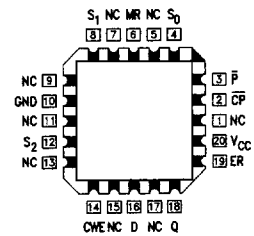
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0–S_2	Polynomial Select Inputs	1.0/1.0	20 μA/−0.6 mA
D	Data Input	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}$	Clock Input (Operates on HIGH-to-LOW Transition)	1.0/1.0	20 μA/−0.6 mA
CWE	Check Word Enable Input	1.0/1.0	20 μA/−0.6 mA
$\overline{P}$	Preset (Active LOW) Input	1.0/1.0	20 μA/−0.6 mA
MR	Master Reset (Active HIGH) Input	1.0/1.0	20 μA/−0.6 mA
Q	Data Output	50/33.3	−1 mA/20 mA
ER	Error Output	50/33.3	−1 mA/20 mA

Functional Description

The 'F401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F401 implements the polynomials listed in Table I by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 'F401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates *(Figure 1)*. The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating *(Figure 2)*.

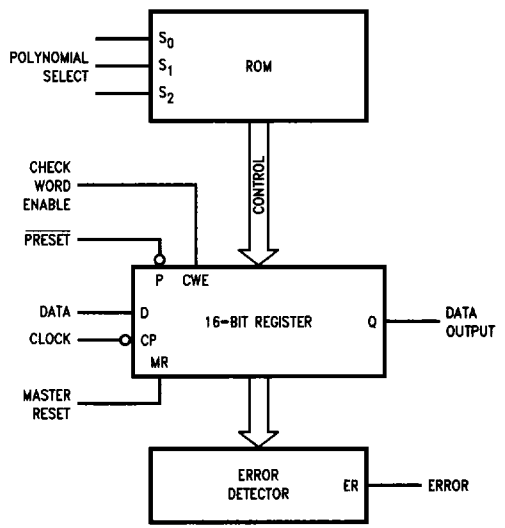
To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 'F401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 'F401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12- or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE I

Select Code			Polynomial	Remarks
S_2	S_1	S_0		
L	L	L	$X^{16} + X^{15} + X^2 + 1$	CRC-16
L	L	H	$X^{16} + X^{14} + X + 1$	CRC-16 REVERSE
L	H	L	$X^{16} + X^{15} + X^{13} + X^7 + X^4 + X^2 + X^1 + 1$	
L	H	H	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	CRC-12
H	L	L	$X^8 + X^7 + X^5 + X^4 + X + 1$	
H	L	H	$X^8 + 1$	LRC-8
H	H	L	$X^{16} + X^{12} + X^5 + 1$	CRC-CCITT
H	H	H	$X^{16} + X^{11} + X^4 + 1$	CRC-CCITT REVERSE

Block Diagram



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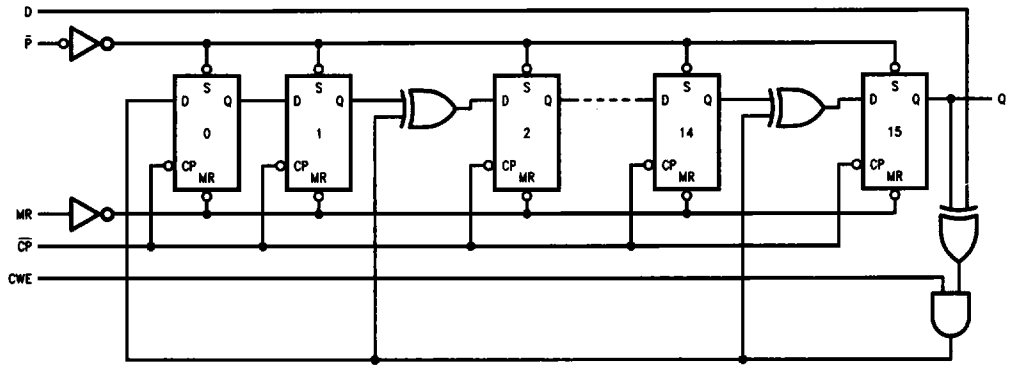

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FIGURE 1. Equivalent Circuit for $X^{16} + X^{15} + X^2 + 1$

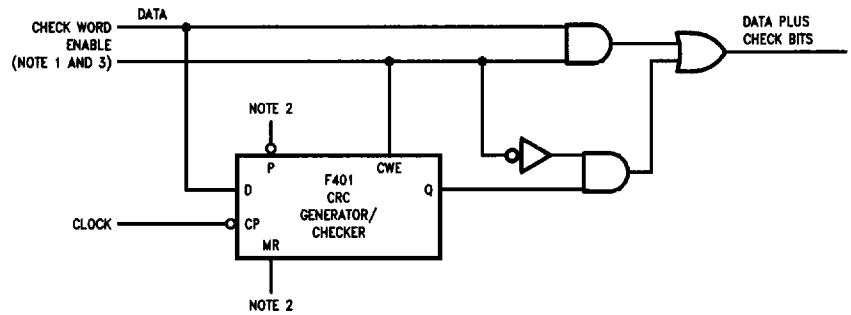

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FIGURE 2. Check Word Generation

Note 1: Check word Enable is HIGH while data is being clocked, LOW while transmission of check bits.

Note 2: 'F401 must be reset or preset before each computation.

Note 3: CRC check bits are generated and appended to data bits.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			70	105	mA	Max	V_O = HIGH

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100					85		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q	4.5 4.0		11.5 10.0			4.5 4.0	13.5 11.0	ns	2-3
t_{PHL}	Propagation Delay MR to Q	3.0		7.5			3.0	8.0	ns	2-3
t_{PLH}	Propagation Delay $\overline{P}$ to Q	3.0		8.5			3.0	9.5	ns	2-3
t_{PHL}	Propagation Delay MR to ER	3.5		11.0			3.5	12.0	ns	2-3
t_{PLH}	Propagation Delay $\overline{P}$ to ER	3.0		8.5			3.0	10.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to ER	5.0 4.5		13.0 11.5			5.0 4.5	14.5 12.5	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW D to $\overline{CP}$	5.0 5.0				5.5 5.5		ns	2-6
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW CWE to $\overline{CP}$	4.0 4.0				4.5 4.5			
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D and CWE to $\overline{CP}$	2.0 2.0				2.0 2.0			
$t_w(L)$	$\overline{P}$ Pulse Width, LOW	7.0				8.0		ns	2-4
$t_w(H)$ $t_w(L)$	Clock Pulse Width, HIGH or LOW	5.0 5.0				6.0 6.0		ns	2-4
$t_w(H)$	MR Pulse Width, HIGH	5.0				5.5		ns	2-4
t_{rec}	Recovery Time MR to $\overline{CP}$	4.0				4.5		ns	2-6
t_{rec}	Recovery Time $\overline{P}$ to $\overline{CP}$	2.0				2.0		ns	2-6